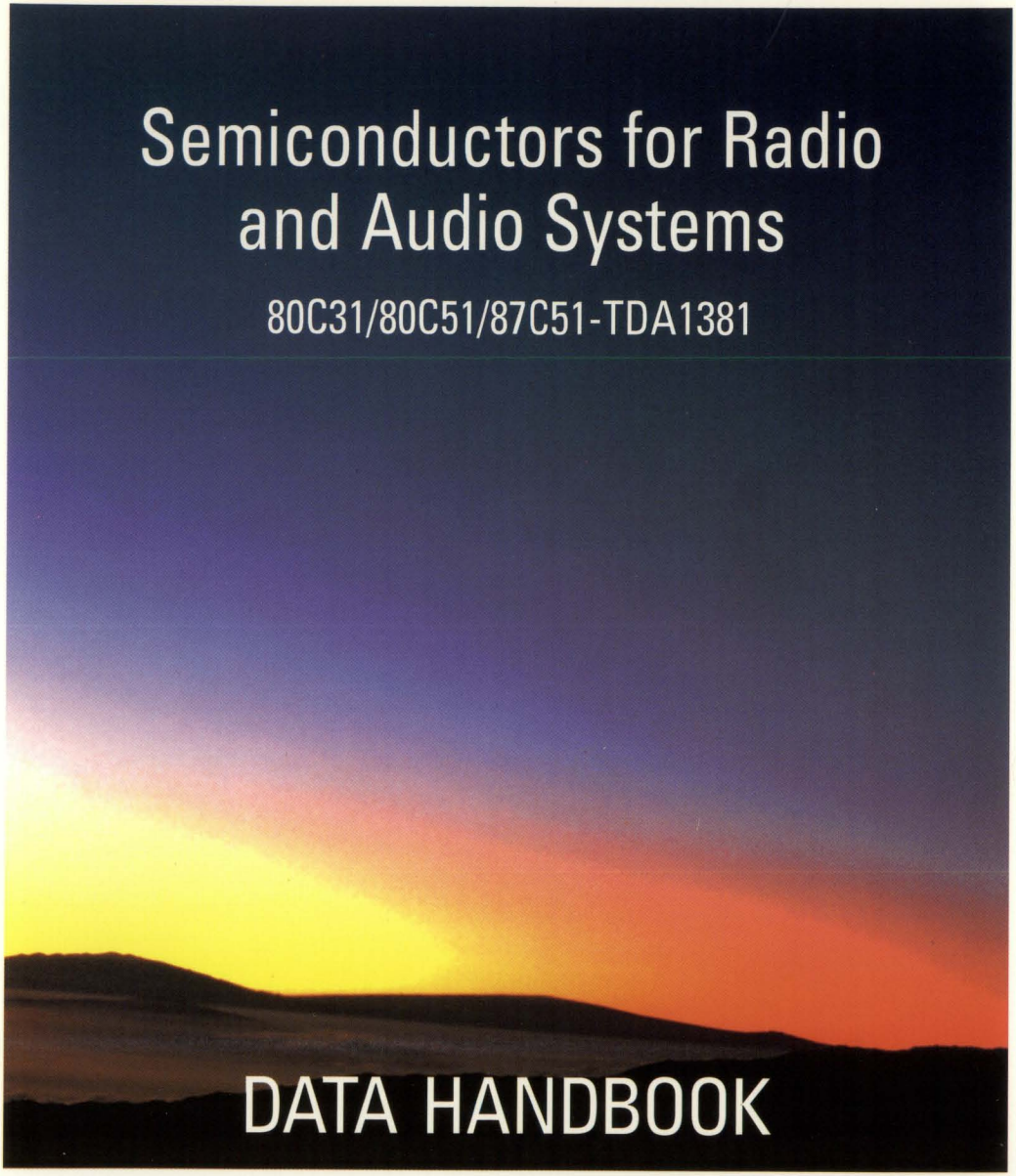
Semiconductors for Radio and Audio Systems

80C31/80C51/87C51-TDA1381



DATA HANDBOOK

BOOK IC01a 1995

Philips Semiconductors

PHILIPS

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

Semiconductors for Radio and Audio Systems

CONTENTS

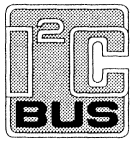
DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

SELECTION GUIDE

Semiconductors for Radio and Audio Systems

Functional index

PACS (Precision Adjacent Channel Selectivity)

Combination AM/FM, IF, PLL, MPX and NC circuits

SEMICONDUCTORS

AM receiver JFET input

Varicap diodes for AM tuning

Varicap diodes for FM tuning

MOSFETs for AM/FM tuning

Frequency/voltage synthesizers

Read/write amplifiers

Miscellaneous digital audio circuits

MPEG audio en/decoders

DSP circuits

AUDIO CONVERTORS

Digital to analog convertors DACs

DISPLAY DRIVERS

LCD display

LED DISPLAY

IR REMOTE CONTROL CIRCUITS

GENERAL

TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ, and the CECC system of conformity. Our factories are certified to ISO 9000 and CECC by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

DISCRETE SEMICONDUCTORS

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

A Germanium or other material with a band gap of 0.6 to 1 eV

B Silicon or other material with a band gap of 1 to 1.3 eV

C Gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more

R Compound materials, e.g. cadmium sulphide.

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements.

In the following list low power types are defined by $R_{th\ j\text{-}mb} > 15$ K/W and power types by $R_{th\ j\text{-}mb} \leq 15$ K/W.

A Diode; signal, low power

B Diode; variable capacitance

C Transistor; low power, audio frequency

D Transistor; power, audio frequency

E Diode; tunnel

F Transistor; low power, high frequency

G multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter, see under "Serial number/special third letter"

H Diode; magnetic sensitive

L Transistor; power, high frequency

N Photocoupler

P Radiation detector; e.g. high sensitivity photo-transistor; with special third letter

Q Radiation generator; e.g. LED, laser; with special third letter

R Control or switching device; e.g. thyristor, low power; with special third letter

S Transistor; low power, switching

T Control and switching device; e.g. thyristor, power; with special third letter

U Transistor; power, switching

W Surface acoustic wave device

X Diode; multiplier, e.g. varactor, step recovery

Y Diode; rectifying, booster

Z Diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER/SPECIAL THIRD LETTER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.(1) The letter has no fixed meaning, except in the following cases:

A For triacs, after second letter 'R' or 'T'

F For emitters and receivers in fibre-optic communication, after second letter 'G', 'P' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

L For lasers in non-fibre-optic applications, after second letter 'G' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

O For opto-triacs, after second letter 'R'

T For 3-state bicolour LEDs, after second letter 'Q'

W For transient voltage suppressor diodes, after second letter 'Z'.

EXAMPLES OF BASIC TYPE NUMBERS

AA112 Germanium, low power signal diode (consumer type)

ACY32 Germanium, low power AF transistor (industrial type)

BD232 Silicon, power AF transistor (consumer type)

CQY17 GaAs, light-emitting diode (industrial type)

RPY84 CdS, photo-conductive cell (industrial type).

Version letter(s)

One or two letters may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type. The letters never have a fixed meaning, except that the letter 'R' indicates reverse polarity and the letter 'W' indicates a surface mounted device (SMD).

(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

Suffix

Sub-classification can be used for devices supplied in a wide range of variants, called associated types. The following sub-coding suffixes are in use:

VOLTAGE REFERENCE AND VOLTAGE REGULATOR DIODES

One letter and one number, preceded by a hyphen (-). The letter, if required, indicates the nominal tolerance of the Zener voltage.

A 1%

B 2%

C 5%

D 10%

E 20%.

In the case of a 3% tolerance, the letter 'F' is used.

The number denotes the typical operating (Zener) voltage, related to the nominal current rating for the entire range. The letter 'V' is used in place of the decimal point.

Example: BZY74-C6V3 or -C10.

TRANSIENT VOLTAGE SUPPRESSOR DIODES

One number, preceded by a hyphen (-). The number indicates the maximum recommended continuous reversed (stand-off) voltage, V_R. The letter 'V' is used in place of the decimal point.

Example: BZW70-9V1 or –39.

The letter 'B' may be used immediately after the last number, to indicate a bidirectional suppressor diode.

Example: BZW10-15B.

CONVENTIONAL AND CONTROLLED AVALANCHE RECTIFIER DIODES AND THYRISTORS

One number, preceded by a hyphen (-). The number indicates the rated maximum repetitive peak reverse voltage, V_{RRM}, or the rated repetitive peak off-state voltage, V_{DRM}, whichever is the lower. Reversed polarity with respect to the case is indicated by the letter 'R' immediately after the number.

Example: BYT-100 or -100R.

RADIATION DETECTORS

One number, preceded by a hyphen (-). The number indicates the depletion layer in micrometres (μm). The resolution is indicated by a version letter.

Example: BPX10-2A.

ARRAY OF RADIATION DETECTORS AND GENERATORS

One number, preceded by a hyphen (-). The number indicates the number of basic devices assembled into the array.

Examples: BPW50-6, BPW50-9, BPW50-12.

HIGH FREQUENCY POWER TRANSISTORS

One number, preceded by a hyphen (-). The number indicates the supply voltage.

Example: BLU80-24.

INTEGRATED CIRCUITS

Basic type number

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

FIRST AND SECOND LETTERS

Digital family circuits

The first two letters identify the family.(1)

Solitary circuits

The first letter divides solitary circuits into:

S Solitary digital circuits

T Analog circuits

U Mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(2)

Microprocessors

The first two letters identify microprocessors and related circuits:

MA Microcomputer or central processing unit

MB Slice processor (functional slice of microprocessor)

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

(2) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

MD Related memories

ME Other related circuits such as interfaces, clocks, peripheral controllers, etc.

Charge-transfer devices and switched capacitors

The first two letters identify:

NH Hybrid circuits

NL Logic circuits

NM Memories

NS Analog signal processing using switched capacitors

NT Analog signal processing using charge-transfer devices

NX Imaging devices

NY Other related circuits.

THIRD LETTER

The third letter indicates the operating ambient temperature range:

A temperature range not specified below

B 0 to + 70 °C

C −55 to +125 °C

D −25 to + 70 °C

E −25 to + 85 °C

F −40 to + 85 °C

G −55 to + 85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

Serial number

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

Version letter

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C Cylindrical

D Ceramic dual in-line (CERDIL, CERDIP)

F Flat pack (two leads)

G Flat pack (four leads)

H Quad flat pack (QFP)

L Chip on tape (foil)

P Plastic dual in-line (DIL)

Q Quad in-line (QUIL)

T Mini pack (SOL, SO, VSO)

U Uncased chip.

Two-letter suffix

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

FIRST LETTER (GENERAL SHAPE)

C Cylindrical

D Dual in-line (DIL)

E Power DIL (with external heatsink)

F Flat pack (leads on two sides)

G Flat pack (leads on four sides)

H Quad flat pack (QFP)

K Diamond (TO-3 family)

M Multiple in-line (except dual, triple and quad)

Q Quad in-line (QUIL)

R Power QUIL (with external heatsink)

S Single in-line (SIL)

T Triple in-line

W Leaded chip carrier (LCC)

X Leadless chip carrier (LLCC)

Y Pin grid array (PGA).

SECOND LETTER (MATERIAL)

C Metal-ceramic

G Glass-ceramic

M Metal

P Plastic.

Examples

PCF1105WP: digital IC; PC family; operating temperature range –40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range –55 to +125 °C; serial number 2000.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental

conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor
- All mains-powered electrical equipment should be connected via an earth leakage switch
- Equipment cases should be earthed
- Relative humidity should be maintained between 50 and 65%
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

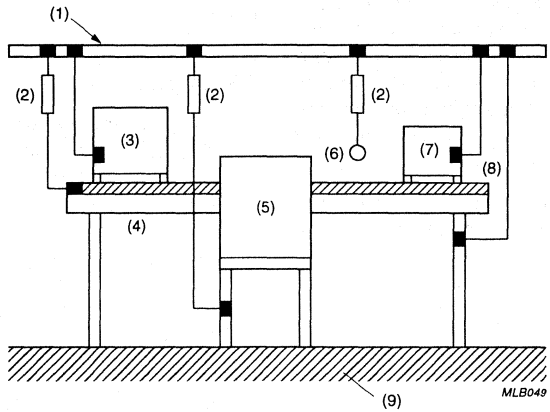
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



Earthing rail.
Resistor (500 kΩ ± 10%, 0.5 W).
Ionizer.
Work bench.
Chair.
Wrist strap.
Electrical equipment.
Conductive surface/antistatic sheet.

Fig.1 Protected work station.

DEVICE DATA

CMOS single-chip 8-bit microcontroller — 80C31/80C51/87C51

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The Philips 80C31/80C51/87C51 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The CMOS 8XC51 is functionally compatible with the NMOS 8031/8051 microcontrollers. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity.

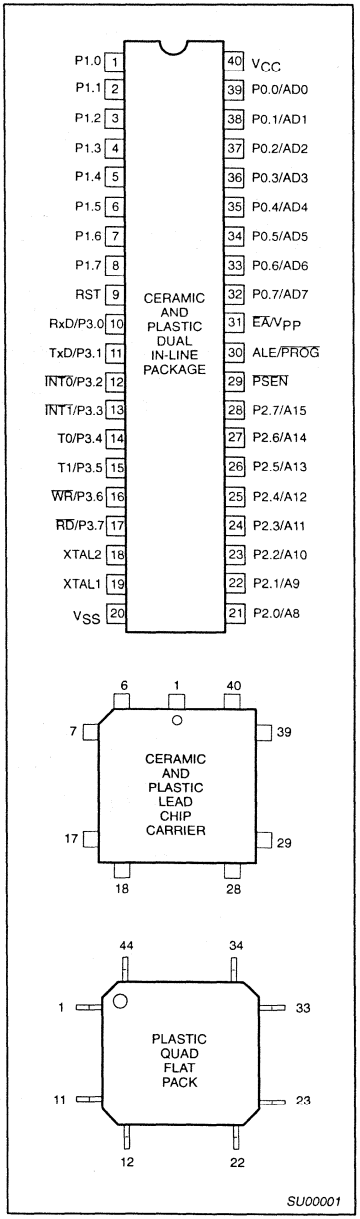
The 8XC51 contains a 4k × 8 ROM (80C51) EPROM (87C51), a 128 × 8 RAM, 32 I/O lines, two 16-bit counter/timers, a five-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the device has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

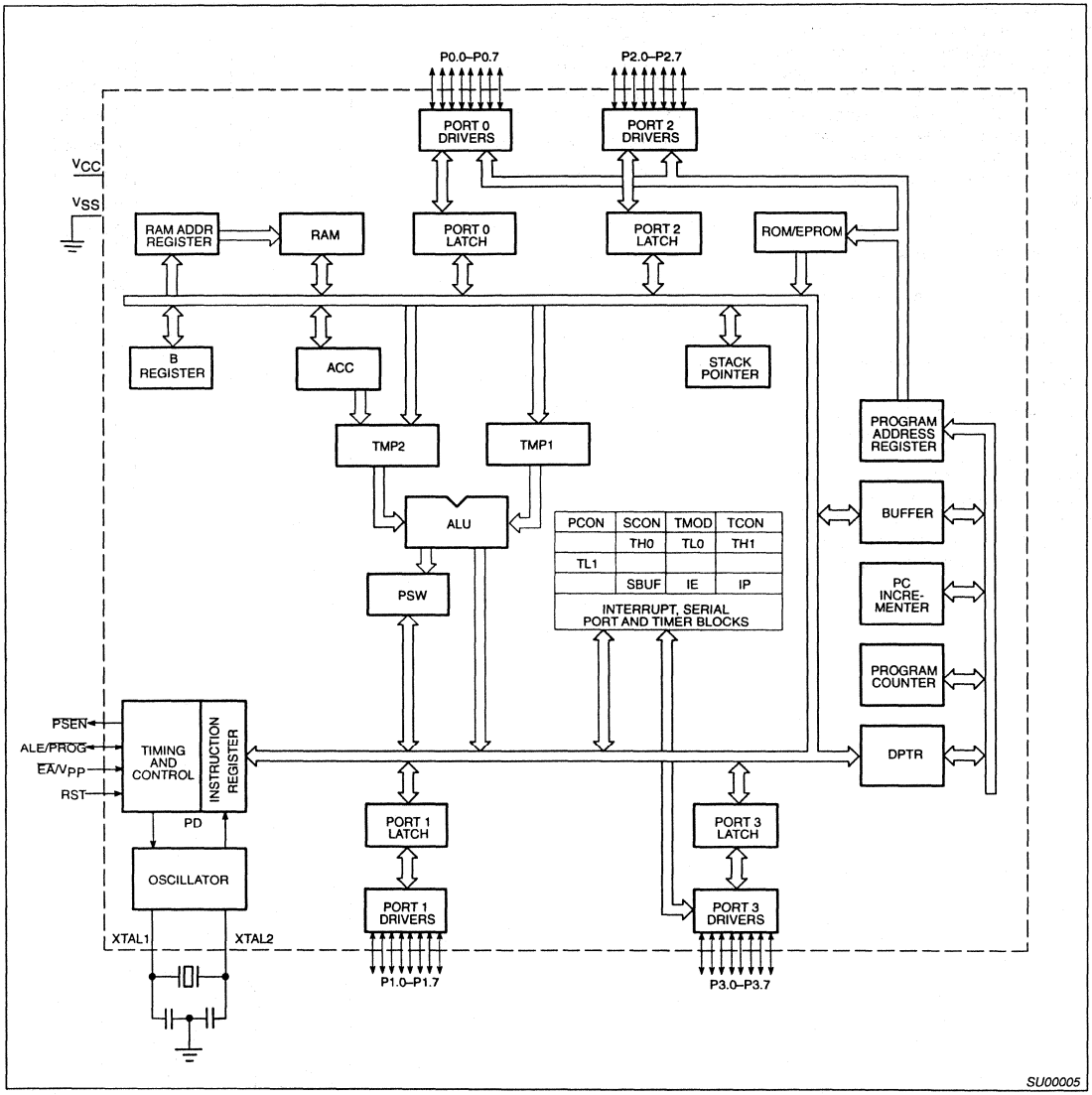
- 8031/8051 compatible
  - 4k × 8 ROM (80C51)
  - 4k × 8 EPROM (87C51)
  - ROMless (80C31)
  - 128 × 8 RAM
  - Two 16-bit counter/timers
  - Full duplex serial channel
  - Boolean processor
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- Five speed ranges at V_{CC} = 5V
  - 12MHz
  - 16MHz
  - 24MHz
  - 30MHz
  - 33MHz
- Five package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATIONS



SEE PAGE 5 FOR QFP AND LCC PIN FUNCTIONS.

BLOCK DIAGRAM



CMOS single-chip 8-bit microcontrollers — 80C32/80C52/87C52

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The Philips 80C32/80C52/87C52 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The CMOS 8XC52 is functionally compatible with the NMOS SCN- 8032/8052 microcontrollers. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity.

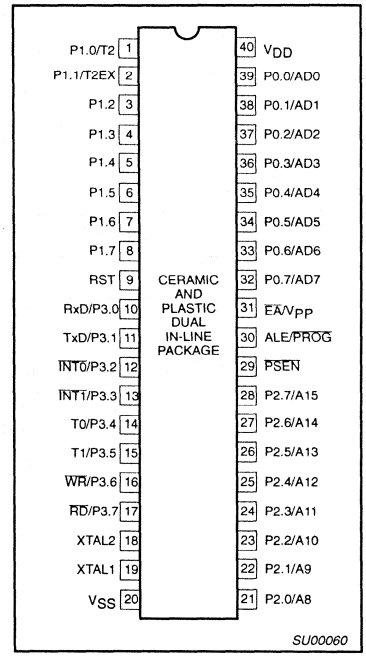
The 8XC52 contains an 8k × 8 ROM (80C52) EPROM (87C52), a 256 × 8 RAM, 32 I/O lines, three 16-bit counter/timers, a six-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the 8XC52 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

- 80C51 based architecture
- 8032/8052 compatible
  - 8k × 8 ROM (80C52)
  - 8k × 8 EPROM (87C52)
  - ROMless (80C32)
  - 256 × 8 RAM
  - Three 16-bit counter/timers
  - Full duplex serial channel
  - Boolean processor
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- Two speed ranges:
  - 3.5 to 16MHz
  - 3.5 to 24MHz
- Five package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATIONS



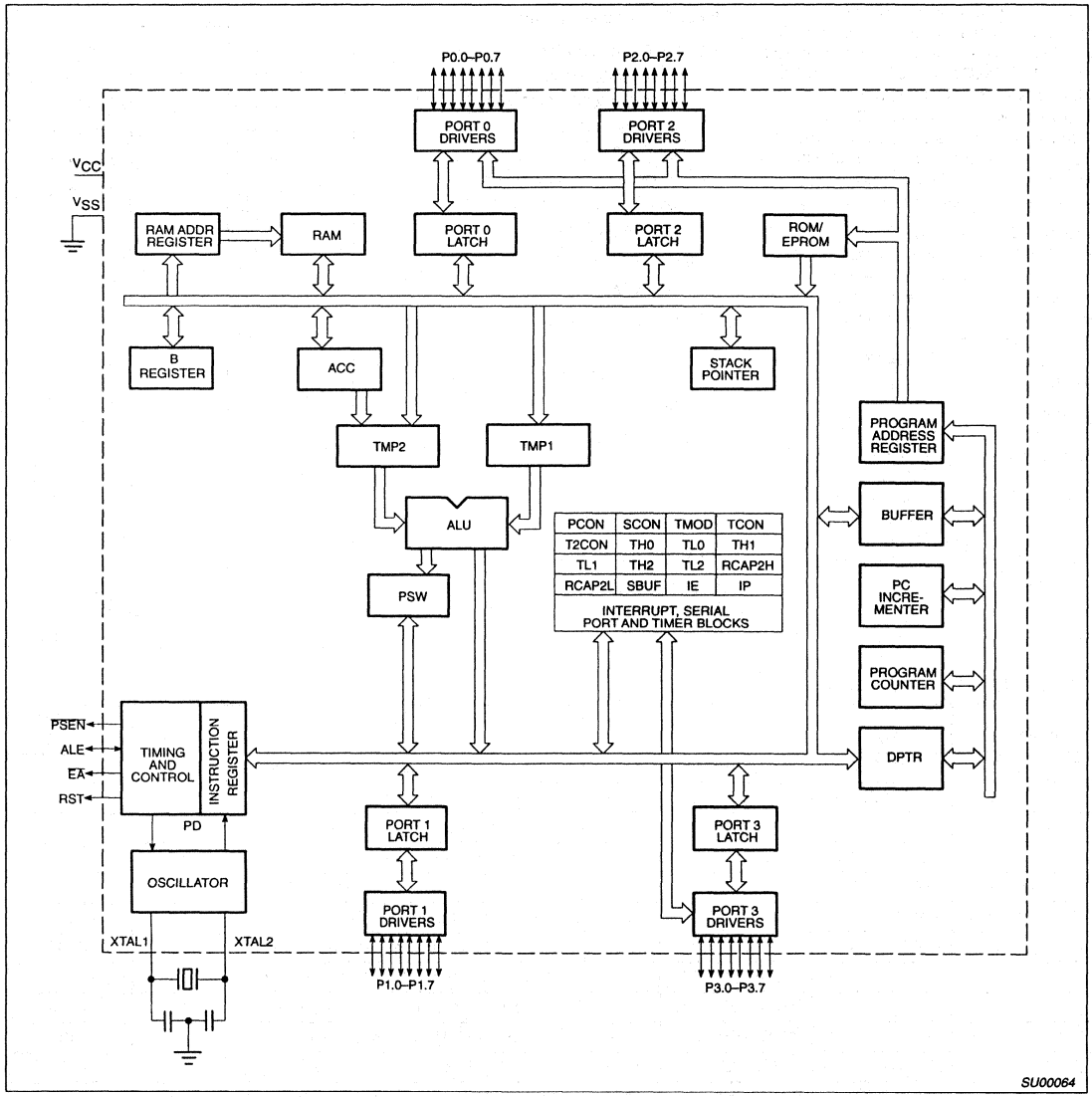
ORDERING INFORMATION

ROMless	ROM	EPROM[1]		TEMPERATURE RANGE °C AND PACKAGE	FREQ MHz	DRAWING NUMBER
P80C32EBP N	P80C52EBP N	P87C52EBP N	OTP	0 to +70, Plastic Dual In-line Package	16	0415C
P80C32EBA A	P80C52EBA A	P87C52EBA A	OTP	0 to +70, Plastic Leaded Chip Carrier	16	0403G
		P87C52EBF FA	UV	0 to +70, Ceramic Dual In-line Package	16	0590B
		P87C52EBL KA	UV	0 to +70, Ceramic Leaded Chip Carrier	16	1472A
P80C32EBB B	P80C52EBB B	P87C52EBB B	OTP	0 to +70, Plastic Quad Flat Pack	16	1118D
P80C32EFP N	P80C52EFP N	P87C52EFP N	OTP	–40 to +85, Plastic Dual In-line Package	16	0415C
P80C32EFA A	P80C52EFA A	P87C52EFA A	OTP	–40 to +85, Plastic Leaded Chip Carrier	16	0403G
		P87C52EFF FA	UV	–40 to +85, Ceramic Dual In-line Package	16	0590B
		P87C52EFL KA	UV	–40 to +85, Ceramic Leaded Chip Carrier	16	1472A
P80C32EFB B	P80C52EFB B	P87C52EFB B	OTP	–40 to +85, Plastic Quad Flat Pack	16	1118D
P80C32IBP N	P80C52IBP N	P87C52IBP N	OTP	0 to +70, Plastic Dual In-line Package	24	0415C
P80C32IBA A	P80C52IBA A	P87C52IBA A	OTP	0 to +70, Plastic Leaded Chip Carrier	24	0403G
		P87C52IBF FA	UV	0 to +70, Ceramic Dual In-line Package	24	0590B
		P87C52IBL KA	UV	0 to +70, Ceramic Leaded Chip Carrier	24	1472A
P80C32IFP N	P80C52IFP N	P87C52IFP N	OTP	–40 to +85, Plastic Dual In-line Package	24	0415C
P80C32IFA A	P80C52IFA A	P87C52IFA A	OTP	–40 to +85, Plastic Leaded Chip Carrier	24	0403G
		P87C52IFF FA	UV	–40 to +85, Ceramic Dual In-line Package	24	0590B
		P87C52IFL KA	UV	–40 to +85, Ceramic Leaded Chip Carrier	24	1472A

NOTE:

1. OTP = One Time Programmable EPROM. UV = UV erasable EPROM

BLOCK DIAGRAM



CMOS single-chip 8-bit microcontroller — 80C451/83C451/87C451

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The Philips 8XC451 is an I/O expanded single-chip microcontroller fabricated with Philips high-density CMOS technology. Philips epitaxial substrate minimizes latch-up sensitivity.

The 8XC451 (includes the 80C451, 87C451 and 83C451) is a functional extension of the 87C51 microcontroller with three additional I/O ports and four I/O control lines for a total of 68 pins. Four control lines associated with port 6 facilitate high-speed asynchronous I/O functions.

The 8XC451 includes a 4k × 8 ROM (83C451) EPROM (87C451), a 128 × 8 RAM, 56 (LCC), two 16-bit timer/counters, a five source, two priority level, nested interrupt structure, a serial I/O port for either a full duplex UART, I/O expansion, or multi-processor communications, and on-chip oscillator and clock circuits. The 80C451 ROMless version includes all of the 83C451 features except the on-board 4k × 8 ROM.

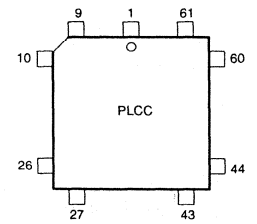
The 87C451 has 4k of EPROM on-chip as program memory and is otherwise identical to the 83C451.

The 8XC451 has two software selectable modes of reduced activity for further power reduction; idle mode and power-down mode. Idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. Power-down mode freezes the oscillator, causing all other chip functions to be inoperative while maintaining the RAM contents.

FEATURES

- 80C51 based architecture
- Seven 8-bit I/O ports
- Port 6 features:
  - Eight data pins
  - Four control pins
  - Direct MPU bus interface
  - Parallel printer interface
- On the microcontroller:
  - 4k × 8 ROM (83C451)
    4k × 8 EPROM (87C451)
    ROMless version (80C451)
  - 128 × 8 RAM
  - Two 16-bit counter/timers
  - Two external interrupts
- External memory addressing capability
  - 64k ROM and 64k RAM
- Low power consumption:
  - Normal operation: less than 24mA at 5V, 12MHz
  - Idle mode
  - Power-down mode

PIN CONFIGURATION



Pin	Function	Pin	Function
1	$\overline{EA}$/Vpp	35	RST
2	P2.0/A8	36	P3.0/RxD
3	P2.1/A9	37	P3.1/TxD
4	P2.2/A10	38	P3.2/$\overline{INT0}$
5	P2.3/A11	39	P3.3/$\overline{INT1}$
6	P2.4/A12	40	P3.4/T0
7	P2.5/A13	41	P3.5/T1
8	P2.6/A14	42	P3.6/$\overline{WR}$
9	P2.7/A15	43	P3.7/$\overline{RD}$
10	P0.7/AD7	44	P5.0
11	P0.6/AD6	45	P5.1
12	P0.5/AD5	46	P5.2
13	P0.4/AD4	47	P5.3
14	P0.3/AD3	48	P5.4
15	P0.2/AD2	49	P5.5
16	P0.1/AD1	50	P5.6
17	P0.0/AD0	51	P5.7
18	Vcc	52	XTAL2
19	P4.7	53	XTAL1
20	P4.6	54	Vss
21	P4.5	55	$\overline{ODS}$
22	P4.4	56	$\overline{IDS}$
23	P4.3	57	BFLAG
24	P4.2	58	AFLAG
25	P4.1	59	P6.0
26	P4.0	60	P6.1
27	P1.0	61	P6.2
28	P1.1	62	P6.3
29	P1.2	63	P6.4
30	P1.3	64	P6.5
31	P1.4	65	P6.6
32	P1.5	66	P6.7
33	P1.6	67	$\overline{PSEN}$
34	P1.7	68	ALE/$\overline{PROG}$

SU00084

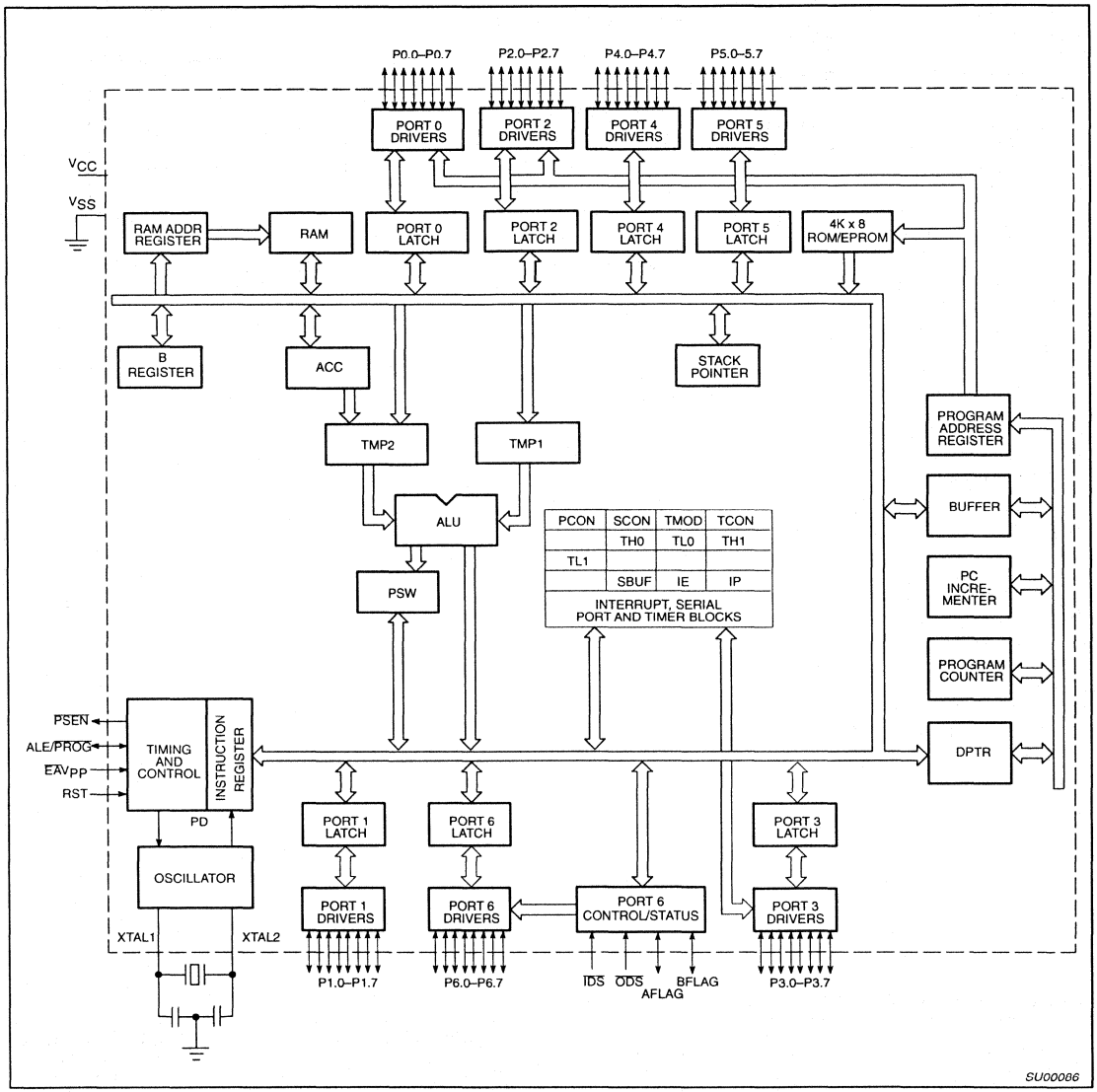
ORDERING INFORMATION

ROMless	ROM	EPROM[1]		TEMPERATURE RANGE °C AND PACKAGE	FREQ MHz	DRAWING NUMBER
SC80C451CCA68	SC83C451CCA68	SC87C451CCA68	OTP	0 to +70, Plastic Leaded Chip Carrier,	3.5 to 12	0398E
SC80C451CGA68	SC83C451CGA68	SC87C451CGA68	OTP	0 to +70, Plastic Leaded Chip Carrier	3.5 to 16	0398E
SC80C451ACA68	SC83C451ACA68	SC87C451ACA68	OTP	–40 to +85, Plastic Leaded Chip Carrier	3.5 to 12	0398E
SC80C451AGA68	SC83C451AGA68	SC87C451AGA68	OTP	–40 to +85, Plastic Leaded Chip Carrier	3.5 to 16	0398E

NOTE:

1. OTP = One Time Programmable

BLOCK DIAGRAM



CMOS single-chip 8-bit microcontroller — 80C528/83C528

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

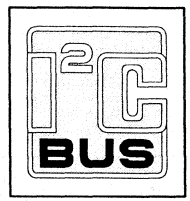
The 8XC528 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 8XC528 has the same instruction set as the 80C51. Three versions of the derivative exist:

- 83C528 — 32k bytes mask programmable ROM
- 80C528 — ROMless version of the 83C528
- 87C528 — 32k bytes EPROM (described in a separate data sheet)

This device provides architectural enhancements that make it applicable in a variety of applications in consumer, telecom and general control systems, especially in those systems which need large ROM and RAM capacity on-chip.

The 8XC528 contains a 32k × 8 ROM (83C528), a 512 × 8 RAM, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a 16-bit timer (identical to the timer 2 of the 80C52), a watchdog timer with a separate oscillator, a multi-source, two-priority-level, nested interrupt structure, two serial interfaces (UART and I²C-bus), and on-chip oscillator and timing circuits.

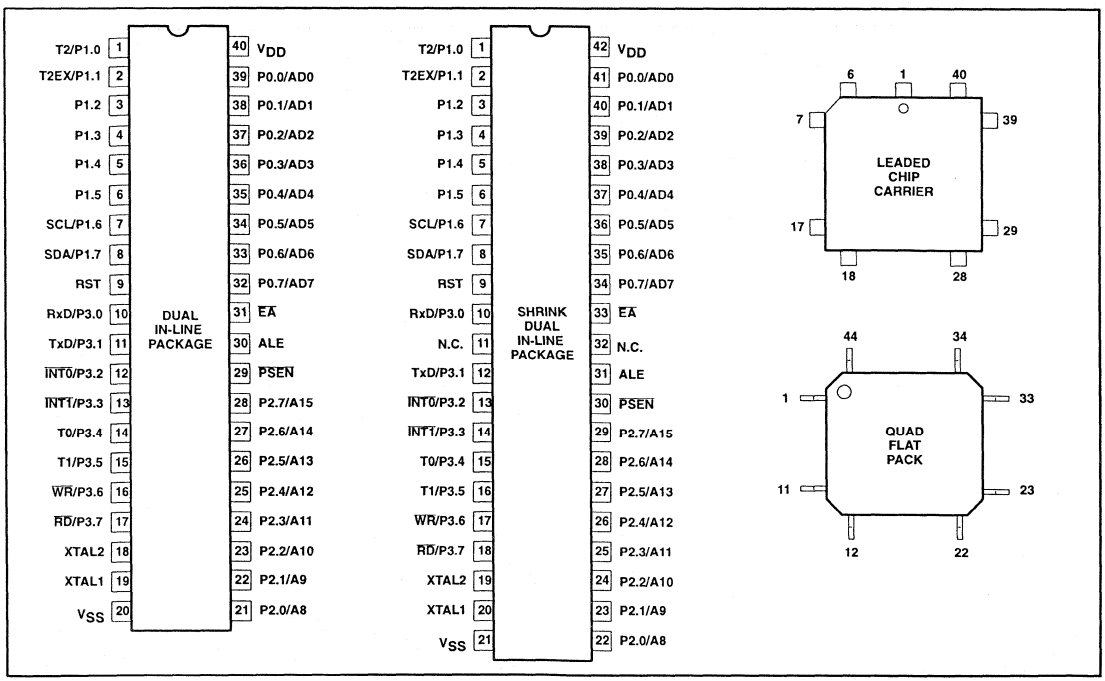
In addition, the 8XC528 has two software selectable modes of power reduction — idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.



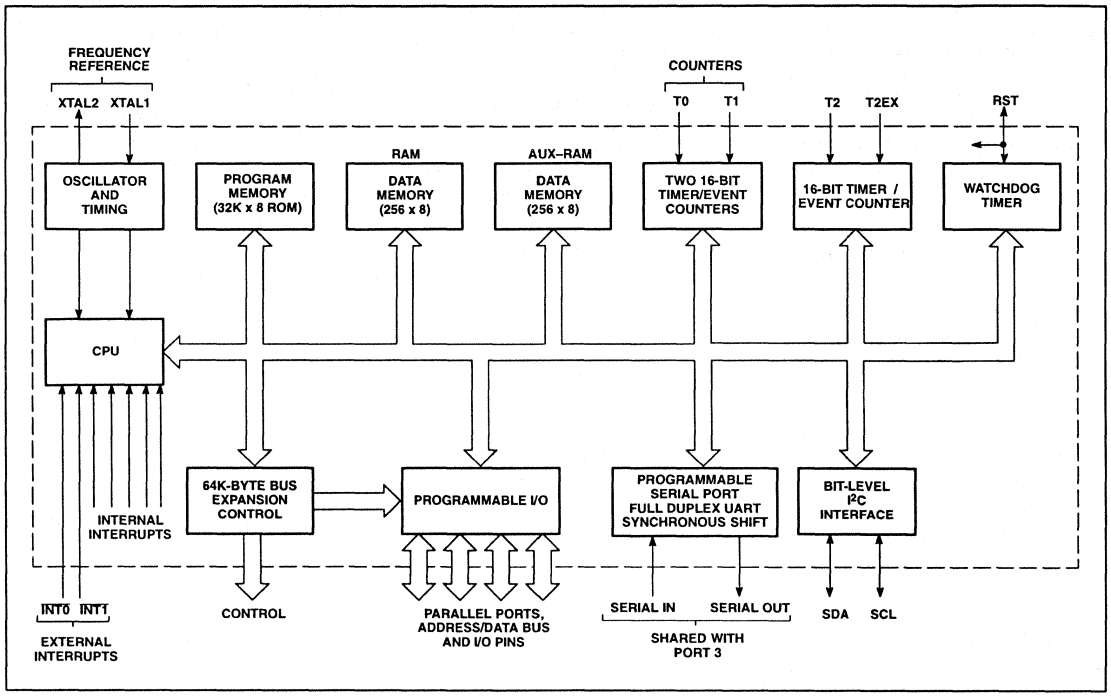
FEATURES

- 80C51 instruction set
  - 32k × 8 ROM (83C528)
  - ROMless (80C528)
  - 512 × 8 RAM
  - Memory addressing capability 64k ROM and 64k RAM
  - Three 16-bit counter/timers
  - On-chip watchdog timer with oscillator
  - Full duplex UART
  - I²C serial interface
  - Four 8-bit I/O ports
- Power control modes:
  - Idle mode
  - Power-down mode
  - Warm start from power-down
- CMOS and TTL compatible
- Extended temperature ranges
- ROM code protection
- 7-source and 7-vector interrupt structure with 2 priority levels
- Up to 3 external interrupt request inputs
- Two programmable power reduction modes (Idle and Power-down)
- Termination of Idle mode by any interrupt, external or WDT (watchdog) reset
- XTAL frequency range: 1.2 MHz to 16 MHz

PIN CONFIGURATIONS



BLOCK DIAGRAM



CMOS single-chip 8-bit microcontroller with A/D and watchdog timer

80C550/83C550/87C550

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The Philips 8XC550 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. This Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity. The CMOS 8XC550 has the same instruction set as the 80C51.

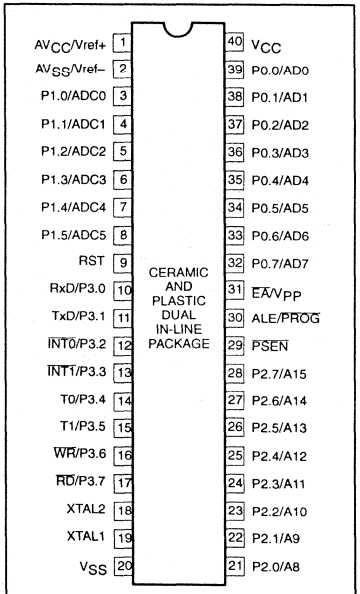
The 8XC550 contains a 4k × 8 EPROM (87C550)/ROM (83C550)/ROMless (80C550 has no program memory on-chip), a 128 × 8 RAM, 8 channels of 8-bit A/D, four 8-bit ports (port 1 is input only), a watchdog timer, two 16-bit counter/timers, a seven-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and an on-chip oscillator and clock circuits.

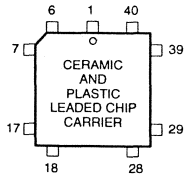
In addition, the 8XC550 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

- 80C51 based architecture
  - 4k × 8 EPROM (87C550)/ ROM (83C550)
  - 128 × 8 RAM
  - Eight channels of 8-bit A/D
  - Two 16-bit counter/timers
  - Watchdog timer
  - Full duplex serial channel
  - Boolean processor
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- One speed range at V_{CC} = 5V ±10%
  - 3.5 to 16MHz
- Four package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATIONS





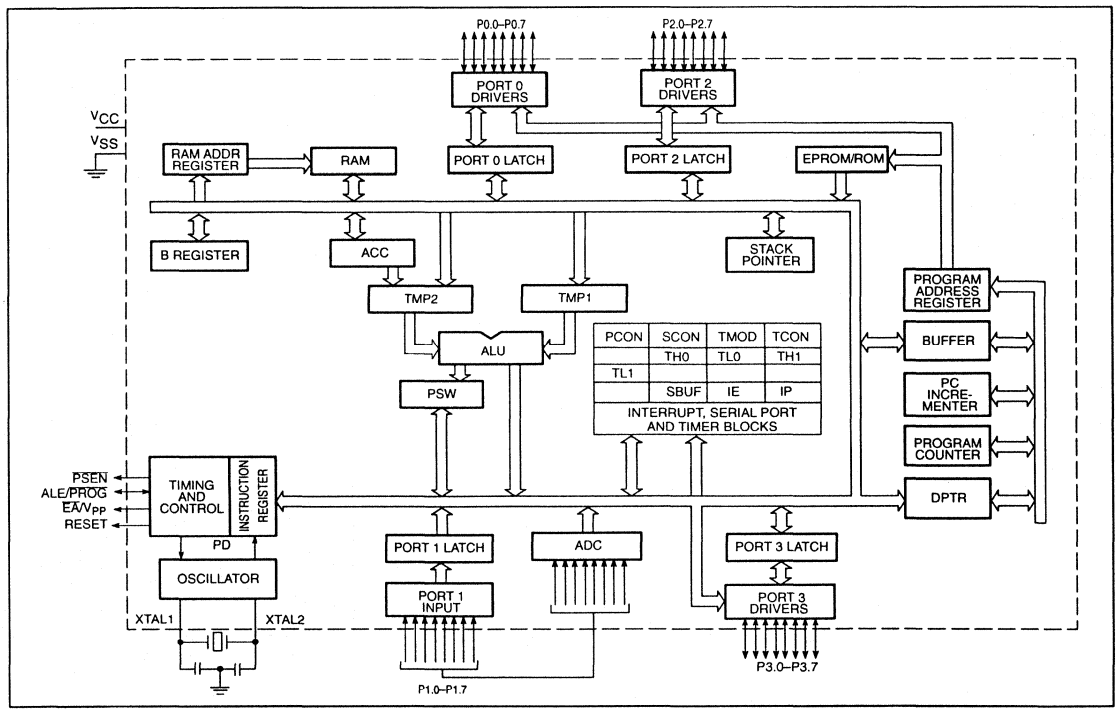
Pin	Function	Pin	Function	Pin	Function
1	AV_{CC}	16	P3.2/$\overline{INT0}$	31	P2.6/A14
2	Vref+	17	P3.3/$\overline{INT1}$	32	P2.7/A15
3	Vref–	18	P3.4/T0	33	$\overline{PSEN}$
4	AV_{SS}	19	P3.5/T1	34	ALE/$\overline{PROG}$
5	P1.0/ADC0	20	P3.6/$\overline{WR}$	35	$\overline{EA}/V_{PP}$
6	P1.1/ADC1	21	P3.7/$\overline{RD}$	36	P0.7/AD7
7	P1.2/ADC2	22	XTAL2	37	P0.6/AD6
8	P1.3/ADC3	23	XTAL1	38	P0.5/AD5
9	P1.4/ADC4	24	V_{SS}	39	P0.4/AD4
10	P1.5/ADC5	25	P2.0/A8	40	P0.3/AD3
11	P1.6/ADC6	26	P2.1/A9	41	P0.2/AD2
12	P1.7/ADC7	27	P2.2/A10	42	P0.1/AD1
13	RST	28	P2.3/A11	43	P0.0/AD0
14	P3.0/RxD	29	P2.4/A12	44	V_{CC}
15	P3.1/TxD	30	P2.5/A13		

ORDERING INFORMATION

ROMless	ROM	EPROM		TEMPERATURE RANGE °C AND PACKAGE [1]	FREQ MHz	DRAWING NUMBER
		P87C550EBF FA	UV	0 to +70, Ceramic Dual In-Line Package	3.5 to 16	0590B
		P87C550EBL KA	UV	0 to +70, Ceramic Leaded Chip Carrier	3.5 to 16	1472A
P80C550EBP N	P83C550EBP N	P87C550EBP N	OTP	0 to +70, Plastic Dual In-Line Package	3.5 to 16	0415C
P80C550EBA A	P83C550EBA A	P87C550EBA A	OTP	0 to +70, Plastic Leaded Chip Carrier	3.5 to 16	0403G
P80C550EFP N	P83C550EFP N	P87C550EFP N	OTP	–40 to +85, Plastic Dual In-Line Package	3.5 to 16	0415C
P80C550EFA A	P83C550EFA A	P87C550EFA A	OTP	–40 to +85, Plastic Leaded Chip Carrier	3.5 to 16	0403G
		P87C550EFL KA	UV	–40 to +85, Ceramic Leaded Chip Carrier	3.5 to 16	1472A
		P87C550EFF FA	UV	–40 to +85, Ceramic Dual In-Line Package	3.5 to 16	0590B

NOTES:
1. OTP = One Time Programmable EPROM. UV = UV Erasable EPROM.

BLOCK DIAGRAM



Single-chip 8-bit microcontroller — 80C552/83C552

Single-chip 8-bit microcontroller with 10-bit A/D, capture/compare timer, high-speed outputs, PWM

DESCRIPTION

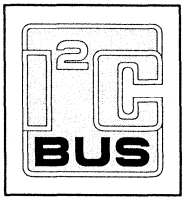
The 80C552/83C552 (hereafter generically referred to as 8XC552) Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 8XC552 has the same instruction set as the 80C51. Three versions of the derivative exist:

- 83C552—8k bytes mask programmable ROM
- 80C552—ROMless version of the 83C552
- 87C552—8k bytes EPROM (described in a separate chapter)

The 8XC552 contains a non-volatile 8k × 8 read-only program memory (83C552), a volatile 256 × 8 read/write data memory, five 8-bit I/O ports, one 8-bit input port, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I²C-bus), a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC552 can be expanded using standard TTL compatible memories and logic.

In addition, the 8XC552 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial ports, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

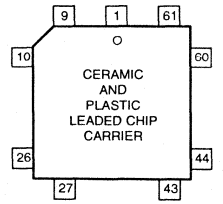
The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte, and 17 three-byte. With a 16MHz (24MHz) crystal, 58% of the instructions are executed in 0.75μs (0.5μs) and 40% in 1.5μs (1μs). Multiply and divide instructions require 3μs (2μs).



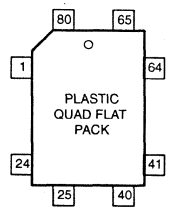
FEATURES

- 80C51 central processing unit
- 8k × 8 ROM expandable externally to 64k bytes
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Two standard 16-bit timer/counters
- 256 × 8 RAM, expandable externally to 64k bytes
- Capable of producing eight synchronized, timed outputs
- A 10-bit ADC with eight multiplexed analog inputs
- Two 8-bit resolution, pulse width modulation outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- I²C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Three speed ranges:
  - 1.2 to 16MHz
  - 1.2 to 24MHz (ROM, ROMless only)
  - 1.2 to 30MHz (ROM, ROMless only)
- Three operating ambient temperature ranges:
  - PCB83C552–5: 0°C to +70°C
  - PCF83C552–5: –40°C to +85°C (XTAL frequency max. 24 MHz)
  - PCA83C552–5: –40°C to +125°C (XTAL frequency max. 16 MHz)

PIN CONFIGURATIONS

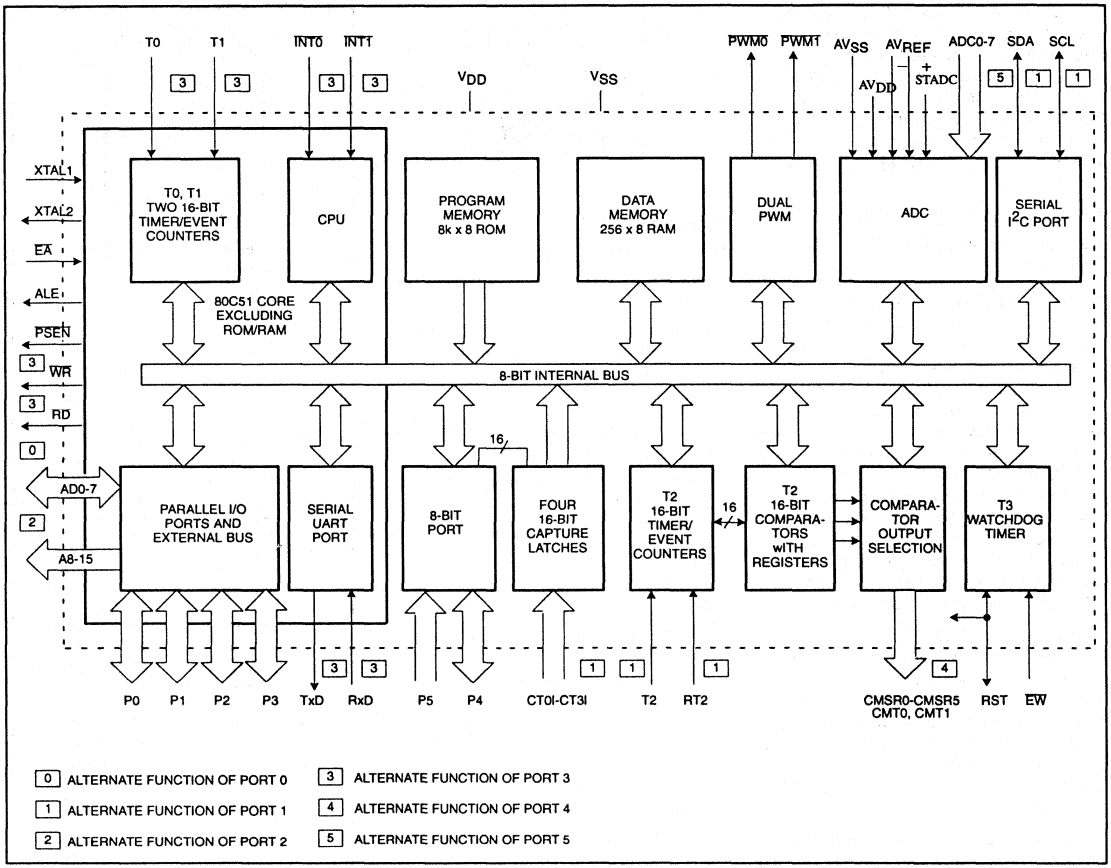


Pin	Function	Pin	Function
1	P5.0/ADC0	35	XTAL1
2	V_{DD}	36	V_{SS}
3	STADC	37	V_{SS}
4	$\overline{PWM0}$	38	NC
5	$\overline{PWM1}$	39	P2.0/A08
6	$\overline{EW}$	40	P2.1/A09
7	P4.0/CMSR0	41	P2.2/A10
8	P4.1/CMSR1	42	P2.3/A11
9	P4.2/CMSR2	43	P2.4/A12
10	P4.3/CMSR3	44	P2.5/A13
11	P4.4/CMSR4	45	P2.6/A14
12	P4.5/CMSR5	46	P2.7/A15
13	P4.6/CMT0	47	$\overline{PSEN}$
14	P4.7/CMT1	48	ALE
15	RST	49	$\overline{EA}$
16	P1.0/CT0I	50	P0.7/AD7
17	P1.1/CT1I	51	P0.6/AD6
18	P1.2/CT2I	52	P0.5/AD5
19	P1.3/CT3I	53	P0.4/AD4
20	P1.4/T2	54	P0.3/AD3
21	P1.5/RT2	55	P0.2/AD2
22	P1.6/SCL	56	P0.1/AD1
23	P1.7/SDA	57	P0.0/AD0
24	P3.0/RxD	58	AVref–
25	P3.1/TxD	59	AVref+
26	P3.2/$\overline{INT0}$	60	AV_{SS}
27	P3.3/$\overline{INT1}$	61	AV_{DD}
28	P3.4/T0	62	P5.7/ADC7
29	P3.5/T1	63	P5.6/ADC6
30	P3.6/$\overline{WR}$	64	P5.5/ADC5
31	P3.7/$\overline{RD}$	65	P5.4/ADC4
32	NC	66	P5.3/ADC3
33	NC	67	P5.2/ADC2
34	XTAL2	68	P5.1/ADC1



FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

BLOCK DIAGRAM



Single-chip 8-bit microcontroller — 80C562/83C562

Single-chip 8-bit microcontroller with 8-bit A/D, capture/compare timer, high-speed outputs, PWM

DESCRIPTION

The 80C562/83C562 (hereafter generically referred to as 8XC562) Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 83C562/83C562 has the same instruction set as the 80C51.

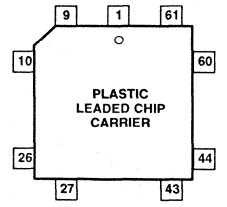
The 8XC562 contains a non-volatile 256 × 8 read-only program memory, a volatile 256 × 8 read/write data memory (83C562) (the 80C562 is ROMless), a volatile 256 × 8 read/write data memory, six 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, two pulse width modulated outputs, standard 80C51 UART, a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 83C562 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12MHz crystal, 58% of the instructions are executed in 1μs and 40% in 2μs. Multiply and divide instructions require 4μs.

FEATURES

- 80C51 instruction set
- 8k × 8 ROM expandable externally to 64k bytes
- 256 × 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Capable of producing eight synchronized, timed outputs
- An 8-bit ADC with eight multiplexed analog inputs
- Two 8-bit resolution, pulse width modulated outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Three temperature ranges
  - 0 to +70°C
  - –40 to +85°C
  - –40 to +125°C

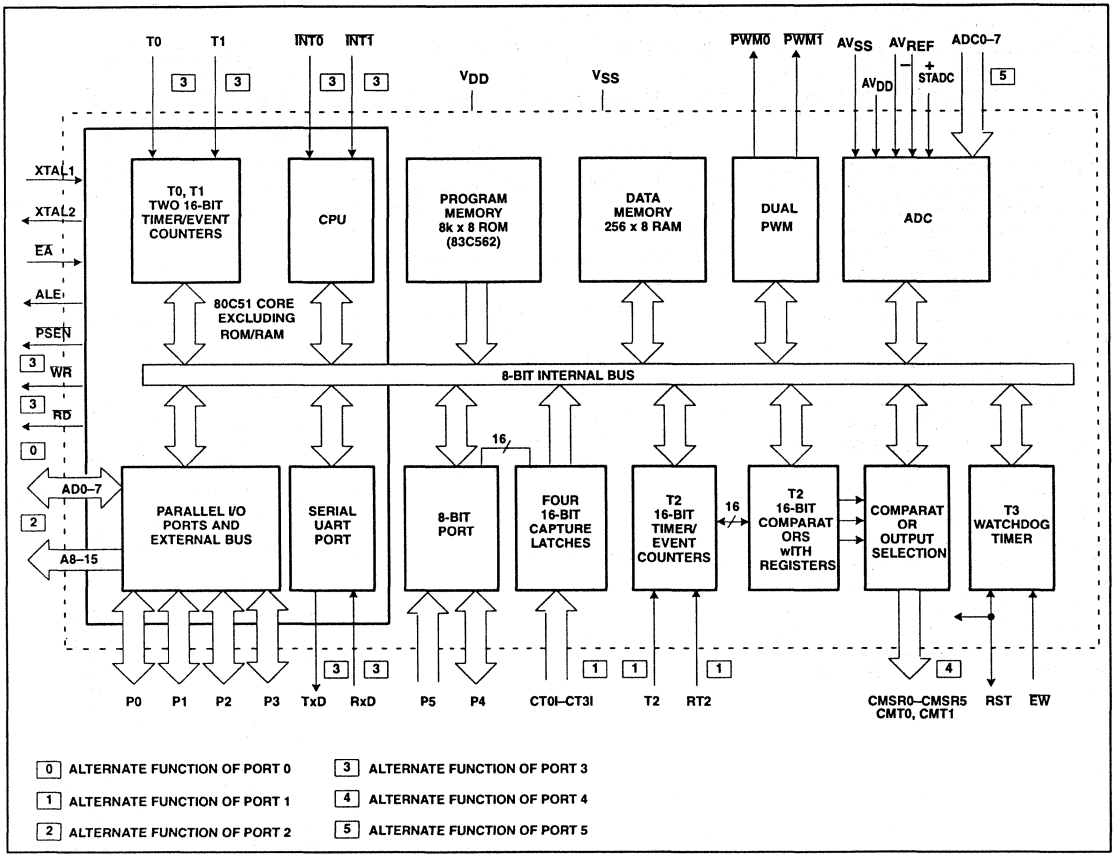
PIN CONFIGURATION



Pin	Function	Pin	Function
1	P5.0/ADC0	35	XTAL1
2	V_{DD}	36	V_{SS}
3	STADC	37	V_{SS}
4	$\overline{PWM0}$	38	NC
5	$\overline{PWM1}$	39	P2.0/A08
6	$\overline{EW}$	40	P2.1/A09
7	P4.0/CMSR0	41	P2.2/A10
8	P4.1/CMRS1	42	P2.3/A11
9	P4.2CMSR2	43	P2.4/A12
10	P4.3/CMSR3	44	P2.5/A13
11	P4.4/CMSR4	45	P2.6/A14
12	P4.5/CMSR5	46	P2.7/A15
13	P4.6/CMT0	47	$\overline{PSEN}$
14	P4.7/CMT1	48	ALE
15	RST	49	$\overline{EA}$
16	P1.0/CT01	50	P0.7/AD7
17	P1.1/CT1I	51	P0.6/AD6
18	P1.2/CT2I	52	P0.5/AD5
19	P1.3/CT3I	53	P0.4/AD4
20	P1.4/T2	54	P0.3/AD3
21	P1.5/RT2	55	P0.2/AD2
22	P1.6	56	P0.1/AD1
23	P1.7	57	P0.0/AD0
24	P3.0/RxD	58	AVref–
25	P3.1TxD	59	AVref+
26	P3.2/$\overline{INT0}$	60	AV_{SS}
27	P3.3/$\overline{INT1}$	61	AV_{DD}
28	P3.4/T0	62	P5.7/ADC7
29	P3.5/T1	63	P5.6/ADC6
30	P3.6/$\overline{WR}$	64	P5.5/ADC5
31	P3.7/$\overline{RD}$	65	P5.4/ADC4
32	NC	66	P5.3/ADC3
33	NC	67	P5.2/ADC2
34	XTAL2	68	P5.1/ADC1

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

BLOCK DIAGRAM



CMOS single-chip 8-bit microcontroller — 80C652/83C652

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The P80C652/83C652 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 80C652/83C652 has the same instruction set as the 80C51. Three versions of the derivative exist:

83C652 — 8k bytes mask programmable ROM

80C652 — ROMless version

80C652 — EPROM version (described in a separate chapter)

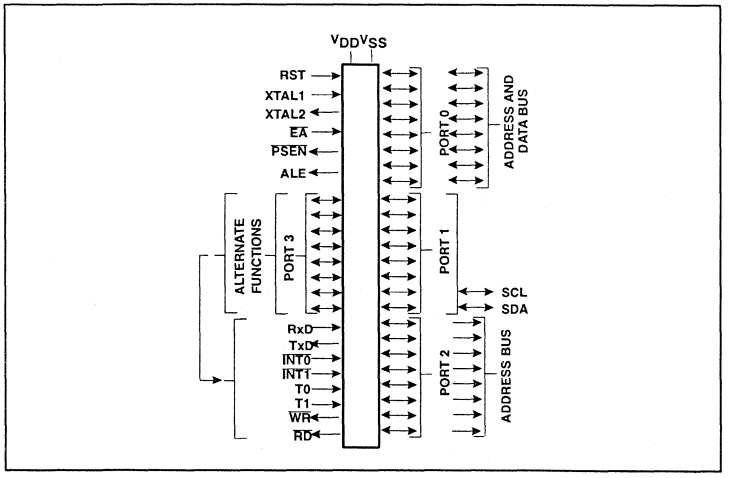
This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 8XC652 contains a non-volatile 8k × 8 read-only program memory, a volatile 256 × 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC652 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 16(24)MHz crystal, 58% of the instructions are executed in 0.75(0.5)µs and 40% in 1.5(1)µs. Multiply and divide instructions require 3(2)µs.

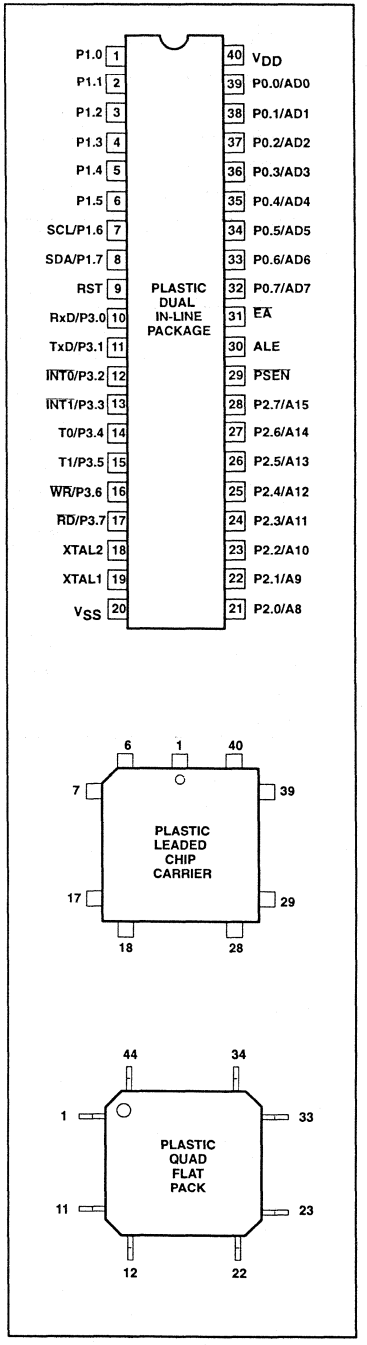
FEATURES

- 80C51 central processing unit
- 8k × 8 ROM expandable externally to 64k bytes
- 256 × 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART facilities
- Power control modes
  - Idle mode
  - Power-down mode
- ROM code protection
- Extended frequency range: 1.2 to 24 MHz
- Three operating ambient temperature ranges:
  - 0 to +70°C
  - –40 to +85°C
  - –40 to +125°C

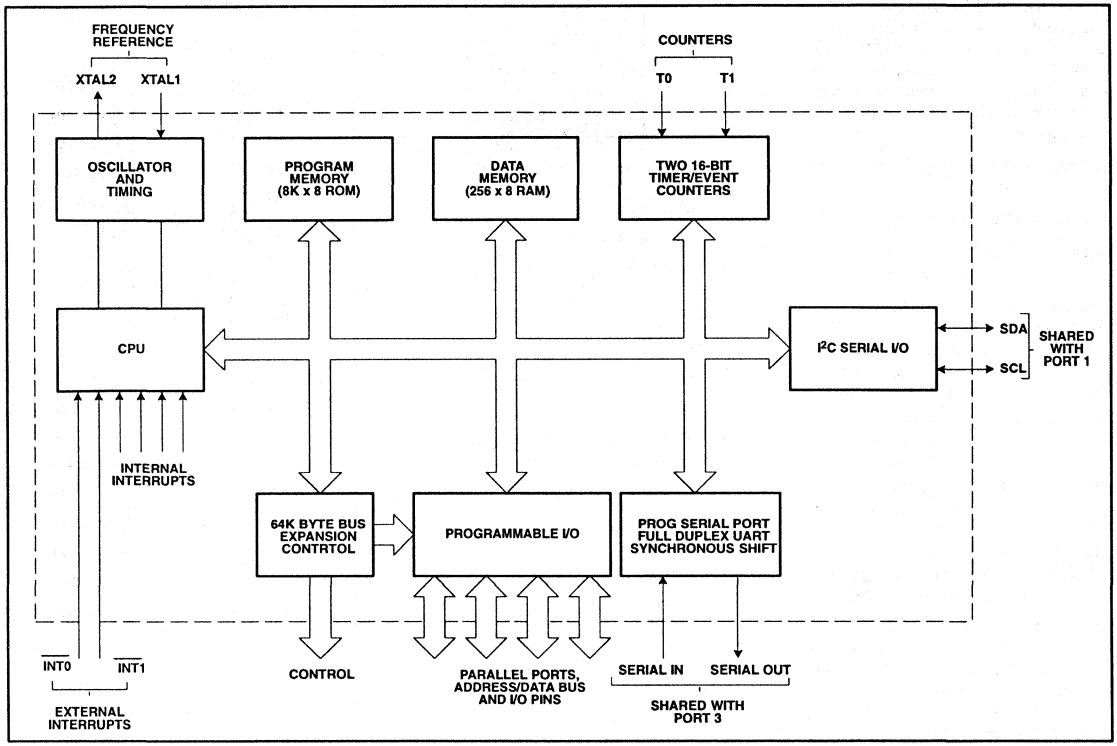
LOGIC SYMBOL



PIN CONFIGURATIONS



BLOCK DIAGRAM



CMOS single-chip 8-bit microcontroller with on-chip EEPROM

80C851/83C851

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The Philips 80C851/83C851 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The 80C851/83C851 has the same instruction set as the 80C51. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. The Philips epitaxial substrate minimizes latch-up sensitivity.

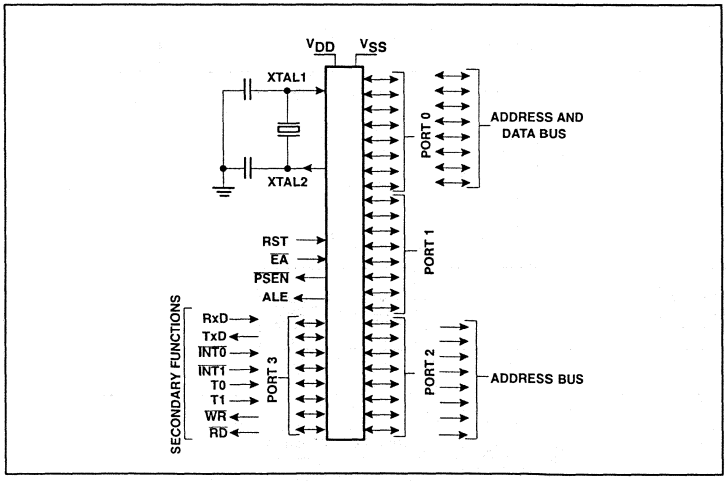
The 80C851/83C851 contains a 4k × 8 ROM with mask-programmable ROM code protection, a 128 × 8 RAM, 256 × 8 EEPROM, 32 I/O lines, two 16-bit counter/timers, a seven-source, five vector, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the 80C851/83C851 has two software selectable modes of power reduction — idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM and EEPROM contents but freezes the oscillator, causing all other chip functions to be inoperative.

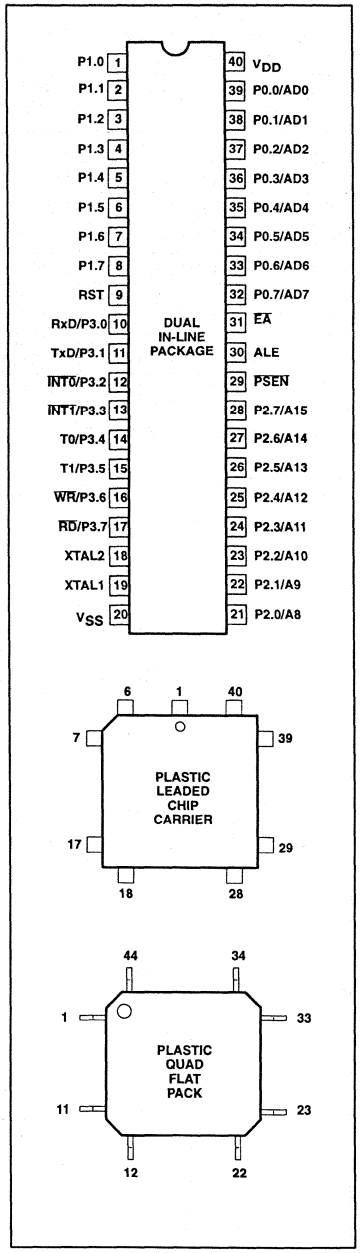
FEATURES

- 80C51 based architecture
  - 4k × 8 ROM
  - 128 × 8 RAM
  - Two 16-bit counter/timers
  - Full duplex serial channel
  - Boolean processor
- Non-volatile 256 × 8-bit EEPROM (electrically erasable programmable read only memory)
  - On-chip voltage multiplier for erase/write
  - 50,000 erase/write cycles per byte
  - 10 years non-volatile data retention
  - Infinite number of read cycles
  - User selectable security mode
  - Block erase capability
- Mask-programmable ROM code protection
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- 1.2 to 16MHz
- Three package styles
- Three temperature ranges
- ROM code protection

LOGIC SYMBOL



PIN CONFIGURATIONS

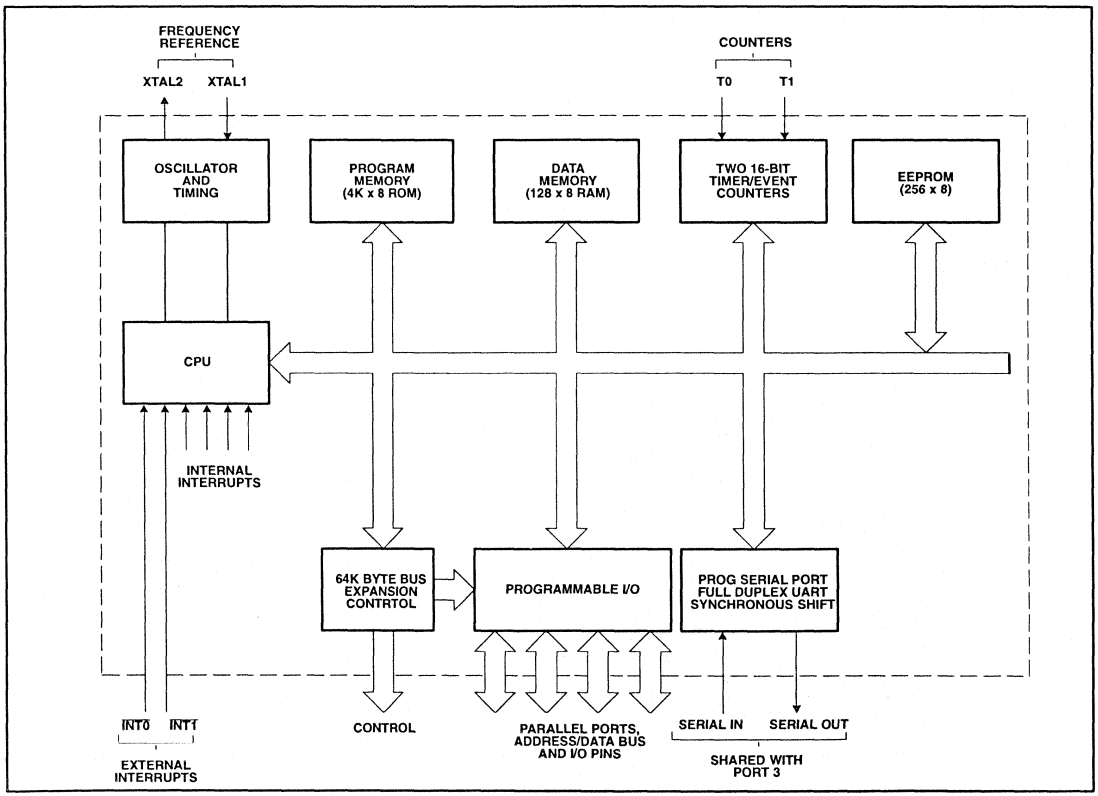


ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		NORTH AMERICA PHILIPS PART ORDER NUMBER		TEMPERATURE RANGE °C AND PACKAGE	FREQ. (MHz)	DRAWING NUMBER
ROMless Version	ROM Version	ROMless Version	ROM Version			
P80C851 FBP	P83C851 FBP	S80C851-4N40	S83C851-4N40	0 to +70, Plastic Dual In-line Package	1.2 to 16	SOT129
P80C851 FBA	P83C851 FBA	S80C851-4A44	S83C851-4A44	0 to +70, Plastic Leaded Chip Carrier	1.2 to 16	SOT187
P80C851 FBB	P83C851 FBB	S80C851-4B44	S83C851-4B44	0 to +70, Plastic Quad Flat Pack	1.2 to 16	SOT307-2 [1]
P80C851 FFP	P83C851 FFP	S80C851-5N40	S83C851-5N40	–40 to +85, Plastic Dual In-line Package	1.2 to 16	SOT129
P80C851 FFA	P83C851 FFA	S80C851-5A44	S83C851-5A44	–40 to +85, Plastic Leaded Chip Carrier	1.2 to 16	SOT187
P80C851 FFB	P83C851 FFB	S80C851-5B44	S83C851-5B44	–40 to +85, Plastic Quad Flat Pack	1.2 to 16	SOT307-2 [1]
P80C851 FHP	P83C851 FHP	S80C851-6N40	S83C851-6N40	–40 to +125, Plastic Dual In-line Package	1.2 to 16	SOT129
P80C851 FHA	P83C851 FHA	S80C851-6A44	S83C851-6A44	–40 to +125, Plastic Leaded Chip Carrier	1.2 to 16	SOT187
P80C851 FHB	P83C851 FHB	S80C851-6B44	S83C851-6B44	–40 to +125, Plastic Quad Flat Pack	1.2 to 16	SOT307-2 [1]

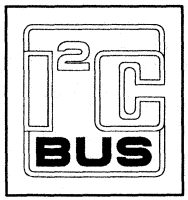
NOTE:
1. SOT311 replaced by SOT307-2.

BLOCK DIAGRAM



Single-chip 8-bit microcontroller — 80CE558/83CE558/89CE558

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET



GENERAL DESCRIPTION

The 80CE558/83CE558/89CE558 (hereafter generically referred to as 8XCE558) Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 8XCE558 has the same instruction set as the 80C51. Three versions of the derivative exist:

- 83CE558 — 32k bytes mask programmable ROM
- 80CE558 — ROMless version of the 83CE558
- 89CE558 — 32k bytes FEEPROM

The 8XCE558 contains a non-volatile 32k × 8 read-only program memory (83CE558) or FEEPROM (89CE558), a volatile 1024 × 8 read/write data memory, five 8-bit I/O ports, one 8-bit input port, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority- level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I²C-bus), a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XCE558 can be expanded using standard TTL compatible memories and logic.

In addition, the 8XCE558 has two software selectable modes of power reduction — idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial ports, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte, and 17 three-byte. With a 16 MHz system clock, 58% of the instructions are executed in 0.75µs and 40% in 1.5µs. Multiply and divide instructions require 3µs.

FEATURES

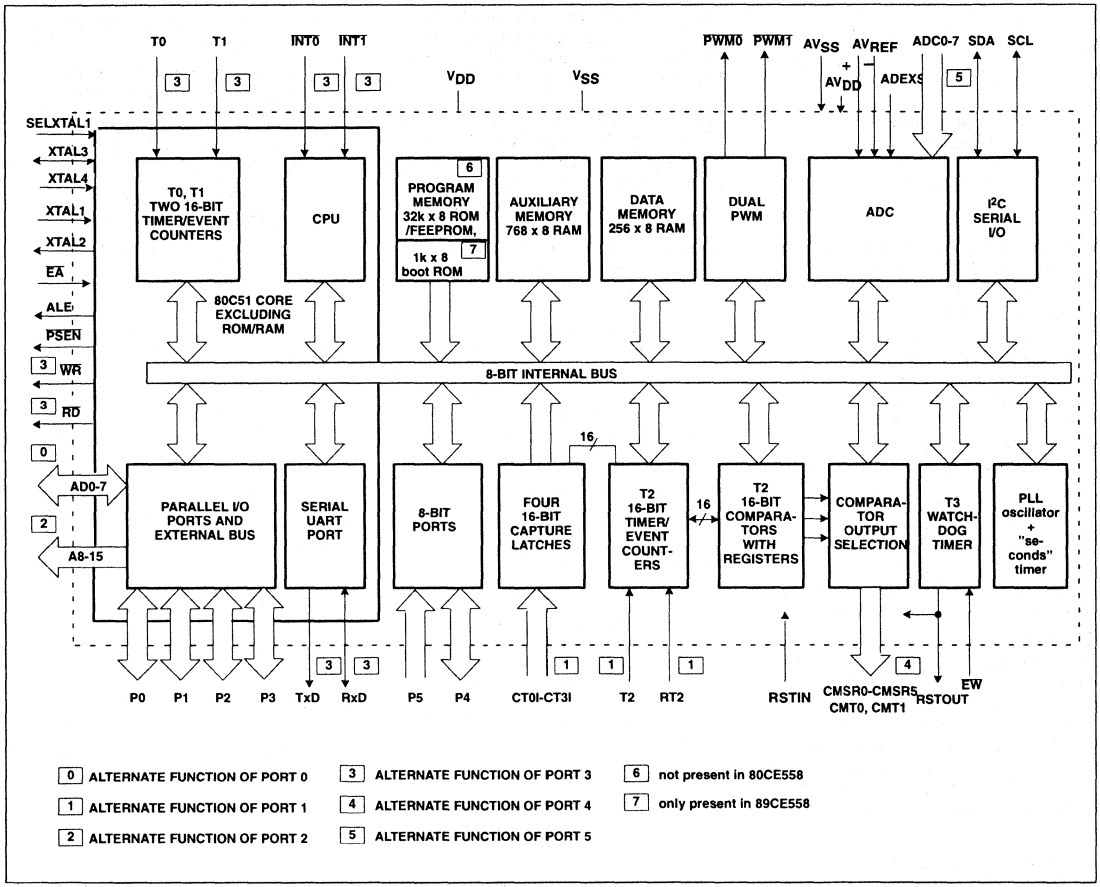
- 80C51 central processing unit
- 32k × 8 ROM resp. FEEPROM expandable externally to 64k bytes
- ROM/FEEPROM Code protection
- 1024 × 8 RAM, expandable externally to 64k bytes
- Seconds Timer
- Two standard 16-bit timer/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- A 10-bit ADC with eight multiplexed analog inputs and programmable autoscan
- Two 8-bit resolution, pulse width modulation outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- I²C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- 15 interrupt sources with 2 priority levels (2 to 6 external sources possible)
- Extended temperature range (–40 to +85°C)
- 4.5 to 5.5V supply voltage range
- Frequency range for 80C51 standard oscillator: 3.5 MHz to 16 MHz
- PLL oscillator with 32 kHz reference and software-selectable system clock frequency[1]
- Software enable/disable of ALE output pulse
- Electromagnetic compatibility improvements
- Wake-up from Power-down by external or seconds interrupt

Note 1 Not available yet in the 89CE558

ORDERING INFORMATION

ROMless	ROM	EPROM	TEMPERATURE RANGE °C AND PACKAGE	FREQUENCY MHz	DRAWING NUMBER
80CE558EBB	83CE558EBB	89CE558EBB	0 to +70, 80-Pin Plastic Quad Flat Pack	3.5 to 16	SOT318
80CE558EFB	83CE558EFB	89CE558EFB	–40 to +85, 80-Pin Plastic Quad Flat Pack	3.5 to 16	SOT318

BLOCK DIAGRAM



CMOS single-chip 8-bit microcontroller with Electromagnetic Compatibility improvements

80CE654/83CE654

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The 83CE654 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 83CE654 has the same instruction set as the 80C51. Two versions of the derivative exist:

83CE654 — 16k bytes mask programmable ROM, 256 bytes RAM

80CE654 — ROMless version of the 83CE654

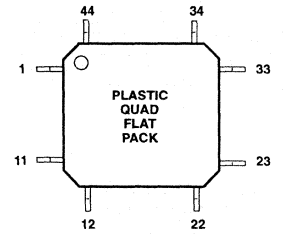
This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 8XCE654 contains a non-volatile 16k × 8 read-only program memory (83CE654), a volatile 256 × 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XCE654 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 16MHz crystal, 58% of the instructions are executed in 0.75µs and 40% in 1.5µs. Multiply and divide instructions require 3µs.

FEATURES

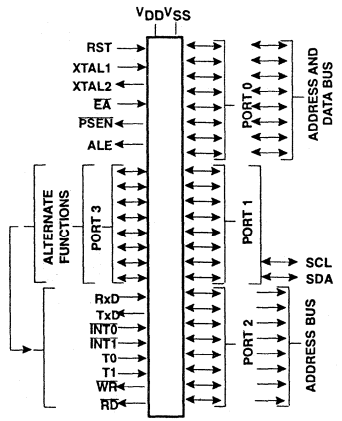
- 80C51 central processing unit
- 16k × 8 ROM expandable externally to 64k bytes
- 256 × 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART facilities
- ROM code protection
- XTAL frequency range: 1.2MHz to 16MHz
- Software enable/disable of ALE output pulse
- Electromagnetic compatibility (EMC) improvements
- Operating ambient temperature range:
  - P83CE654 FBB T_{amb} 0°C to +70°C
  - P83CE654 FFB T_{amb} −40°C to +85°C

PIN CONFIGURATION



Pin	Function	Pin	Function
1	P1.5	23	P2.5/A13
2	P1.6/SCL	24	P2.6/A14
3	P1.7/SDA	25	P2.7/A15
4	RST	26	$\overline{PSEN}$
5	P3.0/RxD	27	ALE
6	V_{SS4}	28	V_{SS2}
7	P3.1/TxD	29	$\overline{EA}$
8	P3.2/$\overline{INT0}$	30	P0.7/AD7
9	P3.3/$\overline{INT1}$	31	P0.6/AD6
10	P3.4/T0	32	P0.5/AD5
11	P3.5/T1	33	P0.4/AD4
12	P3.6/$\overline{WR}$	34	P0.3/AD3
13	P3.7/$\overline{RD}$	35	P0.2/AD2
14	XTAL2	36	P0.1/AD1
15	XTAL1	37	P0.0/AD0
16	V_{SS1}	38	V_{DD2}
17	V_{DD1}	39	V_{SS3}
18	P2.0/A8	40	P1.0
19	P2.1/A9	41	P1.1
20	P2.2/A10	42	P1.2
21	P2.3/A11	43	P1.3
22	P2.4/A12	44	P1.4

LOGIC SYMBOL



ORDERING INFORMATION

ROMless	ROM	TEMPERATURE RANGE °C AND PACKAGE	FREQUENCY MHz	DRAWING NUMBER
P80CE654FBB	P83CE654FBB	0 to +70, Plastic Quad Flat Pack	1.2 to 16	SOT307-2[1]
P80CE654FFB	P83CE654FFB	–40 to +85, Plastic Quad Flat Pack	1.2 to 16	SOT307-2[1]

NOTE:
1. SOT311 replaced by SOT307-2.

ELECTROMAGNETIC COMPATIBILITY (EMC) IMPROVEMENTS

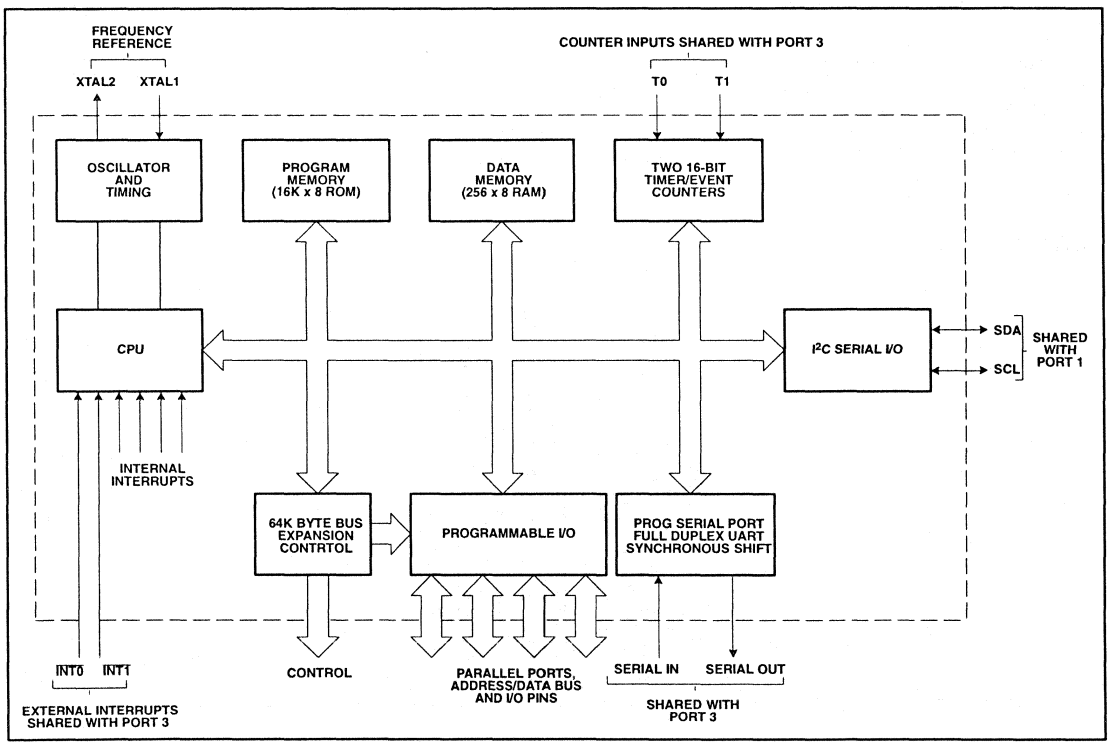
Primary attention is paid on the reduction of electromagnetic emission of the microcontroller P83CE654.

The following features effect in reducing the electromagnetic emission and additionally improve the electromagnetic susceptibility:

- Two supply voltage pins (V_{DD1}, V_{DD2}) and four ground pins (V_{SS1} to V_{SS4})
- Separate V_{DD} pins for the internal logic and the port buffers
- Internal decoupling capacitance improves the EMC radiation behavior and the EMC immunity
- External capacitors are to be located as close as possible between pins V_{DD2} and V_{SS3} as well as V_{DD1} and V_{SS1}; ceramic chip capacitors are recommended (100nF).
- The ALE output signal (pulses at a frequency of $f_{OSC}/6$) can be disabled under software control (bit 5 in the SFR PCON: "RFI"); if disabled, no ALE pulse will occur.

ALE pin will be pulled down internally, switching an external address latch to a quiet state. The MOVX instruction will still toggle ALE as a normal MOVX. ALE will retain its normal high value during Idle mode and a low value during Power-down mode while in the "RFI" reduction mode. Additionally during internal access ($\overline{EA}$ = 1) ALE will toggle normally when the address exceeds the internal program memory size. During external access ($\overline{EA}$ = 0) ALE will always toggle normally, whether the flag "RFI" is set or not.

BLOCK DIAGRAM



Low-voltage single-chip 8-bit microcontrollers — 80CL31/80CL51

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

FEATURES

- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM, 1/0 in a single 40-lead DIL / mini-pack
- 4K x 8 ROM, expandable externally to 64K bytes
- 128 bytes RAM, expandable externally to 64K bytes
- Four 8-bit ports, 321/0 lines
- Two 16-bit timer / event counters
- External memory expandable up to 128K, external ROM up to 64K and / or RAM up to 64K
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Thirteen source, thirteen vector interrupt structure with two priority levels
- Full duplex serial port (UART)
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four eight byte RAM register banks
  - stack depth up to 128 bytes
  - multiply, divide, subtract and compare instructions
- Power-Down and IDLE instructions
- Wake-up via external interrupts at Port 1
- Single supply voltage of 1.8V to 6.0V (5.0V ±10% for P80C51)
- Frequency range of 0 to 16MHz (3.5MHz to 16MHz for P80C51)
- Very low current consumption
- Operating temperature range: -40 to +85°C

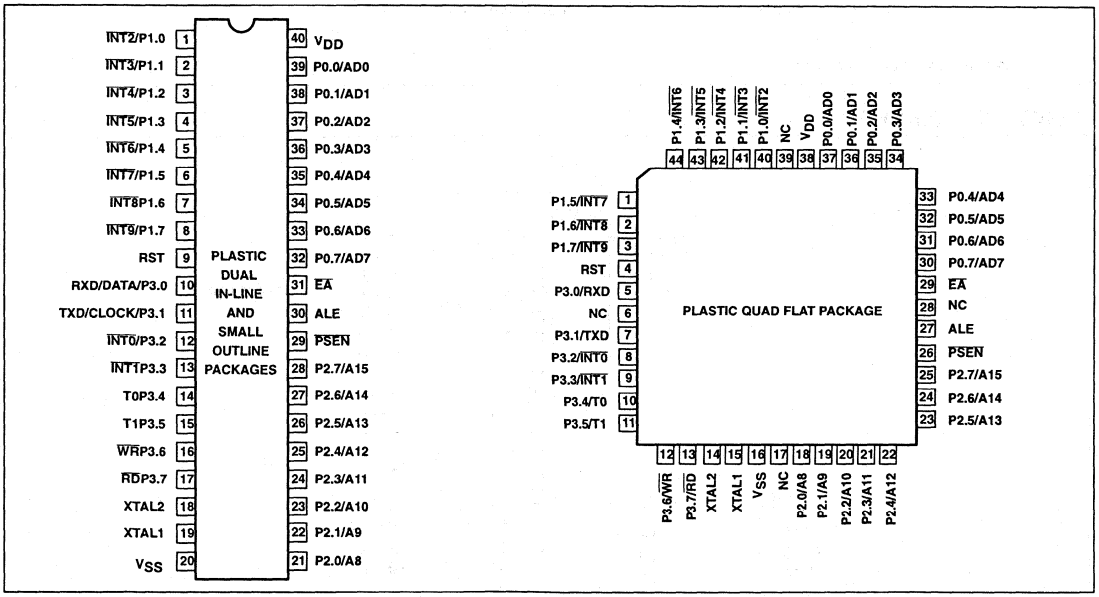
DESCRIPTION

The 80CL51 is manufactured in an advanced CMOS technology. The instruction set of the 80CL51 is based on that of the 8051. The 80CL51 is a general purpose microcontroller especially suited for battery-powered applications. The device has low power consumption and a wide range of supply voltage. For emulation purposes, the 85CL000 (Piggy-back version) with 256 bytes of RAM is recommended. The 80CL51 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The 80CL51 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte.

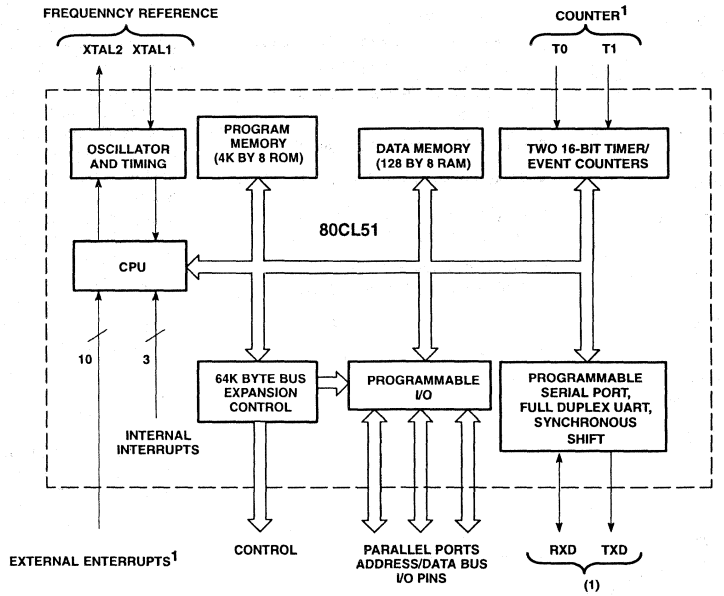
The P80CL31 is the ROMless version of the P80CL51. P80C51 is a 5V version of the low voltage P80CL51.

The P80CL31 is the ROMless version of the P80CL51. P80C51 is a 5V version of the low voltage P80CL51.

PIN CONFIGURATIONS

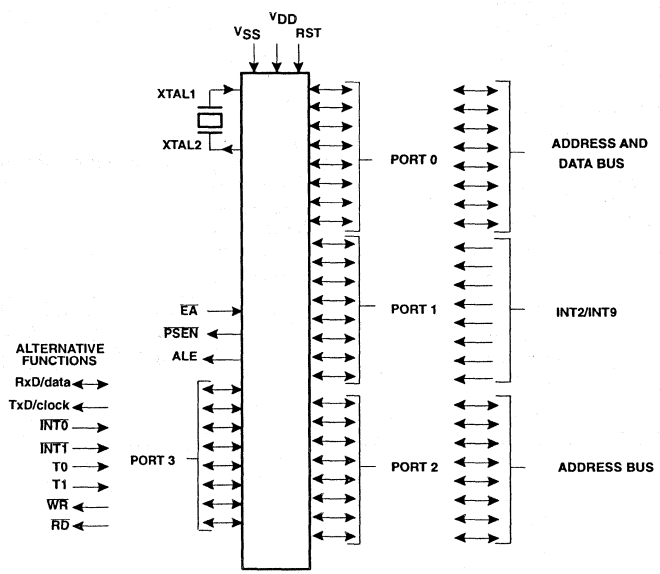


BLOCK DIAGRAM



1. Pins shared with parallels ports pins.

FUNCTIONAL DIAGRAM



Low voltage/low power single-chip 8-bit microcontroller with I²C

80CL410/83CL410

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The 80CL410/83CL410 (hereafter generically referred to as 8XCL410) is manufactured in an advanced CMOS process that allows the part to operate at supply voltages down to 1.8V and oscillator frequencies down to DC. The 8XCL410 has the same instruction set as the 80C51.

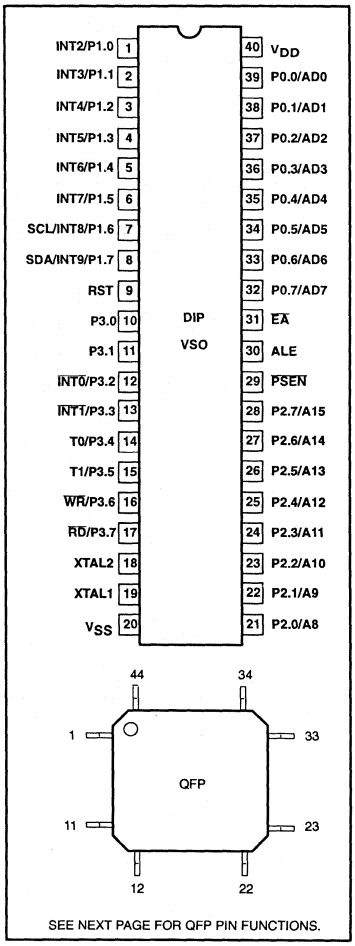
The 8XCL410 features a 4k byte ROM (83CL410), 128 bytes RAM (both ROM and RAM are externally expandable to 64k bytes), four 8-bit ports, two 16-bit timer/counters, an I²C serial interface, a thirteen source, two priority level nested interrupt structure, and on-chip oscillator circuitry suitable for quartz crystal, ceramic resonator, RC, or LC.

The 8XCL410 has two reduced power modes that are the same as those on the standard 80C51. The special reduced power feature of this part is that it can be stopped and then restarted. Running from an external clock source, the clock can be stopped and after a period of time restarted. The 8XCL410 will resume operation from where it was when the code stopped with no loss of internal state, RAM contents, or Special Function Register contents. If the internal oscillator is used the part cannot be stopped and started, but the power-down mode, which can be terminated via an interrupt, can be used to achieve similar power savings and then restart without loss of on-chip RAM and Special Function Register values.

FEATURES

- Single supply voltage 1.8V to 6.0V
- Frequency from DC to 12MHz
- 80C51 based architecture
  - 4k × 8 ROM (64k external)
  - 128 × 8 RAM (64k external)
  - Four 8-bit I/O ports
  - Two 16-bit timer/counters
  - A thirteen-source, two-level, nested priority interrupt structure
  - 10 external interrupts
- Fully static 80C51 CPU
- I²C Serial Interface
- Two power control modes
  - Idle mode
  - Power-down mode – can be terminated by reset or external interrupt
- Wake-up via external interrupts at port 1
- Single supply voltage 1.8V to 6.0V
- Frequency range of DC to 12MHz
- On-chip oscillator (quartz crystal, ceramic resonator, RC, LC)
- Very low power consumption
- Operating temperature range: –40 to +85°C

PIN CONFIGURATION



SEE NEXT PAGE FOR QFP PIN FUNCTIONS.

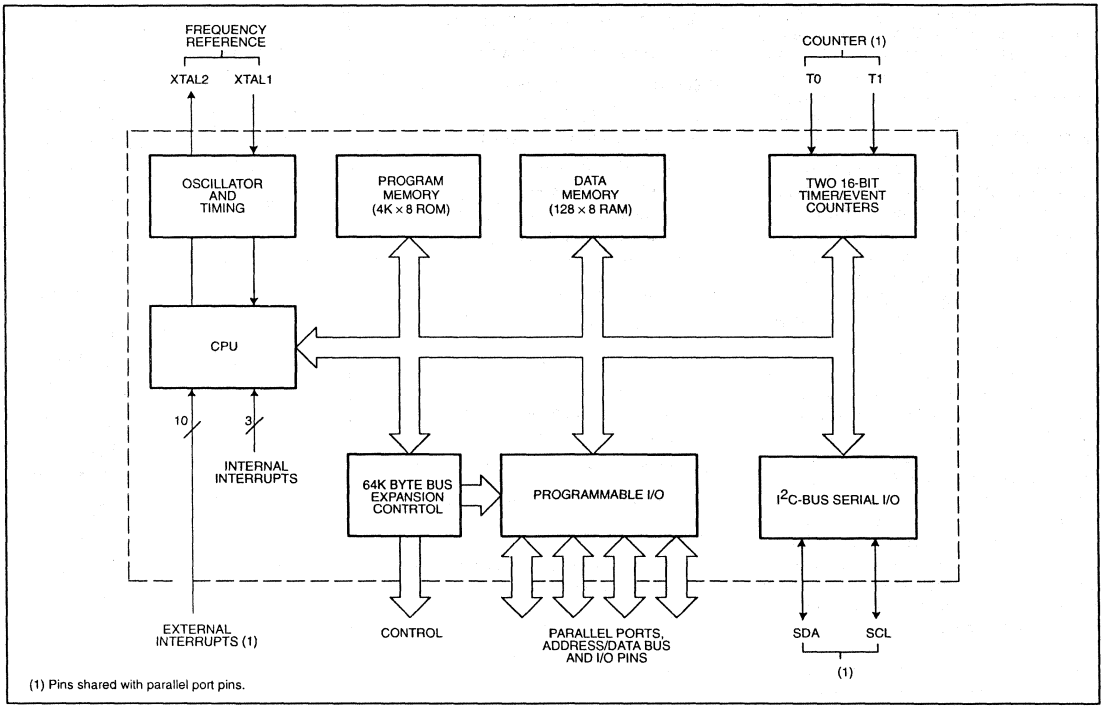
ORDERING CODE

PHILIPS PART ORDER NUMBER PART MARKING		PHILIPS NORTH AMERICA PART ORDER NUMBER[1]		TEMPERATURE °C AND PACKAGE	FREQUENCY	Drawing Number
ROMless	ROM	ROMless	ROM			
P80CL410HFP	P83CL410HFP	P80CL410HF N	P83CL410HF N	–40 to +85, 40-Pin Plastic Dual In-line Package	32kHZ to 12MHz	SOT129
P80CL410HFT	P83CL410HFT	P80CL410HF D	P83CL410HF D	–40 to +85, 40-Pin Plastic Very Small Outline Package	32kHZ to 12MHz	SOT158A
	P83CL410HFH			–40 to +85, 44-Pin Plastic Quad Flat Pack	32kHZ to 12MHz	SOT307B

NOTE:
1. Parts ordered by the Philips North America part number will be marked with the Philips part marking.

For emulation purposes, the P85CL000 (Piggyback version) with 256 bytes of RAM is recommended.

BLOCK DIAGRAM



(1) Pins shared with parallel port pins.

Low-voltage single-chip 8-bit microcontroller — 80CL580/83CL580

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

GENERAL DESCRIPTION

The 83CL580 is manufactured in an advanced CMOS technology. The instruction set of the 83CL580 is based on that of the 8051. The 83CL580 is an 8-bit general purpose microcontroller especially suited for cordless telephones and mobile communication applications. The device has low power consumption and a wide range of supply voltages. For emulation purposes, the 85CL580 (Piggy-back version) with 256 bytes of RAM is recommended. The 83CL580 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The 83CL580 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions:
49 one-byte, 46 two-byte, and 16 three-byte.

FEATURES

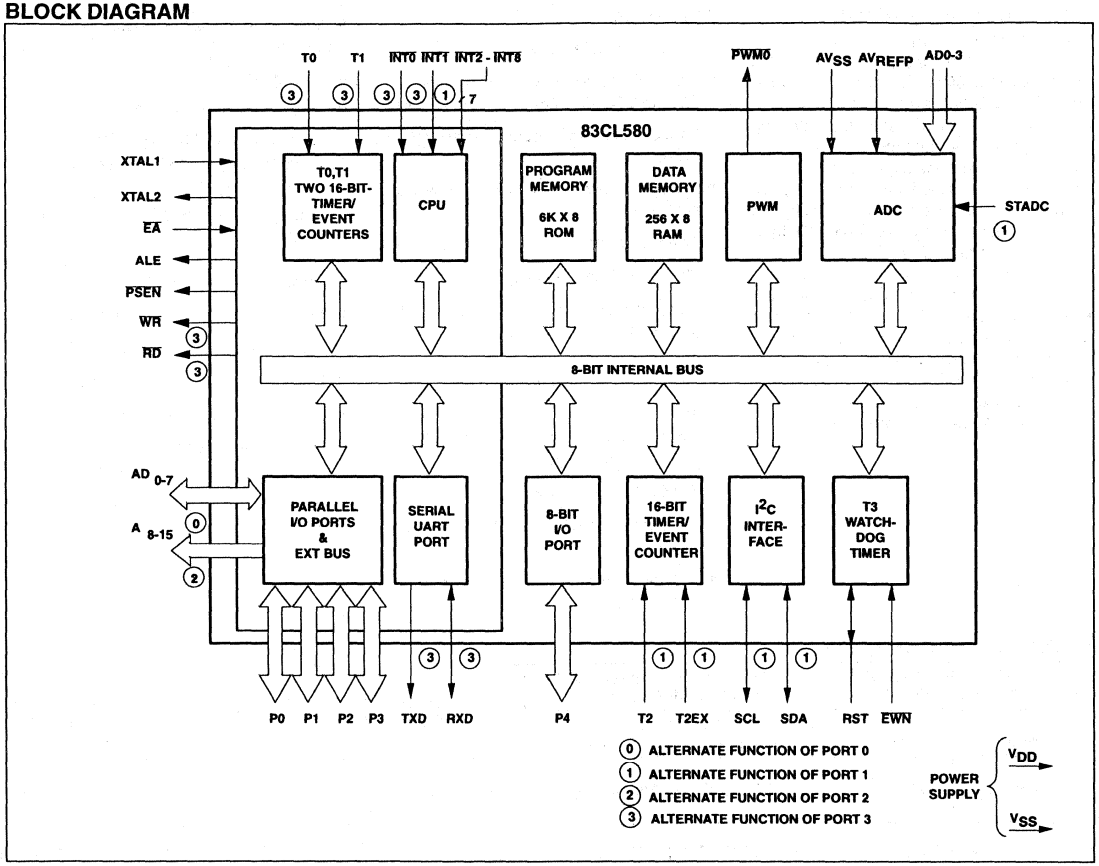
- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM, I/O in a single 56-lead VSO56 or 64-lead QFP64 package
- 6K × 8 ROM, expandable externally to 64K bytes
- 256 bytes RAM, expandable externally to 64K bytes
- Five 8-bit ports, 40 I/O lines
- Three 16-bit timer / event counters
- External memory expandable up to 128K, external ROM up to 64K and / or RAM up to 64K
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Fifteen source, fifteen vector interrupt structure with two priority levels
- Full duplex serial UART
- I^2C-bus interface for serial transfer on two lines
- A/D converter with power-down mode (8-bit, 4 inputs)
- Pulse width modulated output (8-bit resolution)
- Watchdog timer
- Enhanced architecture with:
  - non-page oriented instructions
  - four eight byte RAM register banks
  - direct addressing
  - multiply, divide, subtract and compare instructions
  - stack depth limited only by available internal RAM (max. 256 bytes)
- Power-Down and IDLE instructions
- Wake-up via external interrupts at Port 1
- Single supply voltage of 2.5V to 6.0V
- Frequency range of 0 to 12MHz
- Very low current consumption: typically 4.5mA at 2.5V / 8MHz
- Operating temperature range: –40 to +85°C

ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		PHILIPS NORTH AMERICA [1] PART ORDER NUMBER		TEMPERATURE RANGE °C AND PACKAGE	FREQUENCY	DRAWING NUMBER
ROMless	ROM	ROMless	ROM			
P80CL580HFT	P83CL580HFT	P80CL580HF D	P83CL580HF D	–40 to +85 56-Lead Plastic VSO (Very Small Outline) Dual In-line Package	32KHz to 12MHz	SOT190
P80CL580HFH	P83CL580HFH	P80CL580HF B	P83CL580HF B	–40 to +85 64-Lead Plastic Quad Flat Pack	32KHz to 12MHz	SOT319

NOTE:
1. Parts ordered by the Philips North America part number will be marked with the Philips part marking.

BLOCK DIAGRAM



CMOS single-chip 8-bit microcontroller — 83C654

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The P83C654 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 83C654 has the same instruction set as the 80C51. Two versions of the derivative exist:

83C654 — 16k bytes mask programmable ROM

87C654 — EPROM version (described in a separate data sheet)

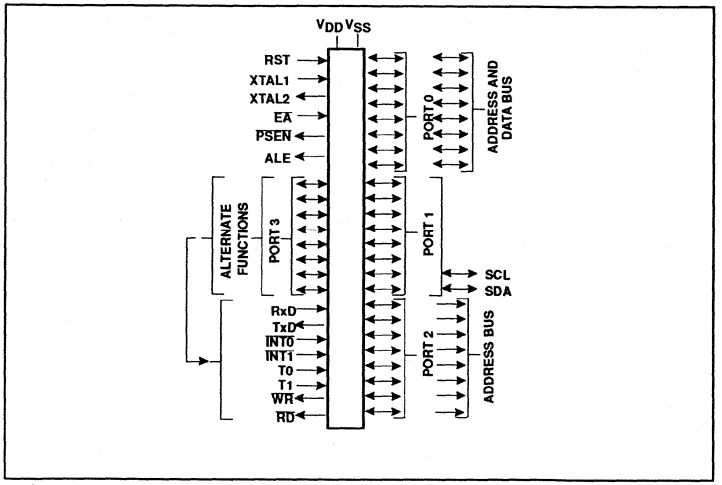
This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 83C654 contains a non-volatile 16k × 8 read-only program memory, a volatile 256 × 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC654 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 16(24)MHz crystal, 58% of the instructions are executed in 0.75(0.5)µs and 40% in 1.5(1)µs. Multiply and divide instructions require 3(2)µs.

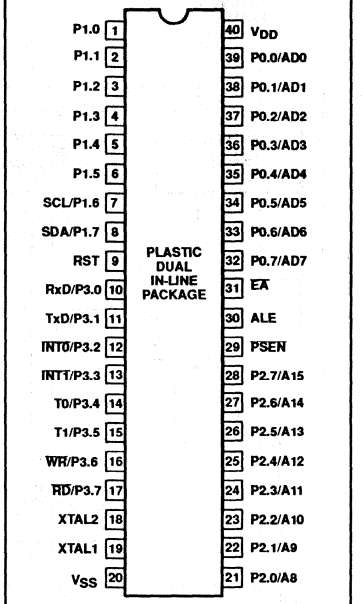
FEATURES

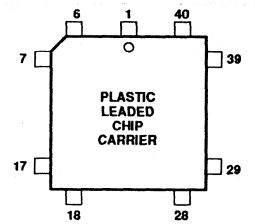
- 80C51 central processing unit
- 16k × 8 ROM expandable externally to 64k bytes
- 256 × 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART facilities
- Power control modes
  - Idle mode
  - Power-down mode
- ROM code protection
- Extended frequency range: 1.2 to 24 MHz
- Three operating ambient temperature ranges:
  - 0 to +70°C
  - –40 to +85°C
  - –40 to +125°C

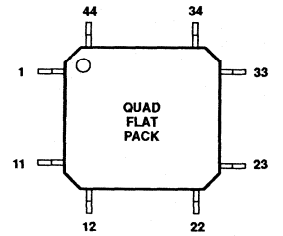
LOGIC SYMBOL



PIN CONFIGURATIONS

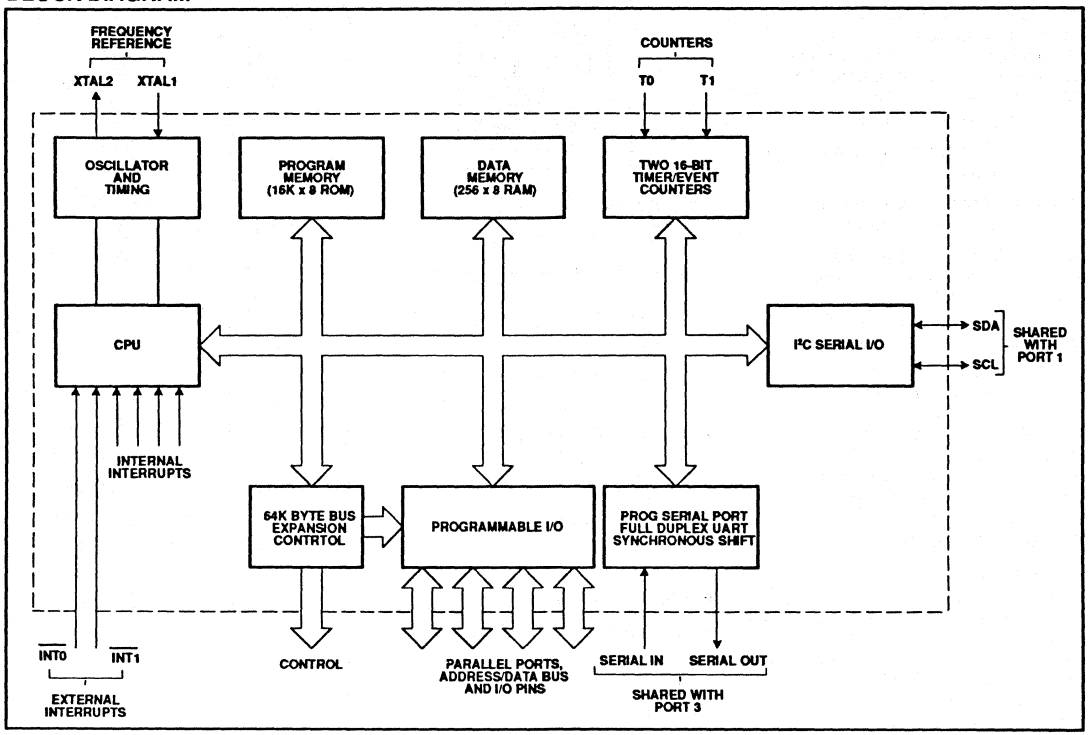






SEE PAGE 984 FOR QFP AND LCC PIN FUNCTIONS.

BLOCK DIAGRAM



CMOS single-chip 8-bit microcontroller — 83C751/87C751

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

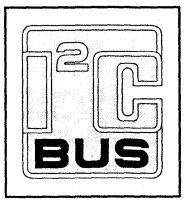
DESCRIPTION

The Philips 83C751/87C751 offers the advantages of the 80C51 architecture in a small package and at low cost.

The 8XC751 Microcontroller is fabricated with Philips high-density CMOS technology. Philips epitaxial substrate minimizes CMOS latch-up sensitivity.

The 8XC751 contains a 2k × 8 ROM (83C751) EPROM (87C751), a 64 × 8 RAM, 19 I/O lines, a 16-bit auto-reload counter/timer, a five-source, fixed-priority level interrupt structure, a bidirectional inter-integrated circuit (I^2C) serial bus interface, and an on-chip oscillator.

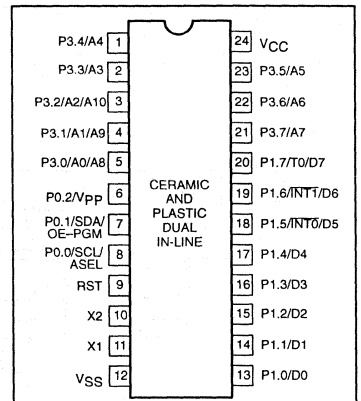
The on-board inter-integrated circuit (I^2C) bus interface allows the 8XC751 to operate as a master or slave device on the I^2C small area network. This capability facilitates I/O and RAM expansion, access to EEPROM, processor-to-processor communication, and efficient interface to a wide variety of dedicated I^2C peripherals.

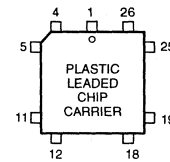


FEATURES

- 80C51 based architecture
- Inter-Integrated Circuit (I^2C) serial bus interface
- Small package sizes
  - 24-pin DIP (300 mil "skinny DIP")
  - 28-pin PLCC
- 87C751 available in erasable quartz lid or one-time programmable plastic packages
- Wide oscillator frequency range
- Low power consumption:
  - Normal operation: less than 11mA @ 5V, 12MHz
  - Idle mode
  - Power-down mode
- 2k × 8 ROM (83C751)
  2k × 8 EPROM (87C751)
- 64 × 8 RAM
- 16-bit auto reloadable counter/timer
- Fixed-rate timer
- Boolean processor
- CMOS and TTL compatible
- Well suited for logic replacement, consumer and industrial applications
- LED drive outputs

PIN CONFIGURATIONS





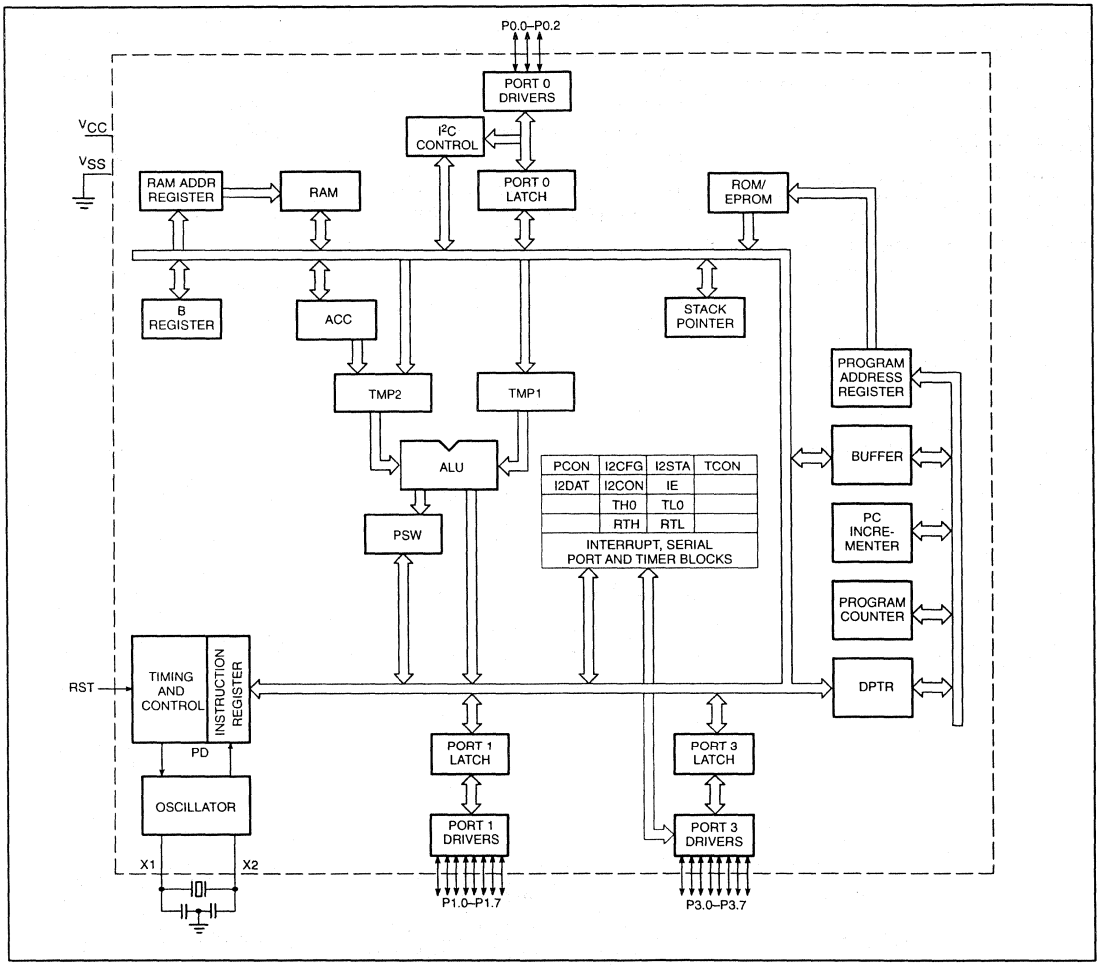
Pin	Function	Pin	Function
1	P3.4/A4	15	P1.0/D0
2	P3.3/A3	16	P1.1/D1
3	P3.2/A2/A10	17	P1.2/D2
4	P3.1/A1/A9	18	P1.3/D3
5	N.C.	19	P1.4/D4
6	P3.0/A0/A8	20	P1.5/INT0/D5
7	P0.2/V_{PP}	21	N.C.
8	P0.1/SDA/OE–PGM	22	N.C.
9	P0.0/SCL/ASEL	23	P1.6/INT1/D6
10	N.C.	24	P1.7/T0/D7
11	RST	25	P3.7/A7
12	X2	26	P3.6/A6
13	X1	27	P3.5/A5
14	V_{SS}	28	V_{CC}

ORDERING INFORMATION

ROM	EPROM[1]		TEMPERATURE RANGE °C AND PACKAGE	FREQUENCY MHz	DRAWING NUMBER
	S87C751–1F24	UV	0 to +70, Ceramic Dual In-line Package	3.5 to 12	0586B
	S87C751–2F24	UV	–40 to +85, Ceramic Dual In-line Package	3.5 to 12	0586B
	S87C751–4F24	UV	0 to +70, Ceramic Dual In-line Package	3.5 to 16	0586B
	S87C751–5F24	UV	–40 to +85, Ceramic Dual In-line Package	3.5 to 16	0586B
S83C751–1N24	S87C751–1N24	OTP	0 to +70, Plastic Dual In-line Package	3.5 to 12	0410D
S83C751–2N24	S87C751–2N24	OTP	–40 to +85, Plastic Dual In-line Package	3.5 to 12	0410D
S83C751–4N24	S87C751–4N24	OTP	0 to +70, Plastic Dual In-line Package	3.5 to 16	0410D
S83C751–5N24	S87C751–5N24	OTP	–40 to +85, Plastic Dual In-line Package	3.5 to 16	0410D
S83C751–1A28	S87C751–1A28	OTP	0 to +70, Plastic Leaded Chip Carrier	3.5 to 12	0401F
S83C751–2A28	S87C751–2A28	OTP	–40 to +85, Plastic Leaded Chip Carrier	3.5 to 12	0401F
S83C751–4A28	S87C751–4A28	OTP	0 to +70, Plastic Leaded Chip Carrier	3.5 to 16	0401F
S83C751–5A28	S87C751–5A28	OTP	–40 to +85, Plastic Leaded Chip Carrier	3.5 to 16	0401F

NOTE:
1. OTP = One Time Programmable EPROM. UV = UV Erasable EPROM.

BLOCK DIAGRAM



CMOS single-chip 8-bit microcontroller — 83C752/87C752

CMOS single-chip 8-bit microcontroller with A/D, PWM

DESCRIPTION

The Philips 83C752/87C752 offers many of the advantages of the 80C51 architecture in a small package and at low cost.

The 8XC752 Microcontroller is fabricated with Philips high-density CMOS technology. Philips epitaxial substrate minimizes CMOS latch-up sensitivity.

The 8XC752 contains a 2k × 8 ROM (83C752) EPROM (87C752), a 64 × 8 RAM, 21 I/O lines, a 16-bit auto-reload counter/timer, a fixed-priority level interrupt structure, a bidirectional inter-integrated circuit (I^2C) serial bus interface, an on-chip oscillator, a five channel multiplexed 8-bit A/D converter, and an 8-bit PWM output.

The onboard inter-integrated circuit (I^2C) bus interface allows the 8XC752 to operate as a master or slave device on the I^2C small area network. This capability facilitates I/O and RAM expansion, access to EEPROM, processor-to-processor communication, and efficient interface to a wide variety of dedicated I^2C peripherals.

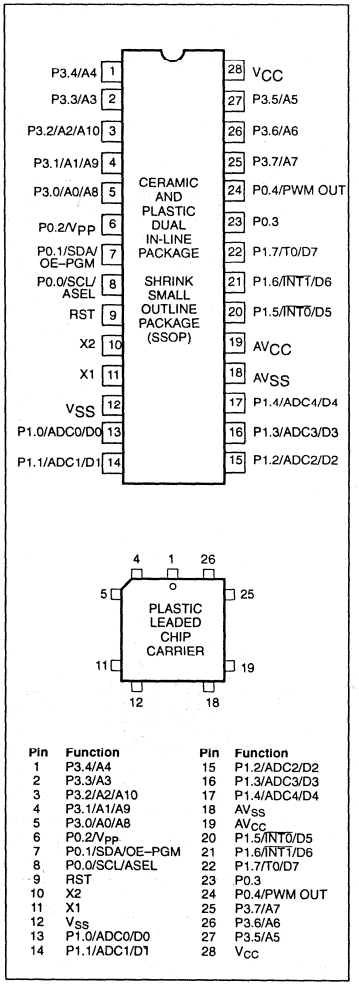
The EPROM version of this device, the 87C752, is also available in both quartz-lid erasable and plastic one-time programmable (OTP) packages. Once the array has been programmed, it is functionally equivalent to the masked ROM 83C752. Thus, unless explicitly stated otherwise, all references made to the 83C752 apply equally to the 87C752.

The 83C752 supports two power reduction modes of operation referred to as the idle mode and the power-down mode.

FEATURES

- Available in erasable quartz lid or One-Time Programmable plastic packages
- 80C51 based architecture
- Inter-integrated Circuit (I^2C) serial bus interface
- Small package sizes
  - 28-pin DIP
  - 28-pin PLCC
  - 28-pin SSOP
- Wide oscillator frequency range
- Low power consumption:
  - Normal operation: less than 11mA @ 5V, 12MHz
  - Idle mode
  - Power-down mode
- 2k × 8 ROM (83C752) EPROM (87C752)
- 64 × 8 RAM
- 16-bit auto reloadable counter/timer
- 5-channel 8-bit A/D converter
- 8-bit PWM output/timer
- Fixed-rate timer
- Boolean processor
- CMOS and TTL compatible
- Well suited for logic replacement, consumer and industrial applications

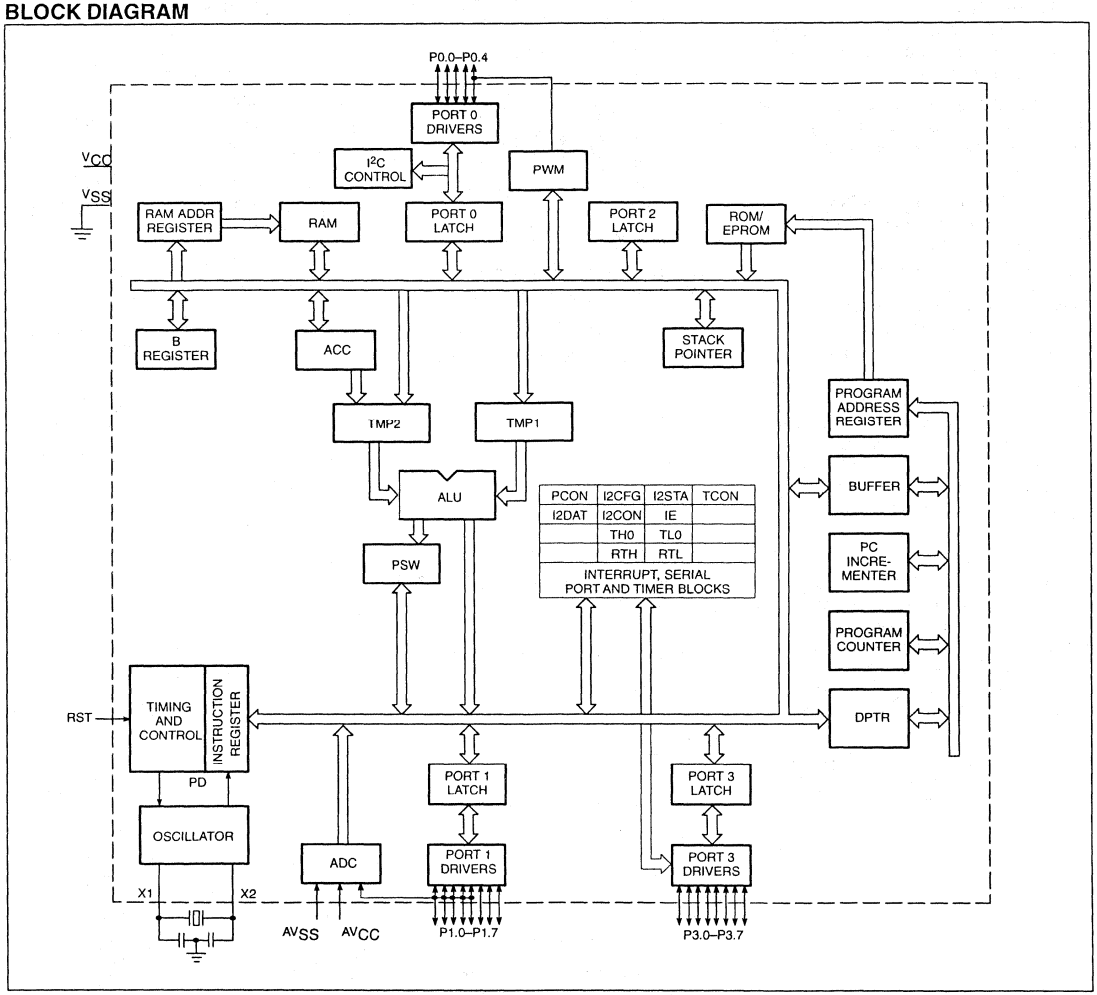
PIN CONFIGURATION



Pin	Function	Pin	Function
1	P3.4/A4	15	P1.2/ADC2/D2
2	P3.3/A3	16	P1.3/ADC3/D3
3	P3.2/A2/A10	17	P1.4/ADC4/D4
4	P3.1/A1/A9	18	AV_{SS}
5	P3.0/A0/A8	19	AV_{CC}
6	P0.2/V_{PP}	20	P1.5/$\overline{INT0}$/D5
7	P0.1/SDA/OE–PGM	21	P1.6/$\overline{INT1}$/D6
8	P0.0/SCL/ASEL	22	P1.7/T0/D7
9	RST	23	P0.3
10	X2	24	P0.4/PWM OUT
11	X1	25	P3.7/A7
12	V_{SS}	26	P3.6/A6
13	P1.0/ADC0/D0	27	P3.5/A5
14	P1.1/ADC1/D1	28	V_{CC}

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

BLOCK DIAGRAM



Low-voltage single-chip 8-bit microcontrollers — 83CL781/83CL782

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

GENERAL DESCRIPTION

The 83CL781 and 83CL782 are manufactured in an advanced CMOS technology. The instruction set of the 83CL781/83CL782 is based on that of the 8051. The 83CL781/83CL782 is an 8-bit general purpose microcontroller especially suited for cordless telephone applications. The device has low power consumption and a wide range of supply voltage. For emulation purposes, the 85CL782 (Piggy-back version) with 256 bytes of RAM is recommended. The 83CL781/83CL782 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The 83CL781/83CL782 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte.

The 83CL782 is a faster version of the 83CL781 with a maximum speed of 12MHz at $V_{DD} \geq 3.1V$.

FEATURES

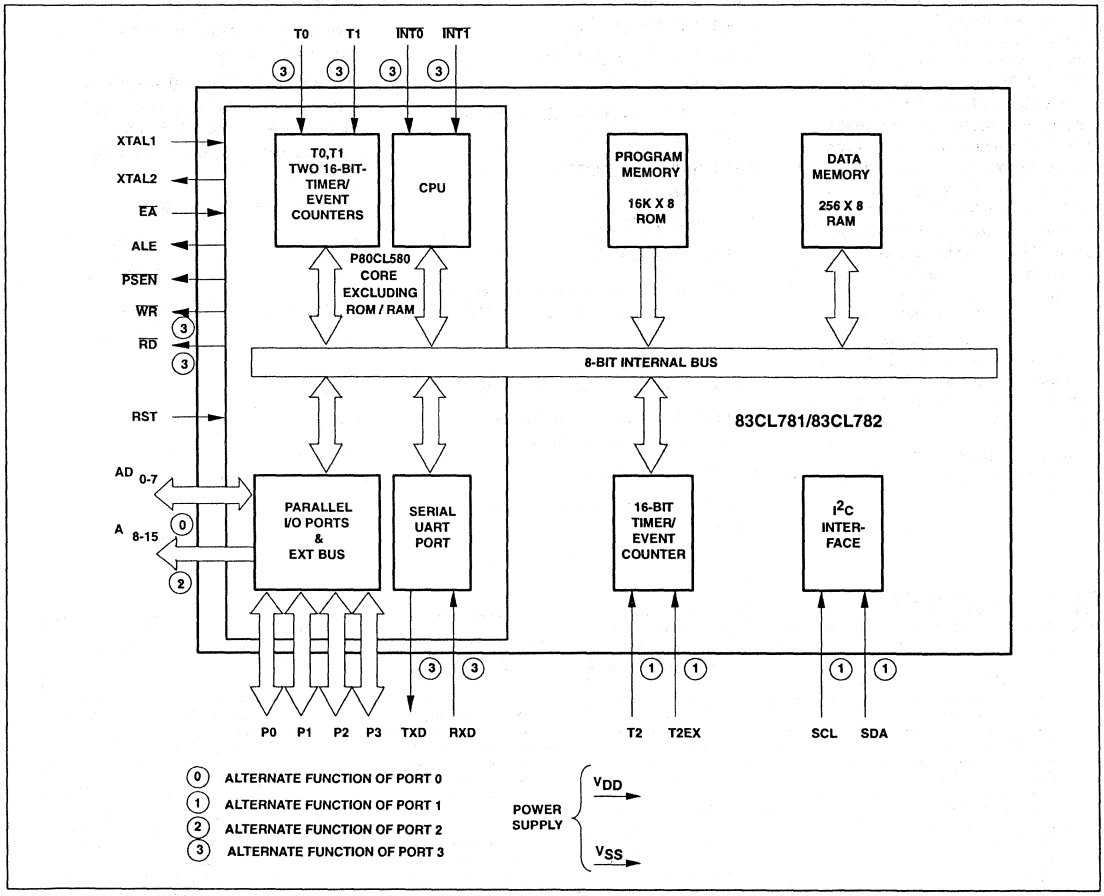
- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM, I/O in a single package
- 16K × 8 ROM, expandable externally to 64K bytes
- 256 bytes RAM, expandable externally to 64K bytes
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- External memory expandable up to 128K, external ROM up to 64K and/or RAM up to 64K
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Fifteen source, fifteen vector interrupt structure with two priority levels
- Full duplex serial UART
- I^2C bus interface for serial transfer on two lines.
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four eight-byte RAM register banks
  - stack depth limited only by available internal RAM (max. 256 bytes)
  - multiply, divide, subtract and compare instructions
- Power-down and IDLE instructions
- Wake-up via external interrupts at Port 1
- Single supply voltage of 1.8V to 6.0V
- Frequency range of DC to 12MHz
- 12MHz operation at 3.1V (8XCL782)
- Very low current consumption, typ 8mA at 12MHz/3.1V
- Operating temperature range:
  - 83CL781: -40 to +85°C
  - 83CL782: -25 to +55°C

ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING	PHILIPS NORTH AMERICA[3] PART ORDER NUMBER	TEMPERATURE RANGE °C AND PACKAGE	FREQUENCY	DRAWING NUMBER
ROM	ROM			
P83CL781HFP	P83CL781HF N	–40 to +85; 40-Pin Plastic DIP[1]	DC to 12MHz	SOT129
P83CL781HFH	P83CL781HF B	–40 to +85; 44-Pin Plastic QFP[2]	DC to 12MHz	SOT205
P83CL781HFH	P83CL781HF B	–40 to +85; 44-Pin Plastic QFP[2]	DC to 12MHz	SOT307
P83CL782HDP	P83CL782HD N	–25 to +55 40-Pin Plastic DIP[1]	DC to 12MHz	SOT129
P83CL782HDH	P83CL782HD B	–25 to +55 44-Pin Plastic QFP[2]	DC to 12MHz	SOT205
P83CL782HDH	P83CL782HD B	–25 to +55 44-Pin Plastic QFP[2]	DC to 12MHz	SOT307

NOTES:
1. DIP = Dual In-line Package
2. QFP = Quad Flat Pack.
   Two body sizes are available: SOT205 – 14mm × 14mm and SOT307 – 10mm × 10mm. See package dimension section for details.
3. Parts ordered by the Philips North America part number will be marked with the Philips part marking.

BLOCK DIAGRAM



SILICON PLANAR VARIABLE CAPACITANCE DIODE

The BB112 is a single 9 V variable capacitance diode in a plastic encapsulation for application in tuning circuits in a.m. receivers. The diodes are supplied in matched sets of three items.

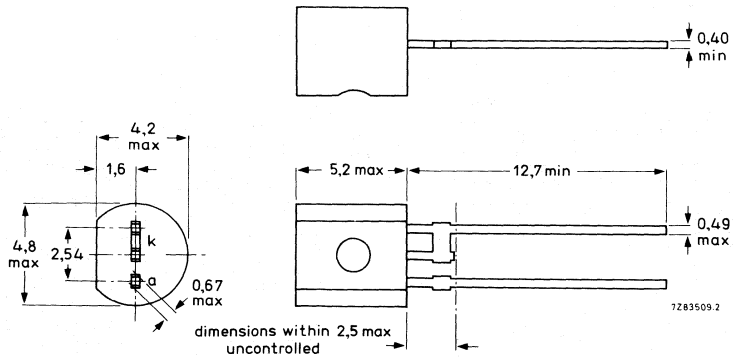
QUICK REFERENCE DATA

Continuous reverse voltage	V_R	max.	12 V
Operating junction temperature	T_j	max.	85 °C
Forward current	I_F	max.	50 mA
Reverse current at T_{amb} = 25 °C V_R = 12 V	I_R	<	50 nA
Diode capacitance at f = 1 MHz V_R = 1 V V_R = 8,5 V	C_d C_d	440 to 540 17 to 29	pF pF
Series resistance at f = 500 kHz V_R = 1 V	r_s	<	1,5 Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-69



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Continuous reverse voltage	V_R	max.	12	V
Forward current (d.c.)	I_F	max.	50	mA
Operating junction temperature	T_j	max.	85	°C
Storage temperature	T_{stg}	−55 to + 125		°C

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Reverse current				
V_R = 12 V	I_R	<	50	nA
V_R = 12 V; T_{amb} = 85 °C	I_R	<	300	nA
Diode capacitance at f = 1 MHz				
V_R = 1 V	C_d		440 to 540	pF
V_R = 8,5 V	C_d		17 to 29	pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\,(V_R = 1\,V)}{C_d\,(V_R = 8{,}5\,V)}$	>	18	
Series resistance at f = 500 kHz				
V_R = 1 V	r_s	<	1,5	Ω
Temperature coefficient of the diode capacitance at f = 1 MHz; T_{amb} = −40 to + 85 °C; V_R = 1 V	η	typ.	0,05	%/K

Matching properties

D.C. capacitance ratio for a set of 3 diodes; V_P = 1 to 9 V	ΔC	⩽	3	%

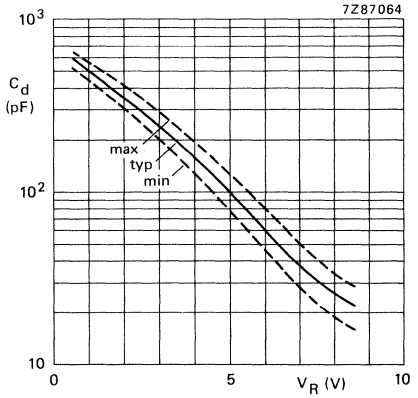


Fig. 2 Diode capacitance at f = 1 MHz as a function of the reverse voltage.

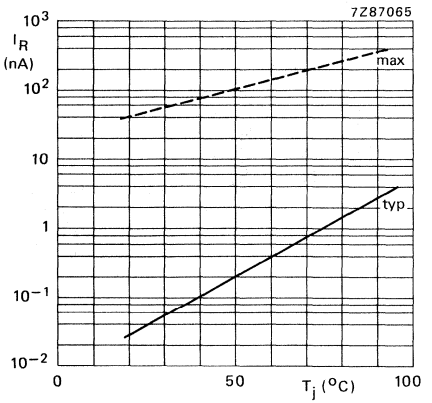


Fig. 3 Reverse current as a function of junction temperature at V_R = 12 V.

VARIABLE CAPACITANCE DIODE

A single variable capacitance diode, in a plastic envelope. The diode is for tuning of long, medium and short wavebands. Also suitable for frequency synthesizer applications.

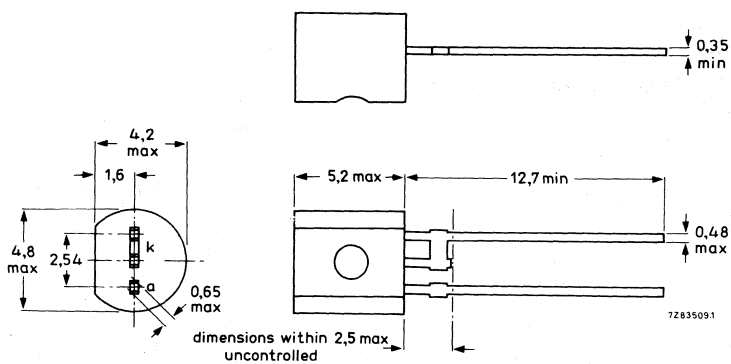
QUICK REFERENCE DATA

Continuous reverse voltage	V_R	max.	30 V
Reverse current at V_R = 30 V	I_R	<	50 nA
Diode capacitance at f = 1 MHz; V_R = 28 V	C_d		12 to 21 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 1\ V)}{C_d\ (V_R = 28\ V)}$	>	23
Series resistance f = 1 MHz; V_R = 1 V	r_s	<	2 Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-69 (TO-92 variant).



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Continuous reverse voltage	V_R	max.	30	V
Reverse voltage (peak value)	V_{RM}	max.	32	V
Forward current (d.c.)	I_F	max.	50	mA
Storage temperature	T_{stg}	−55 to +	125	°C
Operation junction temperature	T_j	max.	85	°C

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Reverse current				
V_R = 30 V	I_R	<	50	nA
V_R = 30 V; T_{amb} = 85 °C	I_R	<	300	nA
Diode capacitance at f = 1 MHz				
V_R = 1 V	C_d	450 to	550	pF
V_R = 28 V	C_d	12 to	21	pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 1\ V)}{C_d\ (V_R = 28\ V)}$	>	23	
Series resistance				
at f = 1 MHz and V_R = 1 V	r_s	<	2	Ω
Temperature coefficient of the diode capacitance at f = 1 MHz; T_{amb} = −20 °C to + 85 °C				
V_R = 1 V	η	typ.	0,05	%/°C
Capacitance matching				
Relative capacitance difference between two diodes at V_R = 1 to 28 V	$\frac{\Delta C}{C}$	<	3	%

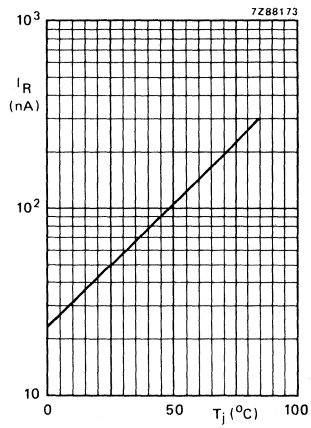


Fig. 2 Maximum values. Reverse current as a function of the junction temperature. V_R = 30 V.

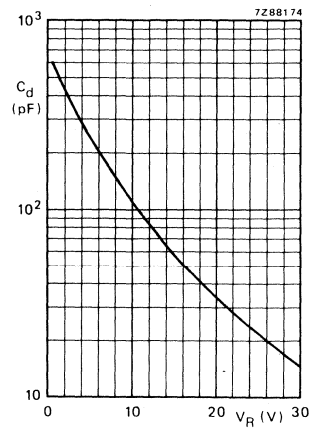


Fig. 3 Typical diode capacitance as a function of reverse voltage; f = 1 MHz.

UHF variable capacitance diode BB135

DESCRIPTION

The BB135 is a silicon, double-implanted variable capacitance diode in planar technology, intended for use in UHF tuners. It has a high linearity and is encapsulated in the ultra-small plastic SMD package, SOD323.

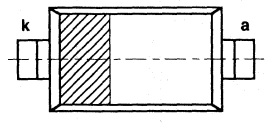
The diodes are delivered on tape (3000 or 10 000 pieces), without gaps.

QUICK REFERENCE DATA

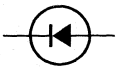
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
I_R	reverse current	V_R = 30 V	–	10	nA
C_d	diode capacitance	V_R = 0.5 V; f = 1 MHz	17.5	21	pF
		V_R = 28 V; f = 1 MHz	1.7	2.1	pF
$C_{0.5\ V}/C_{28\ V}$	capacitance ratio	f = 1 MHz	8.9	12	
R_s	series resistance	f = 470 MHz; note 1	–	0.75	Ω

Note

1. V_R is the value at which C_d = 9 pF.



MSB045



MBB206

Marking code: BB135 = P5.

Fig.1 Simplified outline (SOD323) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
V_{RM}	reverse voltage	peak value	–	30	V
I_F	forward current	DC value	–	20	mA
T_{stg}	storage temperature range		−55	150	°C
T_{amb}	ambient operating temperature range		−55	125	°C

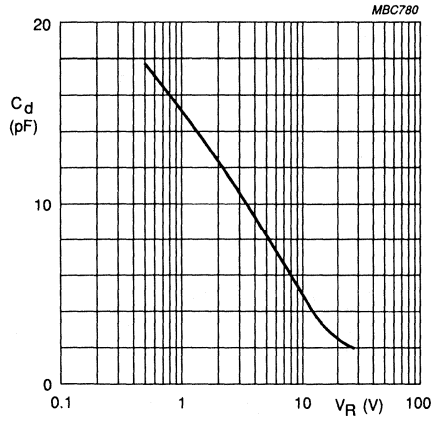
CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_R	reverse current	V_R = 30 V	–	10	nA
		V_R = 30 V; T_{amb} = 85 °C	–	200	nA
C_d	diode capacitance	V_R = 0.5 V; f = 1 MHz	17.5	21	pF
		V_R = 28 V; f = 1 MHz	1.7	2.1	pF
$C_{0.5\ V}/C_{28\ V}$	capacitance ratio	f = 1 MHz	8.9	12	
R_s	series resistance	f = 470 MHz; note 1	–	0.75	Ω

Note

1. V_R is the value at which C_d = 9 pF.



f = 1 MHz; T_{amb} = 25 °C.

Fig.2 Diode capacitance as a function of reverse voltage, typical values.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

SILICON PLANAR
VARIABLE CAPACITANCE DOUBLE DIODES

The BB204B and BB204G are double diodes with common cathode in a plastic TO-92 variant, primarily intended for electronic tuning in band II (f.m.). They are recommended for stages where large signals occur (e.g. oscillator circuits).

QUICK REFERENCE DATA

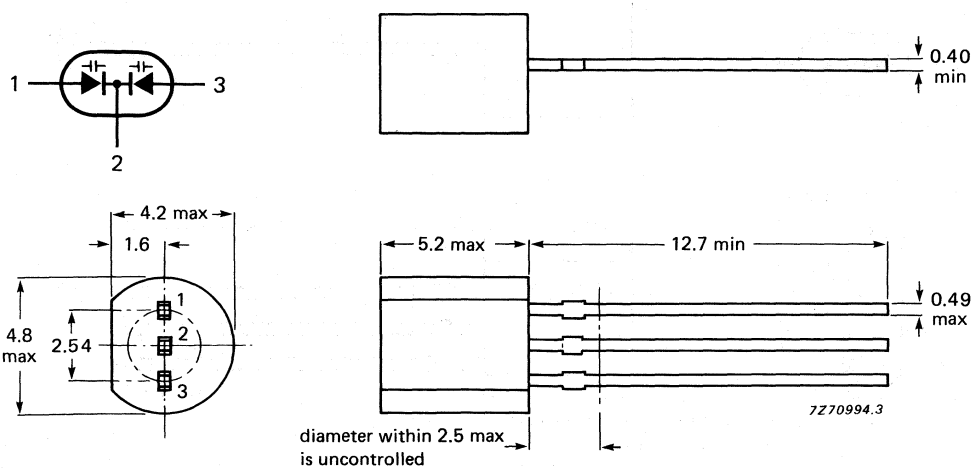
For each diode:

Continuous reverse voltage	V_R	max.		30	V
Junction temperature	T_j	max.		100	°C
Reverse current at V_R = 30 V	I_R	<		50	nA
			BB204G | BB204B		
Diode capacitance at f = 1 MHz					
V_R = 3 V	C_d		34 – 39 | 37 – 42		pF
V_R = 8 V	C_d		22 – 27 | 24 – 29		pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 3\ V)}{C_d\ (V_R = 30\ V)}$		2,5 to 2,8		
Series resistance at f = 100 MHz					
V_R is that value at which C_d = 38 pF	r_D	typ.		0,2	Ω
		<		0,4	Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

A.M. VARIABLE CAPACITANCE DOUBLE DIODES

The BB212 is a double 9V variable capacitance diode with common cathode in a plastic TO-92 variant.

A special feature is the low tuning voltage which makes the device particularly suited to car and domestic receivers in the L.W., M.W. and S.W. bands.

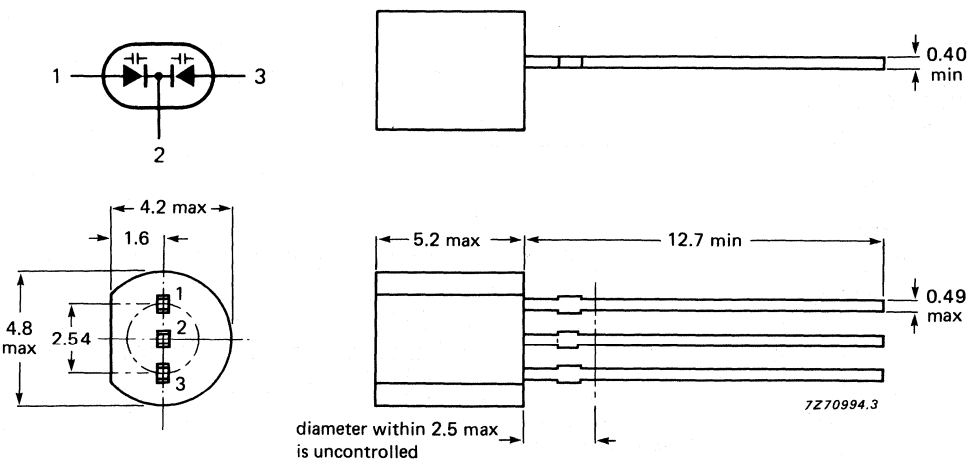
QUICK REFERENCE DATA

For each diode:			
Continuous reverse voltage	V_R	max.	12 V
Operating junction temperature	T_j	max.	85 °C
Reverse current at T_j = 25 °C V_R = 10 V	I_R	<	50 nA
Diode capacitance at f = 1 MHz			
V_R = 0,5 V	C_d		500 to 620 pF
V_R = 8,0 V	C_d	<	22 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 0{,}5\ V)}{C_d\ (V_R = 8{,}0\ V)}$	>	22,5
Series resistance at f = 500 kHz V_R is that value at which C_d = 500 pF	r_s	<	2,5 Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



The anode of the diode with the higher capacitance C_1 at V_R = 3 V, i.e. a more positive mismatch, is identified by a white dot.

VHF VARIABLE CAPACITANCE DOUBLE DIODE

The BB804 is a variable capacitance double diode in planar technology with common cathode in a plastic SOT23 envelope. It is intended for FM tuning especially for car radios.

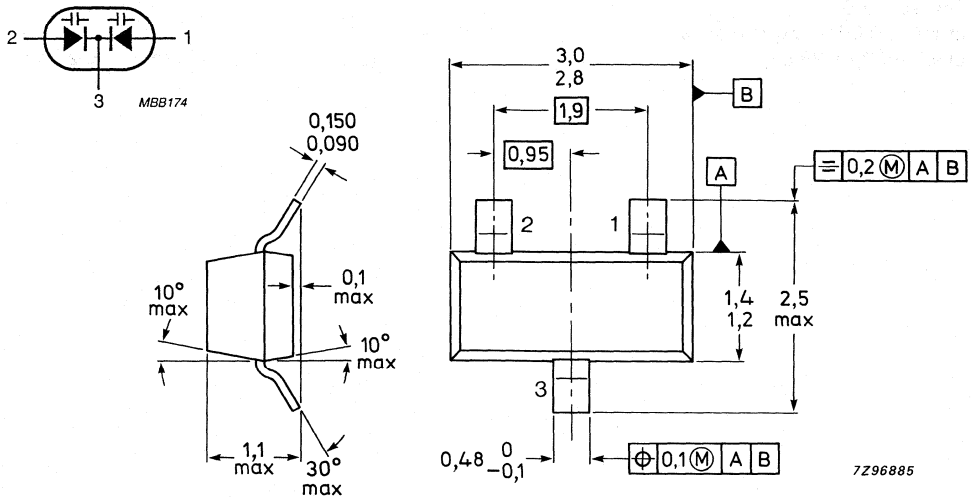
QUICK REFERENCE DATA

Continuous reverse voltage	V_R	max.	18 V
Repetitive peak reverse voltage	V_{RRM}	max.	20 V
Forward current (DC)	I_F	max.	50 mA
Operating junction temperature	T_j	max.	100 °C
Reverse current	I_R	max.	20 nA
Diode capacitance at f = 1 MHz V_R = 2 V	C_d		42 to 47.5 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 2\ V)}{C_d\ (V_R = 8\ V)}$		1.65 to 1.75
Series resistance at f = 100 MHz V_R is that value at which C_d = 38 pF	r_s	typ.	0.20 Ω

MECHANICAL DATA

Dimensions in mm

Marking SF



TOP VIEW

Fig.1 SOT23.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Continuous reverse voltage	V_R	max.	18 V
Forward current (DC)	I_F	max.	50 mA
Repetitive peak reverse voltage	V_{RRM}	max.	20 V
Storage temperature range	T_{stg}		−55 to + 100 °C
Operating junction temperature	T_j	max.	100 °C

THERMAL RESISTANCE

From junction to ambient mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm	$R_{th\ j\text{-}a}$	=	430 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Reverse current			
V_R = 16 V	I_R	<	20 nA
V_R = 16 V; T_{amb} = 60 °C	I_R	<	200 nA
Diode capacitance at f = 1.0 MHz			
V_R = 2 V			
red 0	C_d		42 to 43.5 pF
yellow 1	C_d		43 to 44.5 pF
white 2	C_d		44 to 45.5 pF
green 3	C_d		45 to 46.5 pF
blue 4	C_d		46 to 47.5 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 2\ V)}{C_d\ (V_R = 8\ V)}$		1.65 to 1.75
Series resistance at f = 100 MHz, V_R is that value at which C_d = 38 pF	r_s	typ.	0.20 Ω

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

General purpose symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications in l.f. and d.c. amplifiers, and in h.f. amplifiers.

QUICK REFERENCE DATA

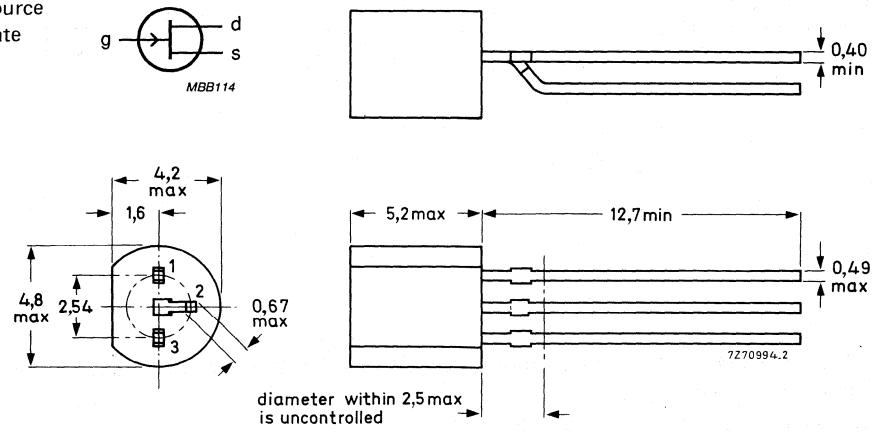
Drain-source voltage	$\pm V_{DS}$			max. 30		V
Gate-source voltage (open drain)	$-V_{GSO}$			max. 30		V
Total power dissipation up to T_{amb} = 75 °C	P_{tot}			max. 300		mW
		BF245A/0	A	B	C	
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	> 0,5	2,0	6	12	mA
		< 2,1	6,5	15	25	mA
Gate-source cut-off voltage I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$			0,25 to 8,0		V
Feedback capacitance at f = 1 MHz V_{DS} = 20 V; $-V_{GS}$ = 1 V; T_{amb} = 25 °C	C_{rs}			typ. 1,1		pF
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	$\lvert y_{fs} \rvert$			3,0 to 6,5		mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Drain current	I_D	max.	25 mA
Gate current	I_G	max.	10 mA
Power dissipation			
up to T_{amb} = 75 °C	P_{tot}	max.	300 mW
up to T_{amb} = 90 °C	P_{tot}	max.	300 mW 1)
Storage temperature	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250 K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	200 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

		BF245A	B	C
Gate cut-off current				
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	< 5	5	5 nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 125 °C	$-I_{GSS}$	< 0,5	0,5	0,5 μA
Drain current 2)				
V_{DS} = 15 V; V_{GS} = 0	I_{DSS} 3)	> 2	6,0	12 mA
		< 6,5	15,0	25 mA
Gate-source breakdown voltage				
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	> 30	30	30 V
Gate-source voltage				
I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$ 3)	> 0,4	1,6	3,2 V
		< 2,2	3,8	7,5 V

1) Transistor mounted on printed-circuit board, maximum lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

2) Measured under pulse conditions: t_p = 300 μs; $\delta \leqslant 0{,}02$.

3) BF245A/0: I_{DSS} = 0,5 to 2,1 mA; $-V_{GS}$ = 0,2 to 1,0 V
BF245A/1: I_{DSS} = 1,9 to 3,0 mA; $-V_{GS}$ = 0,4 to 1,0 V
BF245A/2: I_{DSS} = 3,0 to 4,5 mA; $-V_{GS}$ = 0,7 to 1,4 V
BF245A/3: I_{DSS} = 4,5 to 6,5 mA; $-V_{GS}$ = 1,1 to 2,2 V.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical n-channel planar epitaxial junction field-effect transistors in plastic TO-92 variants, intended for VHF and UHF amplifiers, mixers and general purpose switching.

QUICK REFERENCE DATA

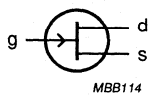
Drain-source voltage	$\pm V_{DS}$	max.			25	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.			250	mW
			A	B	C	
Drain current		min.	30	60	110	mA
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	max.	80	140	250	mA
Gate-source cut-off voltage						
I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$			0.6 to 14.5		V
Feedback capacitance at f = 1 MHz						
I_D = 10 mA; V_{DS} = 15 V	C_{rs}	typ.			3.5	pF
Transfer admittance (common source)						
I_D = 10 mA; V_{DS} = 15 V; f = 1 kHz	$\|y_{fs}\|$	min.			8	mS

MECHANICAL DATA

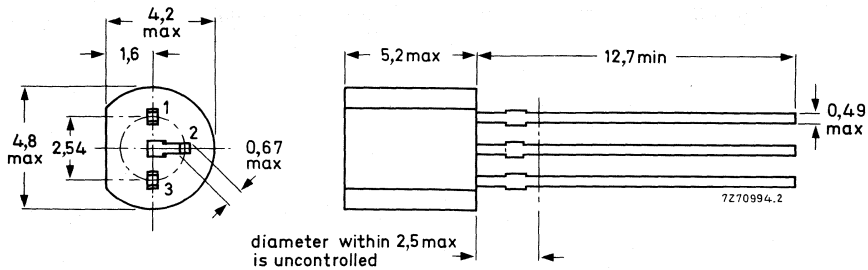
Dimensions in mm

Fig. 1 TO-92 variant.

Pinning (BF246):
1 = drain
2 = gate
3 = source



Pinning (BF247):
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

CHARACTERISTICS

T_{amb} = 25 °C

			A	B	C	
Gate cut-off current $-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	max.	5	5	5	nA
Drain current* V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	min.	30	60	110	mA
		max.	80	140	250	mA
Gate-source breakdown voltage $-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	min.	25	25	25	V
Gate-source voltage I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$	min.	1.5	3.0	5.5	V
		max.	4.0	7.0	12.0	V
Gate-source cut-off voltage I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$			0.6 to 14.5		V
Transfer admittance (common source) I_D = 10 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert y_{fs} \rvert$	min.			8	mS
		typ.			17	mS
Capacitances at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V						
feed-back capacitance	C_{rs}	typ.			3.5	pF
input capacitance	C_{is}	typ.			11	pF
output capacitance	C_{os}	typ.			5	pF
Cut-off frequency** V_{DS} = 15 V; V_{GS} = 0	f_{gfs}	typ.			450	MHz

* Measured under pulse conditions; t_p = 300 μs; $\delta \leqslant 0.02$.

** The frequency at which g_{fs} is 0.7 of its value at 1 kHz.

N-channel silicon junction field-effect transistor

BF545A; BF545B; BF545C

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

FEATURES

- Low leakage level (typ. 500 fA)
- High gain
- Low cut-off voltage (max. 2.2 V for BF545A).

DESCRIPTION

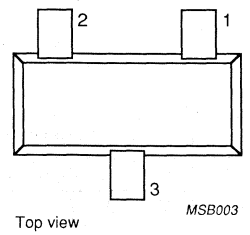
N-channel symmetrical silicon junction FETs in a surface-mountable SOT23 envelope. These devices are specially designed for use as impedance converters in (for example) electret microphones and infra-red detectors, and as VHF amplifiers in oscillators and mixers.

PINNING

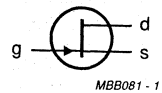
PIN	DESCRIPTION
1	source
2	drain
3	gate

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	30	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	BF545A		2	6.5	mA
	BF545B		6	15	mA
	BF545C		12	25	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 µA	0.4	7.8	V
Y_{fs}	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	3	6.5	mS



Top view



Marking codes:
BF545A: M65.
BF545B: M66.
BF545C: M67.

Fig.1 Simplified outline (SOT23) and symbol.

N-channel silicon junction field-effect transistor

BF545A; BF545B; BF545C

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	30	V
$-V_{GSO}$	gate-source voltage		–	30	V
$-V_{GDO}$	gate-drain voltage		–	30	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature range		−65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500 K/W

Note

1. Mounted on an FR-4 printboard.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{DS}$ = 0; $-V_{GS}$ = 20 V	–	0.5	1000	pA
		$-V_{DS}$ = 0; $-V_{GS}$ = 20 V; T_j = 125 °C	–	–	100	nA
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0				
	BF545A		2	–	6.5	mA
	BF545B		6	–	15	mA
	BF545C		12	–	25	mA
$-V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; $-I_G$ = 1 µA	30	–	–	V
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 200 µA				
	BF545A		0.4	–	2.2	V
	BF545B		1.6	–	3.8	V
	BF545C		3.2	–	7.8	V
		V_{DS} = 15 V; I_D = 1 µA	0.4	–	7.8	V
Y_{fs}	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	3	–	6.5	mS
Y_{os}	common source output admittance	V_{DS} = 15 V; V_{GS} = 0	–	40	–	µS

N-channel field-effect transistors BF556A;BF556B;BF556C

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

FEATURES

- Low leakage level (typ. 500 fA)
- High gain
- Low cut-off voltage.

DESCRIPTION

N-channel symmetrical silicon junction FETs in a surface-mountable SOT23 envelope. These devices are specially designed for use as impedance converters in (for example) electret microphones and infra-red detectors, and as VHF amplifiers in oscillators and mixers.

PINNING - SOT23

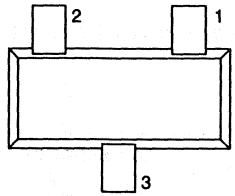
PIN	DESCRIPTION
1	source
2	drain
3	gate

CAUTION

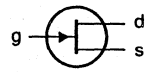
The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	30	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	BF556A		3	7	mA
	BF556B		6	13	mA
	BF556C		11	18	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 200 μA	0.5	7.5	V
$\|Y_{fs}\|$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	4.5	–	mS



Top view



MAM036

Marking codes:
BF556A: M84.
BF556B: M85.
BF556C: M86.

Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	30	V
$-V_{GSO}$	gate-source voltage		–	30	V
$-V_{GDO}$	gate-drain voltage		–	30	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature		–65	150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500 K/W

Note

1. Device mounted on a printed circuit board, maximum lead length 4 mm; mounting pad for the drain lead 10 mm².

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; $-I_G$ = 1 µA	30	–	–	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0				
	BF556A		3	–	7	mA
	BF556B		6	–	13	mA
	BF556C		11	–	18	mA
$-I_{GSS}$	reverse gate leakage current	V_{DS} = 0; $-V_{GS}$ = 20 V	–	0.5	5000	pA
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 200 µA	0.5	–	7.5	V
$\lvert Y_{fs} \rvert$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	4.5	–	–	mS
$\lvert Y_{os} \rvert$	common source output admittance	V_{DS} = 15 V; V_{GS} = 0	–	40	–	µS

N-channel junction FETs BF851A; BF851B; BF851C

FEATURES

- High transfer admittance
- Low input capacitance
- Low feedback capacitance
- Low noise.

APPLICATIONS

- Pre-amplifiers for AM-tuners in car radios.

DESCRIPTION

N-channel symmetrical junction field effect transistors in a SOT54 (TO-92) package.

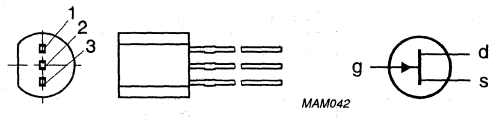


Fig.1 Simplified outline and symbol.

PINNING - SOT54 (TO-92)

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	±25	V
I_{DSS}	drain current	V_{GS} = 0; V_{DS} = 8 V			
	BF851A		2	6.5	mA
	BF851B		6	15	mA
	BF851C		12	25	mA
P_{tot}	total power dissipation	up to T_{amb} = 40 °C	–	400	mW
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{GS} = 0; V_{DS} = 8 V			
	BF851A		12	20	mS
	BF851B		16	25	mS
	BF851C		20	30	mS
C_{iss}	input capacitance	f = 1 MHz	–	10	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	2.5	pF

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

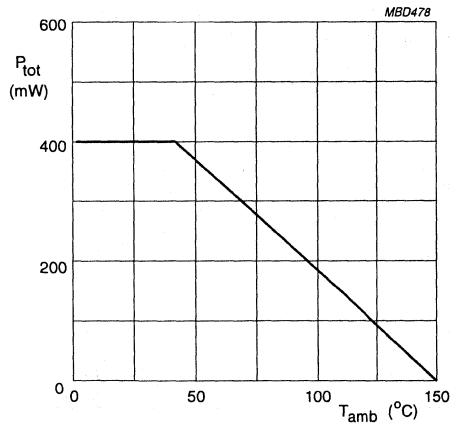
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	±25	V
V_{GSO}	gate-source voltage	open drain	–	–25	V
V_{DGO}	drain-gate voltage (DC)	open source	–	25	V
I_G	forward gate current (DC)		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 40 °C; note 1	–	400	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board; maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm^2.



V_{DS} = 8 V.

Fig.2 Power derating curve.

N-channel junction FETs BF861A; BF861B; BF861C

FEATURES

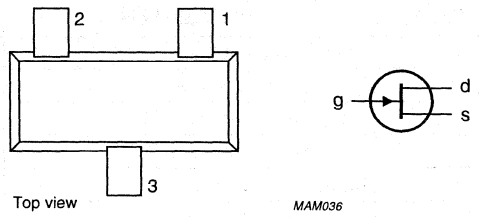
- High transfer admittance
- Low input capacitance
- Low feedback capacitance
- Low noise.

APPLICATIONS

- Pre-amplifiers for AM-tuners in car radios.

DESCRIPTION

N-channel symmetrical junction field effect transistors in a SOT23 package.



Marking codes:
BF861A: M33.
BF861B: M34.
BF861C: M35.

Fig.1 Simplified outline and symbol.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	±25	V
I_{DSS}	drain current	V_{GS} = 0; V_{DS} = 8 V			
	BF861A		2	6.5	mA
	BF861B		6	15	mA
	BF861C		12	25	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{GS} = 0; V_{DS} = 8 V			
	BF861A		12	20	mS
	BF861B		16	25	mS
	BF861C		20	30	mS
C_{iss}	input capacitance	f = 1 MHz	–	10	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	2.5	pF

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

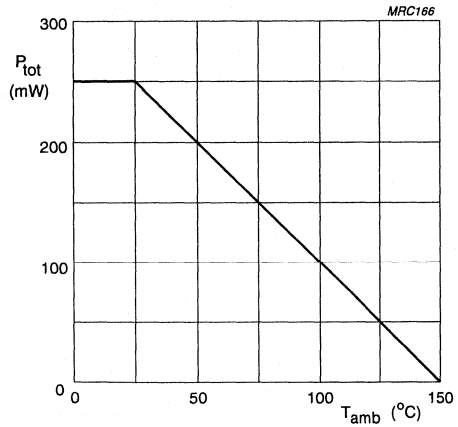
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	±25	V
V_{GSO}	gate-source voltage	open drain	–	–25	V
V_{DGO}	drain-gate voltage (DC)	open source	–	25	V
I_G	forward gate current (DC)		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on an FR4 printed-circuit board.



V_{DS} = 8 V.

Fig.2 Power derating curve.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners, FM tuners with a 12 volt supply voltage. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	40 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	25 mS
Input capacitance at gate 1; f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	4 pF
Feedback capacitance at f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	30 fF
Noise figure at G_S = 2 mS I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.2 dB

MECHANICAL DATA

Fig.1 SOT143.

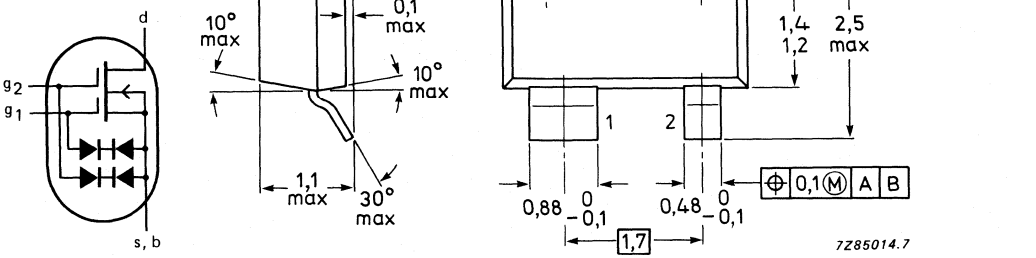
Dimensions in mm

Marking code:

BF992 = M92

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	40 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200 mW
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460 K/W

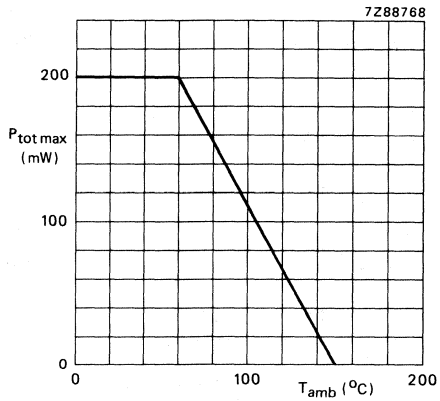


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	April 1991

BF998

Silicon n-channel dual gate MOS-FET

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

FEATURES

- Short channel transistor with high ratio $|Y_{fs}|/C_{is}$.
- Low noise gain controlled amplifier to 1 GHz.

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected, intended for VHF and UHF applications, such as television tuners, with 12 V supply voltage and professional communication equipment. This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	-	12	V
I_D	drain current	-	30	mA
P_{tot}	total power dissipation	-	200	mW
T_j	junction temperature	-	150	°C
$\|Y_{fs}\|$	transfer admittance	24	-	mS
C_{ig1-s}	input capacitance at gate 1	2.1	-	pF
C_{rs}	feedback capacitance	25	-	fF
F	noise figure at 800 MHz	1	-	dB

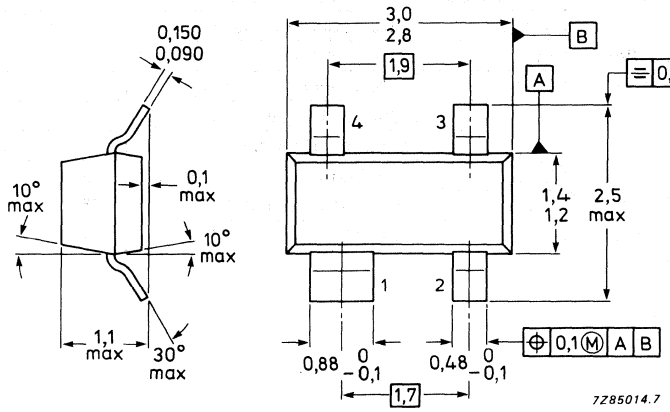
Silicon n-channel dual gate MOS-FET BF998

MECHANICAL DATA

Dimensions in mm

Marking code

BF998 = MOp



TOP VIEW

See also soldering recommendations.

Fig.1 SOT143.

PIN CONFIGURATION

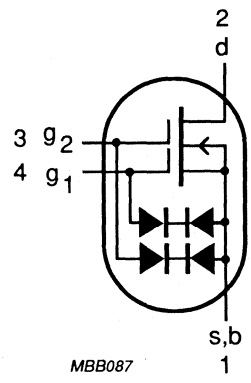


Fig.2 Pin configuration.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	July 1993

J108/J109/J110
N-channel junction FETs

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

FEATURES

- High speed switching
- Interchangeability of drain and source connections
- Low $R_{DS(on)}$ at zero gate voltage (< 8 Ω for J108)

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a TO-92 envelope. They are intended for use in applications such as analog switches, choppers and commutators.

PINNING - TO-92

PIN	DESCRIPTION
1	gate
2	source
3	drain

Note

1. Drain and source are interchangeable.

PIN CONFIGURATION

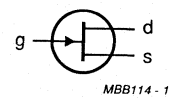


Fig 1. Symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	25	V
$-V_{GSO}$	gate-source voltage		-	25	V
$-V_{GDO}$	gate-drain voltage		-	25	V
I_G	forward gate current	DC	-	50	mA
P_{tot}	total power dissipation	$T_{amb} \leq 50$ °C	-	400	mW
T_{stg}	storage temperature range		−65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	250	K/W

STATIC CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{GS}$ = 15 V V_{DS} = 0		-	3	nA
I_{DSX}	drain-source cut-off current	$-V_{GS}$ = 10 V V_{DS} = 5 V		-	3	nA
I_{DSS}	drain current	V_{GS} = 0 V_{DS} = 15 V	J108 J109 J110	80 40 10	- - -	mA
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 1 μA V_{DS} = 0		-	25	V
$-V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 μA V_{DS} = 5 V	J108 J109 J110	3 2 0.5	10 6 4	V
$R_{DS(on)}$	drain-source on-resistance	V_{GS} = 0 V V_{DS} = 0.1 V	J108 J109 J110	- - -	8 12 18	Ω

N-channel silicon field-effect transistors

J308/309/310

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a TO-92 envelope. They are intended for use in the AM input stage in car radios and in UHF/VHF amplifiers, oscillators and mixers.

PIN CONFIGURATION

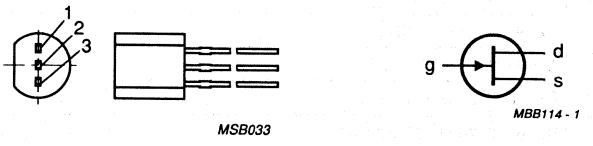


Fig.1 Simplified outline and symbol.

PINNING - TO-92

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0			
	J308		12	60	mA
	J309		12	30	mA
	J310		24	60	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C	–	400	mW
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 µA			
	J308		1	6.5	V
	J309		1	4	V
	J310		2	6.5	V
Y_{fs}	common-source transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	mS

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
$-V_{GSO}$	gate-source voltage		–	25	V
$-V_{GDO}$	gate-drain voltage		–	25	V
I_G	forward gate current	DC value	–	50	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C	–	400	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	250	K/W

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm, mounting pad for the drain lead minimum 10 x 10 mm

NE/SA572
Programmable Analog Compandor

Product Specification

DESCRIPTION

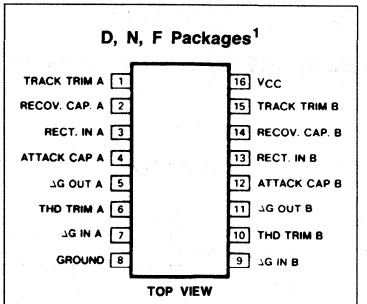
The NE572 is a dual-channel, high-performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full-wave rectifier to detect the average value of input signal, a linearized, temperature-compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high-performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

- **Independent control of attack and recovery time**
- **Improved low frequency gain control ripple**
- **Complementary gain compression and expansion with external op amp**
- **Wide dynamic range — greater than 110dB**
- **Temperature-compensated gain control**
- **Low distortion gain cell**
- **Low noise — 6μV typical**
- **Wide supply voltage range — 6V – 22V**
- **System level adjustable with external components**

PIN CONFIGURATION



NOTE:
1. D package released in large SO (SOL) package only.

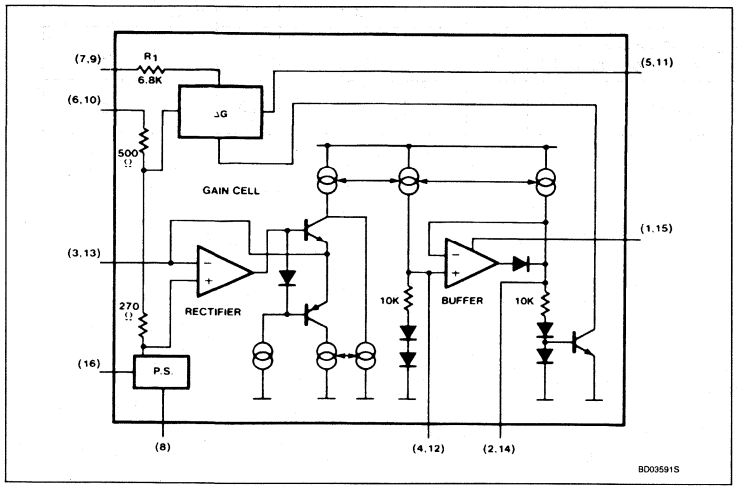
APPLICATIONS

- **Dynamic noise reduction system**
- **Voltage control amplifier**
- **Stereo expandor**
- **Automatic level control**
- **High-level limiter**
- **Low-level noise gate**
- **State variable filter**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE572D
16-Pin Plastic DIP	0 to +70°C	NE572N
16-Pin Plastic SO	−40°C to +85°C	SA572D
16-Pin Cerdip	−40°C to +85°C	SA572F
16-Pin Plastic DIP	−40°C to +85°C	SA572N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

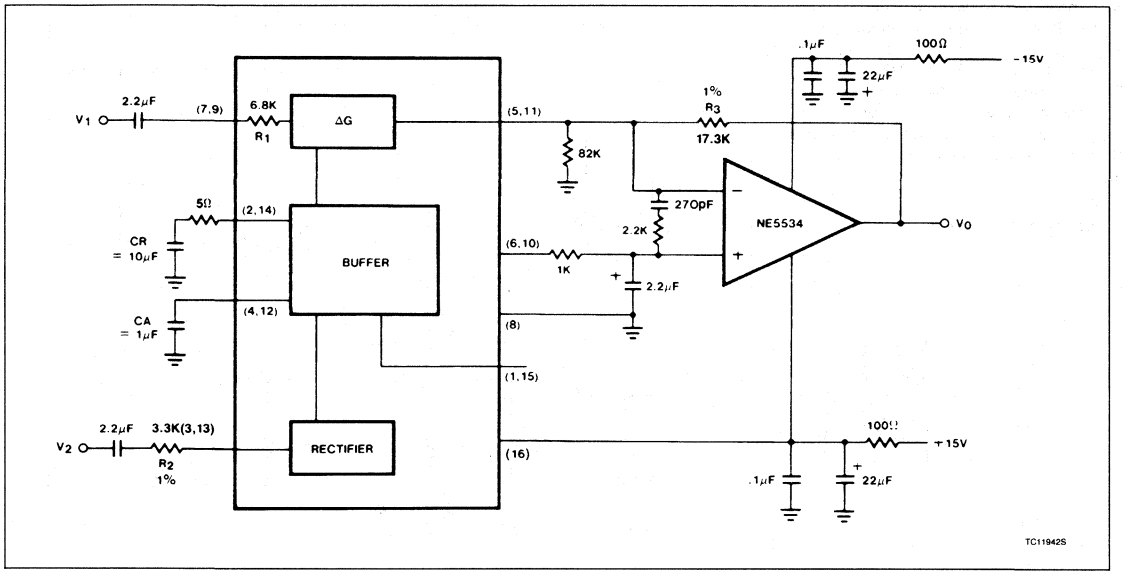
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	22	V_{DC}
T_A	Operating temperature range NE572 SA572	 0 to +70 -40 to +85	 °C
P_D	Power dissipation	500	mW

DC ELECTRICAL CHARACTERISTICS

Standard test conditions (unless otherwise noted) V_{CC} = 15V, T_A = 25°C; Expandor mode (see Test Circuit). Input signals at unity gain level (0dB) = 100mV_{RMS} at 1kHz; $V_1 = V_2$; R_2 = 3.3kΩ; R_3 = 17.3kΩ.

SYMBOL	PARAMETER	TEST CONDITIONS	NE572			SA572			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		6		22	6		22	V_{DC}
I_{CC}	Supply current	No signal			6			6.3	mA
V_R	Internal voltage reference		2.3	2.5	2.7	2.3	2.5	2.7	V_{DC}
THD	Total harmonic distortion (untrimmed)	1kHz C_A = 1.0μF		0.2	1.0		0.2	1.0	%
THD	Total harmonic distortion (trimmed)	1kHz C_R = 10μF		0.05			0.05		%
THD	Total harmonic distortion (trimmed)	100Hz		0.25			0.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20 - 20kHz)		6	25		6	25	μV
	DC level shift (untrimmed)	Input change from no signal to 100mV_{RMS}		±20	±50		±20	±50	mV
	Unity gain level		-1	0	+1	-1.5	0	+1.5	dB
	Large-signal distortion	$V_1 = V_2$ = 400mV		0.7	3.0		0.7	3	%
	Tracking error (measured relative to value at unity gain) = [$V_O - V_O$ (unity gain)]dB - V_2dB	Rectifier input V_2 = +6dB V_1 = 0dB V_2 = -30dB V_1 = 0dB		 ±0.2 ±0.5	 -1.5 +0.8		 ±0.2 ±0.5	 -2.5 +1.6	dB
	Channel crosstalk	200mV_{RMS} into channel A, measured output on channel B	60			60			dB
PSRR	Power supply rejection ratio	120Hz		70			70		dB

TEST CIRCUIT



AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK/SLOW RECOVERY LEVEL SENSOR

In high-performance audio gain control applications, it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics NE572 this high-performance noise reduction concept becomes feasible for consumer hi fi applications. The NE572 is a dual channel gain control IC. Each channel has a linearized, temperature-compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current-to-voltage conversion, the VCA features low distortion, low noise and wide dynamic range.

The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor C_A with an internal 10k resistor R_A defines the attack time t_A. The recovery time t_R of a tone burst is defined by a recovery capacitor C_R and an internal 10k resistor R_R. Typical attack time of 4ms for the high-frequency spectrum and 40ms for the low frequency band can be obtained with 0.1μF and 1.0μF attack capacitors, respectively. Recovery time of 200ms can be obtained with a 4.7μF external capacitor. With the recovery capacitor added in the level sensor, the gain control ripple for low frequency signals is much lower than that of a simple RC ripple filter. As a result, the residual third harmonic distortion of low frequency signal in a two quad transconductance amplifier is greatly improved. With the 1.0μF attack capacitor and 4.7μF recovery capacitor for a 100Hz signal, the third harmonic distortion is improved by more than 10dB over the simple RC ripple filter with a single 1.0μF attack and recovery capacitor, while the attack time remains the same.

The NE572 is assembled in a standard 16-pin dual in-line plastic package and in oversized SOL package. It operates over a wide supply range from 6V to 22V. Supply current is less than 6mA. The NE572 is designed for consumer application over a temperature range 0 – 70°C. The SA572 is intended for applications from −40°C to +85°C.

NE572 BASIC APPLICATIONS

Description

The NE572 consists of two linearized, temperature-compensated gain cells (ΔG), each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 1 shows the circuit configuration of the gain cell. Bases of the differential pairs $Q_1 - Q_2$ and $Q_3 - Q_4$ are both tied to the output and inputs of OPA A_1. The negative feedback through Q_1 holds the V_{BE} of $Q_1 - Q_2$ and the V_{BE} of $Q_3 - Q_4$ equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\triangle V_{BEQ3-Q4} = \triangle_{BEQ1-Q2}$$

$$(V_{BE} = V_T \ln IC/IS)$$

$$V_T \ln\left(\frac{\frac{1}{2}I_G + \frac{1}{2}I_O}{I_S}\right) - V_T \ln\left(\frac{\frac{1}{2}I_G - \frac{1}{2}I_O}{I_S}\right)$$

$$= V_T \ln\left(\frac{I_1 + I_{IN}}{I_S}\right) - V_T \ln\left(\frac{I_2 - I_1 - I_{IN}}{I_S}\right) \quad (2)$$

where $I_{IN} = \frac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$

$I_1 = 140\mu A$

$I_2 = 280\mu A$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation (2) can be simplified to:

$$I_O = \frac{2}{I_2} \cdot I_{IN} \cdot I_G - \frac{1}{I_2}(I_2 - 2I_1) \cdot I_G \quad (3)$$

The first term of Equation 3 shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feedthrough due to the mismatch of devices. In the design, this has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within $\pm 25\mu A$ into the THD trim pin.

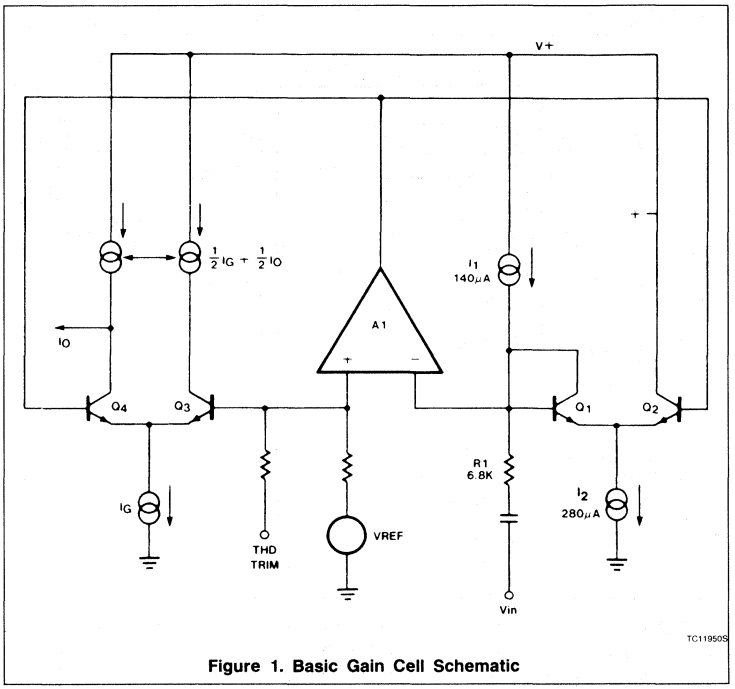


Figure 1. Basic Gain Cell Schematic

The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improve ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of 0.17% typ. Output noise with no input signals is only $6\mu V$ in the audio spectrum (10Hz – 20kHz). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at V_{REF} if the output current I_O is DC coupled.

Rectifier

The rectifier is a full-wave design as shown in Figure 2. The input voltage is converted to current through the input resistor R_2 and turns on either Q_5 or Q_6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A_2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A_2. The input bias current is typically about 70nA. Frequency response of the gain block A_2 also causes second-order error at high frequency. The collector current of Q_6 is mirrored and summed at the collector of Q_5 to form the full wave rectified output current I_R. The rectifier transfer function is

$$I_R = \frac{V_{IN} - V_{REF}}{R_2} \quad (4)$$

If V_{IN} is AC-coupled, then the equation will be reduced to:

$$I_{RAC} = \frac{V_{IN(AVG)}}{R_2}$$

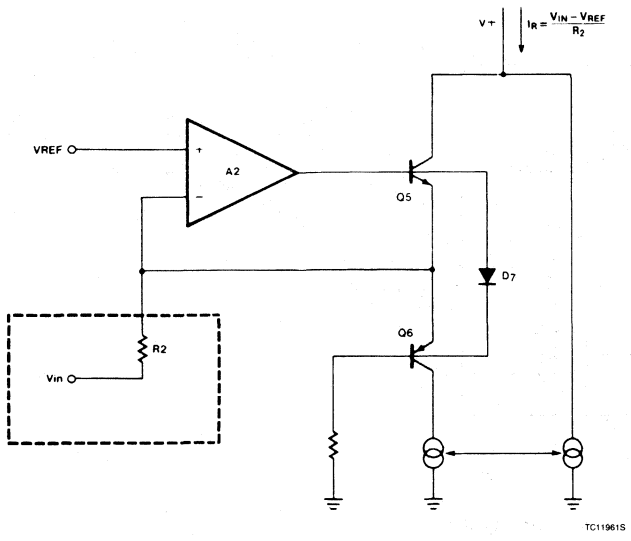


Figure 2. Simplified Rectifier Schematic

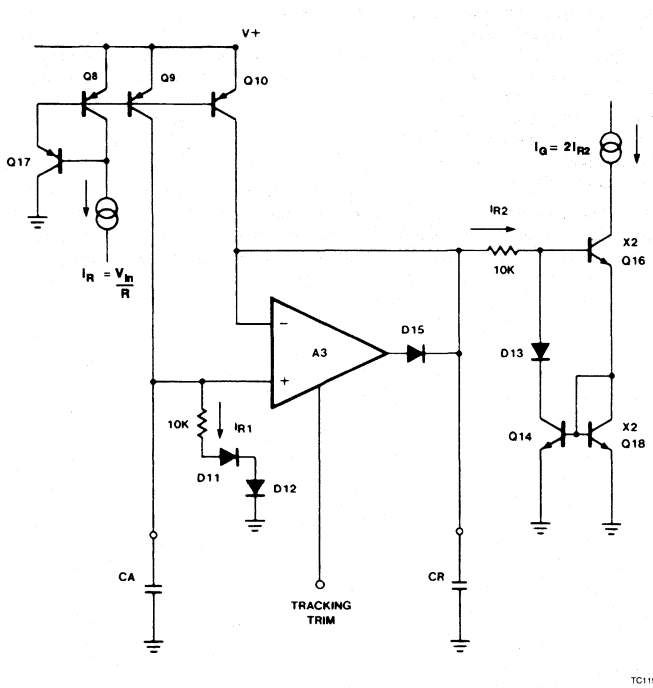


Figure 3. Buffer Amplifier Schematic

The internal bias scheme limits the maximum output current I_R to be around 300μA. Within a $\pm$1dB error band the input range of the rectifier is about 52dB.

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low-frequency ripple distortion. The low-frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 3, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A_3 through Q_8, Q_9 and Q_{10}. Diodes D_{11} and D_{12} improve tracking accuracy and provide common-mode bias for A_3. For a positive-going input signal, the buffer amplifier acts like a voltage-follower. Therefore, the output impedance of A_3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance, the gain Ga(t) for ΔG can be expressed as follows:

$$Ga(t) = (Ga_{INT} - Ga_{FNL})\ e^{\frac{-t}{\tau_A}} + Ga_{FNL}$$

Ga_{INT} = Initial Gain

Ga_{FNL} = Final Gain

$\tau_A = R_A \cdot CA = 10k \cdot CA$

where τ_A is the attack time constant and R_A is a 10k internal resistor. Diode D_{15} opens the feedback loop of A_3 for a negative-going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR $\cdot$ R_R. If the diode impedance is assumed negligible, the dynamic gain G_R (t) for ΔG is expressed as follows.

$$G_R(t) = (G_{R\ INT} - G_{R\ FNL})\ e^{\frac{-t}{\tau_R}} + G_{R\ FNL}$$

$\tau R = R_R \cdot CR = 10k \cdot CR$

where τR is the recovery time constant and R_R is a 10k internal resistor. The gain control current is mirrored to the gain cell through Q_{14}. The low level gain errors due to input bias current of A_2 and A_3 can be trimmed through the tracking trim pin into A_3 with a current source of $\pm$3μA.

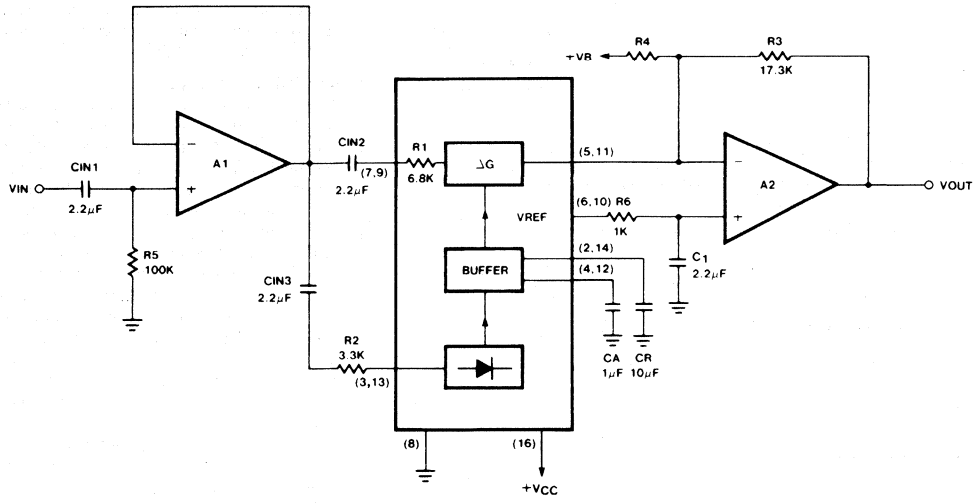


Figure 4. Basic Expandor Schematic

Basic Expandor

Figure 4 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \cdot \frac{R_3 \cdot V_{IN(AVG)}}{R_2 \cdot R_1} \quad (5)$$

($I_1 = 140\mu A$)

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a 6.8k internal resistor. The maximum input current into the gain cell can be as large as 140μA. This corresponds to a voltage level of 140μA • 6.8k = 952mV peak. The input peak current into the rectifier is limited to 300μA by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R_3/R_2 for desirable system voltage and current levels. A small R_2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A_1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2. R_3 and A_2 convert the gain cell output current to the output voltage. In high-performance applications, A_2 has to be low-noise, high-speed and wide band so that the high-performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference Pin 6 or 10. Resistor R_4 is used to bias up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_3}{R_4}\right) - V_B\frac{R_3}{R_4} \quad (6)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant.

Basic Compressor

Figure 5 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_{IN(AVG)}} \right)^{1/2} \quad (7)$$

R_{DC1}, R_{DC2}, and CDC form a DC feedback for A_1. The output DC level of A_1 is given by

$$V_{ODC} = V_{REF} \left(1 + \frac{R_{DC1} + R_{DC2}}{R_4} \right) - V_B \cdot \left(\frac{R_{DC1} + R_{DC2}}{R_4} \right) \quad (8)$$

The zener diodes D_1 and D_2 are used for channel overload protection.

Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 6 shows the system level diagram for reference.

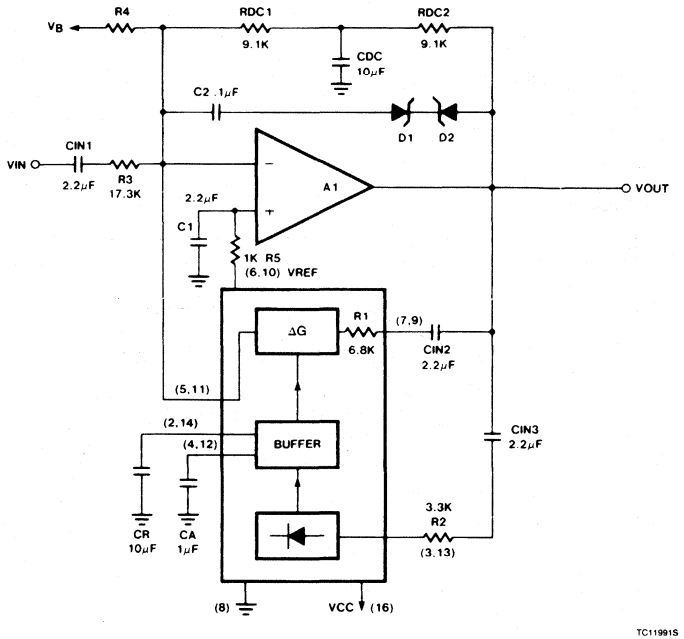


Figure 5. Basic Compressor Schematic

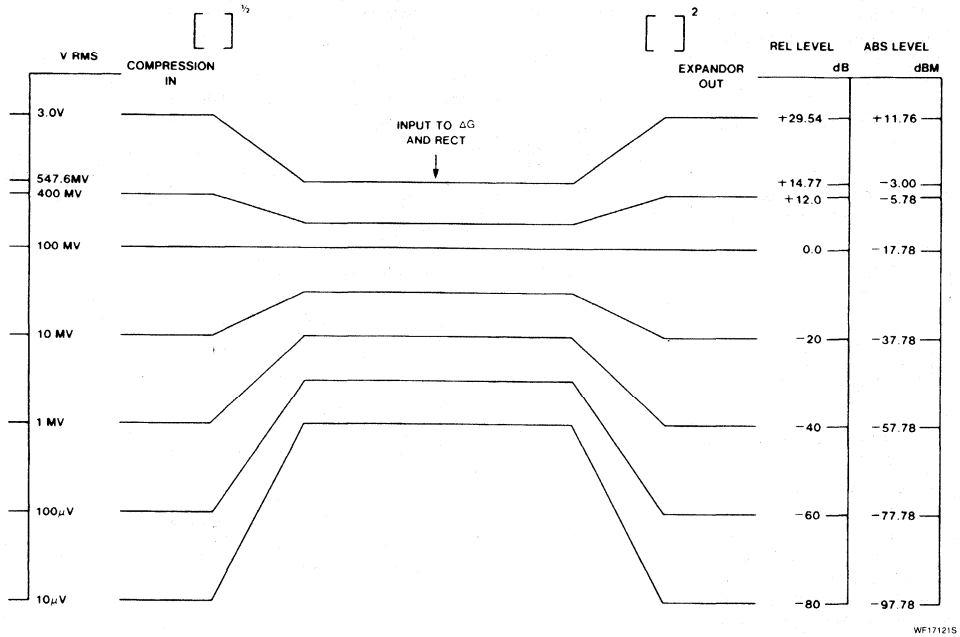


Figure 6. NE572 System Level

Low power compandor — NE/SA576

DESCRIPTION

The NE/SA576 is a unity gain level programmable compandor designed for low power applications. The NE576 is internally configured as an expandor and a compressor to minimize external component count.

The NE576 can operate at 1.8V. During normal operations, the NE576 can operate from at least a 2V battery. If the battery voltage drops to 1.8V, this part will still continue to function, however, turning on the part at a V_{CC} of 1.8V requires two external resistors to bring V_{REF} to half V_{CC}. One resistor connects between V_{CC} and V_{REF}; the other connects from V_{REF} to ground. A typical value for these external resistors is approximately 20k. A lower value can be used, but the power consumption will go up.

The NE576 is available in a 14-pin plastic DIP and SO packages.

FEATURES

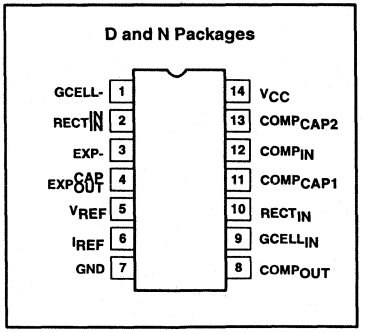
- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- Over 80dB of dynamic range
- Wide input/output swing capability (rail-to-rail)
- Low external component count
- ESD hardened

APPLICATIONS

- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control

PIN CONFIGURATION

D and N Packages



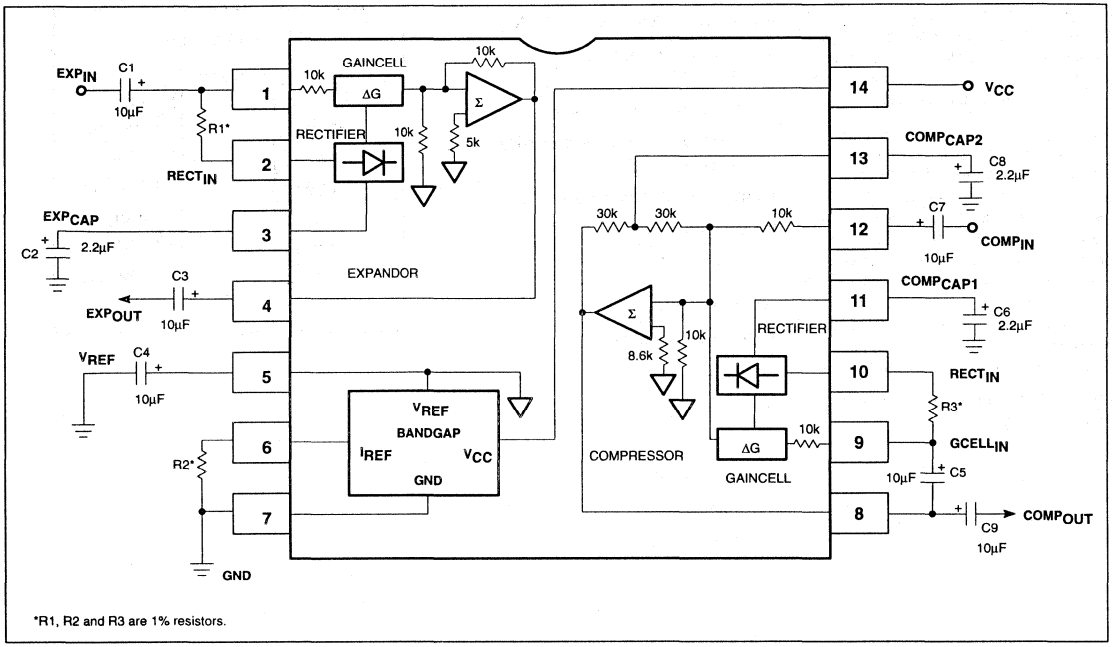
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE576N	0405B
14-Pin Plastic Small Outline (SO)	0 to +70°C	NE576D	0175D
14-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA576N	0405B
14-Pin Plastic Small Outline (SO)	–40 to +85°C	SA576D	0175D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING		UNITS
			NE576	SA576	
V_{CC}	Supply voltage		8	8	V
T_A	Operating ambient temperature range		0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range		–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance	DIP SO	90 125	90 125	°C/W °C/W

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT



*R1, R2 and R3 are 1% resistors.

ELECTRICAL CHARACTERISTICS

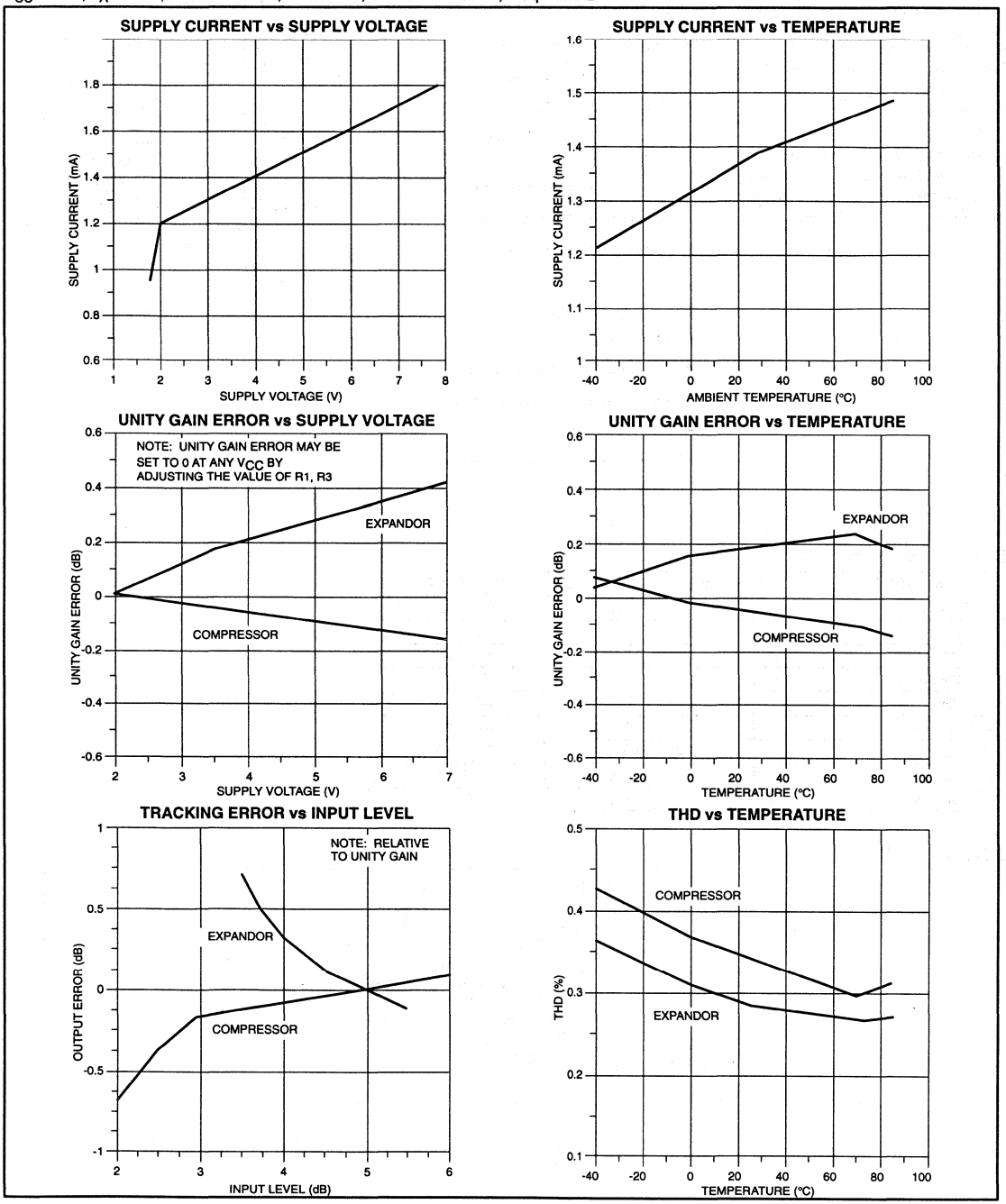
T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA576			UNITS
			MIN	TYP	MAX	
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current	No signal R_2 = 100kΩ		1.4	3	mA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V		1.8		V
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.5	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω		10	30	µV
0dB	Unity gain level	0dB at 1kHz	–1.5	0.18	1.5	dB
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10µF		–80		dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		V

NOTE:
1. Operation down to V_{CC} = 1.8V is possible, see description on front page of NE576 data sheet.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=7.15kΩ, R2=100kΩ, 0dB level = 100mV, Freq. = 1kHz



Compandor — NE570/571/SA571

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full-wave rectifier to detect the average value of the signal, a linerarized temperature-compensated variable gain cell, and an operational amplifier.

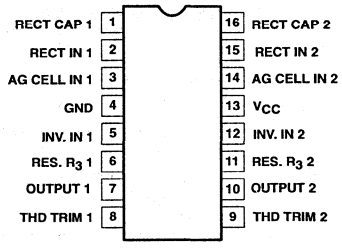
The NE570/571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio systems.

FEATURES

- Complete compressor and expandor in one IChip
- Temperature compensated
- Greater than 110dB dynamic range
- Operates down to 6VDC
- System levels adjustable with external components
- Distortion may be trimmed out
- Dynamic noise reduction systems
- Voltage-controlled amplifier

PIN CONFIGURATION

D, F, and N Packages[1]



TOP VIEW

NOTE:
1. SOL - Released in Large SO Package Only.

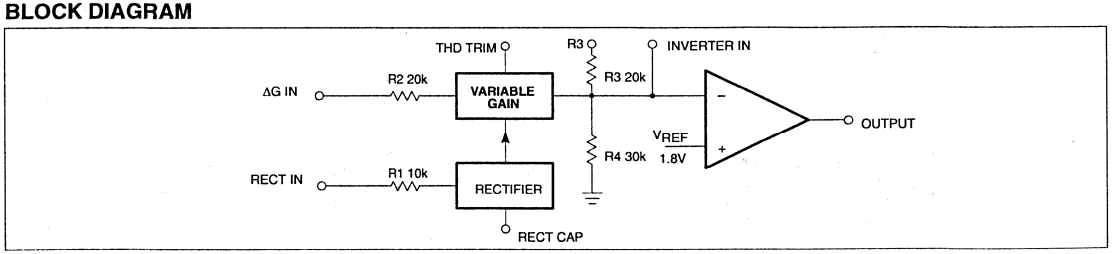
APPLICATIONS

- Cellular radio
- Telephone trunk compandor—570
- Telephone subscriber compandor—571
- High level limiter
- Low level expandor—noise gate
- Dynamic filters
- CD Player

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SOL	0 to +70°C	NE570D
16-Pin Cerdip	0 to +70°C	NE570F
16-Pin Plastic DIP	0 to +70°C	NE570N
16-Pin Plastic SOL	0 to +70°C	NE571D
16-Pin Cerdip	0 to +70°C	NE571F
16-Pin Plastic DIP	0 to +70°C	NE571N
16-Pin Plastic SOL	-40 to +85°C	SA571D
16-Pin Cerdip	-40 to +85°C	SA571F
16-Pin Plastic DIP	-40 to +85°C	SA571N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage 570 571	 24 18	VDC
T_A	Operating ambient temperature range NE SA	 0 to 70 -40 to +85	°C
P_D	Power dissipation	400	mW

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			LIMITS			UNITS
			NE570			NE/SA571[5]			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		6		24	6		18	V
I_{CC}	Supply current	No signal		3.2	4.8		3.2	4.8	mA
I_{OUT}	Output current capability		±20			±20			mA
SR	Output slew rate			±.5			±.5		V/µs
	Gain cell distortion[2]	Untrimmed Trimmed		0.3 0.05	1.0		0.5 0.1	2.0	%
	Resistor tolerance			±5	±15		±5	±15	%
	Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
	Output DC shift[3]	Untrimmed		±20	±100		±30	±150	mV
	Expandor output noise	No signal, 15Hz-20kHz[1]		20	45		20	60	µV
	Unity gain level[6]	1kHz	-1	0	+1	-1.5	0	+1.5	dBm
	Gain change[2, 4]			±0.1	±0.2		±0.1		dB
	Reference drift[4]			±5	±10		+2, -25	+20, -50	mV
	Resistor drift[4]			+1, -0			+8, -0		%
	Tracking error (measured relative to value at unity gain) equals [V_O - V_O (unity gain)] dB - V_2dBm	Rectifier input, V_2 = +6dBm, V_1 = 0dB V_2 = -30dBm, V_1 = 0dB		+0.2 +0.2	 -0.5, +1		+0.2 +0.2	 -1, +1.5	dB
	Channel separation			60			60		dB

NOTES:
1. Input to V_1 and V_2 grounded.
2. Measured at 0dBm, 1kHz.
3. Expandor AC input change from no signal to 0dBm.
4. Relative to value at T_A = 25°C.
5. Electrical characteristics for the SA571 only are specified over -40 to +85°C temperature range.
6. 0dBm = 775mV_{RMS}.

CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full-wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full-wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively-coupled voltage inputs as shown in the following equation. Note that for capacitively-coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|_{avg}}{R_1}$$

or

$$G \propto \frac{|V_{IN}|_{avg}}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expander or compressor application, this would lead to third harmonic distortion, so there is a trade-off to be made between fast attack and decay times and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})e^{-t/\tau} + G_{final} \; ; \; \tau = 10k \times C_{RECT}$$

The variable gain cell is a current-in, current-out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively-coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

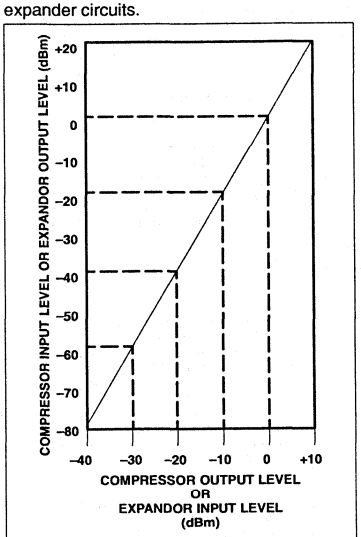
A compensation scheme built into the ΔG cell compensates for temperature and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expander gain to be determined only by internal components.

The output stage is capable of ±20mA output current. This allows a +13dBm ($3.5V_{RMS}$) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

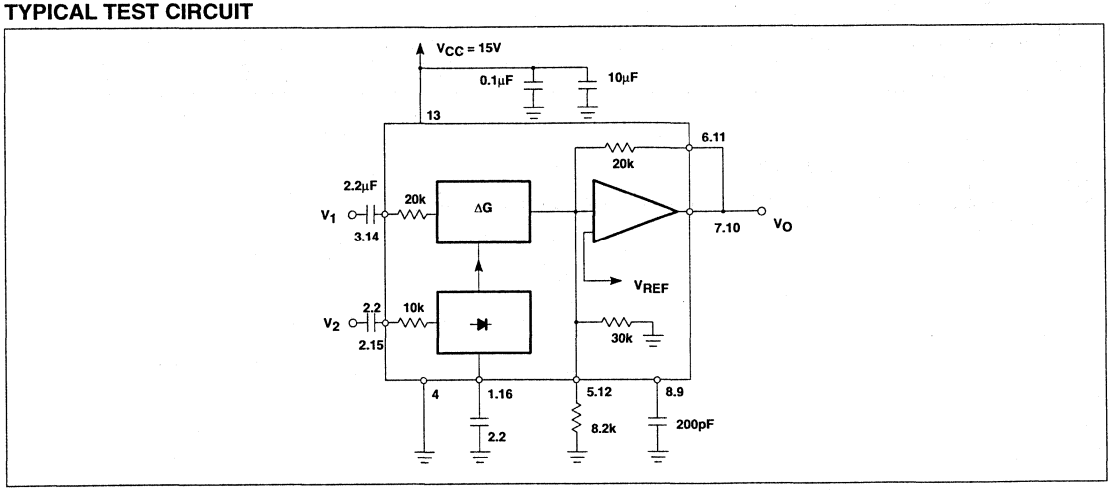
A bandgap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expander circuits.



Basic Input-Output Transfer Curve

TYPICAL TEST CIRCUIT



INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high-performance is required, one has to resort to complex discrete circuitry with many expensive, well-matched components. This paper describes an inexpensive integrated circuit, the NE570 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (<0.1%), high signal-to-noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The NE570 Compandor was originally designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal-to-noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 1 graphically shows what a compandor can do for the signal-to-noise ratio of a restricted dynamic range channel. The input level range of +20 to -80dB is shown undergoing a 2-to-1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

The significant circuits in a compressor or expander are the rectifier and the gain control element. The phone system requires a simple full-wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. These features make the circuit useful in audio and data systems as well as in telecommunications systems.

BASIC CIRCUIT HOOK-UP AND OPERATION

Figure 2 shows the block diagram of one half of the chip, (there are two identical channels on the IC). The full-wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output DC bias.

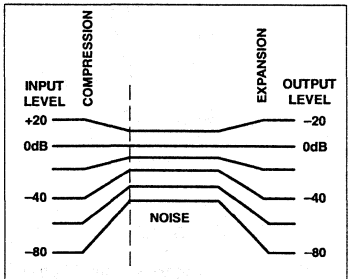


Figure 1. Restricted Dynamic Range Channel

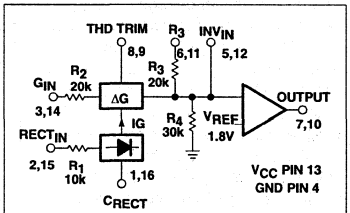


Figure 2. Chip Block Diagram (1 of 2 Channels)

The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8V reference denoted V_{REF}. The non-inverting input of the op amp is tied to V_{REF}, and the summing nodes of the rectifier and ΔG cell (located at the right of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{REF} potential.

Figure 3 shows how the circuit is hooked up to realize an expandor. The input signal, V_{IN}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{OUT} will thus drop 12dB, giving us the desired 2-to-1 expansion.

Figure 4 shows the hook-up for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is setup to provide AC feedback only, so a separate DC feedback loop is provided by the two R_{DC} and C_{DC}. The values of R_{DC} will determine the DC bias at the output of the op amp. The output will bias to:

$$V_{OUT}\ DC = 1 + \frac{R_{DC1} + R_{DC2}}{R_4}$$

$$V_{REF} = \left(1 + \frac{R_{DCTOT}}{30k}\right) 1.8V$$

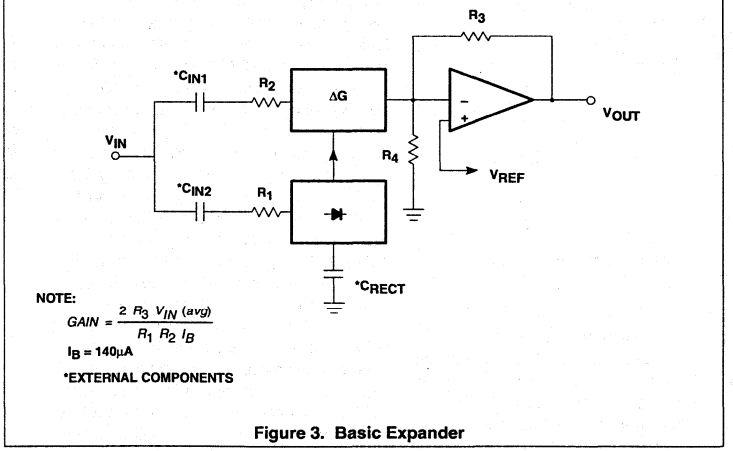


Figure 3. Basic Expander

The output of the expander will bias up to:

$$V_{OUT}\ DC = 1 + \frac{R_3}{R_4}\ V_{REF}$$

$$V_{REF} = \left(1 + \frac{20k}{30k}\right)\ 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the DC bias to any desired value.

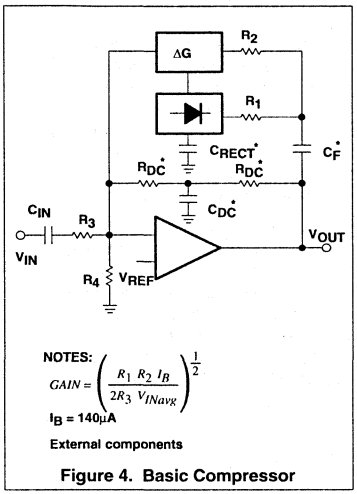


Figure 4. Basic Compressor

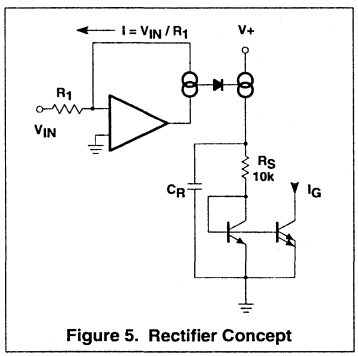


Figure 5. Rectifier Concept

CIRCUIT DETAILS—RECTIFIER

Figure 5 shows the concept behind the full-wave averaging rectifier. The input current to the summing node of the op amp, $V_{IN}R_1$, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_5, CR, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G, the gain control current.

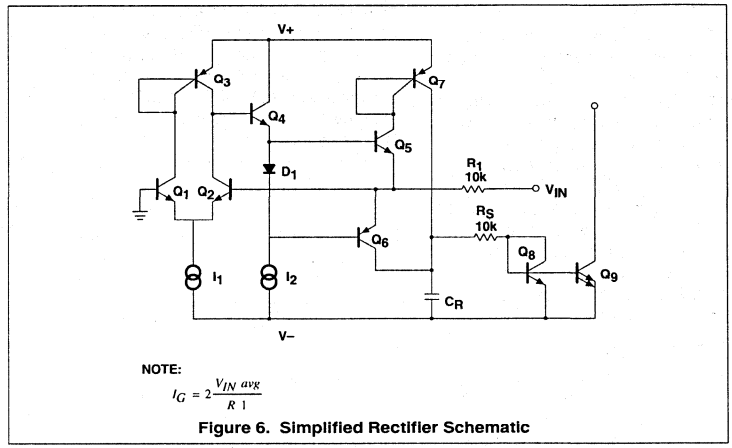


Figure 6. Simplified Rectifier Schematic

Figure 6 shows the rectifier circuit in more detail. The op amp is a one-stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{REF}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the *a* of Q_5 or Q_6 on negative or positive signal swings, respectively. ICs such as this have typical NPN βs of 200 and PNP βs of 40. The *a*'s of 0.995 and 0.975 will produce errors of 0.5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere 0.13dB gain error.

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by DC coupling into the rectifier. If an offset voltage exists between the V_{IN} input pin and the base of Q_2, an error current of V_{OS}/R_1 will be generated. A mere 1mV of offset will cause an input current of 100nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the PNP Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250μA. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 7 shows the rectifier accuracy vs input level at a frequency of 1kHz.

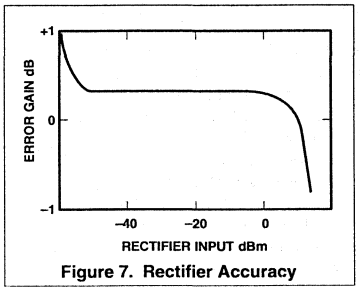


Figure 7. Rectifier Accuracy

At very high frequencies, the response of the rectifier will fall off. The roll-off will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, -20dBm, and -40dBm is shown in Figure 8. The response at all three levels is flat to well above the audio range.

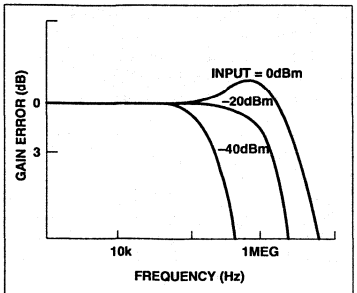


Figure 8. Rectifier Frequency Response vs Input Level

VARIABLE GAIN CELL

Figure 9 is a diagram of the variable gain cell. This is a linearized two-quadrant transconductance multiplier. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3 and Q_4. The gain is controlled by I_G and a current mirror provides the output current.

The op amp maintains the base and collector of Q_1 at ground potential (V_{REF}) by controlling the base of Q_2. The input current I_{IN} (=V_{IN}/R_2) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1}=I_1+I_{IN}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is:

$I_2-(I_1+I_{IN})=I_1-I_{IN}=I_{C2}$.

The op amp has thus forced a linear current swing between Q_1 and Q_2 by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair, Q_1 and Q_2, under large signal conditions.

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair, Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1 + I_{IN}}{I_1 - I_{IN}}$$

plus the relationships $I_G=I_{C3}+I_{C4}$ and $I_{OUT}=I_{C4}-I_{C3}$ will yield the multiplier transfer function,

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{V_{IN}}{R_2}\frac{I_G}{I_1}$$

This equation is linear and temperature-insensitive, but it assumes ideal transistors.

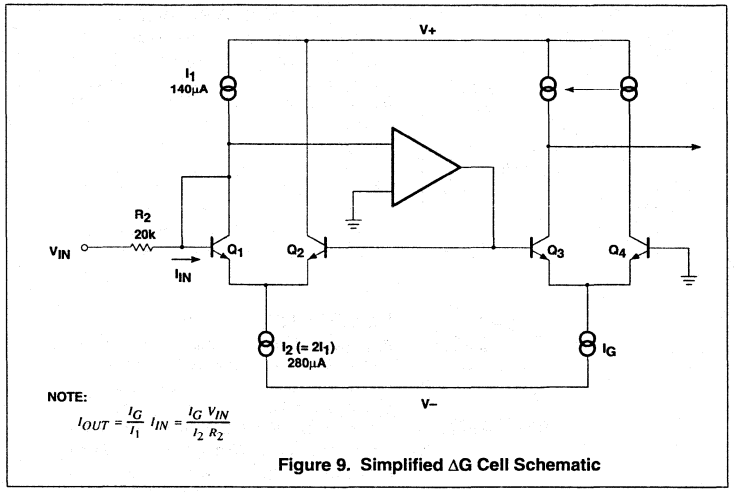


Figure 9. Simplified ΔG Cell Schematic

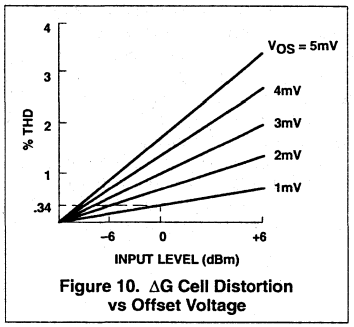


Figure 10. ΔG Cell Distortion vs Offset Voltage

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in second harmonic distortion. Figure 10 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mV offset will yield 0.34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about mV. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 11 shows the simple trim network required.

Figure 12 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

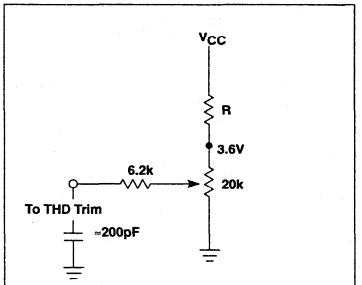


Figure 11. THD Trim Network

Control signal feedthrough is generated in the gain cell by imperfect device matching and mismatches in the current sources, I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feedthrough, but in general, the null for minimum feedthrough will be different than the null in distortion. The control signal feedthrough can be trimmed independently of distortion by tying a current source to the ΔG

input pin. This effectively trims I_1. Figure 13 shows such a trim network.

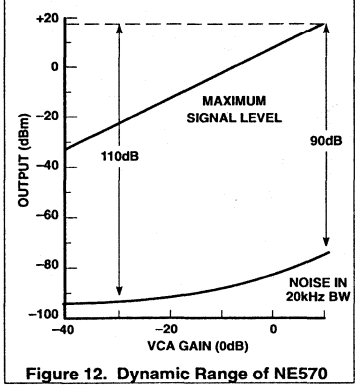


Figure 12. Dynamic Range of NE570

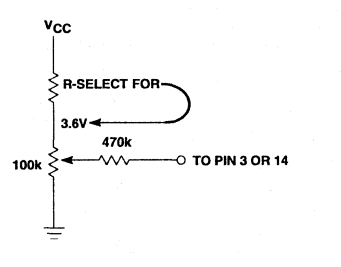


Figure 13. Control Signal Feedthrough Trim

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 14 shows the basic circuit. Split collectors are used in the input pair to reduce g_M, so that a small compensation capacitor of just 10pF may be used. The output stage, although capable of output currents in excess of 20mA, is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

RESISTORS

Inspection of the gain equations in Figures 3 and 4 will show that the basic compressor and expander circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hook-ups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 15 shows the effects of temperature on the diffused resistors which are normally used in integrated circuits, and the ion-implanted resistors which are used in this circuit. Over the critical 0°C to +70°C temperature range, there is a 10-to-1 improvement in drift from a 5% change for the diffused resistors, to a 0.5% change for the implemented resistors. The implanted resistors have another advantage in that they can be made the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

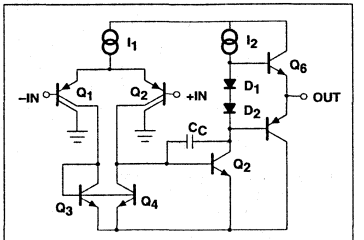


Figure 14. Operational Amplifier

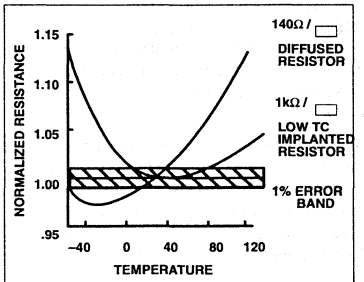


Figure 15. Resistance vs Temperature

8-bit microcontroller P83C524

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

1 FEATURES

- 80C51 CPU
- 16 kbytes on-chip ROM, expandable externally to 64 kbytes Program Memory address space
- 512 bytes on-chip RAM, expandable externally to 64 kbytes Data Memory address space
- Four 8-bit I/O ports
- Full-duplex UART compatible with the standard 80C51 and the 8052
- Two standard 16-bit timer/counters
- An additional 16-bit timer (functionally equivalent to the timer 2 of the 8052)
- On-chip Watchdog Timer (WDT) with a separate on-chip oscillator
- Bit-level I²C-bus hardware serial I/O Port
- 7-source and 7-vector interrupt structure with 2 priority levels
- Up to 3 external interrupt request inputs
- Two programmable power reduction modes (Idle and Power-down)
- Termination of Idle mode by any interrupt, external or WDT (watchdog) reset
- Wake-up from Power-down by external interrupt, external or WDT reset
- ROM code protection
- XTAL frequency range: 1.2 MHz to 16 MHz
- All packaging pin-outs fully compatible to the standard 8051/8052.

2 GENERAL DESCRIPTION

The P83C524 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. The P83C524 is a stand-alone high-performance microcontroller designed for use in real time applications such as instrumentation, industrial control, medium to high-end consumer applications and specific automotive control applications.

The P83C524 contains a non-volatile 16K x 8 read-only program memory, a volatile 512 x 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a 16-bit timer (identical to the timer 2 of the 8052), a multi-source, two-priority-level, nested interrupt structure, two serial interfaces (UART and bit-level I²C-bus), an on-chip oscillator and timing circuits, a watchdog timer (WDT) with a separate on-chip oscillator. For systems that require extra capability, the P83C524 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The P83C524 has the same instruction set as the PCB80C51 which consists of over 100 instructions: 49 one-byte, 46 two-byte and 16 three-byte. With a 16 MHz crystal, 58% of the instructions are executed in 750 ns and 40% in 1.5 µs. Multiply and divide instructions require 3 µs.

3 ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE				TEMPERATURE RANGE (°C)	FREQUENCY (MHz)
	PINS	PIN POSITION	MATERIAL	CODE		
ROM (note 1)						
P83C524FBP	40	DIL	plastic	SOT129	0 to +70	1.2 to 16
P83C524FFP	40	DIL	plastic	SOT129	−40 to +85	1.2 to 16
P83C524FHP	40	DIL	plastic	SOT129	−40 to +125	1.2 to 16
P83C524FBA	44	PLCC	plastic	SOT187	0 to +70	1.2 to 16
P83C524FFA	44	PLCC	plastic	SOT187	−40 to +85	1.2 to 16
P83C524FHA	44	PLCC	plastic	SOT187	−40 to +125	1.2 to 16

Note

1. For EPROM types, refer to the 8051-based 8-bit Microcontrollers Data Handbook IC20.

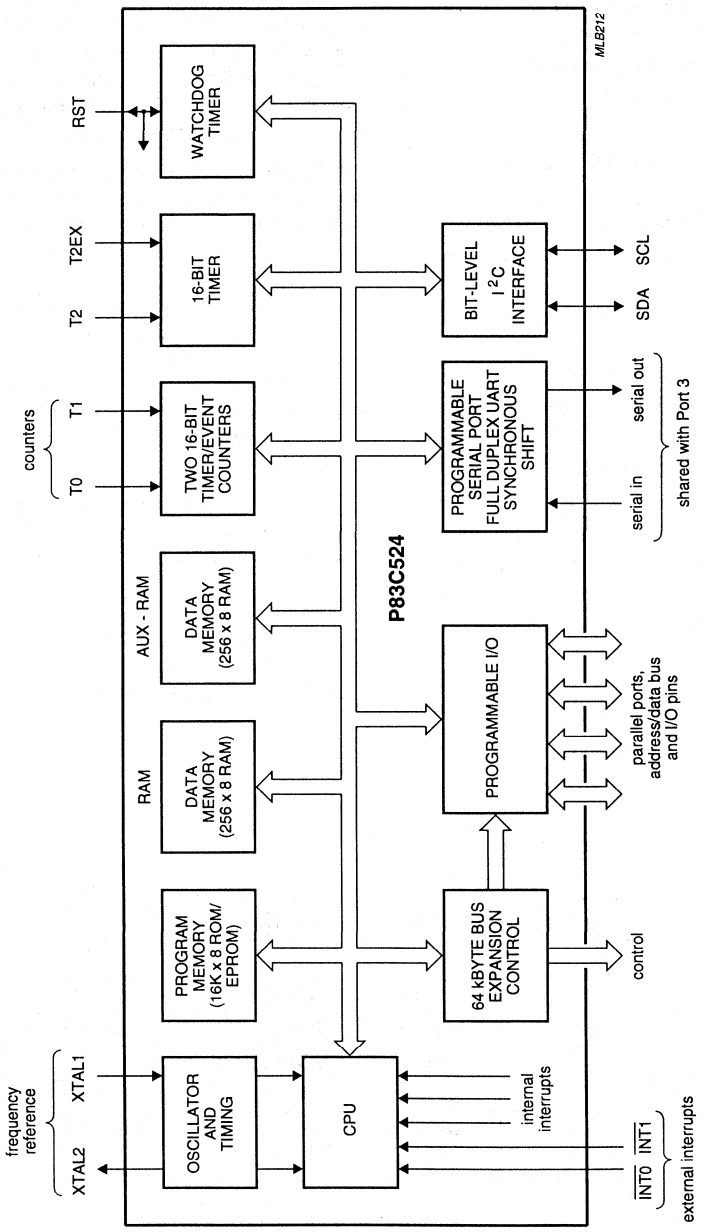


Fig.1 Block diagram.

Single-chip 8-bit microcontroller with on-chip CAN

P8xC592

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

1 FEATURES

- 80C51 central processing unit (CPU)
- 16k byte on-chip ROM (EPROM), externally expandable to 64k byte
- 2 x 256 byte on-chip RAM, externally expandable to 64k byte
- Two standard 16-bit timers/counters
- One additional 16-bit timer/counter coupled to four capture and three compare registers
- 10-bit ADC with 8 multiplexed analog inputs
- Two 8-bit resolution Pulse Width Modulated outputs
- 15 interrupt sources with 2 priority levels (2 to 6 external interrupt sources possible)
- Five 8-bit I/O ports, plus one 8-bit input port shared with analog inputs
- CAN-controller with DMA data transfer facility to internal RAM
- 1 Mbit(s) CAN-controller with bus failure management facility
- $V_{DD}/2$ reference voltage
- Full-duplex UART compatible with the standard 80C51
- On-chip Watchdog Timer (WDT)
- 1.2 to 16 MHz clock frequency.

2 GENERAL DESCRIPTION

The P8xC592 is a stand-alone high-performance microcontroller designed for use in automotive and general industrial applications. In addition to the 80C51 standard features, this device provides a number of dedicated hardware functions for these applications. Fig.1 shows a block diagram of the P8xC592.

Three versions of the P8xC592 will be offered:

- P83C592 (ROM version)
- P80C592 (ROMless version)
- P87C592 (EPROM/OTP version).

The P8xC592 basically combines the functions of the existing P8xC552 and the Philips CAN-controller PCA82C200 (CAN = Controller Area Network) with the following enhanced features:

- 16k byte Program Memory
- 2 x 256 byte Data Memory
- DMA between CAN Transmit/Receive Buffer and internal RAM.

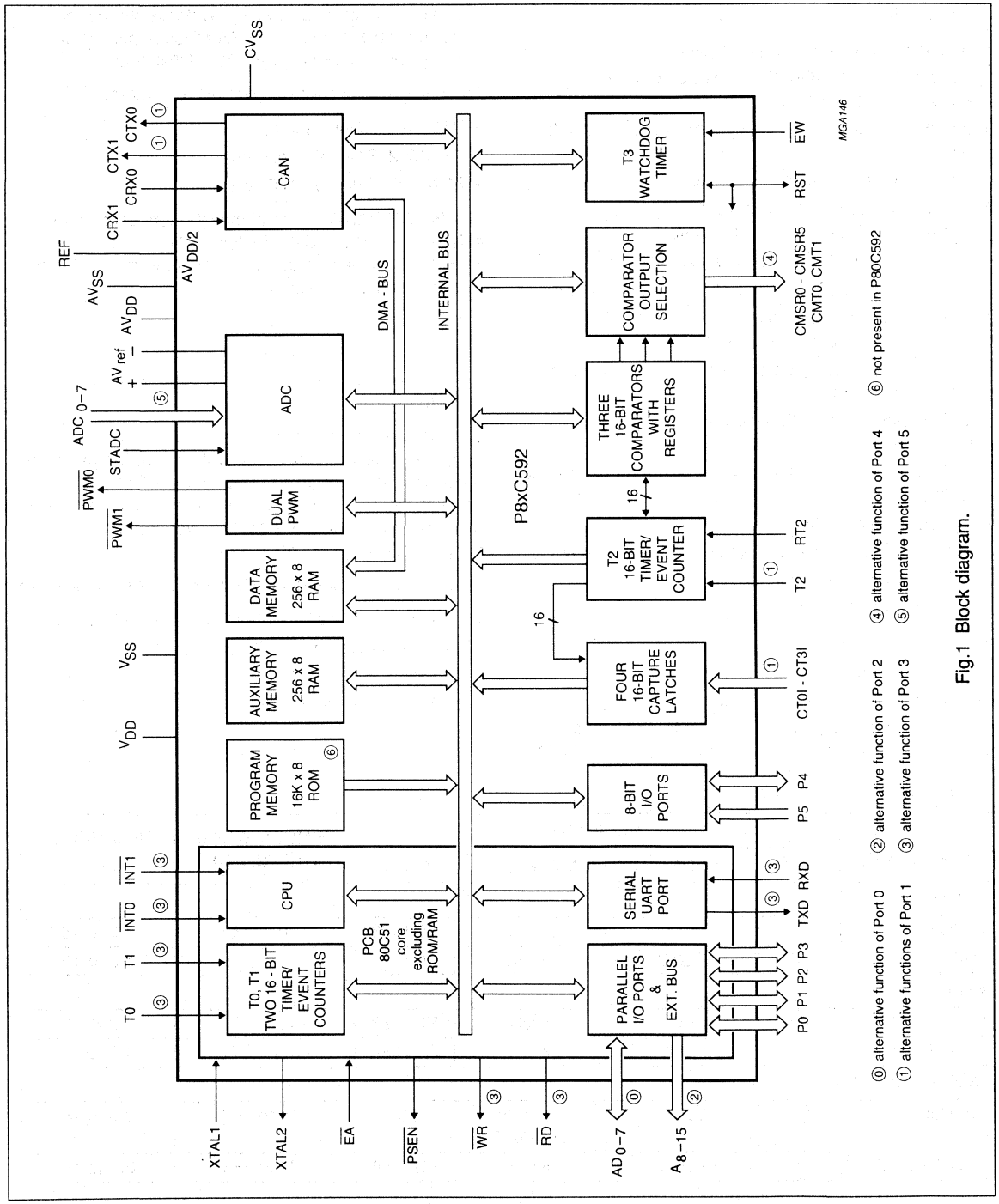
The temperature range includes a –40 to +85 °C version for general applications and an automotive temperature range version of –40 to +125 °C for the ROM and ROMless version with a maximum clock frequency of 16 MHz. The P87C592 (EPROM/OTP version) has a temperature range of –40 to +85 °C.

The main differences to the P8xC552 microcontroller are:

- a CAN-controller substitutes the I²C-serial interface
- 16k byte programmable ROM resp. EPROM (P8xC552 has 8k byte)
- additional 256 byte RAM.

3 ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE				TEMPERATURE RANGE (°C)	FREQUENCY (MHz)
	PINS	PIN POSITION	MATERIAL	CODE		
ROMless						
P80C592FFA	68	PLCC	plastic	SOT188	–40 to +85	1.2 to 16
P80C592FHA	68	PLCC	plastic	SOT188	–40 to +125	1.2 to 16
ROM						
P83C592FFA	68	PLCC	plastic	SOT188	–40 to +85	1.2 to 16
P83C592FHA	68	PLCC	plastic	SOT188	–40 to +125	1.2 to 16
EPROM						
P87C592EFL	68	CLCC	ceramic (window)	N0330	–40 to +85	3.5 to 16
P87C592EFA	68	PLCC	plastic	SOT188	–40 to +85	3.5 to 16



⓪ alternative function of Port 0 ② alternative function of Port 2 ④ alternative function of Port 4 ⑥ not present in P80C592
① alternative functions of Port 1 ③ alternative function of Port 3 ⑤ alternative function of Port 5

Fig.1 Block diagram.

8-bit microcontroller with EMC and FEEPROM

P8xCE528

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

1 FEATURES

- 80C51 central processing unit
- 32K x 8 ROM resp. FEEPROM, expandable externally to 64 kbytes
- ROM/FEEPROM code protection
- 512 x 8 RAM, expandable externally to 64 kbytes
- Four 8-bit I/O ports
- Full-duplex UART compatible with the standard 80C51 and the 8052
- Two standard 16-bit timer/counters
- An additional 16-bit timer (functionally equivalent to the timer 2 of the 8052)
- On-chip Watchdog Timer (WDT) with an on-chip oscillator
- Bit-level I²C-bus hardware serial I/O Port
- 7-source and 7-vector interrupt structure with 2 priority levels
- Up to 3 external interrupt request inputs
- Two programmable power reduction modes (Idle and Power-down)
- Termination of Idle mode by any interrupt, external or WDT (watchdog) reset
- Wake-up from Power-down by external interrupt, external or WDT reset
- Software enable/disable of ALE output pulse
- Electro-Magnetic Compatibility (EMC) improvements
- XTAL frequency range: 3.5 MHz to 16 MHz
- 4.5 to 5.5 V supply voltage range
- Extended Temperature range (–40 to +85 °C)

2 GENERAL DESCRIPTION

The P83CE528; P80CE528; P89CE528 (hereafter generically referred to as P8xCE528) single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family.

The P8xCE528 has the same instruction set as the 80C51. Three versions of the derivative exist:

- P83CE528: 32 kbytes mask programable ROM
- P80CE528: ROMless version of the P83CE528
- P89CE528: 32 kbytes FEEPROM (Flash Electrically Erasable Program Memory).

This device provides architectural enhancements that make it applicable in a variety of applications in general control systems, especially in those systems which need a large ROM and RAM capacity on chip.

The P8xCE528 contains a non-volatile 32K x 8 read-only program memory (P83CE528) or FEEPROM (P89CE528), a volatile 512 x 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a 16-bit timer (identical to the timer 2 of the 8052), a multi-source, two-priority-level, nested interrupt structure, two serial interfaces (UART and bit-level I²C-bus), an on-chip oscillator and timing circuits, a watchdog timer (WDT) with a separate on-chip oscillator. For systems that require extra capability, the P8xCE528 can be expanded using standard TTL compatible memories and logic.

In addition, the P8xCE528 has two software selectable modes of power reduction - Idle mode and Power-down mode. The Idle mode freezes the CPU while allowing the RAM, timers, serial ports and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 16 MHz crystal, 58% of the instructions are executed in 0.75 µs and 40% in 1.5 µs. Multiply and divide instructions require 3 µs.

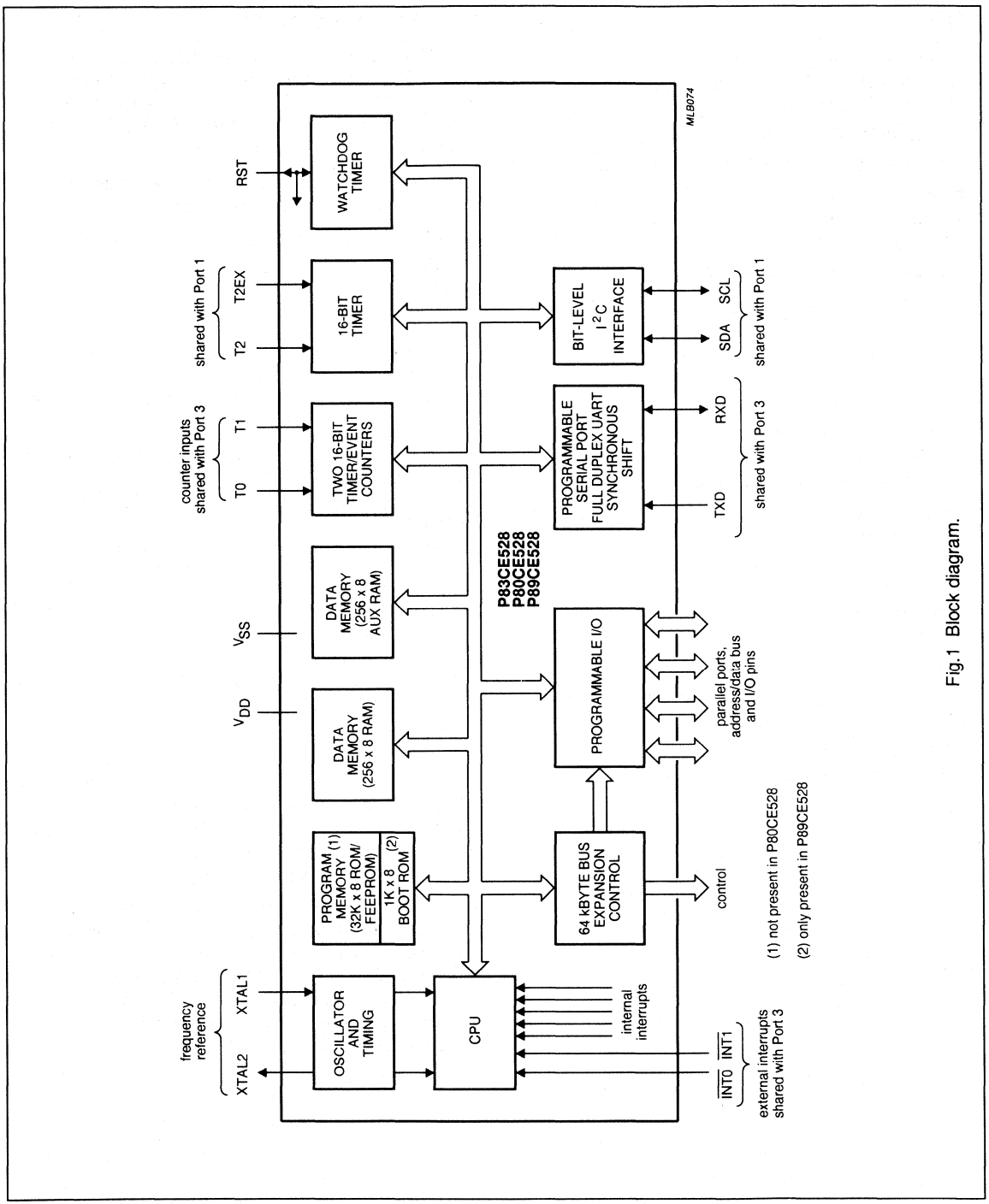


Fig.1 Block diagram.

8-bit microcontroller with on-chip CAN P8xCE598

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

1 FEATURES

- 80C51 central processing unit (CPU)
- 32 kbyte on-chip ROM (EPROM), externally expandable to 64 kbyte
- 2 x 256 byte on-chip RAM, externally expandable to 64 kbyte
- Two standard 16-bit timers/counters
- One additional 16-bit timer/counter coupled to four capture and three compare registers
- 10-bit ADC with 8 multiplexed analog inputs
- Two 8-bit resolution Pulse Width Modulated outputs
- 15 interrupt sources with 2 priority levels (2 to 6 external interrupt sources possible)
- Five 8-bit I/O ports, plus one 8-bit input port shared with analog inputs
- CAN-controller with DMA data transfer facility to internal RAM
- 1 Mbit(s) CAN-controller with bus failure management facility
- $V_{DD}/2$ reference voltage
- Full-duplex UART compatible with the standard 80C51
- On-chip Watchdog Timer (WDT)
- 1.2 to 16 MHz clock frequency (3.5 to 16 MHz for EPROM/OTP version).
- Electro-Magnetic Compatibility (EMC) improvements

2 GENERAL DESCRIPTION

The P80CE598/P83CE598/P87CE598 (hereafter generically referred to as P8xCE598) is a single-chip 8-bit high-performance microcontroller with on-chip CAN-controller designed for use in automotive and general industrial applications. In addition to the 80C51 standard features, this device provides a number of dedicated hardware functions highly suitable for automotive and general industrial applications. Figure 1 illustrates the block diagram of the P8xCE598.

Three versions of the P8xCE598 will be offered:

- P83CE598 (ROM version)
- P80CE598 (ROMless version)
- P87CE598 (EPROM/OTP version) (OTP = One Time Programming).

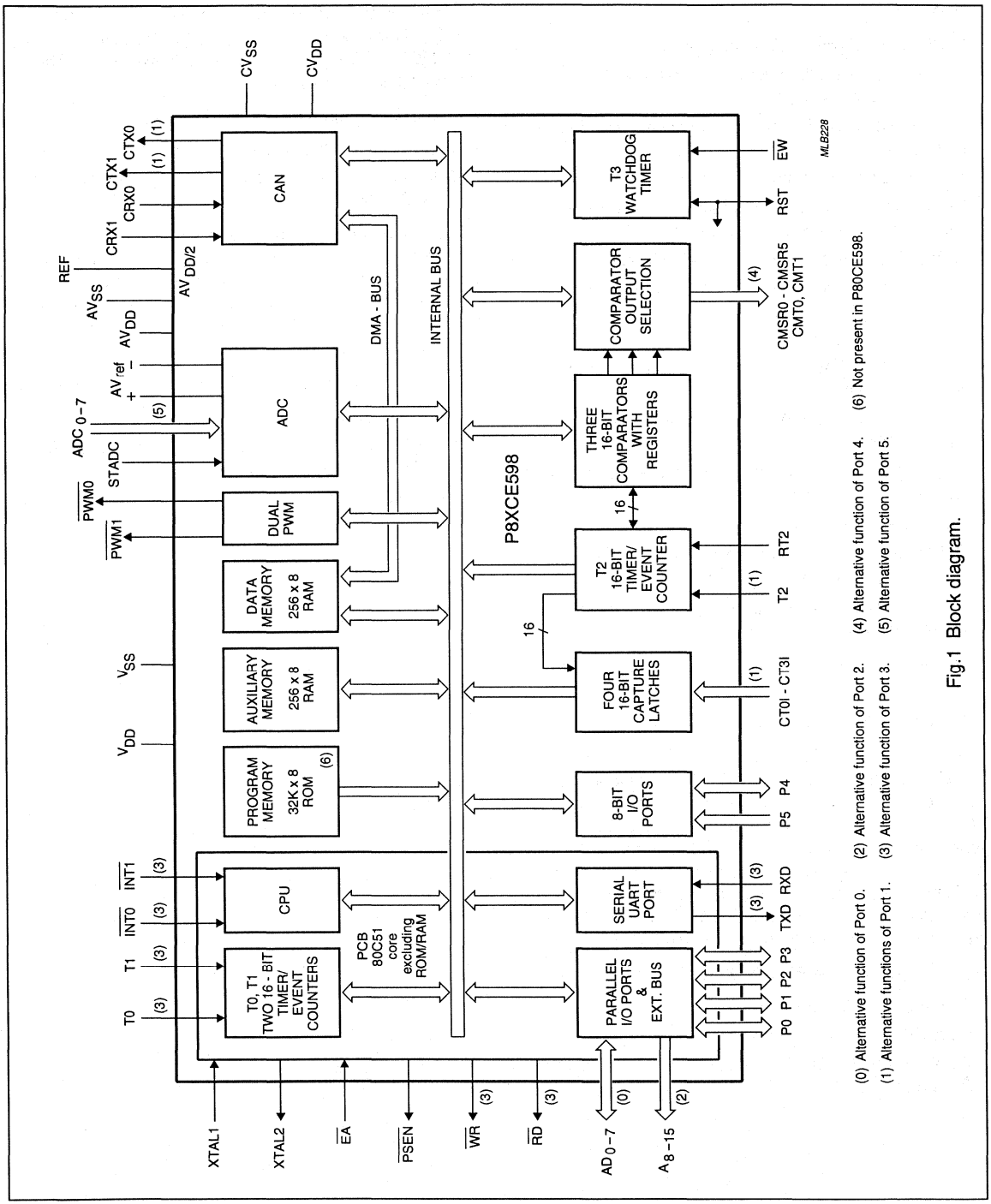
The P8xCE598 basically combines the functions of the existing P8xC552 and the Philips CAN-controller PCA82C200 (CAN = Controller Area Network) with the following enhanced features:

- 32 kbyte Program Memory
- 2 x 256 byte Data Memory
- DMA between CAN Transmit/Receive Buffer and internal RAM.

The temperature range includes a –40 to +85 °C version for general applications and an automotive temperature range version of –40 to +125 °C for the ROM and ROMless version with a maximum clock frequency of 16 MHz. The P87CE598 (EPROM/OTP version) has a temperature range of –40 to +85 °C.

The main differences to the P8xC552 microcontroller are:

- A CAN-controller substitutes the I^2C-serial interface
- 32 kbyte programmable ROM respectively, EPROM (P8xC552 has 8 kbyte)
- Additional 256 byte RAM.



(0) Alternative function of Port 0.
(1) Alternative functions of Port 1.
(2) Alternative function of Port 2.
(3) Alternative function of Port 3.
(4) Alternative function of Port 4.
(5) Alternative function of Port 5.
(6) Not present in P80CE598.

Fig.1 Block diagram.

2 GENERAL DESCRIPTION

The 84C122 is a stand-alone microcontroller designed for use in remote control transmitters for a wide range of applications. The 84C122 for this purpose provides a number of dedicated hardware functions for remote controller applications.

These include the following additional blocks to the 84CXXX core:

- Interrupt Gate
- Hardware Modulator
- Output Driver
- Watchdog Timer.

Although the 84C122 is specifically referred to throughout this data sheet, the information applies to all the devices. The small differences between the 84C122 and the other devices are specified in the text and also highlighted in Chapter 3.

The 84CXXX core 8-bit microcontroller family specification is described in *"Section 4"* of *"Data Handbook IC14"*. With reference specifically to Chapter *"Functional description"* (interrupts, reset, stop mode etc.) and to the Chapter *"Instruction set"*.

The general block diagram of the device is shown in Fig.2. The 84CXXX core plus 8 kbytes ROM and 64 bytes RAM has the same function as described in the data sheet of the 84CXXX.

When the transmitter is not in use the microcontroller is in STOP mode and the oscillator is HALTED. The AND gate from P1 Port line provides the wake-up to end STOP mode.

The Hardware Modulator produces pulse bursts according to the required protocol. By software the 'ON-time' and the 'OFF-time' of each pulse and the number of pulses are controlled.

The Output Driver can handle sufficient current to drive a single transistor, and this can provide the required current for the LED.

The Watchdog Timer will reset the 84C122 when it has not been reloaded (reset) in time, because the program has run out of sequence (endless loop, continuous IDLE mode, etc.). During STOP mode the oscillator is halted, so then the Watchdog Timer is not running.

3 MEMORY AND I/O CONFIGURATIONS

DEVICE	RAM	ROM	I/O LINES
PCA84C122A	32 bytes	1K	16
PCA84C122B	32 bytes	1K	12
PCA84C222A	32 bytes	2K	16
PCA84C222B	32 bytes	2K	12
PCA84C422A	32 bytes	4K	16
PCA84C422B	32 bytes	4K	12
PCA84C622A	64 bytes	6K	16
PCA84C622B	64 bytes	6K	12
PCA84C622C	64 bytes	6K	20[1]
PCA84C822A	64 bytes	8K	16
PCA84C822B	64 bytes	8K	12
PCA84C822C	64 bytes	8K	20[1]

Note

1. 4 I/O lines with 10 mA sink capability.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATASHEET

5 BLOCK DIAGRAM

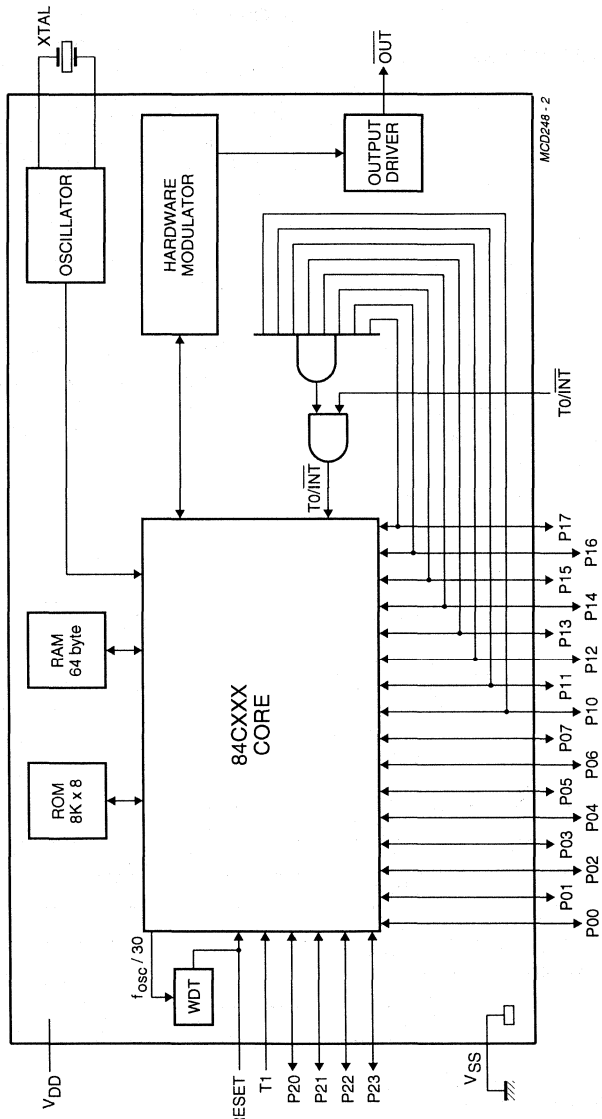


Fig.2 Block diagram.

128 × 8-bit EEPROM with I²C-bus interface PCA8581; PCA8581C

FEATURES

- Operating supply voltage:
  - 4.5 to 5.5 V (PCA8581)
  - 2.5 to 6.0 V (PCA8581C)
- Integrated voltage multiplier and timer for writing (no external components required)
- Automatic erase before write
- Low standby current; maximum 10 μA
- 8-byte page write mode
- Serial input/output bus (I²C-bus)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Designed for minimum 10000 write cycles per byte
- 10 years minimum non-volatile data retention
- Infinite number of read cycles
- Pin and address compatibility to PCF8570, PCF8571 and PCF8582
- Operating temperature: –25 to +85 °C.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

GENERAL DESCRIPTION

The PCA8581 and PCA8581C are low power CMOS EEPROMs with standard and wide operating voltages:

4.5 to 5.5 V (PCA8581)

2.5 to 6.0 V (PCA8581C).

In the following text, the generic term 'PCA8581' is used to refer to both types in all packages except when otherwise specified.

The PCA8581 is organized as 128 words of 8-bytes.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C-bus). The built-in word address register is incremented automatically after each written or read data byte. All bytes can be read in a single operation. Up to 8 bytes can be written in one operation, reducing the total write time per byte. Three address pins, A0, A1 and A2 are used to define the hardware address, allowing the use of up to 8 devices connected to the bus without additional hardware.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage				
	PCA8581		4.5	5.5	V
	PCA8581C		2.5	6.0	V
I_{DD}	supply current (standby)	f_{SCL} = 0 Hz	–	10	μA
T_{amb}	operating ambient temperature		–25	+85	°C
T_{stg}	storage temperature	without EEPROM retention	–65	+150	°C
		with EEPROM retention	–65	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA8581P	8	DIP	plastic	SOT97-1
PCA8581CP	8	DIP	plastic	SOT97-1
PCA8581T	8	SO8	plastic	SOT96-1
PCA8581CT	8	SO8	plastic	SOT96-1

BLOCK DIAGRAM

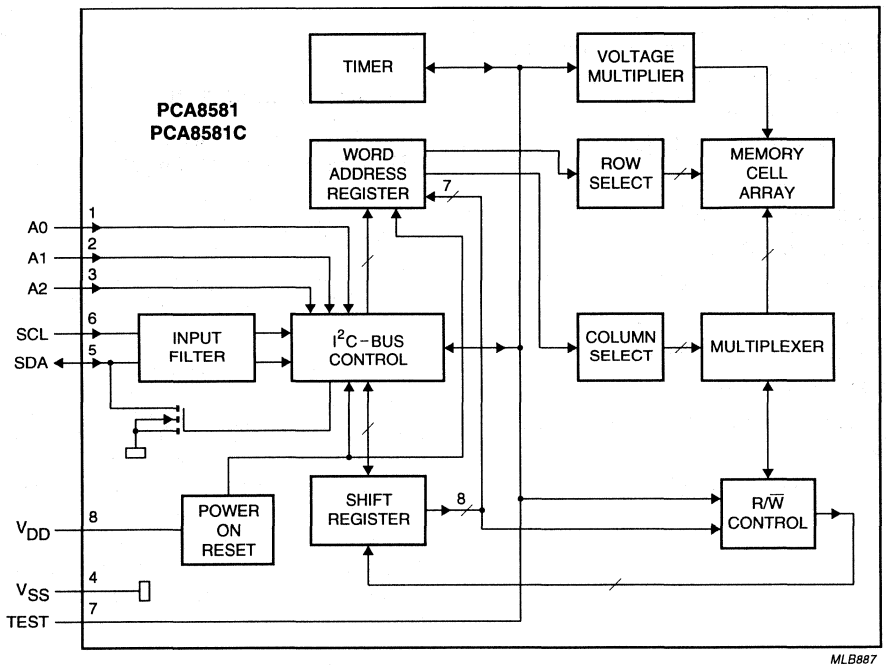


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	hardware address input 0
A1	2	hardware address input 1
A2	3	hardware address input 2
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
TEST	7	test output can be connected to V_{SS}, V_{DD} or left open-circuit
V_{DD}	8	positive supply

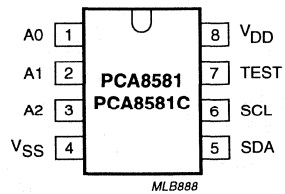


Fig.2 Pin configuration.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

18-ELEMENT BAR GRAPH LCD DRIVER

GENERAL DESCRIPTION

The PCF1303T is an 18-element bar graph LCD driver with linear relation to control voltage (V_c) when in pointer or thermometer mode.

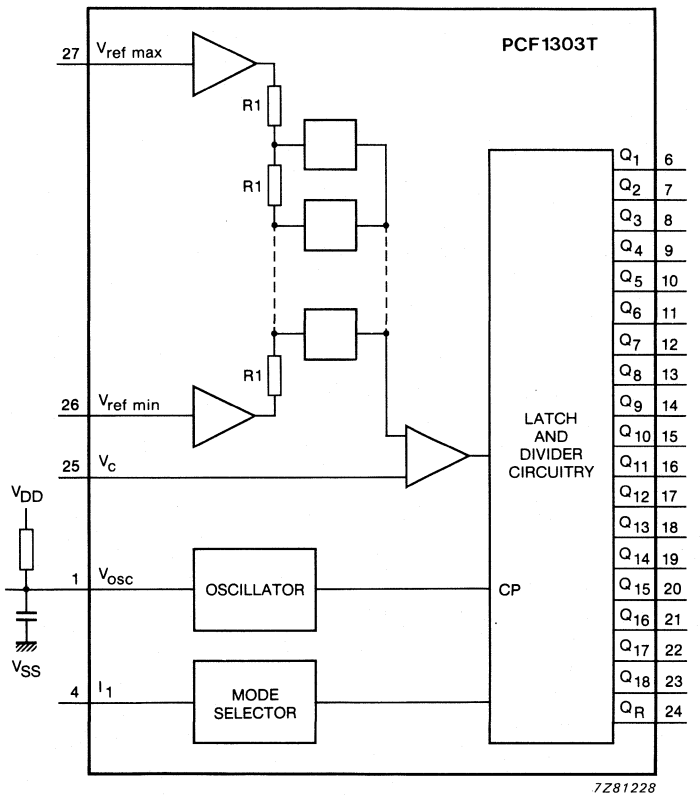


Fig. 1 Block diagram.

PACKAGE OUTLINE

PCF1303T: 28-lead mini-pack; plastic (SO28; SOT136A).

LCD controller/driver for 2-line x 24 or 4-line x 12 character displays

PCF2115

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC03 OR DATASHEET

FEATURES

- Single-chip LCD controller/driver
- 1 or 2-line display with up to 24 characters per line or 4 lines of up to 12 characters per line
- 5 x 7 character format plus cursor (5 x 8 for kana and user defined symbols)
- On-chip generation of LCD supply voltage (external supply also possible)
- On-chip generation of intermediate LCD bias voltages
- On-chip oscillator requires no external components (external clock is also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 5 x 8 characters
- Character generator RAM: 8 5 x 8 characters
- 4 or 8-bit parallel I²C-bus
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1:32 and 1:16 (for 4, 2 and 1-line displays respectively)
- Uses common 11 code instruction set
- Optimized for single-plane wiring applications
- Logic supply voltage range, V_{DD} - V_{SS} = 2.5 to 6.0 V
- Display supply voltage range, V_{DD} - V_{LCD} = 3.5 to 9.0 V
- Low power consumption.

APPLICATIONS

- Car radios
- Telecom equipment
- Portable instruments
- Point-of-sale terminals

GENERAL DESCRIPTION

The PCF2115 is a low-power CMOS LCD controller and driver which has been designed to drive a split screen dot matrix LCD display of 1 or 2 lines x 24 characters or 4 lines x 12 characters with a 5 x 8-dot format. All essential functions for the display are provided on a single chip, including on-chip generation of LCD bias voltages. This results in a minimum requirement of external components and lower system power consumption. The chip contains a character generator and can display alphnumeric and kana characters. The PCF2115 can interface to the majority of microcontrollers via a 4 or 8-bit I²C-bus.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF2115	108	CPGA108	CERAMIC	SOT265

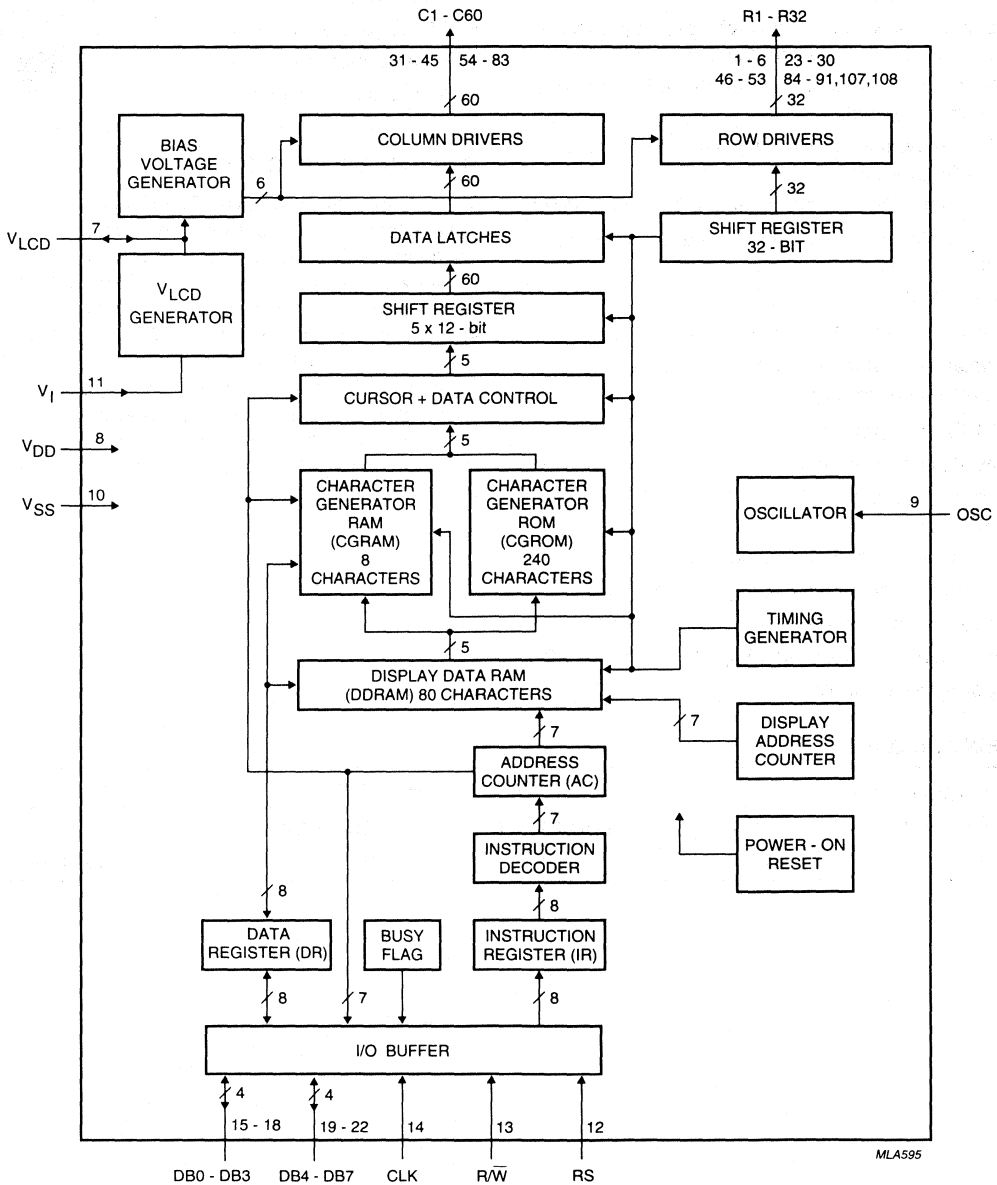


Fig.1 Block diagram.

LCD controller/drivers

PCF2116 family (PCF2114X; PCF2116X)

FEATURES

- Single chip LCD controller / driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- On-chip:
  - generation of LCD supply voltage (external supply also possible)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I²C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

GENERAL DESCRIPTION

The PCF2116 family of LCD controller/drivers consists of 2 similar members: PCF2116X and PCF2114X, later referred to as PCF2116. The specific differences are expressed in separate paragraphs for PCF2116X and PCF2114X respectively. The letter X in PCF2116X or PCF2114X specifies the character set in the character generator ROM (CGROM). The different character sets currently available are specified by the letters A, C, G and J (see Figs 7 to 10). Set 'A' in PCF2116A characterises the built-in standard character set. Other character sets are available on request.

The PCF2116 is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system power consumption. The chip contains a character generator and displays alphanumeric and kana characters. The PCF2116 interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus.

Packages

- PCF2116XU/10; chip on FFC
- PCF2114XU/10; chip on FFC
- PCF2116XU/12; chip with bumps on FFC
- PCF2114XU/12; chip with bumps on FFC
- PCF2116XH; SQFP128 (14 × 20 mm)
- Pin grid array PGA144 (samples only).

For further details see Chapters "Bonding pad locations"and "Package outline".

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF2114XH	128	SQFP128	plastic	SOT387-1
PCF2116XH	128	SQFP128	plastic	SOT387-1
PCF2114XU	116	FFC116	–	–
PCF2116XU	116	FFC116	–	–

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

BLOCK DIAGRAM

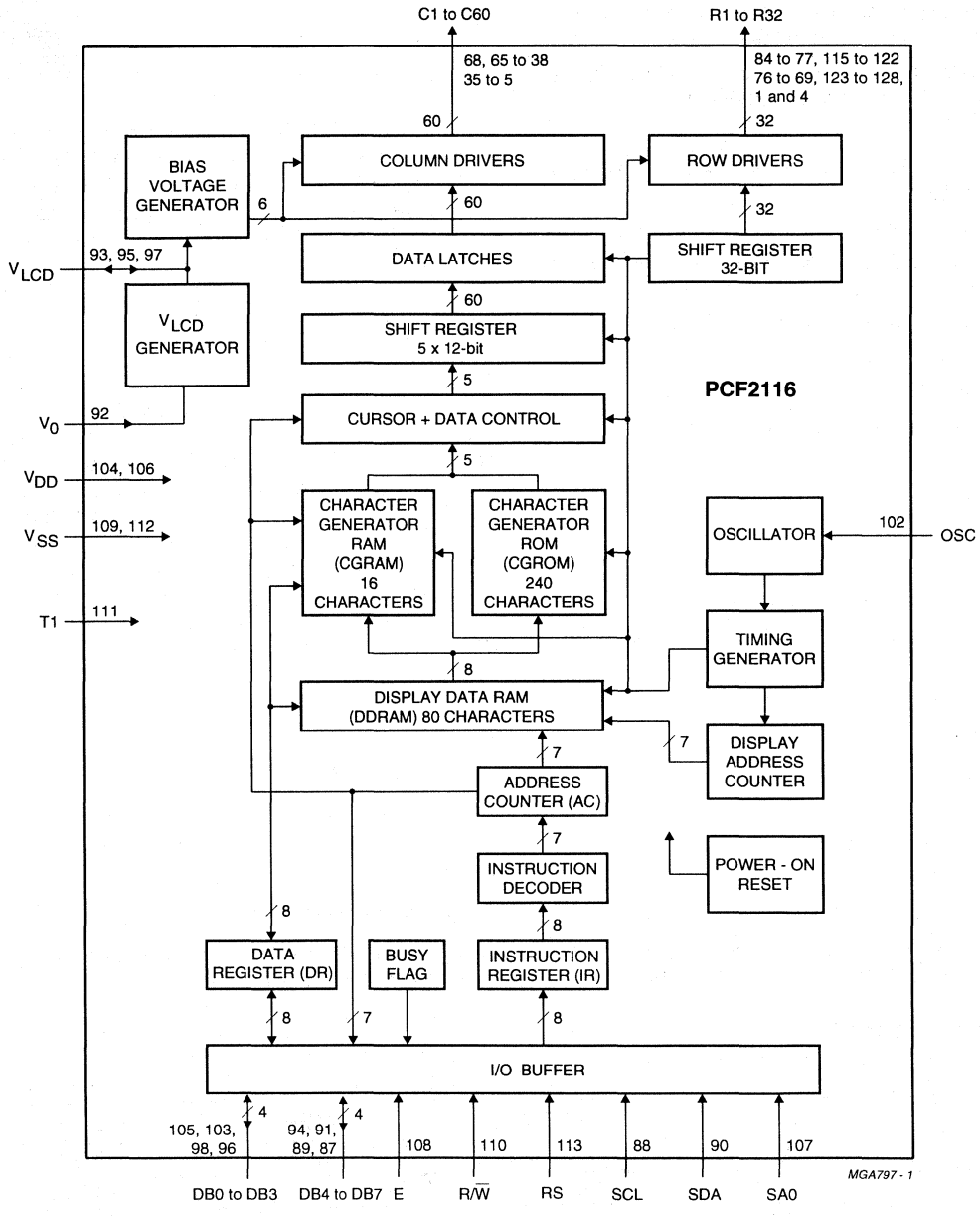


Fig.1 Block diagram (SQFP128).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT129).
PCF8566T: 40-lead mini-pack (VSO40; SOT158A).

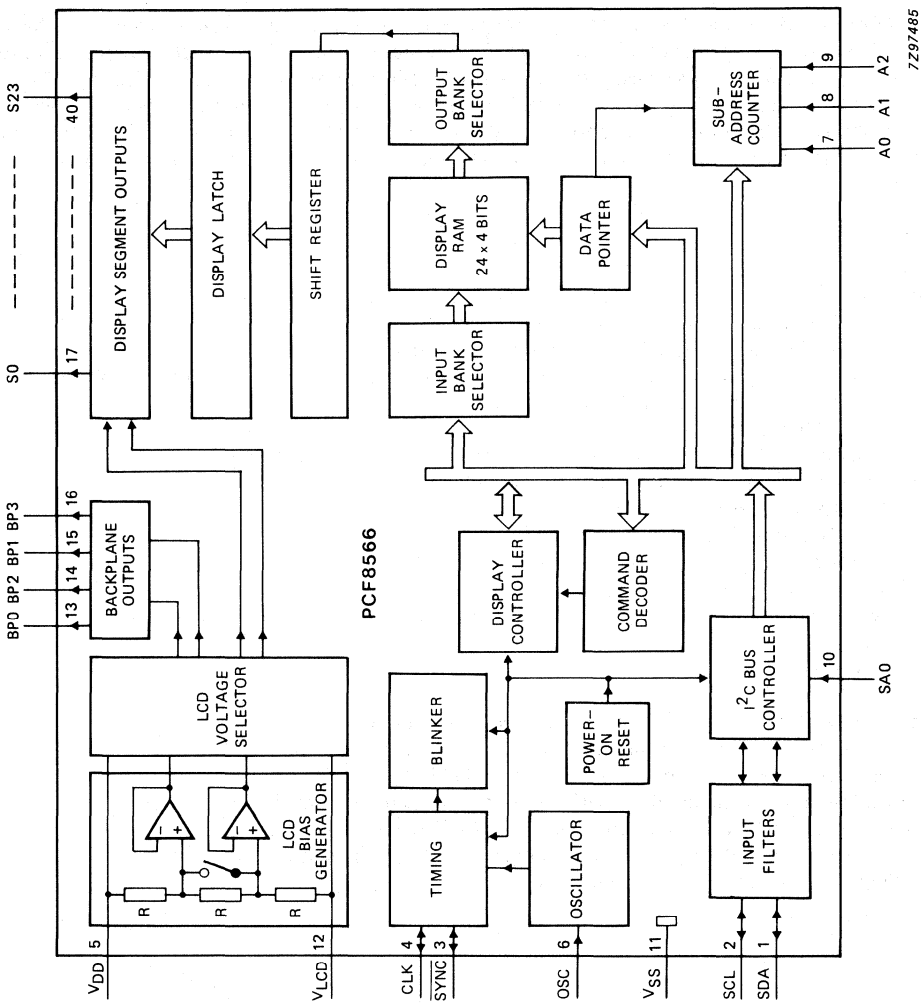


Fig. 1 Block diagram.

LCD row driver for dot matrix displays

PCF8568

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

FEATURES

- Single chip LCD row driver with 16 outputs
- Low power consumption
- Selectable multiplex rate 1:8, 1:16, 1:24, 1:32
- Cascadable to 1:24 or 1:32 multiplex rates
- Internally generated intermediate LCD bias voltages
- LCD column bias voltages available at pins VO3 and VO4
- Minimizes display system power requirements
- On-chip oscillator, requires only one external resistor
- Power-on reset blanks display
- Logic voltage range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9.0 V
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring
- Available in 28-lead plastic DIL or space saving mini-pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- General instrumentation
- Consumer products.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range	+2.5	-	+6.0	V
V_{LCD}	LCD supply voltage range voltage	V_{DD} −9	-	V_{DD} −3.5	V
I_{DD2}	supply current with internal clock (R_{OSC} = 330 kΩ)	-	67	150	µA
T_{amb}	operating ambient temperature range	−40	-	+85	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8568P	28	DIL	plastic	SOT117
PCF8568T	28	SO28	plastic	SOT136A
PCF8568U/7	(28 pads)	die: bumped chip on tape	-	-

GENERAL DESCRIPTION

The PCF8568 is a low power LCD row driver, designed to drive dot matrix graphic displays with multiplex rates of 1:8 or 1:16. The device has 16 row outputs. Two devices may be cascaded to drive displays with multiplex rates of 1:24 or 1:32. The PCF8568 is optimised for use with the PCF8569 and PCF8579 LCD dot matrix column drivers. Intermediate LCD bias voltages are internally generated. LCD column bias voltages are available at pins VO3 and VO4 for connection to the column drivers. The PCF8568 is compatible with most microcontrollers and communicates via a two- line bidirectional bus (I²C).

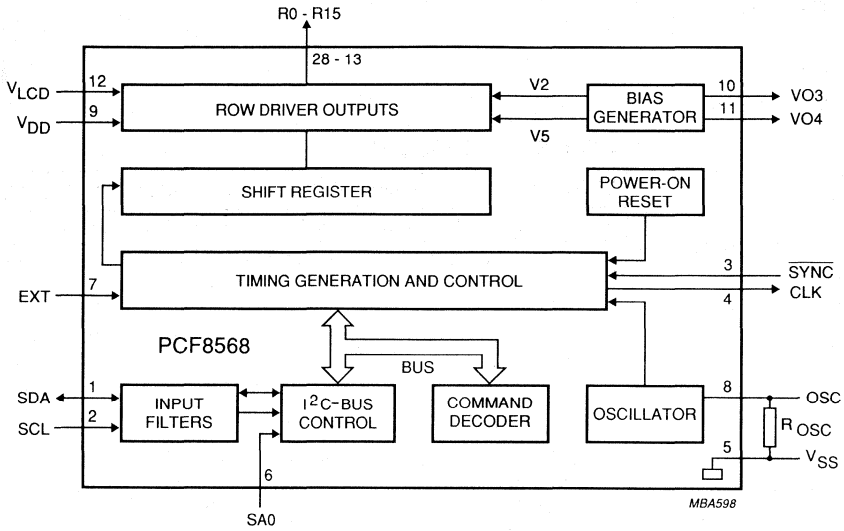


Fig.1 Block diagram.

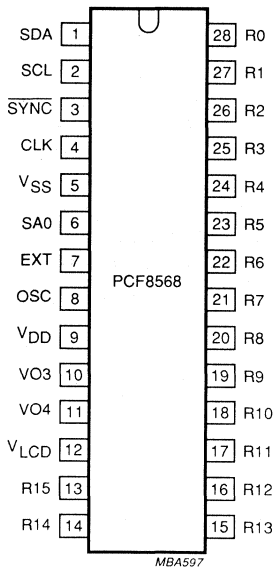


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus serial data line
SCL	2	I²C-bus serial clock line
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	clock output
V_{SS}	5	ground (logic)
SA0	6	I²C-bus slave address input (bit 0)
EXT	7	external clock select pin
OSC	8	oscillator or external clock input pin
V_{DD}	9	positive supply voltage
VO3	10	LCD bias voltage output (V3)
VO4	11	LCD bias voltage output (V4)
V_{LCD}	12	LCD supply voltage
R15 to R0	13 to 28	LCD row driver outputs

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8569 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8 or 1:16. The device has 40 outputs and can drive 16 x 40 dots in a 16 row multiplexed LCD. Up to 16 PCF8569s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8568/78/79 family of LCD row/column drivers. Together the PCF8568, PCF8578 and PCF8569 form a general LCD dot matrix driver chip set, capable of driving displays of up to 20 480 dots. The PCF8569 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

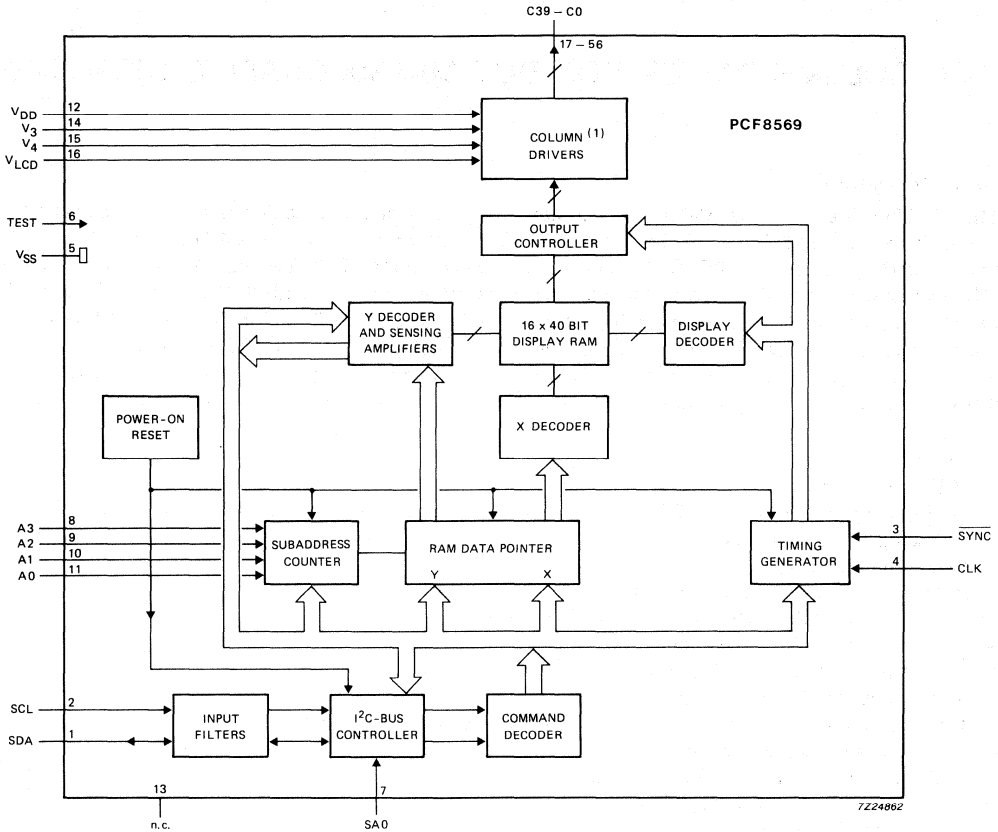
- LCD column driver
- Used in conjunction with the PCF8568 or PCF8578, this device forms part of a chip set capable of driving up to 20 480 dots.
- 40 column outputs
- Selectable multiplex rates; 1:8 or 1:16
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications
- 640-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack or 64-lead tab module

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8569T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8569V: 64-lead tape-automated-bonding (tab) module (SOT267).



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram (pin numbers shown for VSO56; SOT190).

256 × 8-bit static low-voltage RAM with I²C-bus interface

PCF8570

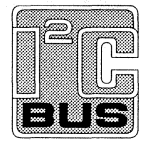
FEATURES

- Operating supply voltage 2.5 to 6.0 V
- Low data retention voltage; minimum 1.0 V
- Low standby current; maximum 15 μA
- Power saving mode; typical 50 nA
- Serial input/output bus (I²C-bus)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Available in DIP8 and SO8L packages.

APPLICATIONS

- Telephony:
  - RAM expansion for stored numbers in repertory dialling (e.g. PCD33XX applications)
- General purpose RAM for applications requiring extremely low current and low-voltage RAM retention (i.e. battery or capacitor backed)
- Radio, television and video cassette recorder:
  - channel presets
- General purpose:
  - RAM expansion for the microcontroller families PCD33XX, PCF84CXX, P80CLXXX and most other microcontrollers.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET



GENERAL DESCRIPTION

The PCF8570 is a low power static CMOS RAM.

The PCF8570 is organized as 256 words by 8-bits.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C-bus). The built-in word address register is incremented automatically after each written or read data byte. Three address pins, A0, A1 and A2 are used to define the hardware address, allowing the use of up to 8 devices connected to the bus without additional hardware.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.5	6.0	
I_{DD}	supply current (standby)	f_{SCL} = 0 Hz	–	15	μA
I_{DDR}	supply current (power-saving mode)	T_{amb} = 25 °C	–	400	nA
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8570P	8	DIP8	plastic	SOT97-1
PCF8570T	8	SO8L	plastic	SOT176-1

256 × 8-bit static low-voltage RAM with I²C-bus interface

PCF8570

BLOCK DIAGRAM

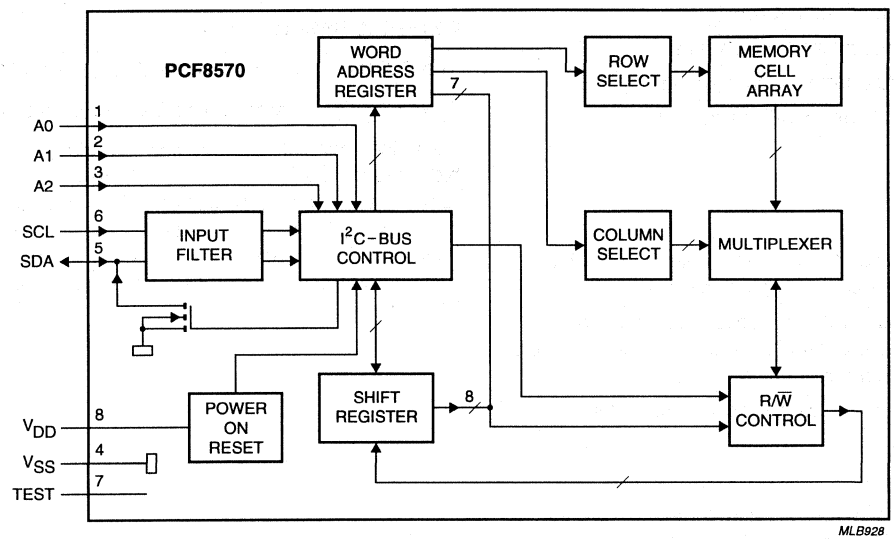


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	hardware address input 0
A1	2	hardware address input 1
A2	3	hardware address input 2
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
TEST	7	test output for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 13 and 14)
V_{DD}	8	positive supply

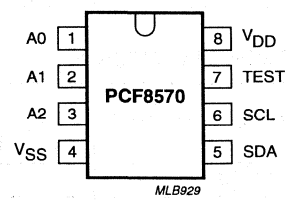


Fig.2 Pin configuration.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, CMOS circuit that functions as a real time clock/calendar with an I^2C-bus interface.
The IC incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred via a serial two-line bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1.2 V nickel cadium battery. The time base is generated from a 32.768 kHz crystal-controlled oscillator.

Features

- Serial input/output I^2C-bus interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32.768 kHz)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range					
clock (pin 16 to pin 15)	$V_{DD}-V_{SS1}$	1.1	–	6.0	V
I^2C interface (pin 16 to pin 8)	$V_{DD}-V_{SS2}$	2.5	–	6.0	V
Crystal oscillator frequency	f_{osc}	–	32.768	–	kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT38).
PCF8573T: 16-lead mini-pack; plastic (SO16L; SOT162A).

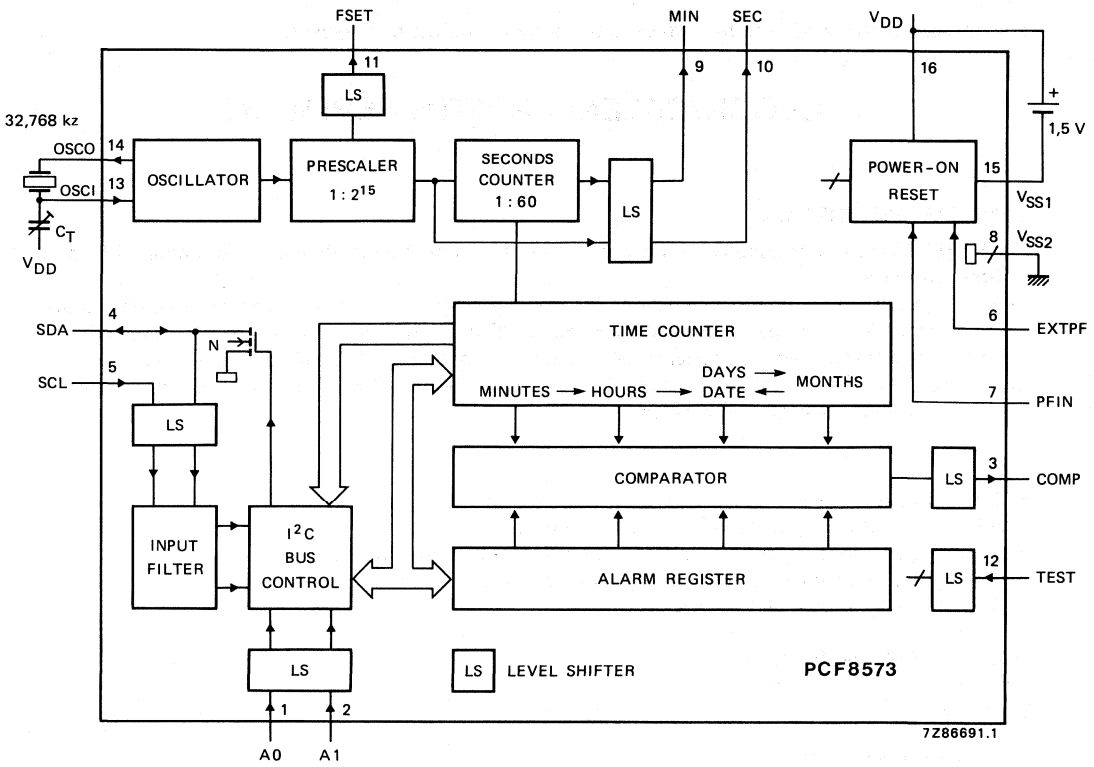


Fig.1 Block diagram.

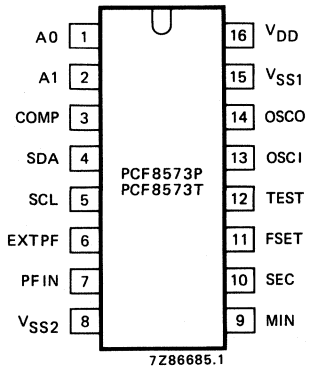


Fig.2 Pinning diagram.

PINNING

1	A0	address input
2	A1	address input
3	COMP	comparator output
4	SDA	serial data line ⎫ I^2C-bus
5	SCL	serial clock line ⎭
6	EXTPF	enable power fail flag input
7	PFIN	power fail flag input
8	V_{SS2}	negative supply 2 (I^2C interface)
9	MIN	one pulse per minute output
10	SEC	one pulse per second output
11	FSET	oscillator tuning output
12	TEST	test input; must be connected to V_{SS2} when not in use
13	OSCI	oscillator input
14	OSCO	oscillator input/output
15	V_{SS1}	negative supply 1 (clock)
16	V_{DD}	common positive supply

Remote 8-bit I/O expander for I²C-bus PCF8574

FEATURES

- Operating supply voltage 2.5 to 6 V
- Low standby current consumption of 10 μA maximum
- I²C to parallel port expander
- Open-drain interrupt output
- 8-bit remote I/O Port for the I²C-bus
- Compatible with most microcontrollers
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)
- DIP16, space-saving SO16 or SSOP20 package.

GENERAL DESCRIPTION

The PCF8574 is a silicon CMOS circuit. It provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I²C).

The device consists of an 8-bit quasi-bidirectional Port and an I²C interface. The PCF8574 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line ($\overline{INT}$) which is connected to the interrupt logic of the microcontroller on the I²C-bus. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and PCF8574A versions differ only in their slave address as shown in Fig.9.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8574P; PCF8574AP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
PCF8574T; PCF8574AT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCF8574TS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

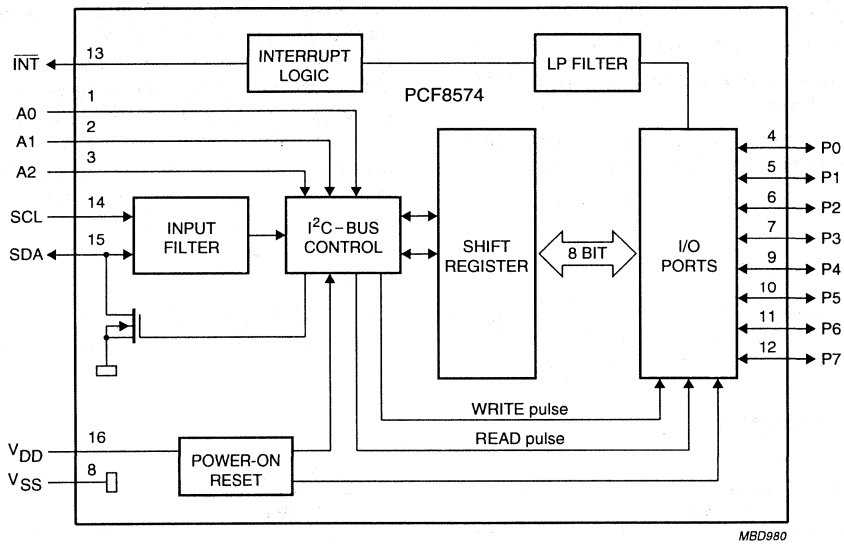


Fig.1 Block diagram (SOT38-1 and SOT162-1).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with the 24-segment LCD driver PCF8566
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO56) or 64-lead tape-automated-bonding (TAB) module (SOT267A)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8576U: uncased chip in tray.
PCF8576U/10: chip-on-film frame carrier (FFC).
PCF8576V: 64-lead tape-automated-bonding module (SOT267A).

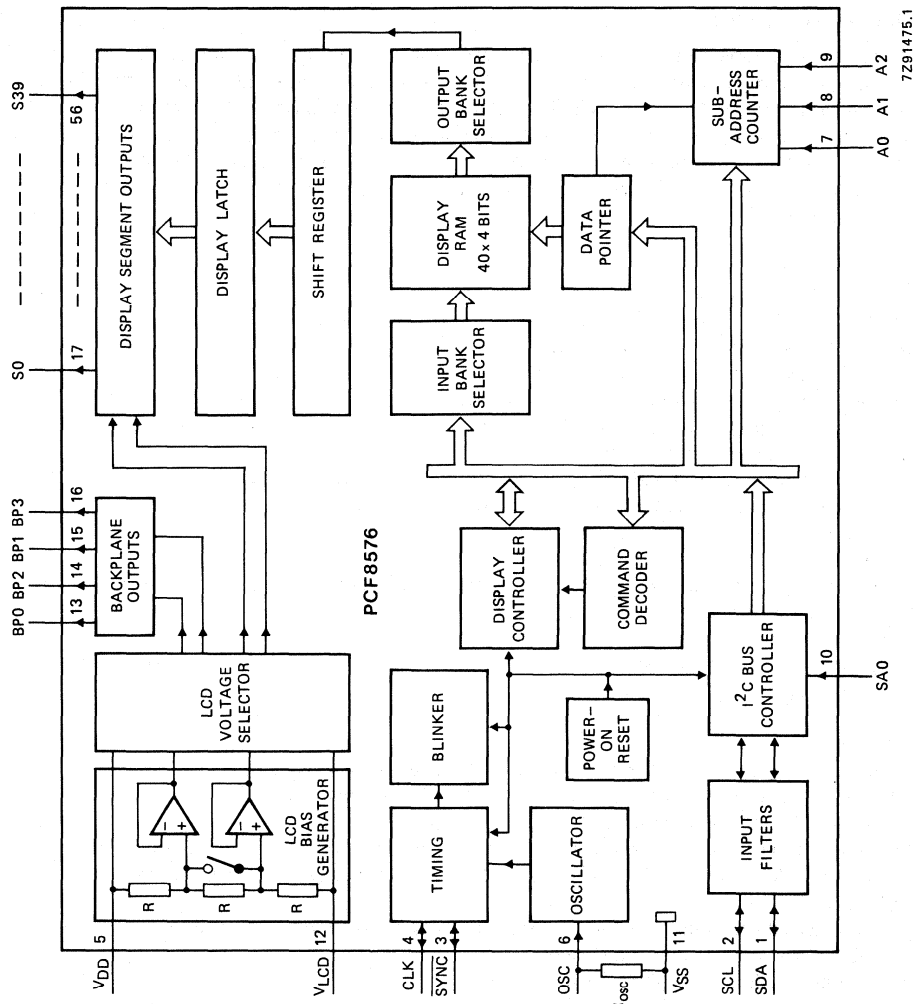


Fig.1 Block diagram; VSO56; SOT190.

LCD direct/duplex driver with I²C-bus interface

PCF8577C

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

FEATURES

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments
- Power-on reset blanks display.

GENERAL DESCRIPTION

The PCF8577C is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware subaddressing and display memory switching (direct drive mode).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8577CP	40	DIL	plastic	SOT129
PCF8577CT	40	VSO40	plastic	SOT158A
PCF8577CT	–	in blister tape	–	–
PCF8577CU/5	–	wafer unsawn	–	–
PCF8577CU/10	–	chip on film-frame-carrier (FFC)	–	–

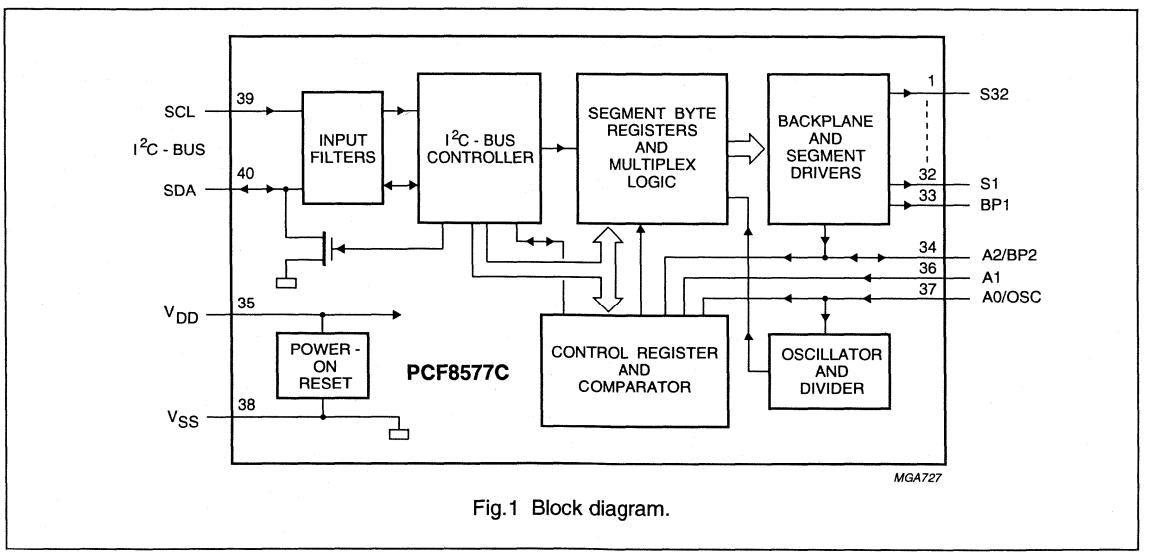


Fig.1 Block diagram.

LCD row/column driver for dot matrix graphic displays

PCF8578

FEATURES

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40960 dots possible)
- 40 driver outputs, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

GENERAL DESCRIPTION

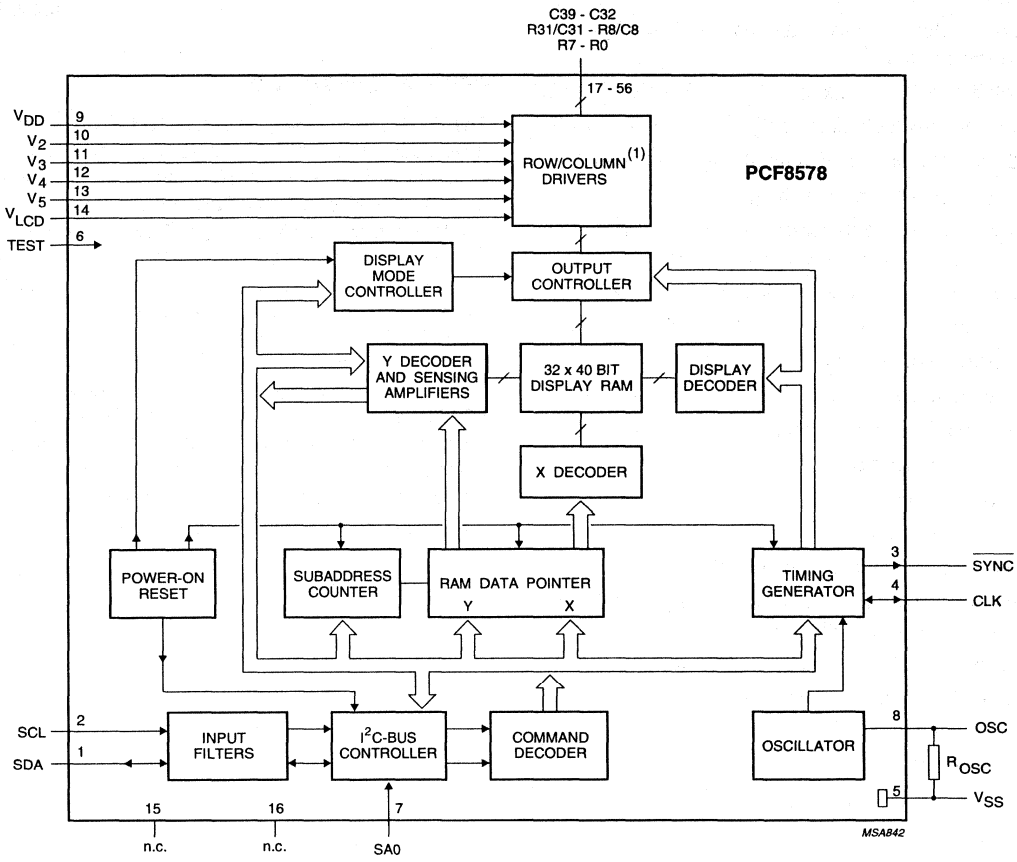
The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs, of which 24 are programmable, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8578T	56	VSO56	plastic	SOT190
PCF8578U7	–	chip with bumps on-tape	–	–

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

BLOCK DIAGRAM



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram.

LCD column driver for dot matrix graphic displays

PCF8579

FEATURES

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40960 dots
- 40 column outputs
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8578)
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8578)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

GENERAL DESCRIPTION

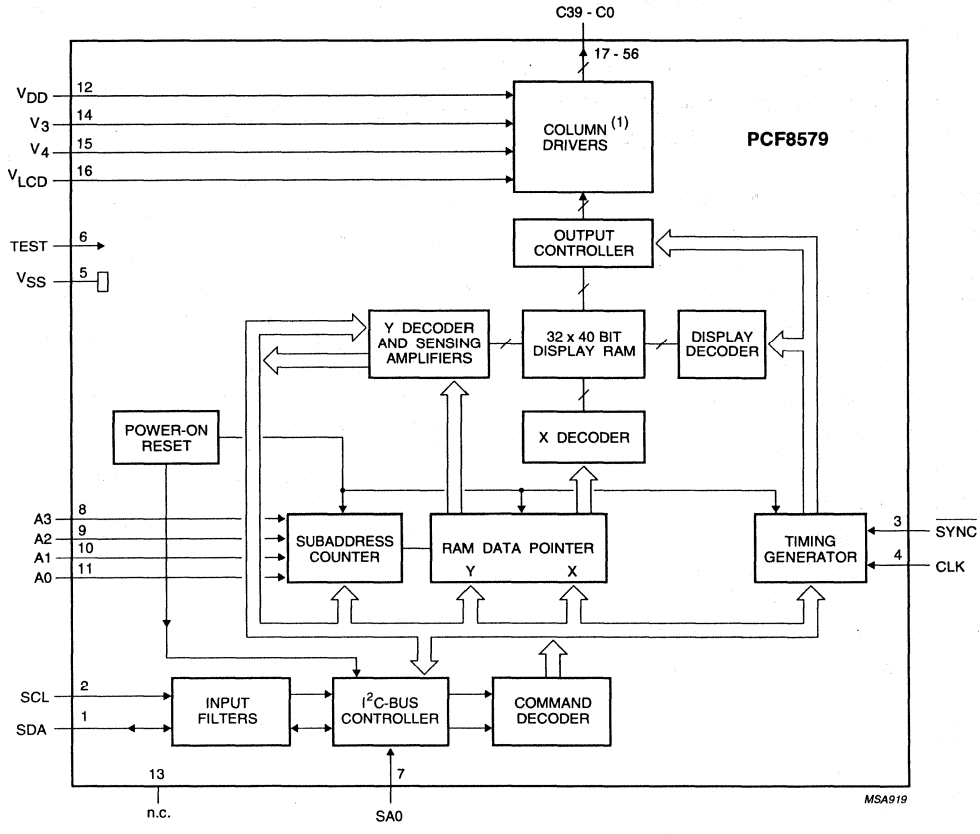
The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs and can drive 32 × 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I²C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8579T	56	VSO56	plastic	SOT190
PCF8579U7	–	chip with bumps on-tape	–	–

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

BLOCK DIAGRAM



(1) LCD voltage levels, all other blocks operate at logic levels.

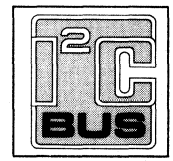
Fig.1 Block diagram.

Clock Calendar with 256 x 8-bit Static RAM

PCF8583

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

FEATURES



- I²C-bus interface operating supply voltage: 2.5 V to 6 V
- Clock operating supply voltage (0 to +70 °C): 1.0 V to 6.0 V
- Data retention voltage: 1.0 V to 6 V
- Operating current (f_{scl} = 0 Hz): max. 50 A
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Slave address, READ: A1 or A3, WRITE: A0 or A2.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
V_{DD}	supply voltage operating range	I²C-bus active	2.5	6.0	V
V_{DD}	supply voltage operating range	I²C-bus inactive	1.0	6.0	V
I_{DD}	supply current operating mode	f_{scl} =100 kHz	-	200	µA
I_{DDO}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V f_{scl} = 0 Hz; V_{DD} = 1 V	- -	50 10	µA µA
T_{amb}	operating ambient temperature range		–40	+85	°C
T_{stg}	storage temperature range		–65	+150	°C

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8 bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8583P	8	DIL	plastic	SOT97
PCF8583T	8	mini-pack	plastic	SO8L; SOT176C

Clock Calendar with 256 x 8-bit Static RAM

PCF8583

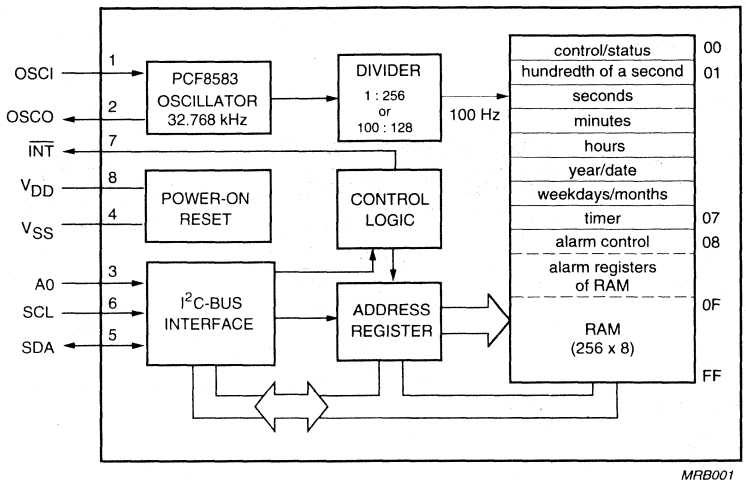


Fig.1 Block diagram.

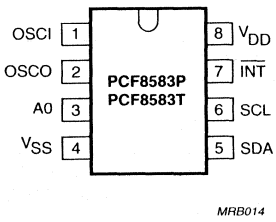


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
A0	3	address input
V_{SS}	4	negative supply
SDA	5	serial data line
SCL	6	serial clock line
$\overline{INT}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

I²C-BUS CONTROLLER

GENERAL DESCRIPTION

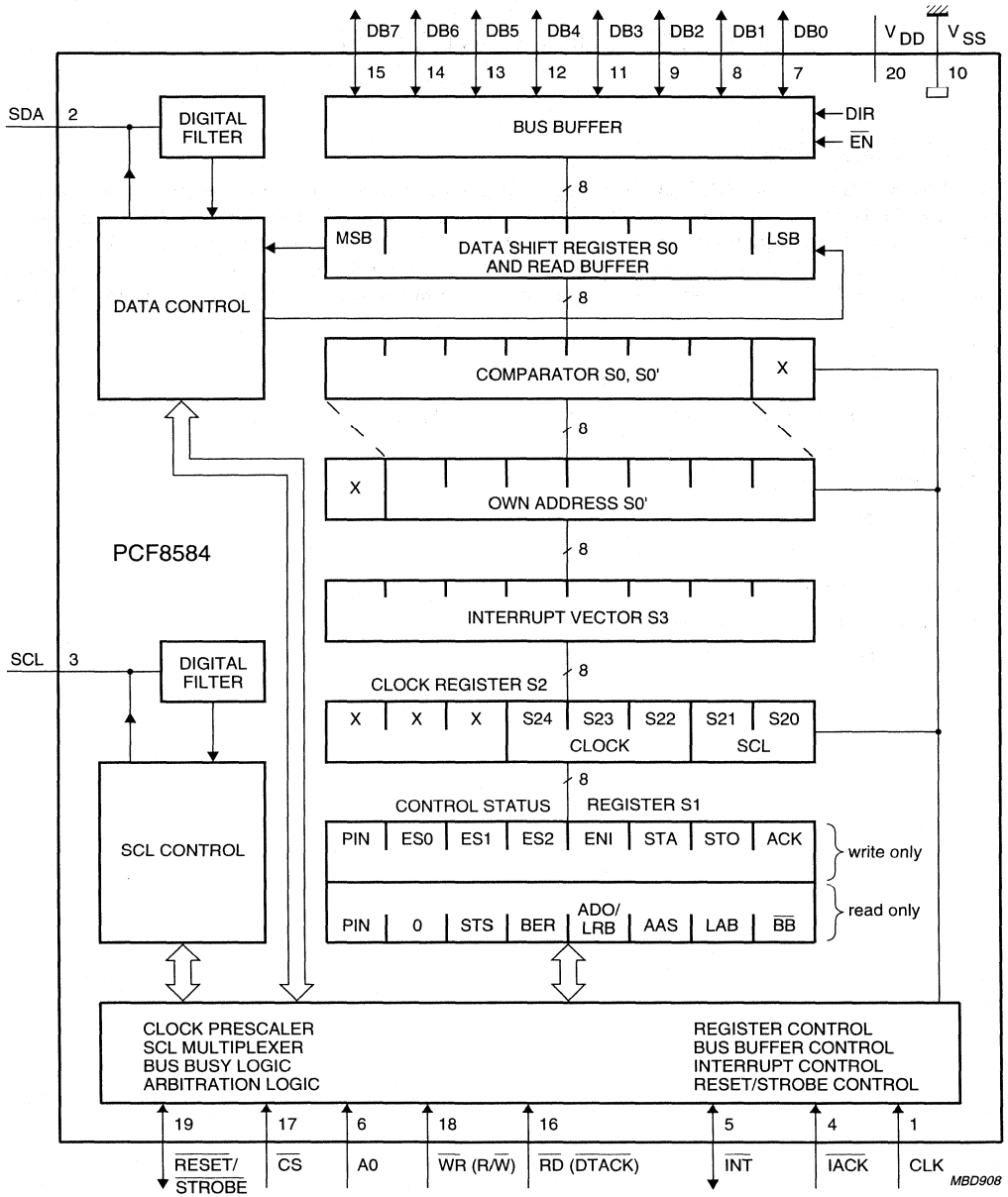
The PCF8584 is an integrated circuit designed in CMOS technology which serves as an interface between most standard parallel-bus microcontrollers/processors and the serial I²C-bus. The PCF8584 provides both master and slave functions. Communication with the I²C-bus is carried out on a byte-wise basis using interrupt or polled handshake. It controls all the I²C-bus specific sequencing, protocol, arbitration and timing. The PCF8584 allows parallel-bus systems to communicate bidirectionally with the I²C-bus.

Features

- Parallel-bus/I²C-bus protocol converter
- Compatible with most parallel-bus processors including MAB8049, MAB8051, SCN68000 and Z80
- Automatic selection of bus interface
- Programmable interrupt vector
- Multi-master capability
- I²C-bus monitor mode
- Long-distance mode
- Operating supply voltage 4.5 to 5.5 V
- Operating temperature range −40 to +85 °C

PACKAGE OUTLINES

PCF8584P: 20-lead DIL; plastic (SOT146).
PCF8584T: 20-lead mini-pack; plastic (SO20; SOT163A).



Where:

( ) indicate the SCN68000 pin name designations.
X = don't care.

Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

8-BIT A/D AND D/A CONVERTER

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

Features

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P: 16-lead DIL; plastic (SOT38).
PCF8591T: 16-lead mini-pack; plastic (SO16L; SOT162A).

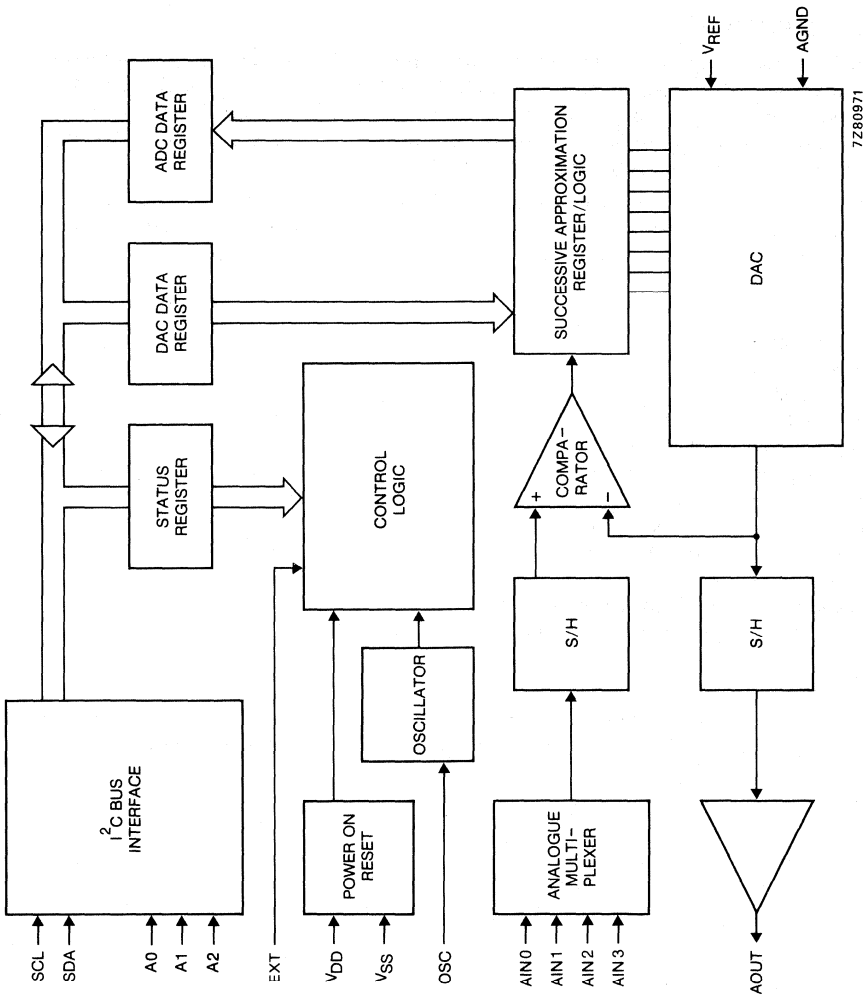


Fig. 1 Block diagram.

Low power clock calendar PCF8593

FEATURES

- I²C-bus interface operating supply voltage: 2.5 to 6.0 V
- Clock operating supply voltage (T_{amb} = 0 to +70 °C): 1.0 to 6.0 V
- Data retention voltage: 1.0 to 6.0 V
- External $\overline{\text{RESET}}$ input pin
- Operating current (f_{scl} = 0 Hz, 32 kHz time base, V_{DD} = 2.0 V): typ. 1 µA
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C-bus)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Space-saving SO8 package
- Slave address:
  - READ A3H
  - WRITE A2H.

GENERAL DESCRIPTION

The PCF8593 is a CMOS Real-time clock/calendar optimized for low power consumption. Addresses and data are transferred serially via a two-line bidirectional bus (I²C-bus). The built-in word address register is incremented automatically after each written or read data byte. The built-in 32.768 kHz oscillator circuit and the first 8 registers are used for the clock/calendar and counter functions. The next 8 registers may be programmed as alarm registers or used as free RAM space.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage operating mode	I²C-bus active	2.5	6.0	V
		I²C-bus inactive	1.0	6.0	V
I_{DD}	supply current operating mode	f_{scl} = 100 kHz	–	200	µA
I_{DD}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V	4.0	15.0	µA
		f_{scl} = 0 Hz; V_{DD} = 2 V	1.0	8.0	µA
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8593P	8	DIL	plastic	SOT97-1
PCF8593T	8	SO8	plastic	SOT96-1

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

BLOCK DIAGRAM

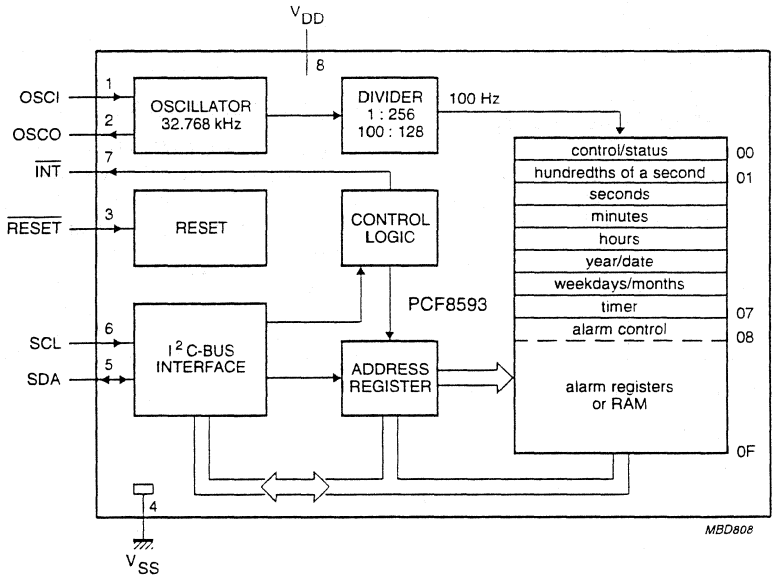


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
$\overline{\text{RESET}}$	3	reset input (active LOW)
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
$\overline{\text{INT}}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

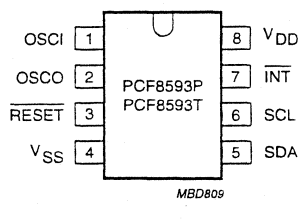


Fig.2 Pin configuration.

256 x 8-BIT CMOS EEPROMS with I²C-bus interface

PCx8582x-2

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

FEATURES

- Non-volatile storage of 2 Kbits organized as 256 x 8-bits
- Only one power supply required
- On chip voltage multiplier
- Serial input/output bus (I²C)
- Low power CMOS; maximum active current 2 mA, maximum standby current 10 µA
- Power-on reset
- 10 years non-volatile data retention time
- Pin and address compatible to PCF8570, PCF8571, PCF8572 and PCF8581
- Write operations

  byte write mode

  8-byte page write mode (minimizes total write time per byte)
- Read operations

  sequential read and random read
- Extended supply voltage range (2.5 to 6.0 V)
- Internal timer for writing (no external components)
- High reliability by using a redundant storage code
- Endurance 100 k; T_{amb} = +85 °C

GENERAL DESCRIPTION

The 2 Kbit (256 x 8-bit) CMOS EEPROMS are floating gate electrically erasable programmable read only memories. By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to eight PCx8582x-2 devices can be connected to the I²C-bus.
Chip select is accomplished by the three address inputs.

Timing of the Erase/Write cycle is achieved internally, thus no external components are required. Pin 7 must be connected to either V_{DD} or left open-circuit.

An option exists for using an external clock for timing the length of an Erase/Write cycle.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive suppy voltage		2.5	–	6.0	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz				
		V_{DD} = 3 V	–	–	60	µA
		V_{DD} = 6 V	–	–	200	µA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz				
		V_{DD} = 3 V	–	–	0.5	mA
		V_{DD} = 6 V	–	–	2.0	mA
I_{DDO}	supply current STANDBY					
		V_{DD} = 3 V	–	–	3.5	µA
		V_{DD} = 6 V	–	–	10	µA

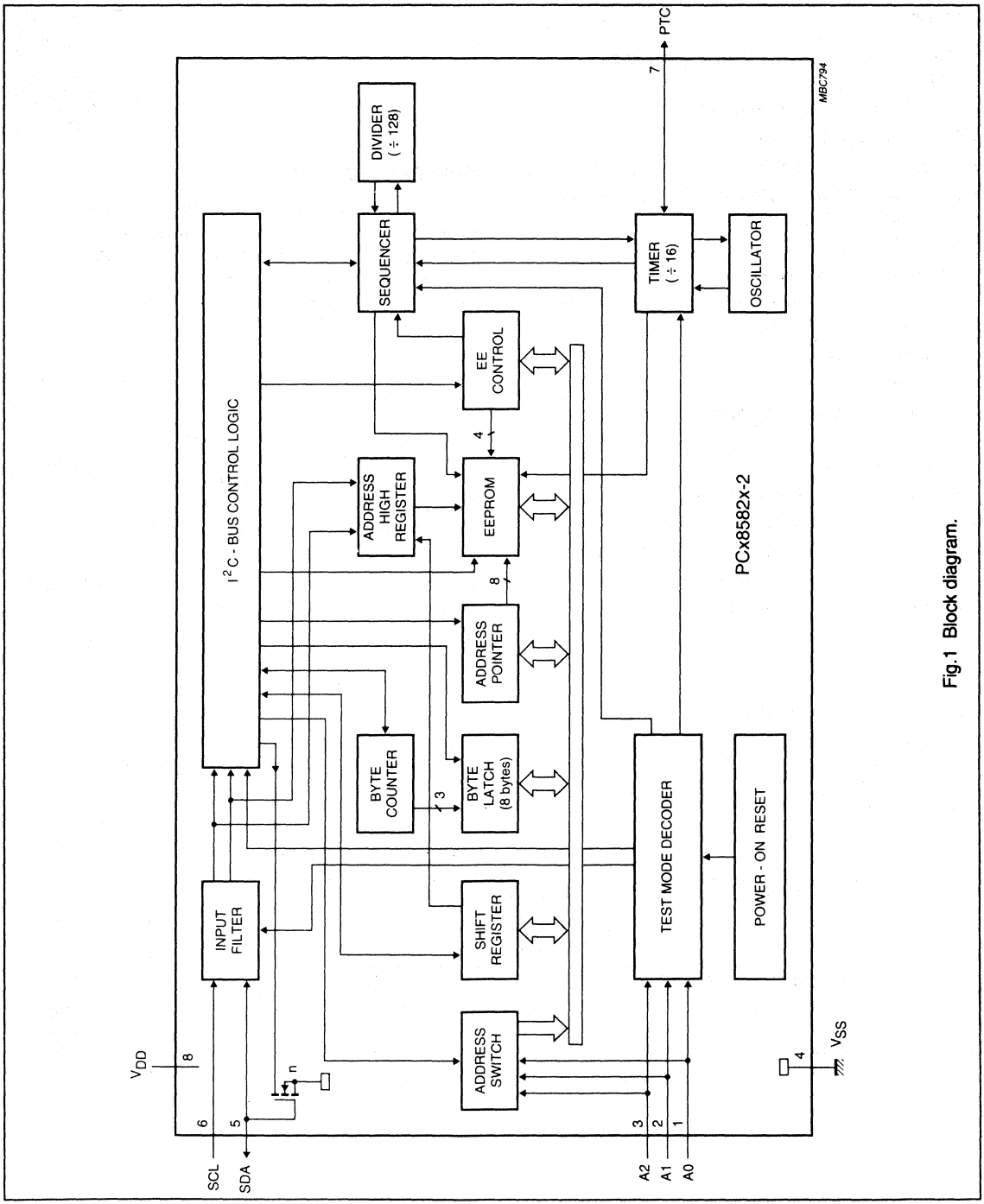


Fig.1 Block diagram.

512 x 8-bit CMOS EEPROMS with I²C-bus interface

PCx8594x-2 Family

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

FEATURES

- Low Power CMOS
  - maximum active current 2.5 mA
  - maximum standby current 10 µA
- Non-volatile storage of 4-Kbits organized as two pages
  - each 256 x 8-bits
- Only one power supply required
- On-chip voltage multiplier
- Serial input/output bus (I²C)
- Write operations
  - byte write mode
  - 8-byte page write mode (minimizes total write time per byte)
- Write-protection input
- Read operations
  - sequential read
  - random read
- Extended supply voltage range (2.5 to 6.0 V)
- Internal timer for writing (no external components)
- Power-on reset
- High reliability by using a redundant storage code (single bit error correction)
- Endurance
  - 100 k; T_{amb} = 85 °C
- 10 years non-volatile data retention time
- Pin and Address compatible to
  - PCx8582x-2 Family and PCx8589x2 Family

GENERAL DESCRIPTION

The PCx8594x-2 is a 4-Kbit (512 x 8-bit) floating gate electrically erasable programmable read only memory (EEPROM). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to four PCx8594x-2 devices may be connected to the I²C-bus. Chip select is accomplished by two address inputs.

Timing of the Erase/Write cycle is done internally, thus no external components are required. Pin 7 must be connected to either V_{DD} or left open-circuit.

There is an option of using an external clock for timing the length of an Erase/Write cycle.

A write protection input (pin 1) allows disable of write-commands from the master by a hardware signal. When pin 1 is HIGH and one of the upper 256 EEPROM cells is addressed, then the data bytes will not be acknowledged by the PCx8594x-2 and the EEPROM contents are not changed.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCx8594x-2P	8	DIL	plastic	SOT97
PCx8594x-2T	8	SO8	plastic	SOT96A

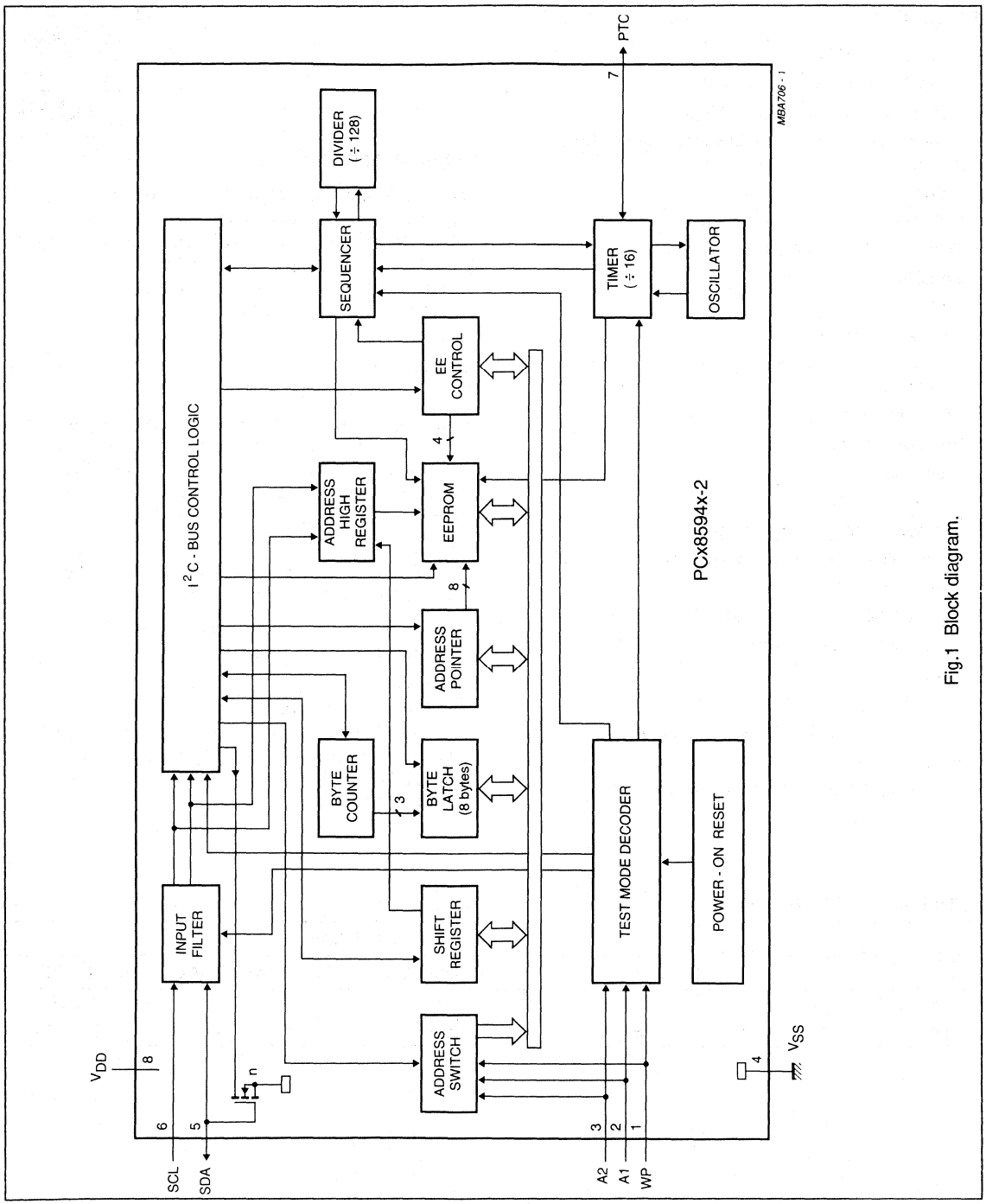


Fig.1 Block diagram.

1024 x 8-bit CMOS EEPROMS with I²C-bus interface

PCx8598x-2 Family

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

FEATURES

- Low Power CMOS
  - maximum active current 2.5 mA
  - maximum standby current 10 µA
- Non-volatile storage of 8-Kbits organized as four pages
  - each 256 x 8 bits
- Only one power supply required
- On-chip voltage multiplier
- Serial input/output bus (I²C)
- Write operations
  - byte write mode
  - 8-byte page write mode (minimizes total write time per byte)
- Write-protection input
- Read operations
  - sequential read
  - random read
- Extended supply voltage range (2.5 to 6.0 V)
- Internal timer for writing (no external components)
- Power-on reset
- High reliability by using a redundant storage code
  - (single bit error correction)
- Endurance
  - 100 k; T_{amb} = 85 °C
- 10 years non-volatile data retention time
- Pin and Address compatible to
  - PCF8570, PCF8571, PCF8572, PCF8581

GENERAL DESCRIPTION

The PCFx8598x-2 is a 8-Kbit (1024 x 8-bit) floating gate electrically erasable programmable read only memory (EEPROM). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to two PCx8598x-2 devices may be connected to the I²C-bus.

Chip select is accomplished by one address input.

Timing of the Erase/Write cycle is done internally, thus no external components are required. Pin 7 must be connected to either V_{DD} or left open-circuit.

There is an option of using an external clock for timing the length of an Erase/Write cycle.

A write protection input (pin 1) allows disable of write-commands from the master by a hardware signal. When pin 1 is HIGH and one of the upper 512 EEPROM cells is addressed, then the data bytes will not be acknowledged by the PCx8598x-2 and the EEPROM contents are not changed.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCx8598x-2P	8	DIL	plastic	SOT97
PCx8598x-2T	8	SO8L	plastic	SOT176C

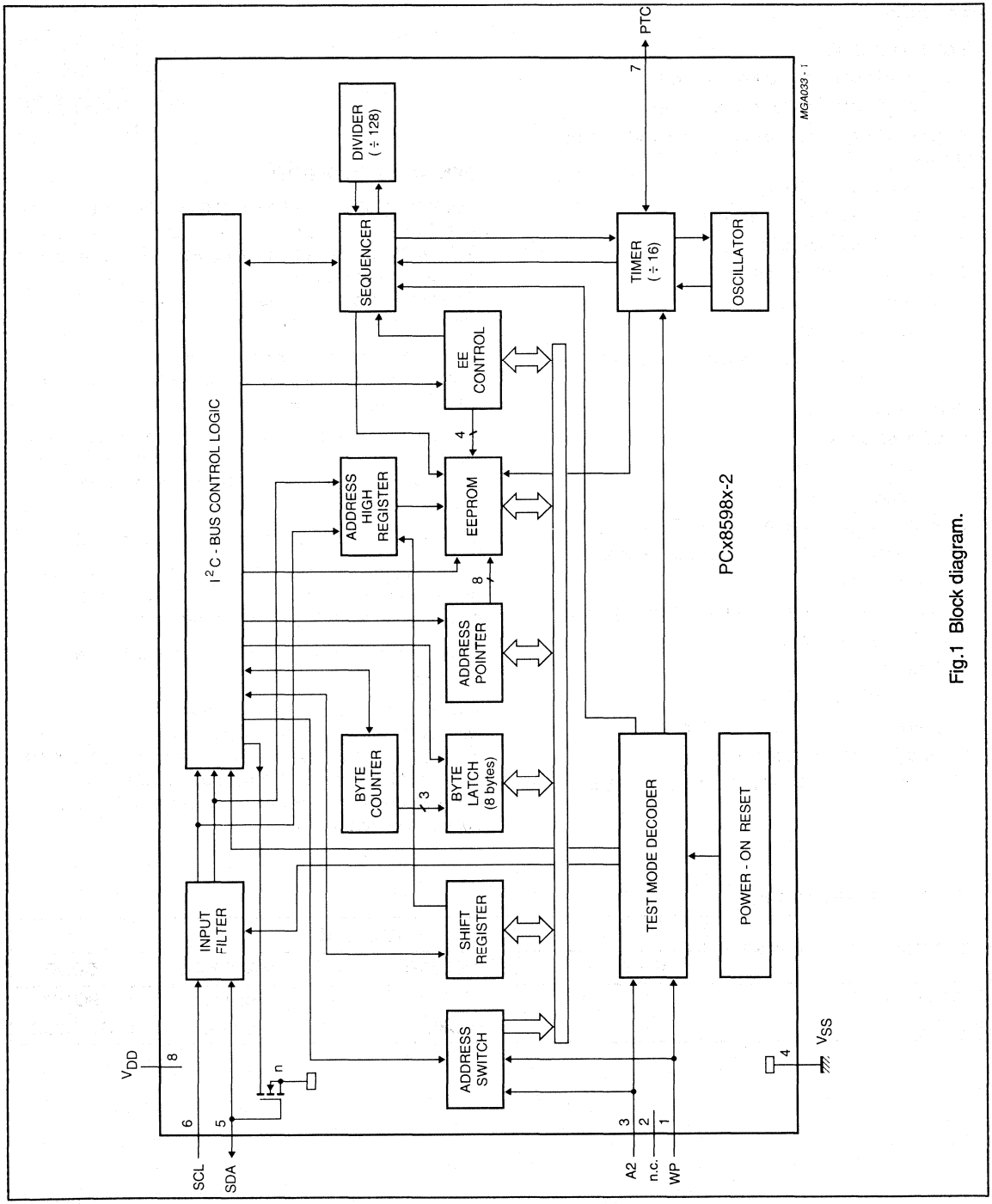


Fig.1 Block diagram.

N-channel silicon field-effect transistors

PMBFJ308/309/310

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

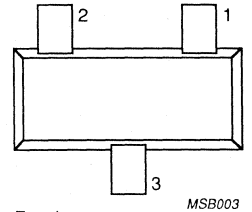
FEATURES

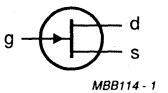
- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a SOT23 envelope. They are intended for use in VHF amplifiers, the AM input stage of car radios, oscillators and mixers.

PIN CONFIGURATION





Marking codes:
PMBFJ308: M08.
PMBFJ309: M09.
PMBFJ310: M10.

Top view

Fig.1 Simplified outline and symbol.

PINNING - SOT23

PIN	DESCRIPTION
1	source
2	drain
3	gate

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0			
	PMBFJ308		12	60	mA
	PMBFJ309		12	30	mA
	PMBFJ310		24	60	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 μA			
	PMBFJ308		1	6.5	V
	PMBFJ309		1	4	V
	PMBFJ310		2	6.5	V
$\|Y_{fs}\|$	common-source transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	mS

RADIO TUNING PLL FREQUENCY SYNTHESIZER

The SAA1057 is a single chip frequency synthesizer IC in I^2L technology, which performs all the tuning functions of a PLL radio tuning system. The IC is applicable to all types of radio receivers, e.g. car radios, hi-fi radios and portable radios.

Features

- On-chip prescaler with up to 120 MHz input frequency.
- On-chip AM and FM input amplifiers with high sensitivity (30 mV and 10 mV respectively).
- Low current drain (typically 16 mA for AM and 20 mA for FM) over a wide supply voltage range (3,6 V to 12 V).
- On-chip amplifier for loop filter for both AM and FM (up to 30 V tuning voltage).
- On-chip programmable current amplifier (charge pump) to adjust the loop gain.
- Only one reference frequency for both AM and FM.
- High signal purity due to a sample and hold phase detector for the in-lock condition.
- High tuning speed due to a powerful digital memory phase detector during the out-lock condition.
- Tuning steps for AM are: 1 kHz or 1,25 kHz for a VCO frequency range of 512 kHz to 32 MHz.
- Tuning steps for FM are: 10 kHz or 12,5 kHz for a VCO frequency range of 70 MHz to 120 MHz.
- Serial 3-line bus interface to a microcomputer.
- Test/features.

QUICK REFERENCE DATA

Supply voltage ranges	V_{CC1}	3,6 to 12	V
	V_{CC2}	3,6 to 12	V
	V_{CC3}	V_{CC2} to 31	V
Supply currents	$I_{CC1} + I_{CC2}$	typ. 18	mA
	I_{CC3}	typ. 0,8	mA
Input frequency ranges			
at pin FAM	f_{FAM}	512 kHz to 32	MHz
at pin FFM	f_{FFM}	70 to 120	MHz
Maximum crystal input frequency	f_{XTAL}	> 4	MHz
Operating ambient temperature range	T_{amb}	−25 to + 80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102H).

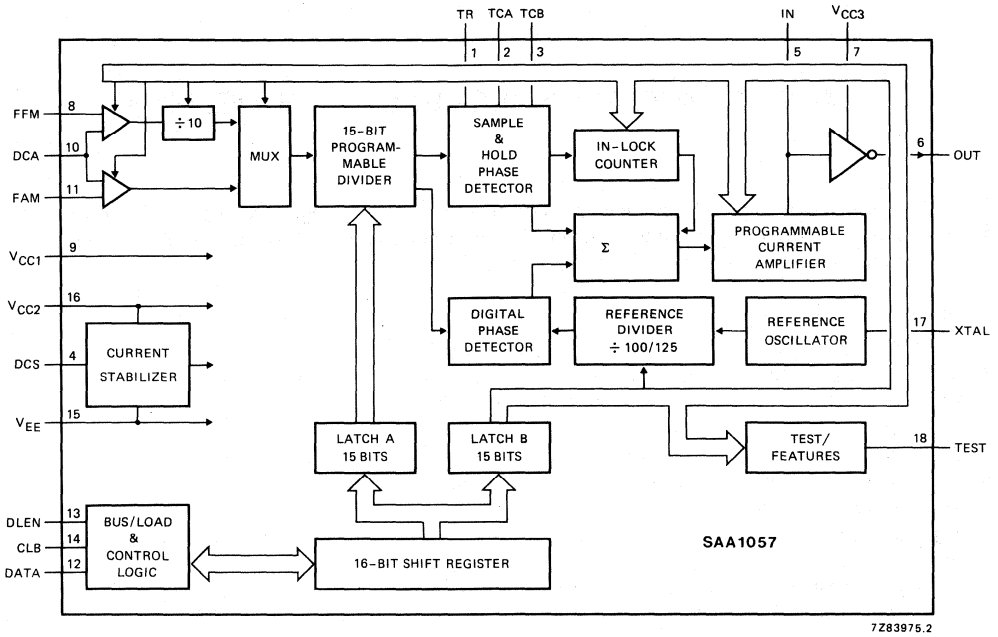


Fig. 1 Block diagram.

GENERAL DESCRIPTION

The SAA1057 performs the entire PLL synthesizer function (from frequency inputs to tuning voltage output) for all types of radios with the AM and FM frequency ranges.
The circuit comprises the following:

- Separate input amplifiers for the AM and FM VCO-signals.
- A divider-by-10 for the FM channel.
- A multiplexer which selects the AM or FM input.
- A 15-bit programmable divider for selecting the required frequency.
- A sample and hold phase detector for the in-lock condition, to achieve the high spectral purity of the VCO signal.
- A digital memory frequency/phase detector, which operates at a 32 times higher frequency than the sample and hold phase detector, so fast tuning can be achieved.
- An in-lock counter detects when the system is in-lock. The digital phase detector is switched-off automatically when an in-lock condition is detected.
- A reference frequency oscillator followed by a reference divider. The frequency is generated by a 4 MHz quartz crystal. The reference frequency can be chosen either 32 kHz or 40 kHz for the digital phase detector (that means 1 kHz and 1,25 kHz for the sample and hold phase detector), which results in tuning steps of 1 kHz and 1,25 kHz for AM, and 10 kHz and 12,5 kHz for FM.
- A programmable current amplifier (charge pump), which controls the output current of both the digital and the sample/hold phase detector in a range of 40 dB. It also allows the loop gain of the tuning system to be adjusted by the microcomputer.
- A tuning voltage amplifier, which can deliver a tuning voltage of up to 30 V.
- BUS; this circuitry consists of a format control part, a 16-bit shift register and two 15-bit latches. Latch A contains the to be tuned frequency information in a binary code. This binary-coded number, multiplied by the tuning spacing, is equal to the synthesized frequency. The programmable divider (without the fixed divide-by-10 prescaler for FM) can be programmed in a range between 512 and 32 767 (see Fig. 3). Latch B contains the control information.

OPERATION DESCRIPTION

Control information

The following functions can be controlled with the data word bits in latch B. For data word format and bit position see Fig. 3.

FM — FM/AM selection; '1' = FM, '0' = AM

REFH — reference frequency selection; '1' = 1,25 kHz, '0' = 1 kHz (sample and hold phase detector)

CP3, CP2, CP1, CP0 — control bits for the programmable current amplifier (see section Characteristics)

SB2 — enables last 8 bits (SLA to T0) of data word B; '1' = enables, '0' = disables; when programmed '0', the last 8 bits of data word B will be set to '0' automatically

SLA — load mode of latch A; '1' = synchronous, '0' = asynchronous

PDM1, PDM0 — phase detector mode

PDM1	PDM0	digital phase detector
0	X	automatic on/off
1	0	on
1	1	off

BRM — bus receiver mode bit; in this mode the supply current of the BUS receiver will be switched-off automatically after a data transmission (current-draw is reduced); '1' = current switched; '0' = current always on

T3 — test bit; must be programmed always '0'

T2 — test bit; selects the reference frequency (32 or 40 kHz) to the TEST pin

T1 — test bit; must be programmed always '0'

T0 — test bit; selects the output of the programmable counter to the TEST pin

T3	T2	T1	T0	TEST (pin 18)
0	0	0	0	1
0	1	0	0	reference frequency
0	0	0	1	output programmable counter
0	1	0	1	output in-lock counter '0' = out-lock '1' = in-lock

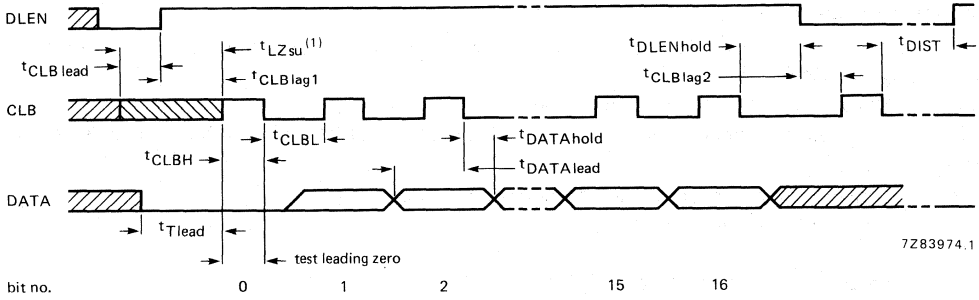


Fig. 2 BUS format.

(1) During the zero set-up time (t_{LZsu}) CLB can be LOW or HIGH, but no transient of the signal is permitted. This can be of use when an I^2C bus is used for other devices on the same data and clock lines.

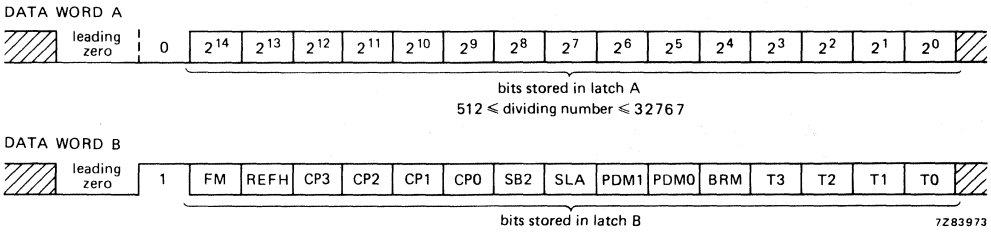


Fig. 3 Bit organization of data words A and B.

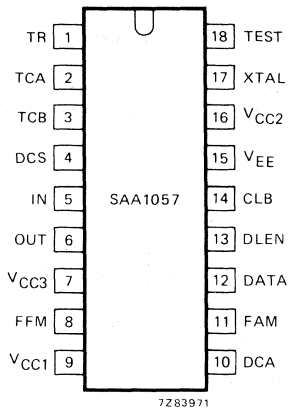


Fig. 4 Pinning diagram.

PINNING

1	TR	} resistor/capacitors for sample and hold circuit
2	TCA	
3	TCB	
4	DCS	decoupling of supply
5	IN	input of output amplifier
6	OUT	output of output amplifier
7	V_{CC3}	positive supply voltage of output amplifier
8	FFM	FM signal input
9	V_{CC1}	positive supply voltage of high frequency logic part
10	DCA	decoupling of input amplifiers
11	FAM	AM signal input
12	DATA	} BUS
13	DLEN	
14	CLB	
15	V_{EE}	ground
16	V_{CC2}	positive supply voltage of low frequency logic part and analogue part
17	XTAL	reference oscillator input
18	TEST	test output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; logic and analogue part	V_{CC1}; V_{CC2}	−0,3 to 13,2 V
Supply voltage; output amplifier	V_{CC3}	V_{CC2} to + 32 V
Total power dissipation	P_{tot}	max. 800 mW
Operating ambient temperature range	T_{amb}	−30 to + 85 °C
Storage temperature range	T_{stg}	−65 to + 150 °C

CHARACTERISTICS

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Supply voltages	V_{CC1}	3,6	5	12	V	
	V_{CC2}	3,6	5	12	V	
	V_{CC3}	V_{CC2}	–	31	V	
Supply currents*						
AM mode	I_{tot}	–	16	–	mA	$I_{tot} = I_{CC1} + I_{CC2}$ in-lock: BRM = '1'; PDM = '0'
FM mode	I_{tot}	–	20	–	mA	
	I_{CC3}	0,3	0,8	1,2	mA	I_{OUT} = 0
Operating ambient temperature	T_{amb}	−25	–	+80	°C	
RF inputs (FAM, FFM)						
AM input frequency	f_{FAM}	512 kHz	–	32	MHz	
FM input frequency	f_{FFM}	70	–	120	MHz	
Input voltage at FAM	$V_{i\ (rms)}$	30	–	500	mV	
Input voltage at FFM	$V_{i\ (rms)}$	10	–	500	mV	
Input resistance at FAM	R_i	–	2	–	kΩ	
Input resistance at FFM	R_i	–	135	–	Ω	
Input capacitance at FAM	C_i	–	3,5	–	pF	
Input capacitance at FFM	C_i	–	3	–	pF	
Voltage ratio allowed between selected and non-selected input	V_s/V_{ns}	–	−30	–	dB	
Crystal oscillator (XTAL)						see note 1
Maximum input frequency	f_{XTAL}	4	–	–	MHz	
Crystal series resistance	R_s	–	–	150	Ω	
BUS inputs (DLEN, CLB, DATA)						
Input voltage LOW	V_{IL}	0	–	0,8	V	
Input voltage HIGH	V_{IH}	2,4	–	V_{CC1}	V	
Input current LOW	$-I_{IL}$	–	–	10	μA	V_{IL} = 0,8 V
Input current HIGH	I_{IH}	–	–	10	μA	V_{IH} = 2,4 V

* When the bus is in the active mode (see BRM in Control Information), 4,5 mA should be added to the figures given.

CHARACTERISTICS (continued)

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
BUS inputs timing (DLEN, CLB, DATA)						see also Fig. 2 and note 2
Lead time for CLB to DLEN	$t_{CLBlead}$	1	–	–	µs	
Lead time for DATA to the first CLB pulse	t_{Tlead}	0,5	–	–	µs	
Set-up time for DLEN to CLB	$t_{CLBlag1}$	5	–	–	µs	
CLB pulse width HIGH	t_{CLBH}	5	–	–	µs	
CLB pulse width LOW	t_{CLBL}	5	–	–	µs	
Set-up time for DATA to CLB	$t_{DATAlead}$	2	–	–	µs	
Hold time for DATA to CLB	$t_{DATAhold}$	0	–	–	µs	
Hold time for DLEN to CLB	$t_{DLENhold}$	2	–	–	µs	
Set-up time for DLEN to CLB load pulse	$t_{CLBlag2}$	2	–	–	µs	
Busy time from load pulse to next start of transmission	t_{DIST}	5	–	–	µs	next transmission after word 'B' to other device or next transmission to SAA1057 after word 'A' (see also note 5)
Busy time asynchronous mode	t_{DIST}	0,3	–	–	ms	
synchronous mode	t_{DIST}	1,3	–	–	ms	
Sample and hold circuit (TR, TCA, TCB)						see also notes 3; 4
Minimum output voltage	V_{TCA}, V_{TCB}	–	1,3	–	V	
Maximum output voltage	V_{TCA}, V_{TCB}	–	–	V_{CC2}–0,7	V	
Capacitance at TCA (external)	C_{TCA}	–	–	2,2	nF	REFH = '1'
	C_{TCA}	–	–	2,7	nF	REFH = '0'
Discharge time at TCA	t_{dis}	–	–	5	µs	REFH = '1'
	t_{dis}	–	–	6,25	µs	REFH = '0'
Resistance at TR	R_{TR}	100	–	–	Ω	external
Voltage at TR during discharge	V_{TR}	–	0,7	–	V	
Capacitance at TCB	C_{TCB}	–	–	10	nF	external
Bias current into TCA, TCB	I_{bias}	–	–	10	nA	in-lock

CHARACTERISTICS (continued)

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Programmable current amplifier (PCA)						
Output current of the dig. phase detector	$\pm I_{dig}$	–	0,4	–	mA	
Current gain of PCA						
CP3 CP2 CP1 CP0						
P1 0 0 0 0	G_{P1}	–	0,023	–		$V_{CC2} \geqslant 5$ V (only for P1)
P2 0 0 0 1	G_{P2}	–	0,07	–		
P3 0 0 1 0	G_{P3}	–	0,23	–		
P4 0 1 1 0	G_{P4}	–	0,7	–		
P5 1 1 1 0	G_{P5}	–	2,3	–		
Ratio between the output current of S/H into PCA and the voltage on C_{TCB}	S_{TCB}	–	1,0	–	μA/V	
Offset voltage on TCB	ΔV_{TCB}	–	–	1	V	in-lock
Output amplifier (IN,OUT)						
Input voltage	V_{IN}	–	1,3	–	V	in-lock; equal to internal reference voltage
Output voltages						
minimum	V_{OUT}	–	–	0,5	V	$-I_{OUT}$ = 1 mA
maximum	V_{OUT}	$V_{CC3}-2$	–	–	V	I_{OUT} = 1 mA
maximum	V_{OUT}	$V_{CC3}-1$	–	–	V	I_{OUT} = 0,1 mA
Maximum output current	$\pm I_{OUT}$	5	–	–	mA	V_{OUT} = ½ V_{CC3}
Test output (TEST)*						
Output voltage LOW	V_{TL}	–	–	0,5	V	
Output voltage HIGH	V_{TH}	–	–	12	V	
Output current OFF	I_{Toff}	–	–	10	μA	V_{TH}
Output current ON	I_{Ton}	150	–	–	μA	V_{TL}
Ripple rejection**						
at f_{ripple} = 100 Hz						
$\Delta V_{CC1}/\Delta V_{OUT}$		–	77	–	dB	
$\Delta V_{CC2}/\Delta V_{OUT}$		–	70	–	dB	
$\Delta V_{CC3}/\Delta V_{OUT}$		–	60	–	dB	$V_{OUT} \leqslant V_{CC3}-3$ V

* Open collector output.

** Measured in Fig. 6.

NOTES

1. Pin 17 (XTAL) can also be used as input for an external clock.
   The circuit for that is given in Fig. 5. The values given in Fig. 5 are a typical application example.

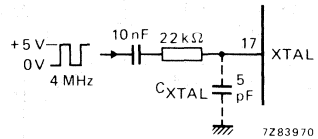


Fig. 5 Circuit configuration showing external 4 MHz clock.

2. See BUS information in section 'operation description'.
3. The output voltage at TCB and TCA is typically ½ V_{CC2}+0,3 V when the tuning system is in-lock via the sample and hold phase detector. The control voltage at TCB is defined as the difference between the actual voltage at TCB and the value calculated from the formula ½ V_{CC2}+0,3 V.
4. Crystal oscillator frequency f_{XTAL} = 4 MHz.
5. The busy-time after word "A" to another device which has more clock pulses than the SAA1057 (> 17) must be the same as the busy-time for a next transmission to the SAA1057.
   When the other device has a separate DLEN or has less clock pulses than the SAA1057 it is not necessary to keep to this busy-time, 5 μs will be sufficient.

APPLICATION INFORMATION

Initialize procedure

Either a train of at least 10 clock pulses should be applied to the clock input (CLB) or word B should be transmitted, to achieve proper initialization of the device.
For the complete initialization (defining all control bits) a transmission of word B should follow. This means that the IC is ready to accept word A.

Synchronous/asynchronous operation

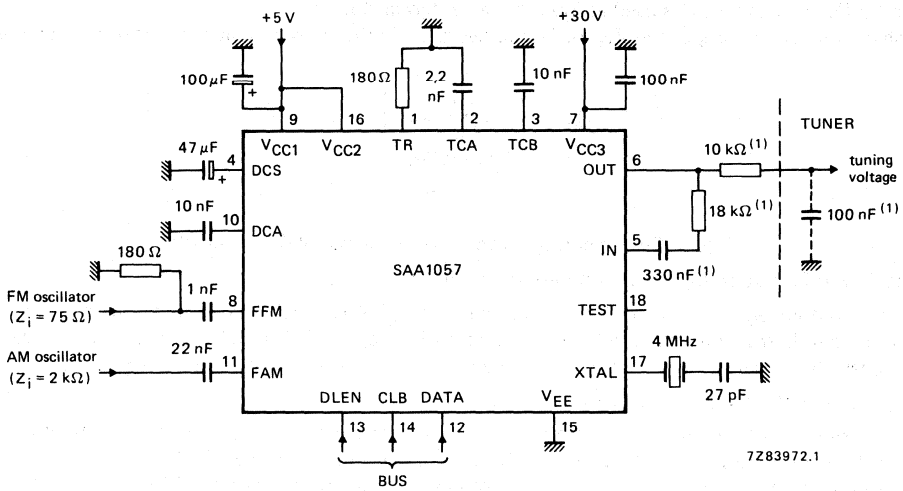
Synchronous loading of the frequency word into the programmable counter can be achieved when bit 'SLA' of word B is set to '1'. This mode should be used for small frequency steps where low tuning noise is important (e.g. search and manual tuning). This mode should not be used for frequency changes of more than 31 tuning steps. In this case asynchronous loading is necessary. This is achieved by setting bit 'SLA' to '0'. The in-lock condition will then be reached more quickly, because the frequency information is loaded immediately into the divider.

Restrictions to the use of the programmable current amplifier

The lowest current gain (0,023) must not be used in the in-lock condition when the supply voltage V_{CC2} is below 5 V (CP3, CP2, CP1 and CP0 are all set to '0'). This is to avoid possible instability of the loop due to a too small range of the sample and hold phase detector in this condition (see also section 'Characteristics').

Transient times of the bus signals

When the SAA1057 is operating in a system with continuous activity on the bus lines, the transient times at the bus inputs should not be less than 100 ns. Otherwise the signal-to-noise ratio of the tuning voltage is reduced.



(1) Values depend on the tuner diode characteristics.

Fig. 6 Application example of the SAA1057PLL frequency synthesizer module.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

4-DIGIT LED-DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The LED-driver is a bipolar integrated circuit made in an I^2L compatible 18 volts process. The circuit is especially designed to drive four 7-segment LED displays with decimal point by means of multiplexing between two pairs of digits. It features an I^2C-Bus slave transceiver interface with the possibility to program four different SLAVE ADDRESSES, a POWER RESET flag, 16 current sink OUTPUTS, controllable by software up to 21 mA, two multiplex drive outputs for common anode segments, an on-chip multiplex oscillator, control bits to select static, dynamic and blank mode, and one bit for segment test.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	$V_{EE} = 0$ V	V_{CC}	4.5	5	15	V
Supply current all outputs OFF	$V_{CC} = 5$ V	I_{CC}*	7	9.5	14	mA
Total power dissipation 24-lead DIL (SOT101B)		P_{tot}	–	–	1000	mW
24-lead DIL SO (SOT137A)		P_{tot}	–	–	500	mW
Operating ambient temperature range		T_{amb}	–40	–	+85	°C

* The positive current is defined as the conventional current flow into a device (sink current).

PACKAGE OUTLINE

SAA1064: 24-lead DIL; plastic with internal heat spreader (SOT101B).
SAA1064T: 24-lead mini-pack; plastic (SO-24; SOT137A).

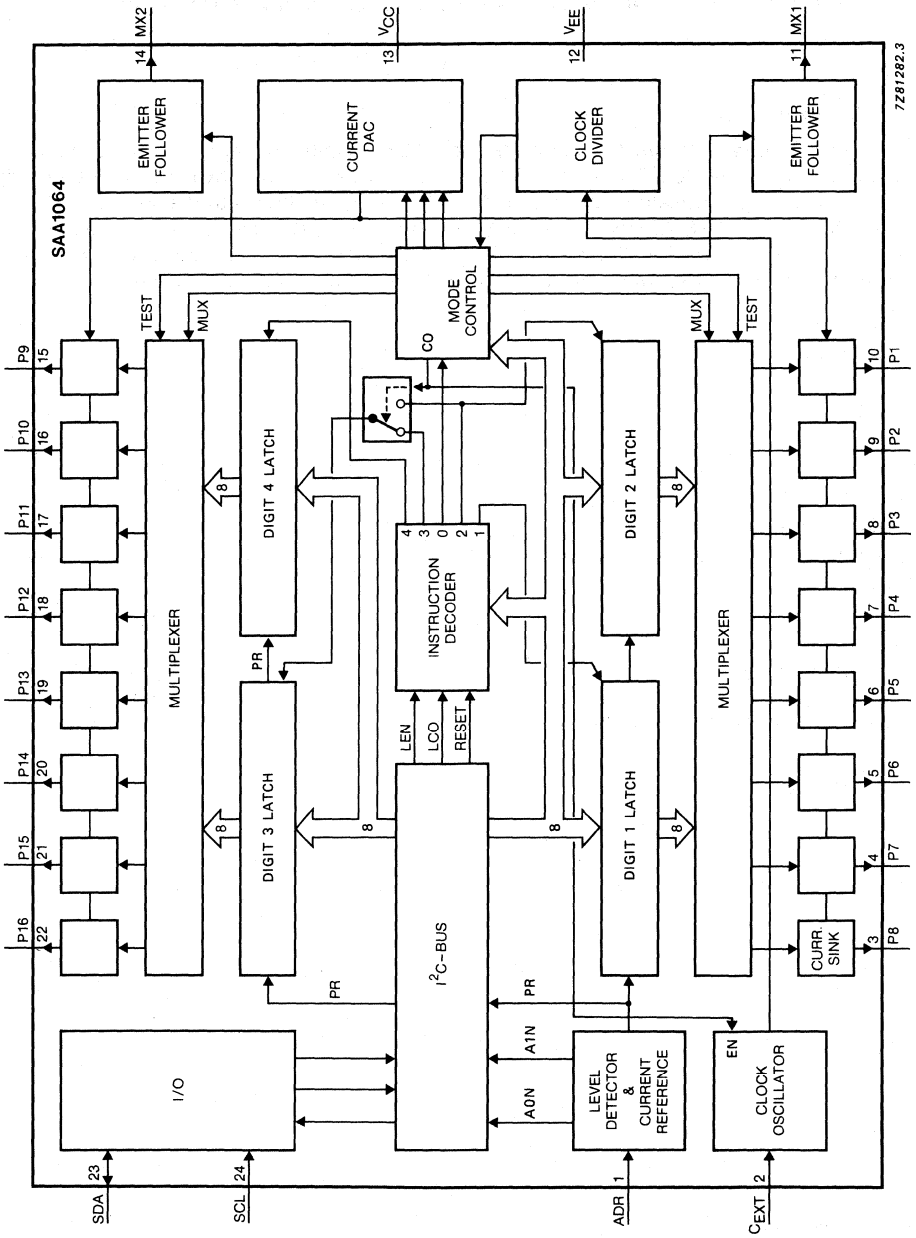


Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

TUNER SWITCHING CIRCUIT

The SAA1300 is for switching on and off the supply lines of various circuit parts via an I²C bus signal. Furthermore, it can be used to supply current for switching diodes in radio and television tuners. It contains 5 output stages, which are capable of supplying up to 85 mA in the ON state or sinking up to −100 μA in the OFF state.

Current limiting and short-circuit protection are included. The output stages are driven by a shift register/latch combination which is loaded via data from the I²C bus. A power-on reset of the latches ensures the OFF state of the output stages (OUT 2 to OUT 5) without data reception from the I²C bus. A subaddressing system allows the connection of up to three circuits on the same I²C bus lines; one of the outputs (OUT 1, pin 7) can also be used as an input to select the device via a simple internal A/D converter.

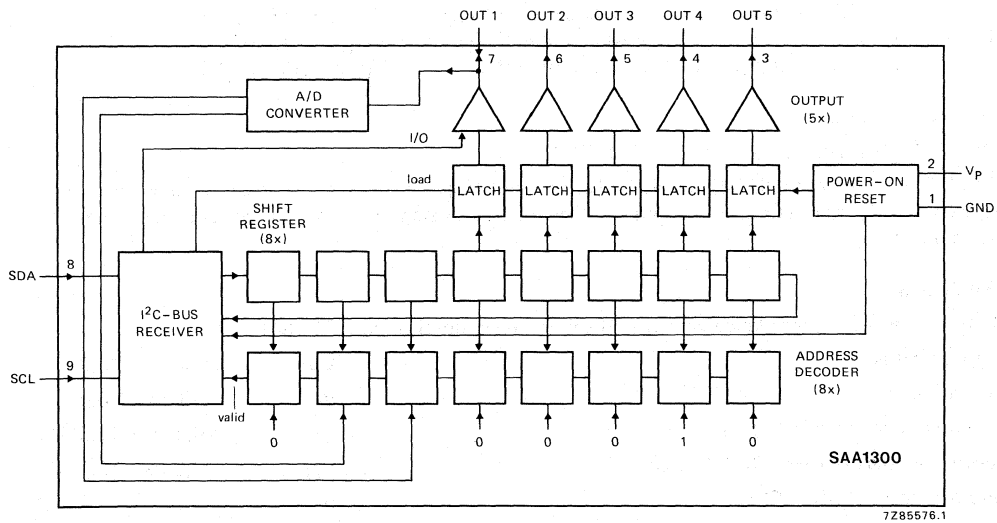


Fig. 1 Block diagram.

PACKAGE OUTLINE

9-lead SIL; plastic (SOT142).

PINNING

pin no.	symbol	function
1	GND	ground
2	V_P	positive supply
3	OUT 5	outputs
4	OUT 4	
5	OUT 3	
6	OUT 2	
7	OUT 1	output and subaddressing input
8	SDA	serial data line (I^2C bus)
9	SCL	serial clock line (I^2C bus)

I^2C BUS INFORMATION

Address, first byte

0 1 0 0 0 A B 0 where,

A	B	function	condition
0	0	general address	OUT 1 = output
0	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,L}$ (LOW)
1	0	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,H}$ (HIGH)
1	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,M}$ (MEDIUM)

Data, second byte

OUT 5, OUT 4, OUT 3, OUT 2, OUT 1, X, X, X

The I/O output stage (OUT 1) is switched as an input stage after a power-on reset. It depends on the contents of the first data transmission whether the output stage is switched as an output or remains as an input.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	13,2	V
Input voltage range at SDA, SCL	V_I		−0,5 to + 6,0	V
Input voltage range at OUT 1	V_I		−0,5 to + 12,5	V
Output voltage range at OUT 1 to OUT 5	V_O		−0,5 to + 12,5	V
Input current at SDA, SCL	I_I	max.	20	mA
Input current at OUT 1	I_I	max.	20	mA
Total power dissipation	P_{tot}	max.	825	mW
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		−20 to + 80	°C

Stereo filter and codec SAA2002

FEATURES

- Stereo filtering and codec functions in a single chip
- Drive processing interface
- Filtered data interface
- Baseband audio data interface
- LT interface to microcontroller
- Clock generator
- Low operating voltage capability.

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

The SAA2002 performs the sub-band filtering and audio frame codec functions in a Precision Adaptive Sub-band Coding (PASC) system. It is capable of functioning as a stand-alone decoder, but requires the addition of an Adaptive Allocation and Scale factor processor (SAA2012) in order to perform PASC encoding in a DCC record system.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2002GP	44	QFP [1]	plastic	SOT205AG

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the Quality Reference Pocketbook are followed. The pocketbook can be ordered using the code 9398 510 34011.

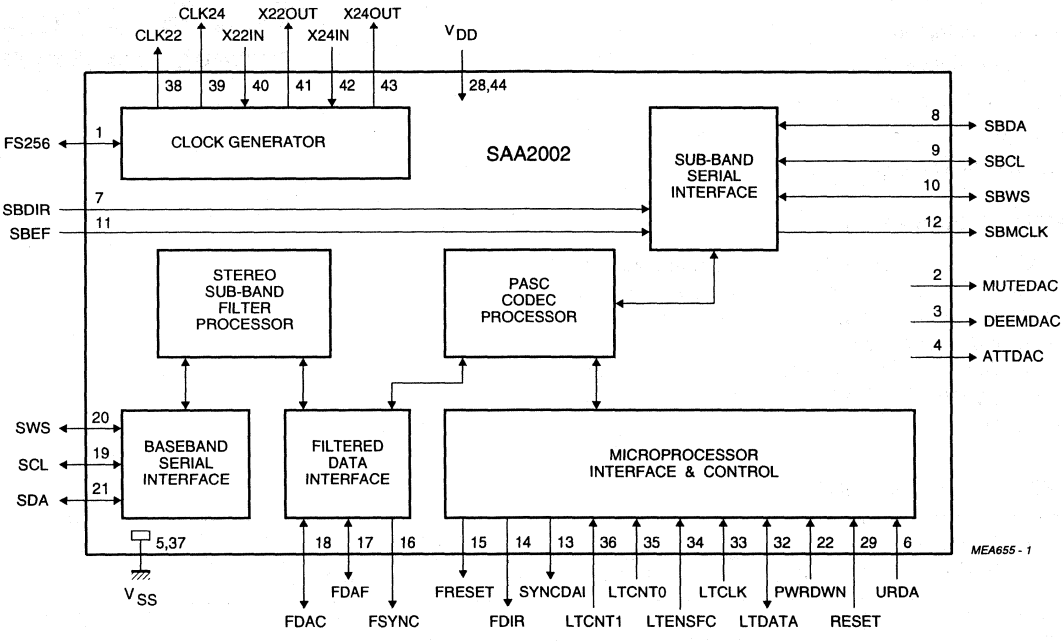


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FS256	1	filtered-I²S clock; 256 x f_s; 12 mA, 3-state output + CMOS input with pull-down
MUTEDAC	2	DAC control/output expander
DEEMDAC	3	DAC control/output expander
ATTDAC	4	DAC control/output expander
V_{SS}	5	supply ground (0 V)
URDA	6	unreliable drive processing data; CMOS level
SBDIR	7	sub-band I²S direction: (SWBS, SBCL, SBDA); CMOS level
SBDA	8	sub-band I²S data; 4 mA, 3-state output + CMOS input with pull-down
SBCL	9	sub-band I²S bit-clock; 4 mA, 3-state output + CMOS input with pull-down
SBWS	10	sub-band I²S word select; 4 mA, 3-state output + CMOS input with pull-down
SBEF	11	sub-band I²S byte error flag input; CMOS level
SBMCLK	12	sub-band I²S clock; 6.144 MHz locked to FS256; 8 mA, 3-state output + CMOS input with pull-down
SYNCDAI	13	Digital Audio Interface (DAI) synchronization pulse
FDIR	14	filtered-I²S direction: (FDAC, FDAF and SDA)
FRESET	15	reset signal for SAA2012
FSYNC	16	filtered-I²S synchronization signal for SAA2012
FDAF	17	filtered-I²S sub-band filter data; 4 mA, 3-state output + CMOS input with pull-down
FDAC	18	filtered-I²S sub-band codec data; 4 mA, 3-state output + CMOS input with pull-down
SCL	19	I²S bit-clock; 4 mA, 3-state output + CMOS input with pull-down
SWS	20	I²S word select; 4 mA, 3-state output + CMOS input with pull-down
SDA	21	I²S baseband data filter; 4 mA, 3-state output + CMOS input with pull-down
PWRDWN	22	sleep mode; CMOS level
DSC4	23	test pin; not to be connected
DSC3	24	test pin; not to be connected
DSC2	25	test pin; not to be connected
DSC1	26	test pin; not to be connected
DSC0	27	test pin; not to be connected
V_{DD}	28	supply voltage (+5 V)
RESET	29	system reset input; CMOS level with pull-down and hysteresis
T1	30	test pin; not to be connected
T0	31	test pin; not to be connected
LTDATA	32	LT interface data; 4 mA, 3-state output + CMOS input with pull-down
LTCLK	33	LT interface bit clock input; CMOS level
LTENSFC	34	LT interface enable input; CMOS level
LTCNT0	35	LT interface control input; CMOS level
LTCNT1	36	LT interface control input; CMOS level
V_{SS}	37	supply ground (0 V)
CLK22	38	22.5792 MHz buffered output
CLK24	39	24.576 MHz buffered output

SYMBOL	PIN	DESCRIPTION
X22IN	40	22.5792 MHz crystal input
X22OUT	41	22.5792 MHz crystal output
X24IN	42	24.576 MHz crystal input
X24OUT	43	24.576 MHz crystal output
V_{DD}	44	supply voltage (+5 V)

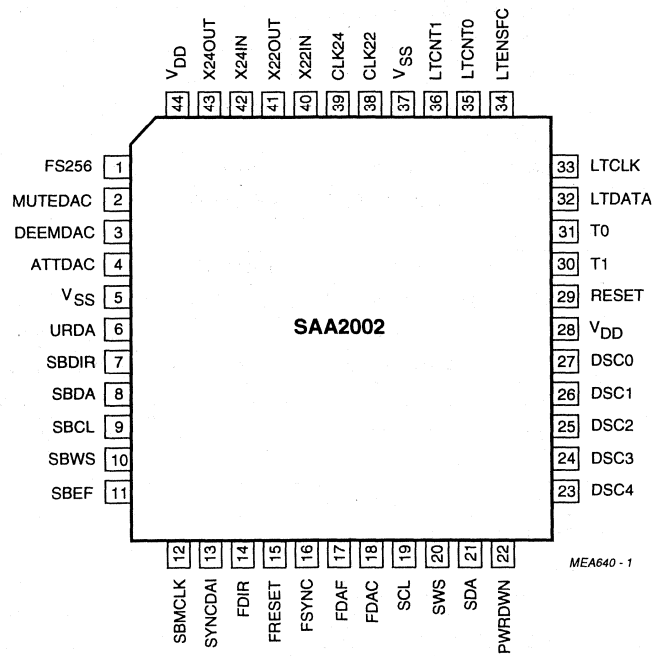


Fig.2 Pin configuration.

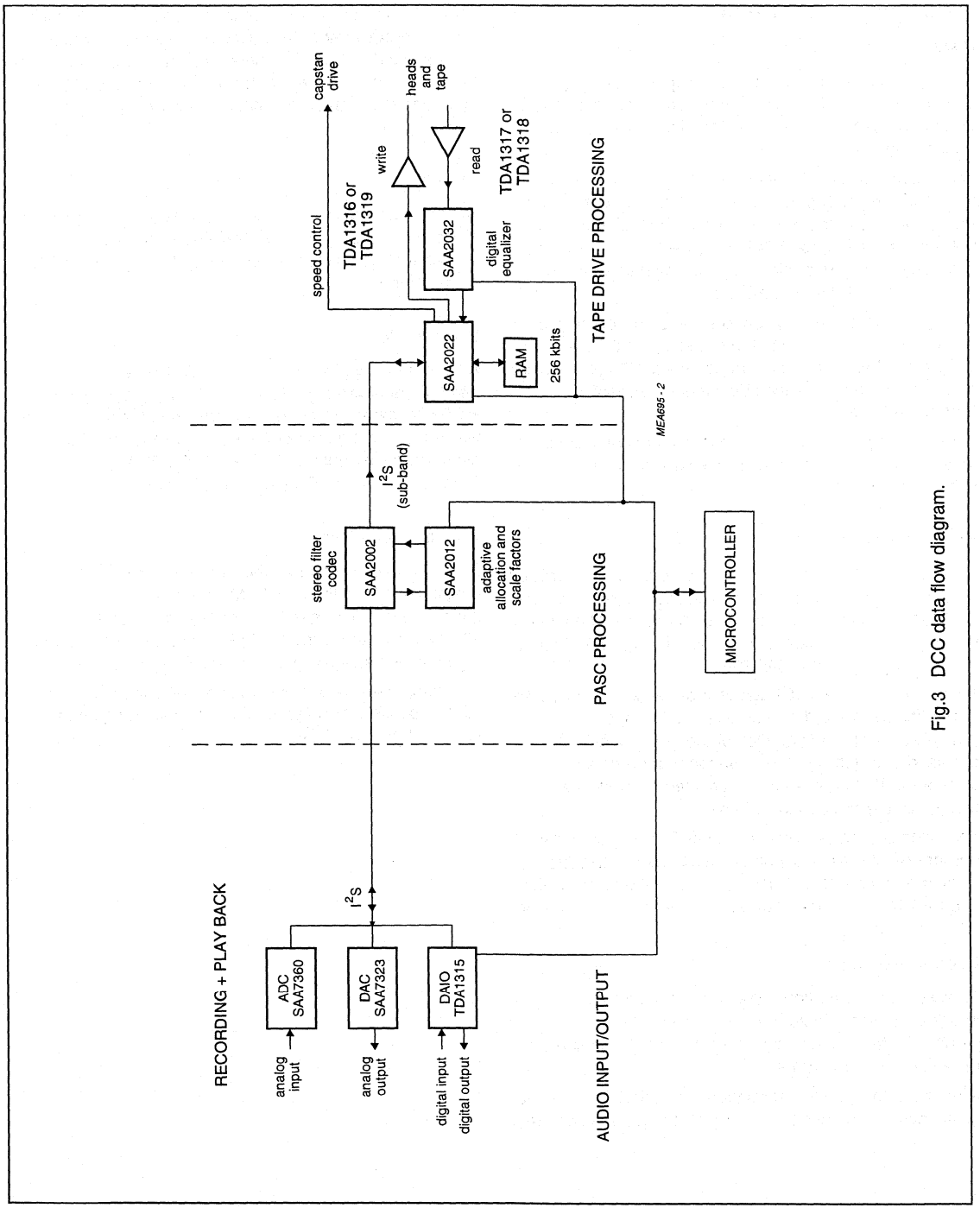


Fig.3 DCC data flow diagram.

FUNCTIONAL DESCRIPTION

PASC

Precision Adaptive Sub-band Coding achieves highly efficient digital encoding of audio signals by using an algorithm based on the characteristics of the human auditory system.

The broad-band audio signal is split into 32 sub-band signals during encoding. For each of the sub-band signals the masking threshold is calculated. The samples of the sub-bands are incorporated in the PASC signal with an accuracy that is determined by the signal to masking threshold ratio for that sub-band.

During decoding, the sub-band signals are reconstructed and combined into a broadband audio signal. The integrated filter processor performs the splitting (encoding) and joining (decoding) including the corresponding formatting functions.

For encoding, a SAA2012 is necessary to calculate the masking threshold and required accuracy of the sub-band samples.

Encoding (see Fig.4)

An encoding algorithm table is used during the recording process but, due to the Adaptive Allocation functions of the SAA2012, this may change with every frame. The table is therefore calculated for each frame by the SAA2012 and then transferred to the SAA2002.

A frame contains 2 x 384 samples of Left and Right audio data. This results in 12 samples per sub-band (32 sub-bands). The samples of the greatest amplitude are used to determine the scale factor for a given sub-band. All samples are then scaled to represent a fraction of the greatest amplitude.

Once scaled, the samples are quantified to reduce the number of bits to correspond with the allocation table as calculated by the SAA2012. Synchronization and coding information data is then added to result in a fully encoded PASC signal.

Decoding (see Fig.5)

All essential information (synchronization, system information, scale factors and encoded sub-band samples) are conveyed by incoming data. Decoding is repeated for every frame.

After sync and coding information, allocation data and the scale factors are used to correctly fill the scale factor array. This is followed by a process of multiplication to provide de-quantification and de-scaling of the PASC samples. The decoded sub-band samples, which are represented in 24-bit two's complement notation, are processed by the sub-band filters and reconstituted into a single digital audio signal.

RESET

Reset must be active from system power-up, or the end of sleep mode (falling edge of PWRDWN), for a period equivalent to 24 cycles of CLK24 plus the crystal oscillator start-up time.

Sleep mode

A HIGH input applied to the PWRDWN pin will halt all internally generated clock signals. As a result, chip activity will halt completely with outputs frozen in the state which was current at the time of PWRDWN activation. The bi-directional outputs: LTDATA, FDAC, FDAF, SDA, SBWS, SBCL and SBDA will be in 3-state.

Crystal Oscillators

A 24.576 MHz crystal together with some external components form the 24.576 MHz oscillator (pins 42 and 43). Similarly a 22.5792 MHz oscillator (pins 40 and 41) is performed by similar peripheral components together with an appropriate crystal (see Fig.6).

The component values shown apply only to crystals from the Philips 4322 156 series which exhibit an equivalent series resistance of $\leq 40\ \Omega$.

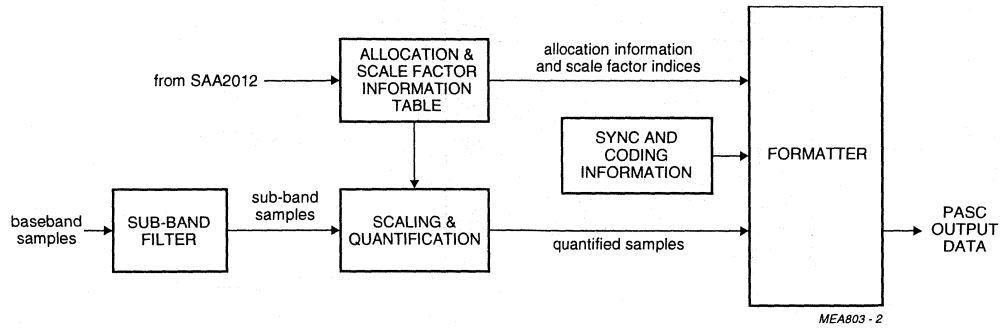


Fig.4 Encoding mode.

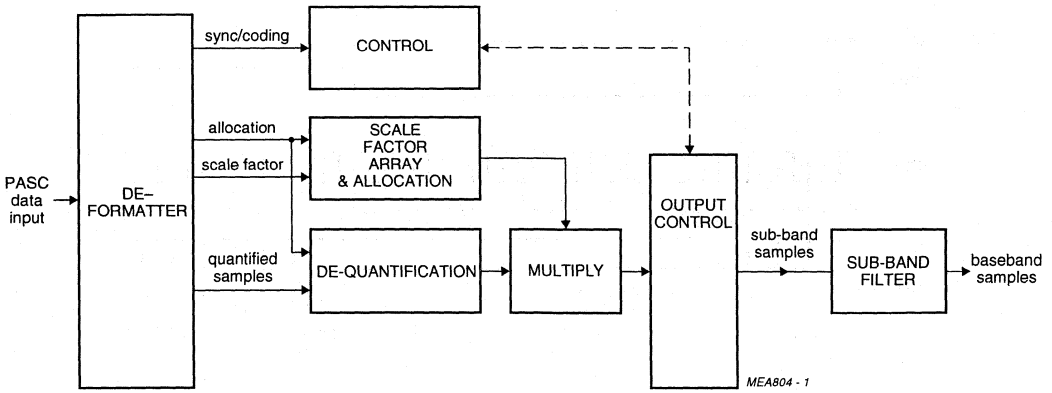
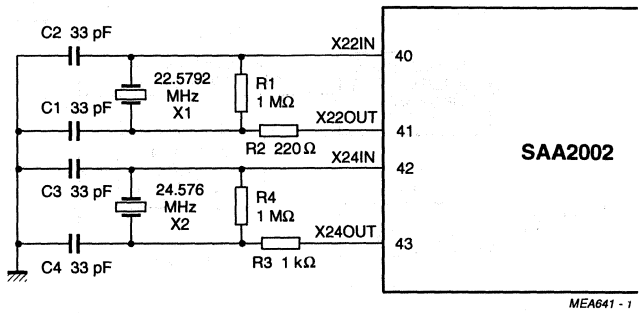


Fig.5 Decoding mode.



Component values apply only to crystals from the Philips 4322 156 series.

Fig.6 Crystal oscillator components.

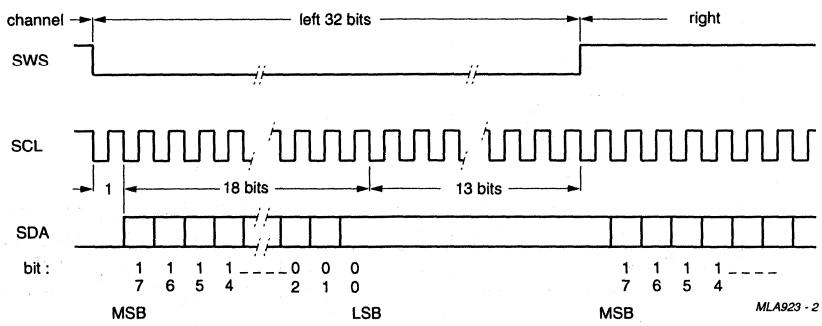


Fig.7 Transfer of SDA data (standard I²S default format).

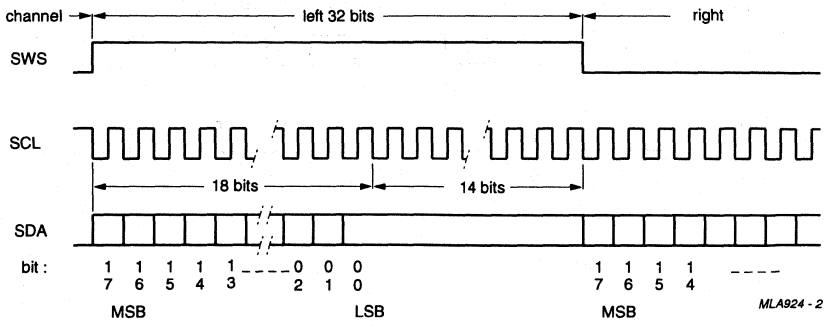


Fig.8 Transfer of SDA data (alternative format).

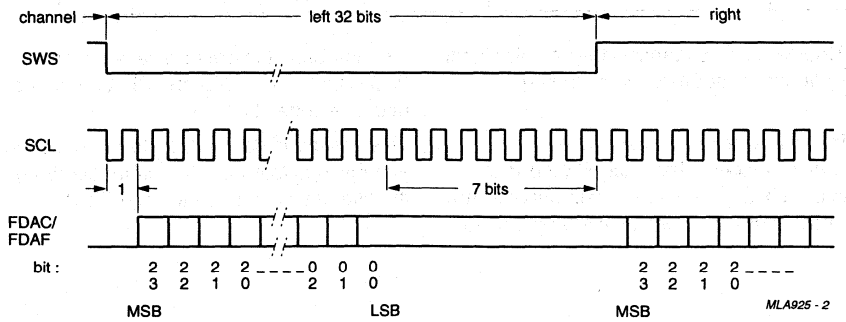


Fig.9 Transfer of FDAF and FDAC (filtered) data.

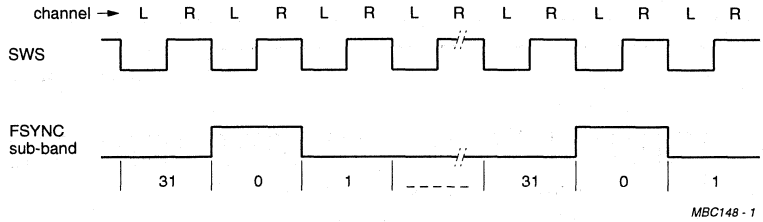


Fig.10 SWS related to phase of FSYNC.

Baseband Interface Signals

Table 1 Interface between the SAA2002 and the baseband input/output circuitry.

SIGNAL	MODE	DESCRIPTION	OPERATING FREQUENCY
SWS	bi-directional	word (channel) select	f_s
SCL	bi-directional	bit clock	$64f_s$
SDA	bi-directional	baseband data	–
FDIR	output	decoding mode (direction control)	–

The SWS signal indicates the channel of the sample signal (either Left or Right) and is equal to the sampling frequency f_s.

Operating at a frequency of 64 x f_s that is used for sampling, the bit clock dictates that each SWS period contains 64 SDA data bits. Of these, a maximum of 36 are used to transfer data (samples may have a length up to 18-bits). Samples are transferred most significant bit (MSB) first. Both SWS and SDA change state at the negative edge of SCL.

This baseband data is transferred between the SAA2002 and the input/output using either standard I^2S (default) or the alternative format shown in Fig.8.

Interface between SAA2002 and SAA2012

Table 2 Filtered I²S interface.

SIGNAL	MODE	DESCRIPTION	OPERATING FREQUENCY
SWS	bi-directional	word select (common to I²S)	f_s
SCL	bi-directional	bit clock (common to I²S)	$64f_s$
FDAC	bi-directional	codec data	–
FDAF	bi-directional	filter data	–
FSYNC	output	synchronization	$f_s/32$

Filtered data is transferred between SAA2002 filter/codec functions and the SAA2012 using the format shown in Fig.9.

The frequency of the SWS signal is equal to the sample frequency f_s and the bit clock SCL is 64 times the sample frequency. Each period of SWS contains 64 data-bits, 48 of which are used to transfer data. The half period in which SWS is LOW is used to transfer the information of the Left channel while the following half period during which SWS is HIGH carries the data of the Right channel. The 24-bit samples are transferred Most Significant Bit (MSB) first. This bit is transferred in the bit clock period with a 1-bit delay following the change in SWS. Both SWS and FDAF/FDAC change state at the negative edge of SCL.

The SAA2012 may be synchronized to the sub-band codec using the FSYNC signal, which defines the SWS period in which the samples of sub-band 0 (containing the lowest frequency components) are transferred (see Fig.9).

SAA2012 AND INPUT/OUTPUT MODE CONTROL

The operation of SAA2012 and the input/output circuitry is controlled by three signals shown in Table 4.

FRESET and SYNCDAI are given whenever:

- FS256, SCL and SWS outputs switch between high and low impedance
- FS256 frequency is changed (12.288/11.2896/8.192 MHz)
- FDIR is switching
- The bit rate is changing
- System reset is active.

PASC CODED INTERFACE

The interface that carries the PASC coded signal uses the signals as indicated in Table 3.

Table 3 The PASC I²S interface.

SIGNAL	MODE	DESCRIPTION
SBWS	bi-directional	word selection
SBCL	bi-directional	bit clock
SBDA	bi-directional	sub-band coded data
SBEF	input	error signal

Operation is further controlled by:

- SBDIR: input; direction of data flow
- URDA: input; unreliable encoded data signal.

The SBMCLK signal is the main frequency from which other clock signals are derived. In encode mode this division is performed internally. In decode mode the external source should provide SBWS and SBCL. The frequency of the signal is equal to 1/32nd of the bit rate. The frequency of the bit clock SBCL is twice that of the bit rate.

Table 4 SAA2012 input/output control.

SIGNAL	MODE	DESCRIPTION
FRESET	output	request a general reset of SAA2012
FDIR	output	logic 1 for decoding and logic 0 for encoding mode (common to I^2S)
SYNCDAI	output	pulse for synchronization of digital input/output (TDA1315)

ENCODE MODE

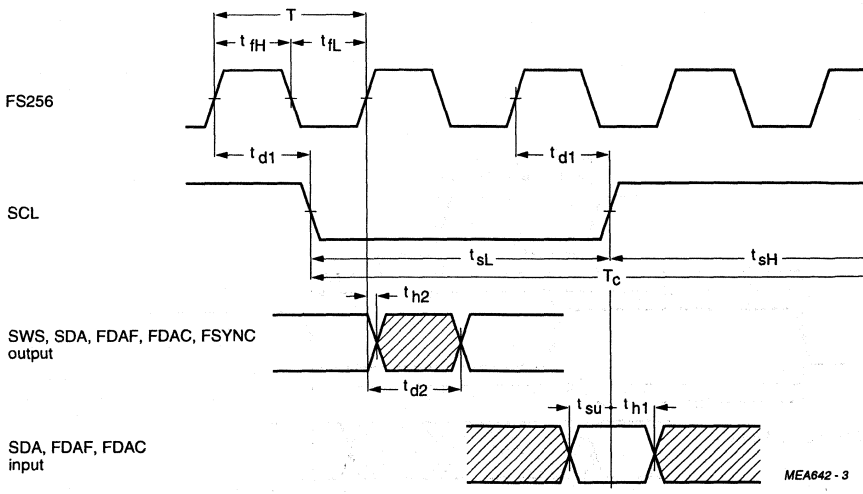
The following modes are supported:

Stereo or 2-channel mono at 384 kbits/s; audio sampling frequencies of 48, 44.1 and 32 kHz.

DECODE MODE

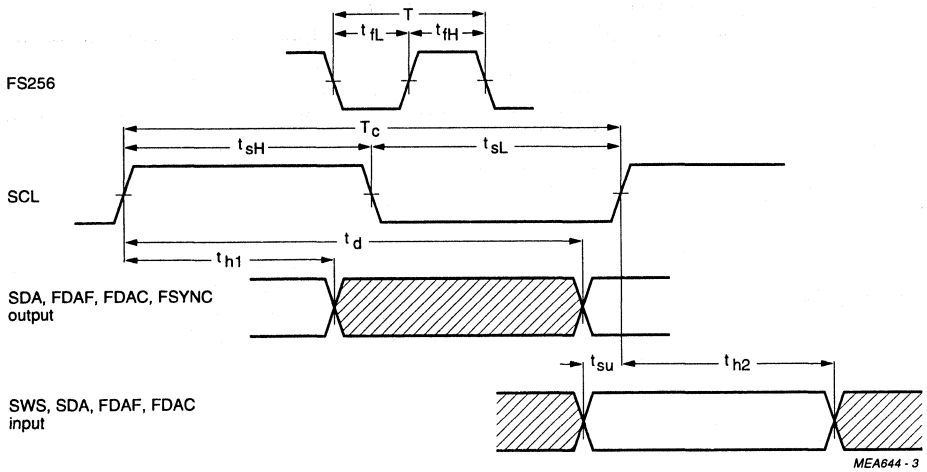
The following modes are supported:

Stereo and joint stereo, 2-channel mono and 1-channel mono at 384 kbits/s; audio sampling frequencies of 48, 44.1 and 32 kHz.



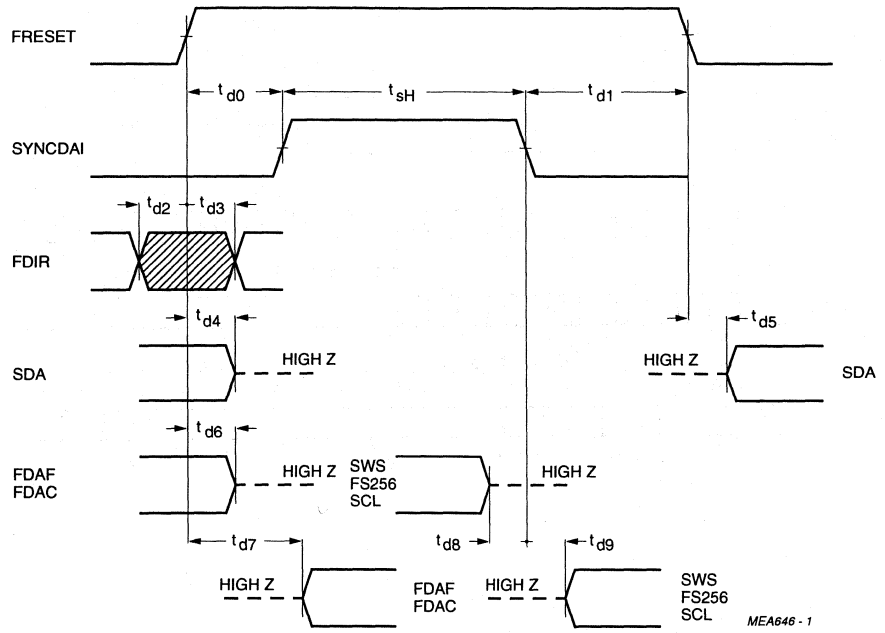
T	FS256 cycle time (f_s = 48 kHz)	81.4 ns nominal
	FS256 cycle time (f_s = 44.1 kHz)	88.6 ns nominal
	FS256 cycle time (f_s = 32 kHz)	122.1 ns nominal
T_c	SCL cycle time	4T ns nominal
t_{fH}	FS256 HIGH time (f_s = 48 kHz)	≥ 35 ns
	FS256 HIGH time (f_s = 44.1 kHz)	≥ 38 ns
	FS256 HIGH time (f_s = 32 kHz)	≥ 75 ns
t_{fL}	FS256 LOW time (f_s = 48 kHz)	≥ 15 ns
	FS256 LOW time (f_s = 44.1 kHz)	≥ 38 ns
	FS256 LOW time (f_s = 32 kHz)	≥ 75 ns
t_{sH}	SCL HIGH time	≥ 2T – 20 ns
t_{sL}	SCL LOW time	≥ 2T – 20 ns
t_{su}	SDA, FDAF and FDAC input set-up time before FS256 HIGH	≥ 20 ns
t_{h1}	SDA, FDAF and FDAC input hold time after FS256 HIGH	≥ 30 ns
t_{h2}	SDA, FDAF and FDAC output hold time after FS256 HIGH	≥ 0 ns
$t_{d1,2}$	FS256 HIGH to SCL, SWS, SDA, FDAF and FDAC output valid	≤ 50 ns

Fig.11 Filtered-I²S interface timing (master mode - FS256, SCL and SWS are output).



t_{fH}	FS256 HIGH time	≥ 35 ns
t_{fL}	FS256 LOW time	≥ 35 ns
t_{sH}	SCL HIGH time	≥ T + 35 ns
t_{sL}	SCL LOW time	≥ T + 35 ns
t_{su}	SDA, FDAF and FDAC input set-up time valid after SCL HIGH	≥ 20 ns
t_{h1}	SDA, FDAF and FDAC output hold time after SCL HIGH	≥ 2T − 15 ns
t_{h2}	SDA, FDAF and FDAC input hold time after SCL HIGH	≥ T + 20 ns
t_d	SCL HIGH to SDA, FDAF and FDAC output valid	≤ 3T + 60 ns

Fig.12 Filtered-I²S interface timing (slave mode - FS256, SCL and SWS are input).



t_{d0}	FRESET HIGH to SYNCDAI HIGH	≥ 300 ns
t_{sH}	SYNCDAI HIGH time	≥ 1280 ns
t_{d1}	SYNCDAI LOW to FRESET LOW	≥ 790 ns
t_{d2}	FDIR hold to FRESET HIGH	≤ 20 ns
t_{d3}	FRESET HIGH to FDIR valid	≤ 20 ns
t_{d4}	SDA change to high impedance after FRESET HIGH	≥ 0 ns and ≤ 170 ns
t_{d5}	SDA remains high impedance after FRESET LOW	≥ 0 ns and ≤ 170 ns
t_{d6}	FDAF and FDAC change to high impedance after FRESET HIGH	≤ 20 ns
t_{d7}	FDAF and FDAC remain high impedance after FRESET HIGH	≥ 460 ns
t_{d8}	FS256, SWS and SCL change to high impedance before SYNCDAI HIGH	≥ 140 ns
t_{d9}	FS256, SWS and SCL remain high impedance after SYNCDAI HIGH	≥ 140 ns

Fig.13 Mode switch timing.

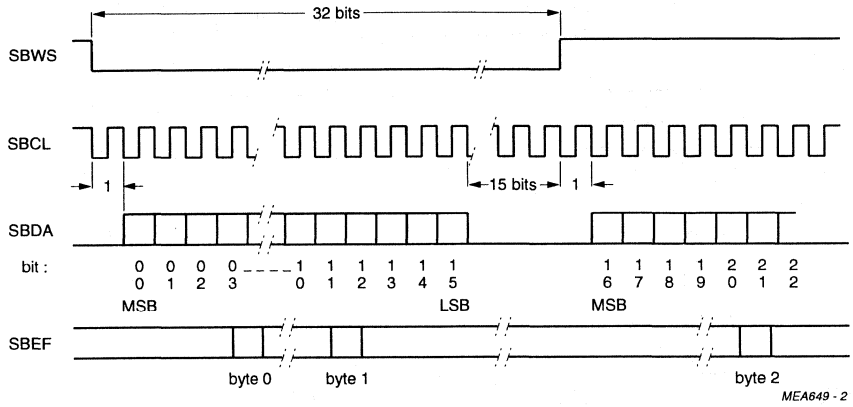


Fig.14 Transferring PASC data to and from the SAA2002.

PASC Coded Interface (sub-band I²S)

The PASC coded data is transferred to and from the SAA2002 using the format shown in Fig.15.

Each period of SBWS contains 64 data bits, 32 of which are used to convey data. The half-period during which SBWS is logic 0 is used to transfer the first 16-bits (0 to 15) of a sub-band slot. The remaining half-period during which SBWS is logic 1 carries the remaining 16-bits (16 to 31). Thus one period of SBWS corresponds with one slot of the sub-band signal.

Bits 0 and 16 are transferred in the bit clock period, one bit-time after the change in SBWS. Both SBWS and SBDA change state during the negative edge of SBCL.

In decode mode a byte error flag SBEF is also transferred. This occurs approximately in the middle of the corresponding byte (byte 0 = bits 0 to 7, byte 1 = bits 8 to 15 etc.).

ENCODING MODE

SBCL, SBWS and SBDA are generated by the SAA2002. However, if the SBDIR signal is logic 1, the output buffers are not enabled and these signals do not appear on the pins. This mode is available to permit a change of operating mode whilst the bus signals are driven from an external source.

DECODING MODE

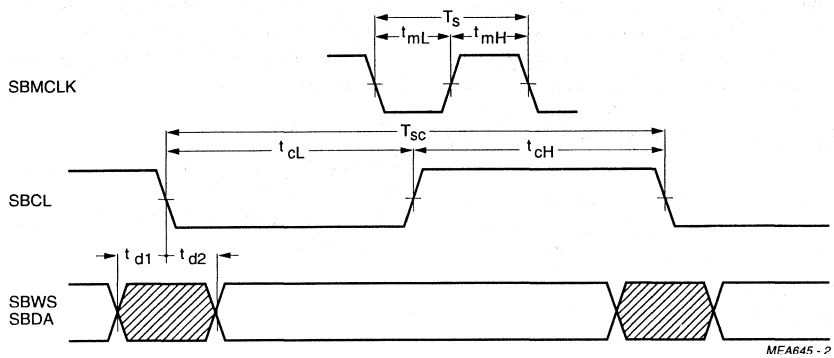
SBCL, SBWS and SBDA are generated by an external source.
Table 5 contains a summary of the source signals in the various modes.

Table 5 Modes and source signals.

MODE	FDIR	SBDIR	SOURCE					REMARKS
			SBWS	SBCL	SBDA	SBEF	SBMCLK	
Encode	0	0	INT	INT	INT	---	INT	note 1
Encode	0	1	EXT	EXT	EXT	---	INT	note 2
Decode	1	0	INT	INT	INT	EXT	INT	note 3
Decode	1	1	EXT	EXT	EXT	EXT	INT	

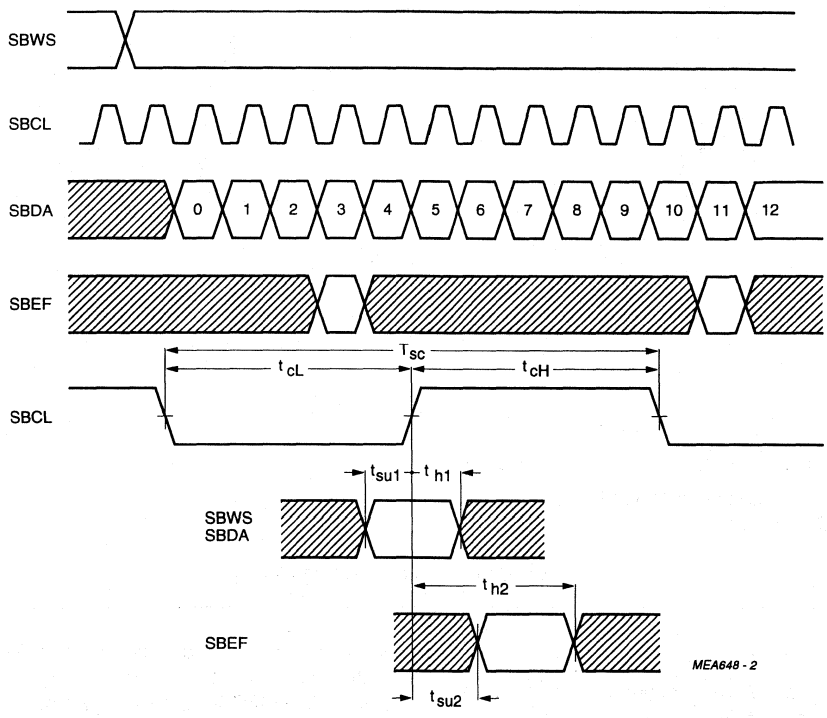
Notes

1. During encoding the SBEF signal is 'don't care'.
2. Incoming data is not decoded. The SAA2002 operates in the encoding mode and the data does not enter the interface.
3. Operation is undefined. The SAA2002 is in decoding mode whilst the SBWS, SBCL and SBDA output drivers are enabled.



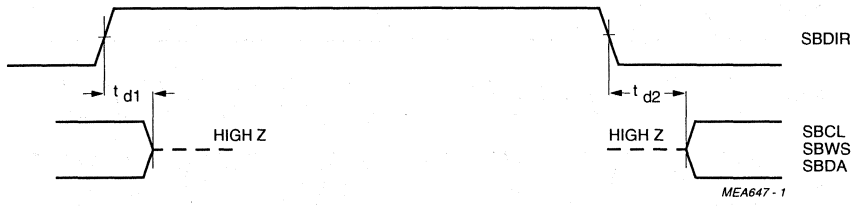
T_s	SBMCLK cycle time	120 to 205 ns (163 ns nominal)
t_{mH}	SBMCLK HIGH time	≥ 35 ns
t_{mL}	SBMCLK LOW time	≥ 75 ns
T_{sc}	SBCL cycle time (384 kbits/s)	$8T_s$ ns nominal
t_{cH}	SBCL HIGH time (384 kbits/s)	≥ $4T_s$ – 20 ns
t_{cL}	SBCL LOW time (384 kbits/s)	≥ $4T_s$ – 20 ns
t_{d1}	SBWS, SBDA hold to SBCL LOW	≤ 20 ns
t_{d2}	SBCL LOW to SBWS, SBDA valid	≤ 20 ns

Fig.15 Sub-band I²S interface timing (master mode - SBCL, SBWS and SBDA are output).



T_s	SBMCLK cycle time	
T_{sc}	SBCL cycle time	$8T_s$ ns nominal
t_{cH}	SBCL HIGH time	$\geq T_s + 30$ ns
t_{cL}	SBCL LOW time	$\geq T_s + 30$ ns
t_{su1}	SBWS, SBDA input set-up time before SBCL HIGH	$\geq T_s + 30$ ns
t_{h1}	SBWS, SBDA input hold time after SBCL HIGH	≥ 30 ns
t_{su2}	SBCL HIGH to SBEF valid	$\leq T_s - 30$ ns
t_{h2}	SBEF hold time after SBCL HIGH	$\geq 2T_s - 30$ ns

Fig.16 Sub-band I²S interface timing (slave mode - SBCL, SBWS and SBDA are input).



t_{d1} SBDIR HIGH to SBCL, SBWS SBDA high impedance ≤ 50 ns

t_{d2} SBCL SBWS, SBDA low impedance after SBDIR LOW ≥ 240 ns

Fig.17 Sub-band I²S mode switch timing.

Microcontroller interface

The SAA2002 has an interface connection to the serial interface of a microcontroller.

Table 6 Signals used.

SIGNAL	DIRECTION	DESCRIPTION
LTCLK	input	bit clock
LTDATA	bi-directional	serial data
LTCNT0	input	control line 0
LTCNT1	input	control line 1
LTENSFC	input	enable

The SAA2002 microcontroller interface is enabled only if LTENSFC (pin 34) is logic 1. Information to or from the SAA2002 is conveyed in serial 8 or 16-bit units, whilst the type of information is controlled by LTCNT0 (pin 35) and LTCNT1 (pin 36).

A transfer commences when the microcontroller sets the control lines to the correct combination for the required action. LTENSFC is set to logic 1. The SAA2002 determines its required action and prepares to transfer data. When the microcontroller supplies the LTCLK, data is transferred to or from the SAA2002 in units of 8-bits. 16-bit transfers are conveyed as two 8-bit units during which LTENSFC remains HIGH.

During the transfer of 8-bit units, the least significant bit is first to be transferred. When 16-bit units are transferred the most significant byte is sent first

EXTENDED SETTINGS (LTCNT1 = LOGIC 0, LTCNT0 = LOGIC 0)

Four information bits together with four address bits are transferred in this mode. The order in which the bits appear on the interface is:

D0 .. D1 .. D2 .. D3 .. A0 .. A1 .. A2 .. A3

Table 7 Extended settings.

BIT A3	BIT A2	BIT A1	BIT A0	DESCRIPTION
0	0	0	0	CODEC external settings; see Table 8
0	0	0	1	FILTER settings; note 1
0	0	1	0	not used
..	..	..	..	..
1	1	1	1	not used

Note

1. When D0 = logic 1 (default) I²S mode is selected. For D0 = logic 0 the alternative mode is selected. The setting of D0 remains dormant until activated by the occurrence of FRESET.

Table 8 Extended settings.

BIT	DESIGNATION	DEFAULT	DESCRIPTION
D0	MUTEDAC (1)	1	connected to DAC mute input
D1	ATTDAC (1)	0	connected to DAC attenuation input
D2	DEEMDAC (1)	0	emphasis control for DAC circuit
D3	HOLDCLKOK	0	selects CLKOK hold mode

Note

1. If not used for DAC control, the MUTEDAC, ATTDAC and DEEMDAC can be used as general purpose output expanders.

Bits D0 to D3 are copied directly to the corresponding output pins/mode flip-flop.

For HOLDCLKOK = logic 1. When CLKOK drops it will remain low until set by an encode/decode mode, sample frequency, external 256FS or bit rate index change.

ALLOCATION/SCALE FACTOR INFORMATION
(LTCNT1 = LOGIC 0, LTCNT0 = LOGIC 1)

For recording, the allocation and scale factor arrays can be filled using this mode. To completely fill the allocation array 16 complete transfers of 16-bits are required. After the first transfer of allocation information a check must be made to determine when the SAA2002 is ready to receive the remaining information. This will ensure synchronization with the internal program of the SAA2002. Transfer of the allocation information is completed by sending the internal settings.

This is then followed by the scale factor information.

In the event that only internal settings information is sent, then a default allocation of logic 0 will be assigned to all sub-bands. If, in addition no internal settings are sent, then the previous settings remain valid.

The allocation information is transferred in 4-bit units. Each of these units contains the number of bits allocated to the sub-band, MINUS 1, except in the case of a logic 0 value, which indicates that no bits are allocated to that sub-band.

Scale factor information is transferred in units of 8-bits, containing the 6-bit scale factor which is extended to 8- bits by adding two logic 0s at the most significant end.

In the case of stereo encoding the channels are indicated by L (left) and R (right). This changes to I and II in the case of 2 channel mono encoding.

Table 9 Allocation information format.

BITS				CHANNEL	SUB-BAND
MSB			LSB		
B15	B14	B13	B12	L or I	0, 2, 4, ... 30 (even)
B11	B10	B9	B8	R or II	0, 2, 4, ... 30 (even)
B7	B6	B5	B4	L or I	1, 3, 5, ... 31 (odd)
B3	B2	B1	B0	R or II	1, 3, 5, ... 31 (odd)

Table 10 Scale factor information format.

BITS			CHANNEL	SUB-BAND
MSB		LSB		
B15	to	B8	L or I	0 to 31
B7	to	B0	R or II	0 to 31

INTERNAL SETTINGS (LTCNT1 = LOGIC 1, LTCNT0 = LOGIC 0)

The operation of the codec is controlled by the bits transferred in this mode.

Table 11 Internal settings (LTCNT1 = LOGIC 1, LTCNT0 = LOGIC 0).

BITS			NAME	FUNCTION	VALID IN
MSB		LSB			
S15	to	S12	bit rate index	bit rate indication	encode
S11	to	S10	sample frequency	44.1, 48 or 32 kHz indication	encode
S9	–	–	decode	1 = decode, 0 = encode	encode/decode
S8	–	–	EXT 256FS	1 = external; 0 = internal 256FS	encode/decode
S7	–	–	2-channel mono	1 = 2-channel mono; 0 = stereo	encode
S6	–	–	MUTESFC	1 = mute; 0 = no mute	encode/decode
S5	–	–		not used	–
S4	–	–	CH1	1 = CH1; 0 = CH2	decode
S3	to	S2	Tr0 to Tr1	transparent bits	encode
S1	to	S0	EMPHASIS	emphasis indication	encode

Table 12 Internal settings (LTCNT1 = LOGIC 1, LTCNT0 = LOGIC 0).

BITS				BIT RATE	REMARK
MSB			LSB		
1	1	0	0	384 kbits/s	default value

The bit rate index indicates the bit rate of the encoded signal and is only effective in the encode mode.

The decode bit determines the operation mode of the SAA2002. The default value is 1 (decoding mode).

EXT 256FS in the encoding mode determines whether or not the SAA2002 is master or slave of the Filtered-I²S interface (default is 0, master mode).

2-channel mono is used in the encoding mode to determine whether the sub-band signal is generated as a stereo or 2-channel mono signal. Default value is 0.

MUTESFC is used in both the encoding and decoding modes to mute the information to or from the Filtered-I²S interface (the default value is 0).

CH1 is utilized in the decoding mode to select one of the 2-channel mono signals to be decoded (default is 1 channel 1). A value of 0 results in channel 2 being decoded.

The transparent bits are copied in the sub-band signal, default is 00.

The information from S15 to S10, S7 and S3 to S0 will be copied into the sub-band signal.

Table 13 Sample frequency indication.

BITS		SAMPLE FREQUENCY	REMARK
MSB	LSB		
0	0	44.1 kHz	default value
0	1	48 kHz	–
1	0	32 kHz	–
1	1	not used	–

Table 14 EMPHASIS indication.

BITS		EMPHASIS	REMARK
MSB	LSB		
0	0	no emphasis	default value
0	1	50/15 μs	–
1	0	reserved	–
1	1	CCITT J.17	–

Before sending internal settings the microcontroller should check whether or not the SAA2002 is ready-to-receive. However, this does not apply for the transfer of internal settings to end a transfer of allocation information.

STATUS (LTCNT1 = LOGIC1, LTCNT0 = LOGIC 1)

Table 15 Status information 16-bits units.

BITS			NAME	FUNCTION	VALID IN
MSB		LSB			
T15	to	T12	bit rate index	bit rate indication	encode/decode
T11	to	T10	sample frequency	44.1, 48 or 32 kHz indication	encode/decode
T9	–	–	ready-to-receive	1 = ready, 0 = not ready	encode/decode
T8	–	–	not used		
T7	to	T6	MODE	sub-band signal mode indication	encode/decode
T5	–	–	SYNC	synchronization indication	decode
T4	–	–	CLKOK	1 = OK; 0 = not OK	encode/decode
T3	to	T2	Tr0 to Tr1	transparent bits	encode/decode
T1	to	T0	EMPHASIS	emphasis indication	encode/decode

The bit rate index indicates the bit rate of the sub-band signal in units of 32 kbits/s. Bit rate index 0000 indicates the 'free format' condition. Bit rate 1111 is illegal and should not be found.

The coding of the sample frequency indication is equal to the one in the internal settings.

Table 16 MODE identification.

BITS		MODE	OUTPUT
MSB	LSB		
0	0	stereo	L and R
0	1	joint stereo	L and R
1	0	2-channel mono	I or II; as selected
1	1	1-channel mono	mono; no selection

Ready-to-receive indicates whether the SAA2002 is ready to receive allocation, scale factor or internal setting transfers. This should be checked in order to synchronize the transfer of such information.

In 2-channel mono decode mode the selected samples are transferred to both output channels. The same occurs with all samples in 1-channel mono decode mode. In both of these cases the L and R filter output channels are identical.

In decode mode the SYNC bit is logic 0 when the SAA2002 is unable to decode the sub-band frames. This will occur in the following situations:

- With the loss of synchronization.
- When the incorrect allocation information is received for two or more subsequent frames (SBEF was HIGH).
- When the URDA input pin (6) is HIGH.

In these situations the SAA2002 data output will be muted. The SYNC bit will return to logic 1 as soon as the decoder is re-synchronized to the incoming sub-band data.

CLKOK indicates whether the 256FS clock corresponds to specified sample frequency. The CLKOK bit is set to logic 1 after a change in sample frequency, operation mode or EXT256FS setting. It drops to logic 0 as soon as the 256FS clock deviates from the nominal frequency by more than approximately 0.2%. Return to logic 1 will only occur automatically when the extended setting CLKOK-hold-mode is logic 0.

The transparent bits are copied from the PASC signal.

The EMPHASIS indication is as defined in the internal settings. It can be used to apply the correct de-emphasis.

Remark: The two bytes of the status are 'sampled' at different moments so the information may not result from the same sub-band frame.

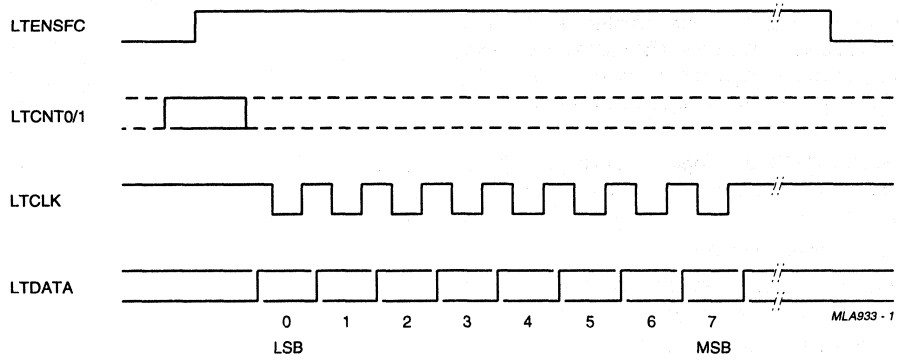


Fig.18 Transfer of data on the SAA2002 microcontroller interface.

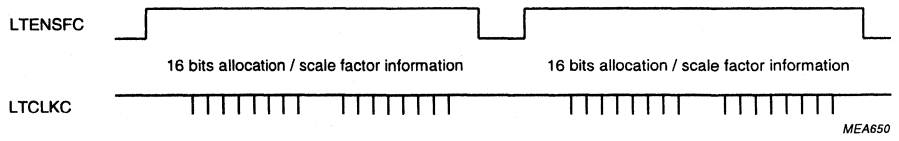


Fig.19 The LTENSFC line must return to logic 0 between information transfers.

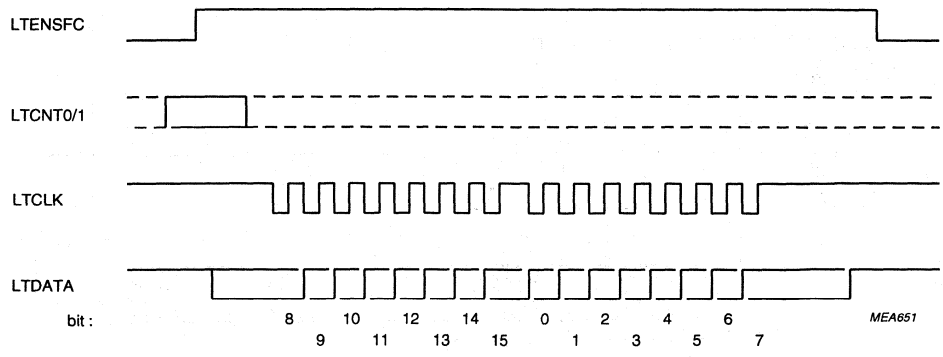
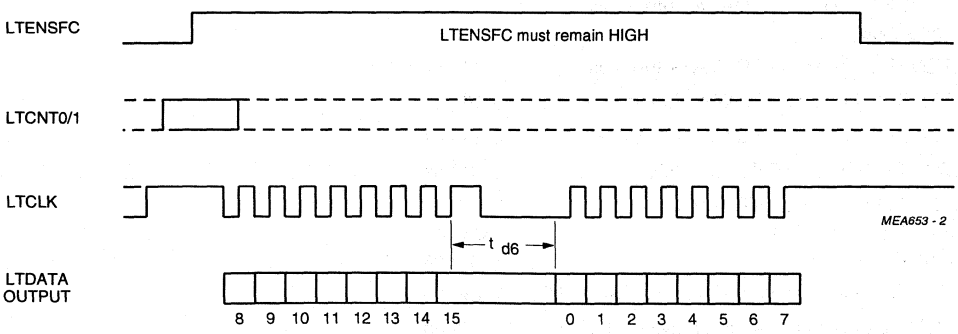
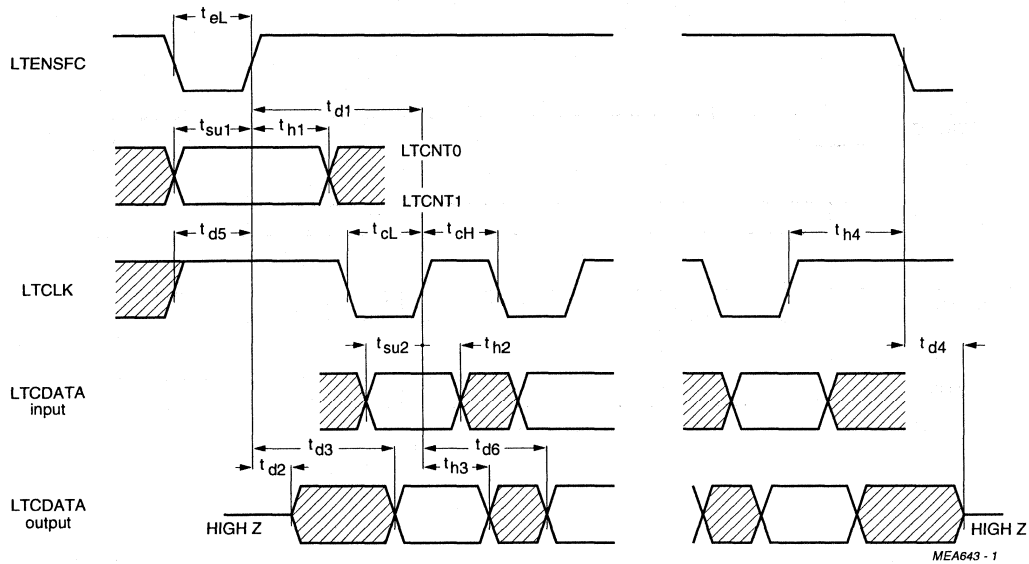


Fig.20 Order of settings and status bits on the SAA2002 microcontroller interface.



t_{d6} delay time LTCLK HIGH to LTDATA valid output for bit 0 in 16-bit transfers.

Fig.21 16-bit transfers.



t_{eL}	LTENSFC LOW time	≥ 190 ns
t_{cH}	LTCLK HIGH time	≥ 190 ns
t_{cL}	LTCLK LOW time	≥ 190 ns
t_{d1}	LTENSFC HIGH to LTCLK HIGH	≥ 190 ns
t_{d2}	LTENSFC HIGH to LTDATA output low impedance	≥ 0 ns
t_{d3}	LTENSFC HIGH to LTDATA output valid	≤ 380 ns
t_{d4}	LTENSFC LOW to LTDATA high impedance	≤ 50 ns
t_{h4}	LTENSFC hold time after LTCLK HIGH	≥ 355 ns
t_{d5}	LTCLK HIGH to LTENSFC HIGH	≥ 190 ns
t_{d6}	LTCLK HIGH to LTDATA output valid; for bit 0 (see Fig.21)	≤ 355 ns
	for bit 8	≤ 520 ns
t_{su1}	LTCNT0/1 set-up time before LTENSFC HIGH	≥ 190 ns
t_{h1}	LTCNT0/1 hold time after LTENSFC HIGH	≥ 190 ns
t_{su2}	LTDATA set-up time before LTCLK HIGH	≥ 190 ns
t_{h2}	LTDATA input hold time after LTCLK HIGH	≥ 30 ns
t_{h3}	LTDATA output hold time after LTCLK HIGH	≥ 145 ns
t_{h4}	LTENSFC hold time after LTCLK HIGH	≥ 355 ns

Fig.22 Microcontroller interface timing.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+6.5	V
V_I	input voltage	note 1	−0.5	V_{DD} + 0.5	V
I_{SS}	supply current in V_{SS}		−	160	mA
I_{DD}	supply current in V_{DD}		−	160	mA
I_I	input current		−10	+10	mA
I_O	output current		−20	+20	mA
P_{tot}	total power dissipation		−	880	mW
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{es1}	electrostatic handling	note 2	−1500	+1500	V
V_{es2}	electrostatic handling	note 3	−70	+70	V

Notes

1. Input voltage should not exceed 6.5 V unless otherwise specified.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

DC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	note 1	3.8	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V; note 2	−	82	110	mA
		V_{DD} = 3.8 V; note 2	−	58	80	mA
Inputs URDA, SBDIR, SBEF, LTCLK, LTCNT0, LTCNT1, X22IN and X24IN						
V_{IL}	LOW level input voltage		−	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	−	V
I_I	input current	V_I = 0 V; T_{amb} = 25 °C	−	−	−10	µA
		V_I = 5.5 V; T_{amb} = 25 °C	−	−	10	µA
Inputs PWRDWN and LTENSFC						
V_{IL}	LOW level input voltage		−	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7\ V_{DD}$	−	−	V
I_I	input current	$V_I = V_{DD}$; T_{amb} = 25 °C	40	−	250	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs RESET						
V_{tLH}	threshold voltage LOW-to-HIGH		–	–	$0.8V_{DD}$	V
V_{tHL}	threshold voltage HIGH-to-LOW		$0.2V_{DD}$	–	–	V
V_{hys}	hysteresis	$V_{tLH} - V_{tHL}$	–	1.5	–	V
I_I	input current	$V_I = V_{DD}$; $T_{amb} = 25$ °C	40	–	250	µA
Outputs MUTEDAC, DEEMDAC, ATTDAC, SYNCDAI, FDIR, FRESET, FSYNC and CLK22						
V_{OL}	LOW level output voltage	$I_O = -2$ mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	$I_O = 2$ mA	$V_{DD} - 0.5$	–	–	V
Output CLK24						
V_{OL}	LOW level output voltage	$I_O = -8$ mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	$I_O = 8$ mA	$V_{DD} - 0.5$	–	–	V
Inputs/outputs SBDA, SBCL, SBWS, FDAF, FDAC, SCL, SWS, SDA and LTDATA						
V_{OL}	LOW level output voltage	$I_O = -2$ mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	$I_O = 2$ mA	$V_{DD} - 0.5$	–	–	V
Outputs SBDA, SBCL, SBWS, FDAF, FDAC, SCL, SWS, SDA and LTDATA in 3-state						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_I	input current	$V_I = V_{DD}$; $T_{amb} = 25$ °C	40	–	250	µA
Input/output SBMCLK						
V_{OL}	LOW level output voltage	$I_O = -8$ mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	$I_O = 8$ mA	$V_{DD} - 0.5$	–	–	V
Output SBMCLK in 3-state						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_I	input current	$V_I = V_{DD}$; $T_{amb} = 25$ °C	40	–	250	µA
Input/output FS256						
V_{OL}	LOW level output voltage	$I_O = -12$ mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	$I_O = 12$ mA	$V_{DD} - 0.5$	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output FS256 in 3-state						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_I	input current	$V_I = V_{DD}$; T_{amb} = 25 °C	40	–	250	μA

Notes

1. For applications requiring minimum power dissipation the device may be operated from a nominal +4 V supply.
2. For load impedances representative of the application.

AC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
C_I	input capacitance		–	–	10	pF
X24IN and X22IN						
f_{xtal}	crystal frequency at X22OUT, CLK22	note 1	21	22.5792	24	MHz
f_{xtal}	crystal frequency at X24OUT, CLK22	note 1	23	24.576	26	MHz
g_m	mutual conductance	f = 100 kHz	1.5	–	–	mA/V
A_v	small signal gain	$A_v = g_m.R_o$	3.5	–	–	V/V
C_{fb}	feedback capacitance		–	–	5	pF
C_O	output capacitance		–	–	10	pF
Outputs						
C_O	output capacitance		–	–	10	pF
Inputs URDA, RESET, LTDATA, LTCLK, LTENSFC, LTNT0 and LTNT1						
t_{su}	set-up time to X24IN		15	–	–	ns
t_h	hold time to X24IN		60	–	–	ns
Outputs LTDATA, MUTEDAC, DEEMDAC, ATTDAC, SYNCDAI, FDIR and FRESET						
t_{PD}	propagation delay time from X24IN		–	–	80	ns
Inputs FDAF, FDAC, SDA, SCL and SWS						
t_{su}	set-up time to FS256		15	–	–	ns
t_h	hold time to FS256		25	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs FDAF, FDAC, SDA, SCL, SWS and FSYNC						
t_{PD}	propagation delay time from FS256		–	–	50	ns
Inputs SBDA, SBCL, SBWS, URDA, SBDIR and SBEF						
t_{su}	set-up time to SBMCLK		15	–	–	ns
t_h	hold time to SBMCLK		25	–	–	ns
Outputs SBDA, SBCL and SBWS						
t_{PD}	propagation delay time from SBMCLK		–	–	50	ns
FS256						
T	FS256 cycle time	f_s = 48 kHz	–	81.4	–	ns
		f_s = 44.1 kHz	–	88.6	–	ns
		f_s = 32 kHz	–	122.1	–	ns
T_c	SCL cycle time		–	4T	–	ns
FS256 master mode (FS256, SCL and SWS are output)						
t_{fH}	FS256 HIGH time	f_s = 48 kHz	35	–	–	ns
		f_s = 44.1 kHz	38	–	–	ns
		f_s = 32 kHz	75	–	–	ns
t_{fL}	FS256 LOW time	f_s = 48 kHz	35	–	–	ns
		f_s = 44.1 kHz	38	–	–	ns
		f_s = 32 kHz	75	–	–	ns
t_{sH}	SCL HIGH time		2T – 20	–	–	ns
t_{sL}	SCL LOW time		2T – 20	–	–	ns
t_{su}	SDA, FDAF, FDAC input set-up time before FS256 HIGH		20	–	–	ns
t_{h1}	SDA, FDAF, FDAC input hold time after FS256 HIGH		30	–	–	ns
t_{h2}	SDA, FDAF, FDAC output hold time after FS256 HIGH		0	–	–	ns
$t_{d1,2}$	FS256 HIGH to SCL, SWS, SDA, FDAF, FDAC output valid		–	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FS256 slave mode (FS256, SCL and SWS are input)						
t_{fH}	FS256 HIGH time		35	–	–	ns
t_{fL}	FS256 LOW time		35	–	–	ns
t_{sH}	SCL HIGH time		T + 35	–	–	ns
t_{sL}	SCL LOW time		T + 35	–	–	ns
t_{h1}	SDA, FDAF, FDAC output hold time after SCL HIGH		2T – 15	–	–	ns
t_d	SCL HIGH to SDA, FDAF, FDAC output valid		–	–	3T + 60	ns
t_{su}	SDA, FDAF, FDAC input valid after SCL HIGH		20	–	–	ns
t_{h2}	SDA, FDAF, FDAC input hold time after SCL HIGH		T + 20	–	–	ns
SBMCLK						
T_s	SBMCLK cycle time		120	163	205	ns
t_{mH}	SBMCLK HIGH time		35	–	–	ns
t_{mL}	SBMCLK LOW time		75	–	–	ns
SBMCLK master mode (SBCL, SBWS and SBDA are output)						
T_{sc}	SBCL cycle time	384 kbits/s	–	$8T_s$	–	ns
t_{cH}	SBCL HIGH time	384 kbits/s	$4T_s - 20$	–	–	ns
t_{cL}	SBCL LOW time	384 kbits/s	$4T_s - 20$	–	–	ns
t_{d1}	SBWS, SBDA hold	to SBCL LOW	20	–	–	ns
t_{d2}	SBWS, SBDA valid	after SBCL LOW	–	–	20	ns
SBMCLK slave mode (SBCL, SBWS and SBDA are input)						
T_{sc}	SBCL cycle time		–	$8T_s$	–	ns
t_{cH}	SBCL HIGH time		$T_s + 30$	–	–	ns
t_{cL}	SBCL LOW time		$T_s + 30$	–	–	ns
t_{su1}	SBWS, SBDA set-up time	before SBCL HIGH	$T_s + 30$	–	–	ns
t_{h1}	SBWS, SBDA hold time	after SBCL HIGH	30	–	–	ns
t_{su2}	set-up time before SBEF valid	after SBCL HIGH	–	–	$T_s - 30$	ns
t_{h2}	SBEF hold time	after SBCL HIGH	$2T_s - 30$	–	–	ns

Notes

1. Percentage deviation from nominal frequency must be the same for X24, X22 and FS256 inputs within 0.2%.
2. For applications requiring minimum power dissipation the device may be operated from a nominal +4 V supply.

Stereo filter and codec SAA2003

FEATURES

- Single-chip stereo filter and codec
- Wide operating voltage range: 2.7 to 5.5 V
- Low-power consumption: 98 mW; 3.0 V
- Sleep mode for low power and low Electromagnetic Interference (EMI)
- Transparent serial audio data mode in sleep
- IEC 958 digital output
- Peak level detector for start of track detection or VU meter
- Versatile fade processor; slow/fast fade, mute, 12 dB attenuation
- Serial audio interface for I^2S or EIAJ formats
- Error concealment
- Three-wire L3 bus microcontroller interface
- Three sample rates:
  - 32 kHz
  - 44.1 kHz
  - 48 kHz
- Internal or external clock source
- Three programmable outputs
- Small surface mounted package (SOT307).

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

The SAA2003 performs the sub-band filtering and audio frame codec functions in the Precision Adaptive Sub-band Coding (PASC) system. It can be used as a stand-alone decoder for playback only applications, but requires the addition of an Adaptive Allocation and Scale Factor processor (SAA2013) in order to perform PASC encoding in a DCC record system.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2003H	44	QFP[1]	plastic	SOT307

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* are followed. The pocketbook can be ordered using the code 9398 510 34011.

BLOCK DIAGRAM

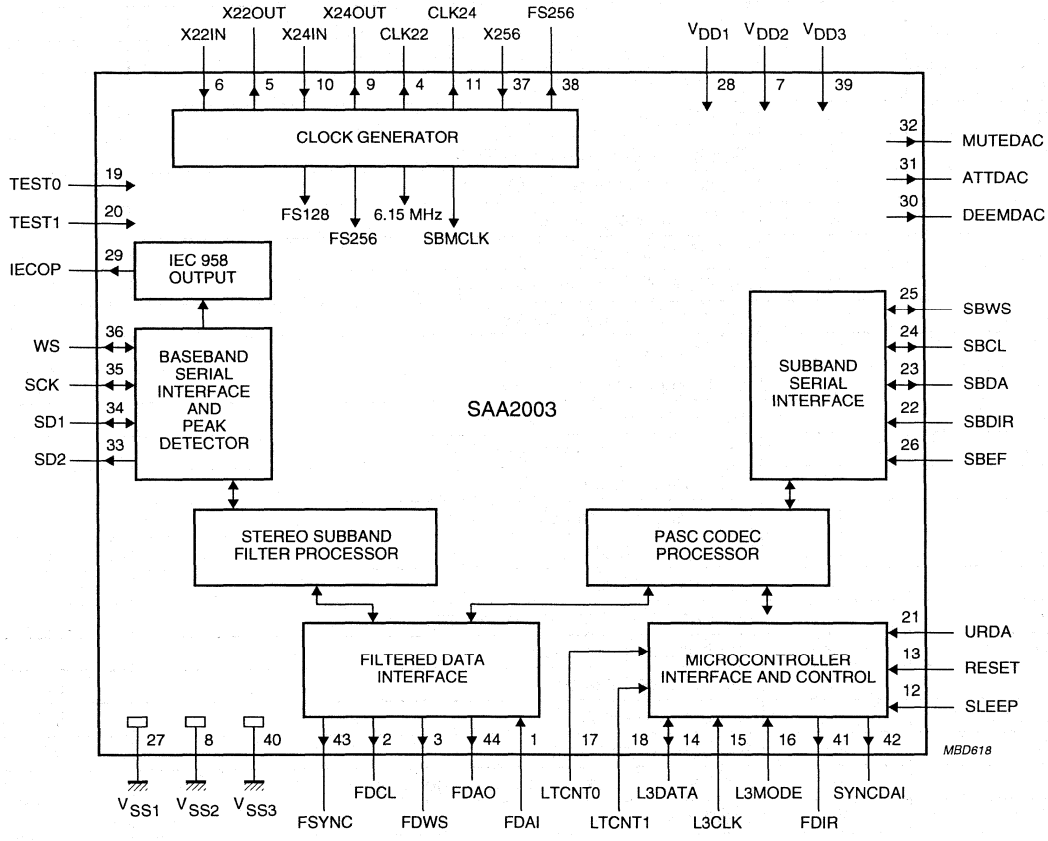


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
FDAI	1	filtered data input from SAA2013	I
FDCL	2	filtered data bit clock	O
FDWS	3	filtered data word select	O
CLK22	4	22.5792 MHz buffered clock output	O
X22OUT	5	22.5792 MHz crystal output	O
X22IN	6	22.5792 MHz crystal input	I
V_{DD2}	7	supply voltage (clock oscillator)	–
V_{SS2}	8	supply ground (clock oscillator)	–
X24OUT	9	24.576 MHz crystal output	O
X24IN	10	24.576 MHz crystal input	I
CLK24	11	24.576 MHz buffered clock output	O
SLEEP	12	sleep mode; device inactive	I
RESET	13	device reset	I
L3DATA	14	3-wire interface; serial data	I/O
L3CLK	15	3-wire interface; bit clock	I
L3MODE	16	3-wire interface; mode control	I
LTCNT0	17	LT interface; control bit 0	I
LTCNT1	18	LT interface; control bit 1	I
TEST0	19	test mode select	I
TEST1	20	test mode select	I
URDA	21	unreliable data flag from drive processor	I
SBDIR	22	sub-band data direction	I
SBDA	23	sub-band serial data	I/O
SBCL	24	sub-band bit clock	I/O
SBWS	25	sub-band word select	I/O
SBEF	26	sub-band error flag from drive processor	I
V_{SS1}	27	digital supply ground	–
V_{DD1}	28	digital supply voltage	–
IECOP	29	IEC 958 digital audio output	O
DEEMDAC	30	DAC control or general purpose output	O
ATTDAC	31	DAC control or general purpose output	O
MUTEDAC	32	DAC control or general purpose output	O
SD2	33	serial audio data to DAC	O
SD1	34	serial audio data to/from DAIO and DAC	I/O
SCK	35	serial audio data bit clock	I/O
WS	36	serial audio data word select	I/O
X256	37	master audio clock from external source	I
FS256	38	master audio clock at 256 times sample frequency	O
V_{DD3}	39	supply voltage (FS256)	–
V_{SS3}	40	supply ground (FS256)	–

SYMBOL	PIN	DESCRIPTION	TYPE
FDIR	41	filter direction; encode or decode	O
SYNCDAI	42	settings synchronization for DAIO	O
FSYNC	43	sub-band 0 sample synchronization for SAA2013	O
FDAO	44	filtered data output to SAA2013	O

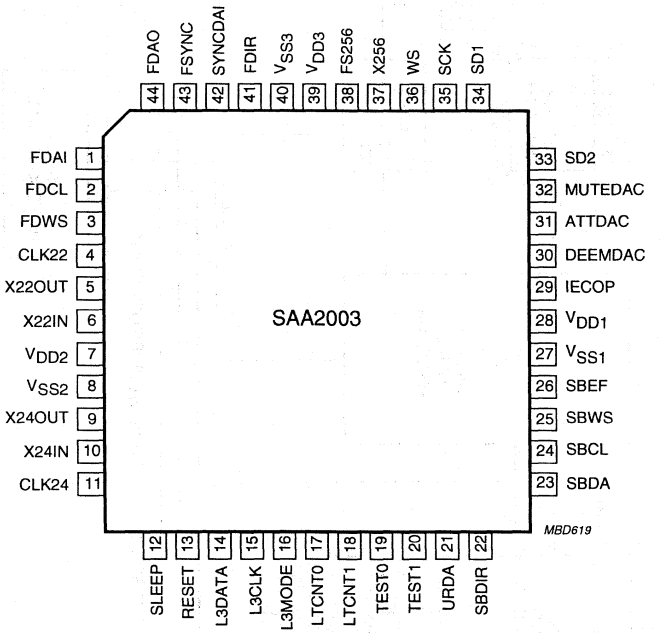


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

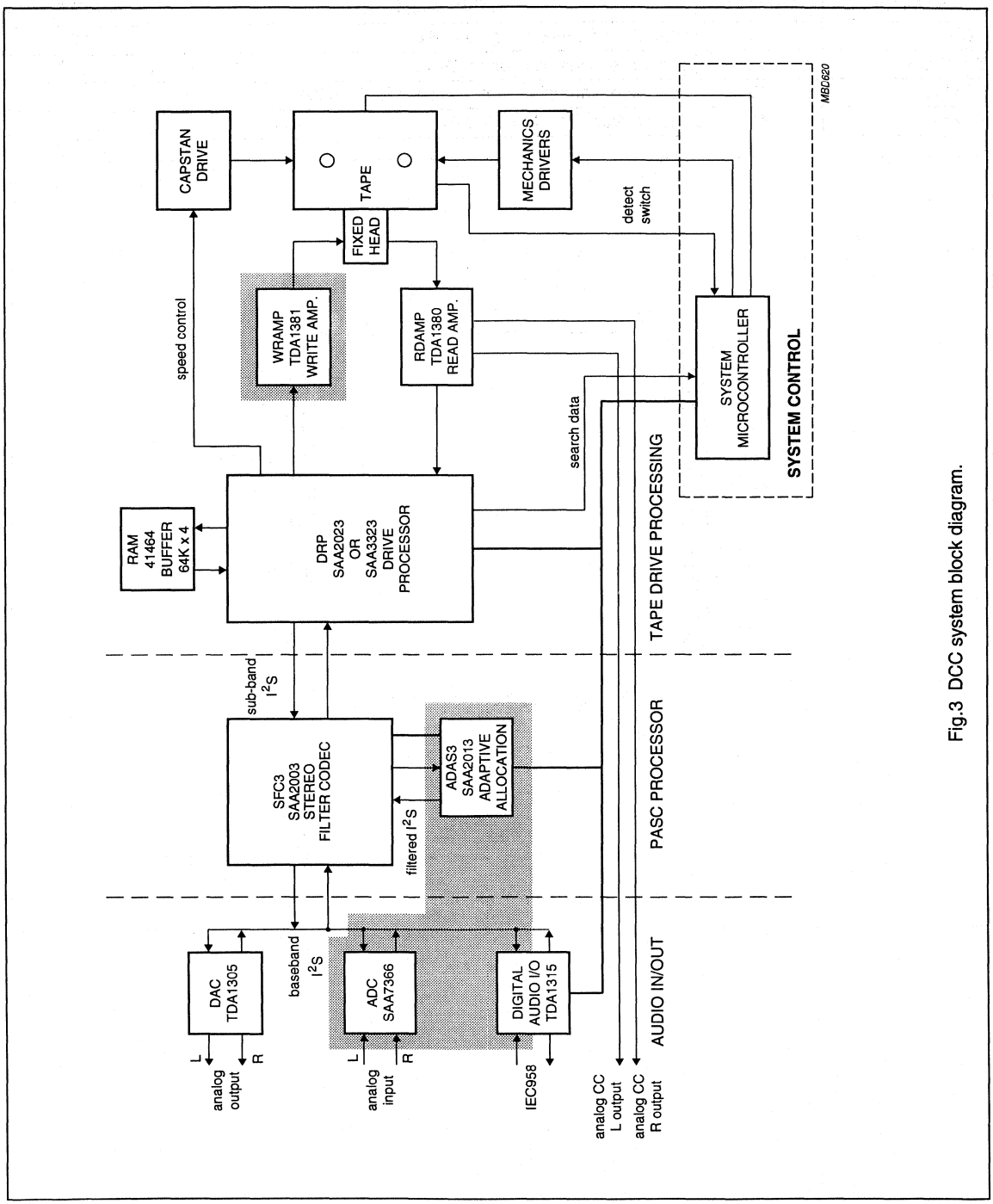


Fig.3 DCC system block diagram.

PASC processor

The PASC processor is a dedicated Digital Signal Processor (DSP) engine which efficiently codes digital audio data at a bit rate of 384 kbits/s without affecting the sound quality. This is achieved using an efficient adaptive data notation and by only encoding the information which can be heard by the human ear.

The audio data is split into 32 equal sub-bands during encoding. For each of the sub-bands a masking threshold is calculated. The samples from each of the sub-bands are included in the PASC data with an accuracy that is determined by the available bit-pool and by the difference between the signal power and the masking threshold for that sub-band.

The stereo filter codec performs the splitting (encoding) and reconstruction (decoding), including the necessary formatting functions. During encoding, the adaptive allocation and scaling circuit calculates the required accuracy (bit allocation) and scale factors of the sub-band samples.

ENCODING (SEE FIG.4)

The incoming serial audio data is filtered into 32 sub-bands for left and right (I and II) channels using the stereo filter part of the SAA2003. A PASC frame is made up of left and right (I and II) audio data for 12 samples from each of the 32 sub-bands, a total of 768 audio samples. For every PASC frame the SAA2013 calculates a bit allocation and scale factor table which is transferred to the SAA2003. All the samples in a frame are scaled in accordance with the scale factor calculated by the SAA2013. Once scaled the samples are re-quantized to reduce the number of bits to correspond with the allocation table calculated by the SAA2013. Synchronization, allocation and scale factor information is then added to provide a fully encoded PASC data signal. These frames of data are then sent to the drive processor IC (SAA2023 or SAA3323).

DECODING (SEE FIG.5)

In decoding mode the SAA2003 synchronizes and recovers frames of data from the drive processor. The recovered allocation data and the scale factors are used to correctly re-quantize and re-scale the PASC sub-band samples. The decoded sub-band samples, which are represented in 24-bits two's complement notation, are reconstructed by the sub-band filters into a single complete digital audio signal.

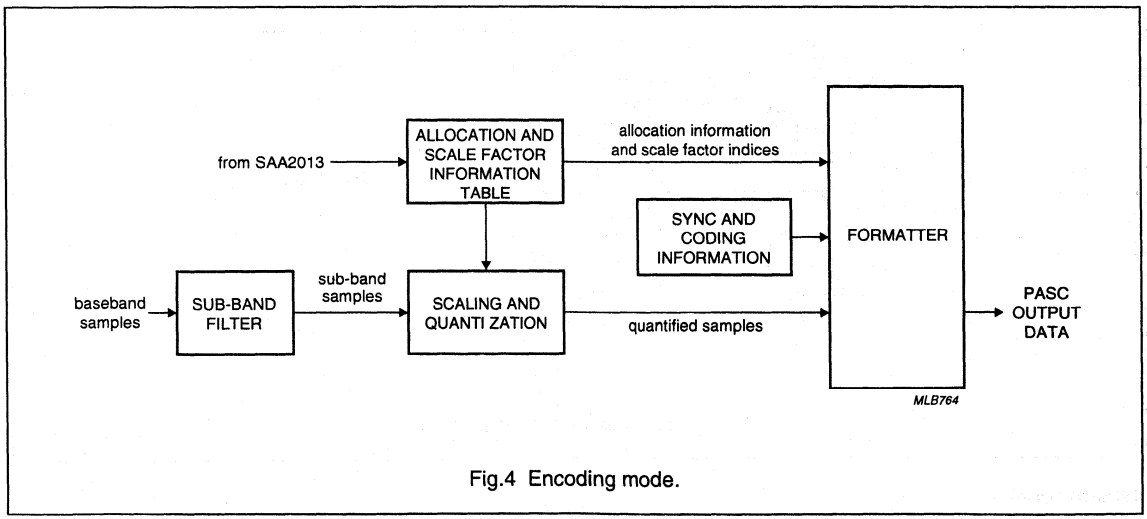


Fig.4 Encoding mode.

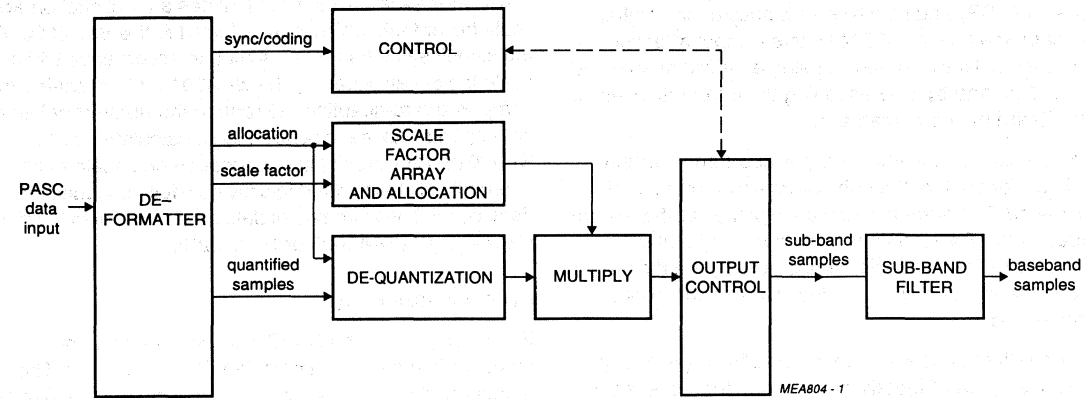


Fig.5 Decoding mode.

Crystal oscillators

The recommended crystal oscillator configuration is shown in Fig.6. The specified component values only apply to crystals with a low equivalent series resistance of <40 Ω.

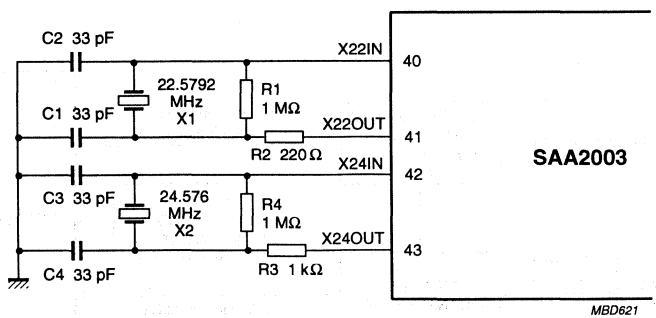


Fig.6 Crystal oscillator components.

System reset

Reset must be active from system power-up for >1 ms. Reset must also be active for >1 ms after the falling edge of sleep as shown in Fig.7.

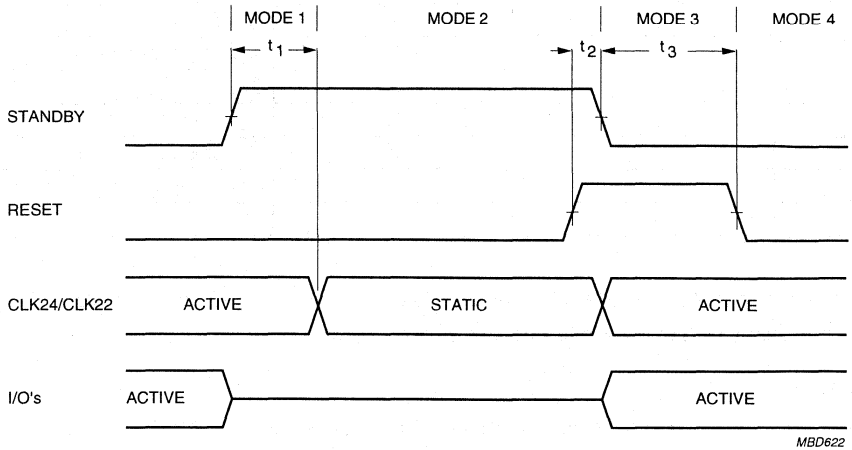


Fig.7 Reset and sleep timing.

Table 1 Reset and sleep timing modes (see Fig.7).

MODE	DESCRIPTION	TIMING	MIN.	MAX.	UNIT
MODE1	standby stage 1; clocks still running	t_1	400	–	ns
MODE2	standby mode; clocks stopped	t_2	0	–	ns
MODE3	clocks running; reset active	t_3	1	–	ms
MODE4	normal operational mode	–	–	–	

Sleep mode

A HIGH input applied to the SLEEP pin halts all internally generated clock signals. If the transparent mode of the serial audio interface is set before entering sleep, the data at the X256 external clock input is sent to the FS256 output and the data at SD1 input is sent to the SD2 output. If transparent mode is not set, these two outputs are high impedance during sleep mode.

The IECOP pin is set to high impedance during sleep mode, unless the transparent mode is selected and WS-SEL is set.

Table 2 Transparent mode function in sleep.

PIN	TRANSPARENT MODE[1]	WS-SEL[2]	PIN FUNCTION
FS256	1	X	FS256
FS256	0	X	high impedance
SD2	1	X	SD1
SD2	0	X	high impedance
IECOP	0	X	high impedance
IECOP	1	0	high impedance
IECOP	1	1	WS

Notes

1. Transparent mode is controlled by bit 3 of the serial audio data interface mode control register.
2. WS-SEL is controlled by bit 3 of the codec extended settings register.

Serial audio interface

The signals between the SAA2003 and the serial audio input/output are shown in Table 3.

Table 3 Interface signals between SAA2003 and serial audio input/output.

PIN	INPUT/OUTPUT	FUNCTION	FREQUENCY
WS	bi-directional	audio data word select	f_s
SCK	bi-directional	audio data bit clock	$64f_s$
SD1	bi-directional	serial audio data to/from DAIO and ADC	–
SD2	output	audio serial data to DAC	–
FDIR	output	PASC mode encode/decode	–
IECOP	output	alternative serial data word select for SD2	–

The word select (WS) line indicates the channel being transmitted (either left or right; I or II) and is equal in frequency to the sampling frequency (f_s).

Operating at a frequency of $64 \times f_s$, the bit clock (SCK) dictates that each WS period contains 64 SD1 or SD2 data bits. Of these bits a maximum of 36 are used to transfer data (samples may have a length up to 18 bits). Samples are transferred most significant bit (MSB) first. Both WS and SD1/SD2 change state at the negative edge of SCK.

The serial audio data is transferred between the SAA2003 and the input/output using either the standard I^2S (default) as shown in Fig.8 or the EIAJ format as shown in Fig.9.

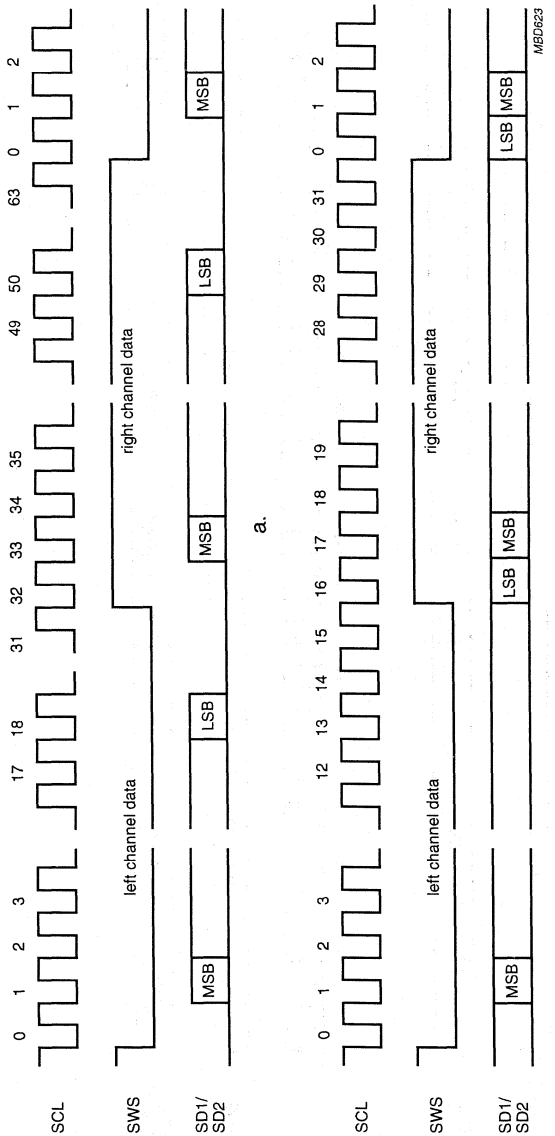
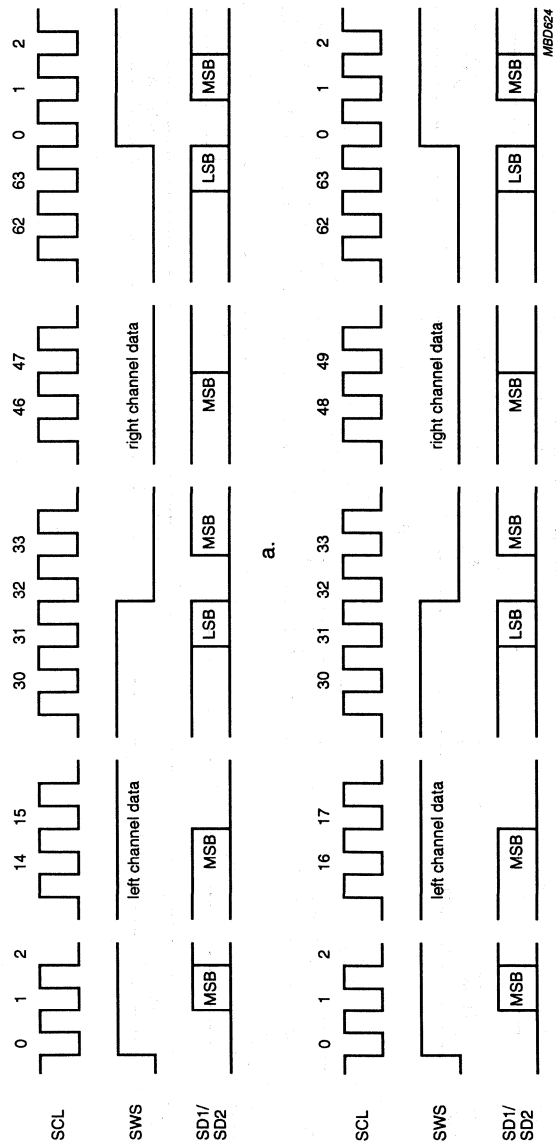


Fig.8 Serial audio interface SD1/SD2; I²S data format.

a. Master and slave modes; 18 bits.
b. Slave mode only; 16 bits.



a. Master mode; 18 bits.
b. Master mode (EIAJ); 16 bits.

Fig.9 Serial audio interface SD1; EIAJ data format.

SERIAL AUDIO INTERFACE DATA FORMATS IN ENCODING MODE

In encoding mode, the serial audio data input for the PASC processor is taken from the SD1 pin. This data is scaled by the fade processor before being sent to the PASC processor. The output from the fade processor is sent in parallel to the SD2 output.

Both I²S and EIAJ formats are supported.

Table 4 Serial audio data interface formats in encoding mode.

SD1 INPUT			SD2 OUTPUT	
FORMAT	**MASTER/SLAVE**	**RESOLUTION**	**FORMAT**	**RESOLUTION**
I²S	master	18 bit	I²S	18 bit
I²S	slave	18 bit	I²S	18 bit
I²S	master	16 bit	I²S	18 bit
I²S	slave	16 bit	I²S	16 bit
EIAJ(1)	master	18 bit	I²S	18 bit
EIAJ(1)	slave	18 bit	I²S	18 bit
EIAJ(1)	master	16 bit	I²S	18 bit
EIAJ(1)	slave	16 bit	I²S	18 bit

Note

1. If SD1 is used in EIAJ mode, and the data from SD2 is required, the IECOP can be re-programmed to provide a suitable I²S WS signal for SD2. The IEC 958 output is not available in this mode.

SERIAL AUDIO INTERFACE DATA FORMATS IN DECODING MODE

In decoding mode, the output from the PASC processor, connected via the fade processor, is present at both SD1 and SD2.

Both I²S and EIAJ formats are supported.

Table 5 SD1/SD2 output decoding formats.

FORMAT	MASTER/SLAVE	RESOLUTION(1)
I²S	master	18 bit
I²S	slave	18 bit
I²S	master	16 bit
I²S	slave	16 bit
EIAJ	master	18 bit
EIAJ	master	16 bit

Note

1. The sub-band filter performs rounding to 16 or 18 bits according to the operating mode of the interface.

SERIAL AUDIO INTERFACE MODE CONTROL

The operating mode of the interface is programmed by the extended settings registers as shown in Table 6.

Table 6 Extended settings register.

A3	A2	A1	A0	D3	D2	D1	D0	MODE
0	0	1	0	X	X	X	0	16 bit operation; 16 bit rounding
0	0	1	0	X	X	X	1	18 bit operation; 18 bit rounding
0	0	1	0	X	X	0	X	I^2S data format
0	0	1	0	X	X	1	X	EIAJ data format
0	0	1	0	X	0	X	X	peak detector input SD1
0	0	1	0	X	1	X	X	peak detector input SD2
0	0	1	0	0	X	X	X	SD1/FS256 transparent mode disabled
0	0	1	0	1	X	X	X	SD1/FS256 transparent mode enabled

Filtered data interface

The filtered data interface transfers the sub-band filtered data between the stereo filter codec and adaptive allocation and scaling parts of the DCC chip-set, and consists of the signals as shown in Table 7.

Table 7 Filtered data interface signals.

PIN	INPUT/OUTPUT	FUNCTION	FREQUENCY
FDCL	output	filtered data bit clock	$64f_s$
FDWS	output	filtered data word select	f_s
FDAO	output	filtered data serial output	–
FDAI	input	filtered data serial input	–
FDIR	output	decode/encode control	–
FSYNC	output	filtered data sync signal; band zero	–

FILTERED DATA INTERFACE FORMAT

The filtered data is transferred over the interface in accordance with the formats illustrated in Figs 10 and 11.

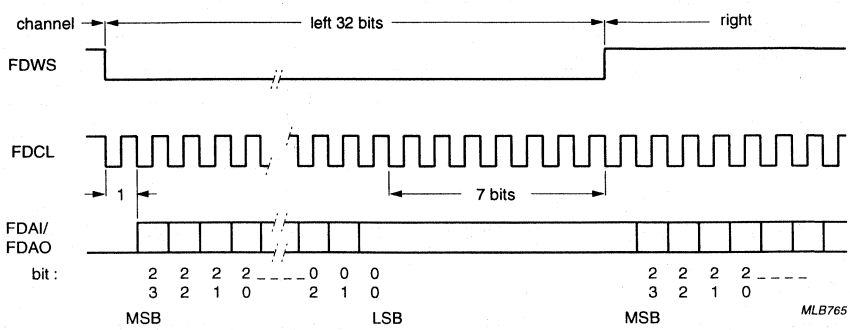


Fig.10 Transfer of filtered data; SAA2003/SAA2013.

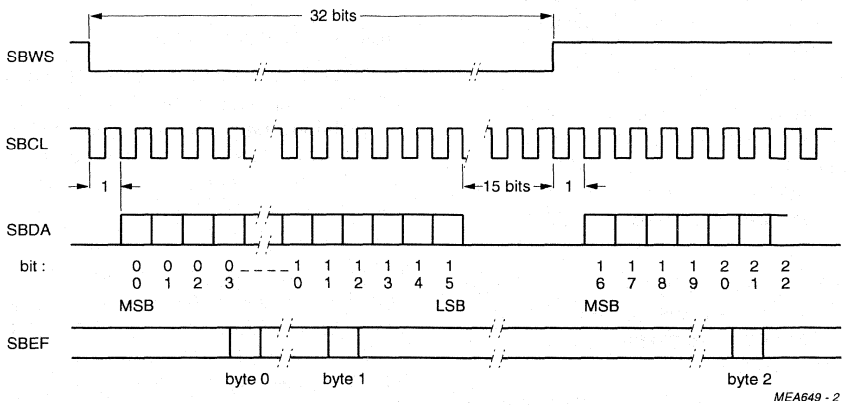


Fig.11 Transfer of sub-band PASC data.

Sub-band serial PASC interface

The sub-band serial interface carries the PASC serial data stream between the stereo filter codec and the drive processor part of the DCC chip-set, and consists of the signals as shown in Table 8.

Table 8 Sub-band serial PASC interface signals.

PIN	INPUT/OUTPUT	FUNCTION	FREQUENCY
SBDIR	input	sub-band data direction control	–
SBDA	input/output	sub-band serial data	–
1SBCL	input/output	sub-band bit clock	768 kHz
SBWS	input/output	sub-band word select	12 kHz
SBEF	input	sub-band data error flag	–
URDA	input	unreliable data flag	–

The SAA2003 generates SBWS and SBCL in both decode and encoding modes. In decode both signals can be set to inputs (slave mode) by bit 0 of the extended settings register. The filtered data interface timing is always derived from the 24.576 MHz clock, regardless of the audio sampling frequency.

Table 9 Extended settings register.

A3	A2	A1	A0	D3	D2	D1	D0	MODE
0	0	0	1	X	X	X	0	slave mode (default)
0	0	0	1	X	X	X	1	master mode

Stereo and 2-channel mono encoding modes are available. Stereo, joint stereo and 2-channel mono decoding modes are available. In decoding and encoding, 48 kHz, 44.1 kHz and 32 kHz sample frequencies can be used.

SUB-BAND SERIAL PASC INTERFACE DATA FORMAT

The PASC data is transferred over the interface described above using the format shown in Fig.11. Each period of SBWS spans 64 periods of the bit clock, SBCL, of which 32 SBCL periods are used to transfer PASC data.

The 32 data bits transferred in one period of SBWS make up a complete sub-band slot, as defined in the DCC standard. The first 16 data bits (0, 1, 2, .., 15) are transferred while SBWS is LOW, and the second 16 data bits (16, 17, 18, .., 31) are transferred while SBWS is HIGH.

SBEF and URDA are generated by the drive processor during decode. The presence of the URDA flag causes the stereo filter codec to mute the audio output data, and lose audio frame synchronization.

The direction of SBDA is controlled by the SBDIR input, which is connected to the drive processor.

SYNCDAI signal

SYNCDAI is a pulse of fixed duration which is generated by the SAA2003 when any of the following conditions occur:

- Change of bit rate
- Change of sampling frequency
- Change from encode to decode and vice-versa
- Change of FS256 clock source
- Change of I^2S bus master
- Reset.

The SYNCDAI signal is used to synchronize the digital audio input/output interface.

Audio peak level detector

The peak level detector continuously encodes the maximum amplitude of the audio data samples for each audio channel until it is reset by the action of reading out the peak level data. The peak level data can be read by the SAA2013, and subsequently by the system microcontroller, or by the microcontroller directly when SAA2013 is not used.

The peak level data is read via the L3 interface in status read mode. The first 16 bits of status read transfer the status bits of SAA2003. The following 32 bits contain the peak level data. The peak level detector is reset when the 32 bits of peak level data are read.

In encode, the peak level detector can be used to monitor the data on either SD1 (pre-fade processor) or SD2 (post fade processor). In slave EIAJ input modes the peak detection is only possible on output SD2. In decode mode, SD1 must be selected for peak detector input data.

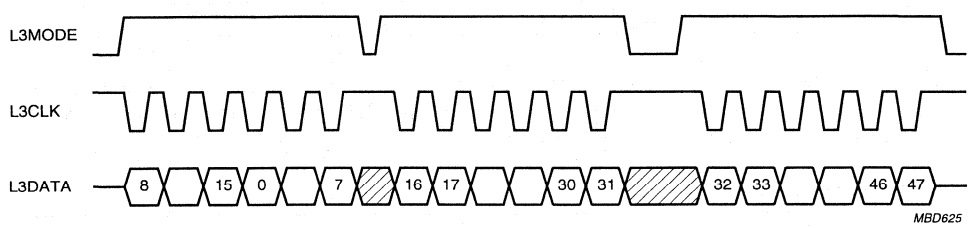


Fig.12 Peak level data format during status read.

Audio fade processor

The fade processor is controlled by the system microcontroller. It achieves level control, or fading, by multiplying the audio samples with a 17 bit accuracy fade coefficient, which is selected by an 8-bit fade counter. The fade coefficients range from 0 to 1.0 according to a ¼ cosine function. The attenuation for a particular fade count (FC) is given as follows:

$$\text{Attenuation (dB)} = -20 \log \cos\left(\frac{\pi \times FC}{510}\right) \text{(dB)} \quad \text{where: } 0 \leq FC \leq 255.$$

In encode mode, audio samples are taken from input SD1 and scaled before sub-band filter processing, and sent to output SD2.

In decode mode, audio samples are scaled following reconstruction by the sub-band filter, and sent to outputs SD1 and SD2.

Table 10 Fade processor operating modes.

MODE	FUNCTION
Fade rate	controls rate of automatic increments and decrements
Step down	increases attenuation by one increment
Step up	reduces attenuation by one increment
Full scale	sets gain to unity, incrementing from current level automatically
Mute	sets gain to zero, decrementing from current level automatically
–12 dB	sets gain to –12 dB, decrementing or incrementing from current level automatically

FADE PROCESSOR MODE CONTROL

The operating mode of the fade processor is controlled by two extended registers

Table 11 Fade processor mode control.

A3	A2	A1	A0	D3	D2	D1	D0	MODE
0	0	1	1	P3	P2	P1	P0	set fade rate
0	1	0	0	0	0	0	1	step down
0	1	0	0	0	0	1	0	step up
0	1	0	0	0	1	X	0	full scale slow
0	1	0	0	0	1	X	1	full scale fast
0	1	0	0	1	0	X	0	mute slow
0	1	0	0	1	0	X	1	mute fast
0	1	0	0	1	1	X	0	–12 dB slow
0	1	0	0	1	1	X	1	–12 dB fast
0	1	0	0	0	0	0	0	no action

FADE RATE OPTION

The fade rate can be set to either fast or slow modes. In fast mode the attenuation changes rate at one step per audio sample. In slow mode the rate of change of level is controlled by the fade rate bits P3 to P0. In slow mode, the fade counter is stepped up or down according to a clock derived from the WS pin.

Table 12 Fade rate in slow and fast modes.

MODE	P3	P2	P1	P0	TIME PER STEP (ms)			TIME FOR 256 STEPS (ms)		
					32 kHz	44.1 kHz	48 kHz	32 kHz	44.1 kHz	48 kHz
Fast	–	–	–	–	31.2 μs	22.7 μs	20.8 μs	8.0	5.8	5.3
Slow	0	0	0	0	1.0	0.997	1.0	256	255	256
Slow	0	0	0	1	2.0	1.994	2.0	512	511	512
Slow	0	0	1	1	4.0	3.988	4.0	1024	1021	1024
Slow	0	1	1	1	8.0	7.980	8.0	2048	2043	2048
Slow	1	1	1	1	16.0	15.96	16.0	4096	4087	4096

IEC 958 output

The IECOP pin provides an output signal in accordance with the IEC 958/SPDIF digital audio interface format.

The function of the IECOP pin is programmed by bit 3 of the codec extended settings register; see Table 13.

Table 13 IECOP pin control.

A3	A2	A1	A0	D3	D2	D1	D0	IECOP FUNCTION
0	0	0	1	0	X	X	X	IEC 958 (default)
0	0	0	1	1	X	X	X	I^2S word select for SD2

The IECOP output will only function when the SAA2003 is in decode mode. The IECOP cannot be used when SAA2013 is present in the system, unless the SAA2013 is in sleep mode. The IECOP output is disabled and set to high impedance by a reset.

L3 bus

The L3 bus is a three-wire clock synchronous data bus common to all ICs in the DCC chip-set. It consists of the L3MODE, L3CLK and L3DATA connections. The bus has two operating modes:

- Addressing mode; selects the IC for communication and sets type of transfer.
- Data mode; is used to send and receive data and control settings.

The L3MODE and L3CLK lines are driven by the system microcontroller and L3DATA is a bi-directional line. LTCNT0 and LTCNT1 must be left unconnected when L3 mode is used.

For normal use in L3 mode, LTCNT0 and LTCNT1 are held HIGH by internal pull-up resistors. The SAA2003 responds to serial addresses as shown in Table 14.

Table 14 SAA2003 serial addresses.

D0[1]	D1[1]	D2	D3	D4	D5	D6	D7
X	X	0	0	0	1	0	0

Note

1. D0 and D1 are interpreted as LTCNT0 and LTCNT1 respectively. These two signals control the operation of the interface as given in Table 15.

Table 15 Interface modes.

D0/LTCNT0	D1/LTCNT1	MODE
0	0	extended setting from microcontroller to SAA2003
1	0	allocation and scale factor information from SAA2013 to SAA2003
0	1	codec internal settings from microcontroller to SAA2003
1	1	codec status from SAA2003 to microcontroller and SAA2013 including peak level data

Table 16 Register address settings.

A3	A2	A1	A0	REGISTER(1)
0	0	0	0	codec external settings
0	0	0	1	codec interface mode control
0	0	1	0	serial audio interface mode control
0	0	1	1	fade counter rate control
0	1	0	0	fade counter control

Note

1. These registers are write only, accessed using the protocol shown in Fig.13.

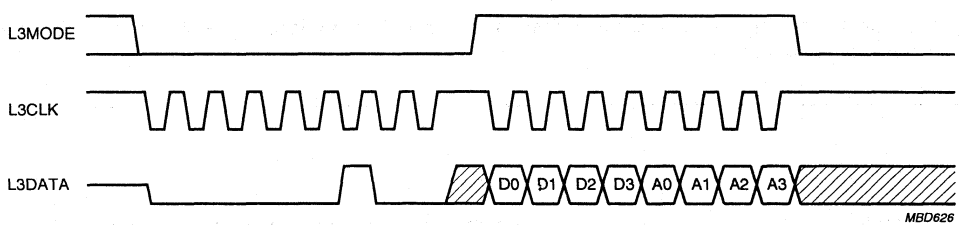


Fig.13 Extended settings protocol.

Operation in LT mode

LT interface mode can be selected by writing an extended settings word to the interface mode control register as shown in Table 17.

Table 17 Interface mode control register.

A3	A2	A1	A0	D3	D2	D1	D0	MODE
0	0	0	1	X	X	1	X	L3 mode (default)
0	0	0	1	X	X	0	X	LT mode

In LT mode the LTCNT0 and LTCNT1 pins are used, and the L3MODE pin becomes LTEN enable line. L3CLK becomes LTCLK, and L3DATA becomes LTDATA.

Table 18 Summary of address registers.

ADDRESS REGISTER		BIT	DESCRIPTION
REGISTER	EXPLANATION		
0	external settings register	0	mute DAC
		1	attenuate DAC
		2	de-emphasis DAC
		3	clock OK hold mode
1	codec extended settings	0	slave receive mode
		1	L3/LT mode select
		2	comparator delay bypass
		3	WS/IEC 958 selection
2	serial audio mode control	0	18 bit operation
		1	I^2S/EIAJ format
		2	peak detector input select
		3	transparent mode
3	fade processor fade rate	0 to 3	rate control, 0 to 15
4	fade processor control	0 to 3	fade command
5 to 15	not used	–	–

Codec internal settings and status

The settings register is write only, and the status register is read only. The interface protocols for accessing these registers is shown in Figs 14 and 15.

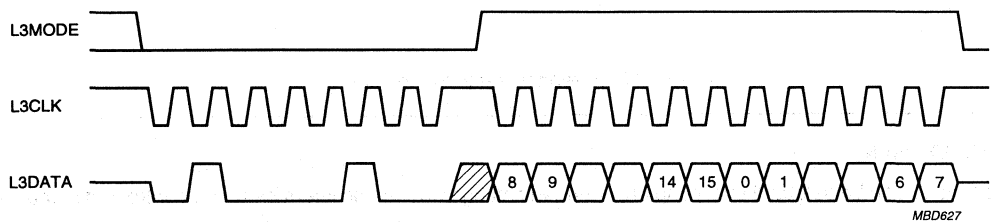


Fig.14 Codec internal settings write transfer.

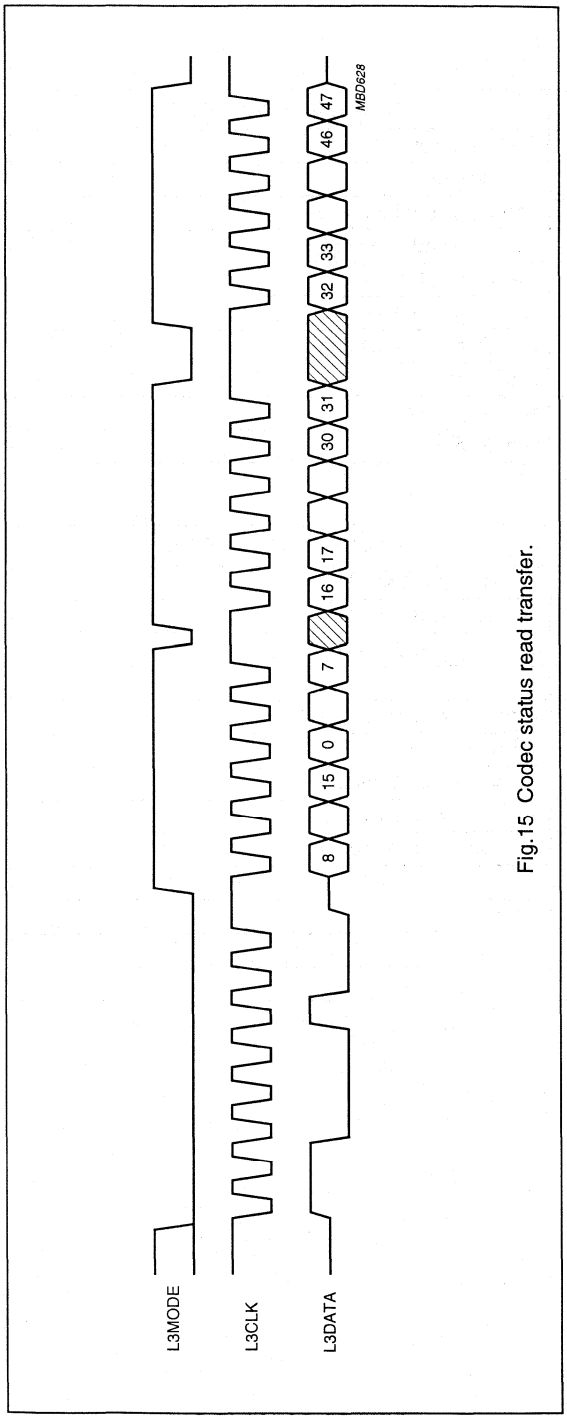


Fig.15 Codec status read transfer.

The codec internal settings register is shown in Table 19.

Table 19 Codec internal settings register formats.

BITS	DESCRIPTION	ENCODING/DECODING
15 to 12	bit rate index	encoding only
11 and 10	sample frequency	encoding only
9	decode mode	encoding and decoding
8	external FS256	encoding and decoding
7	2 channel mono	encoding only
6	mute sub-band filters	encoding and decoding
5	external master I^2S	encoding and decoding
4	select channel I/II	decoding only
3 and 2	transparent bits	encoding only
1 and 0	emphasis indication	encoding only

Table 20 Codec status register formats.

BITS	DESCRIPTION	ENCODING/DECODING
15 to 12	bit rate index	encoding and decoding
11 and 10	sample frequency	encoding and decoding
9	ready-to-receive	encoding and decoding
8	not used	–
7 and 6	sub-band mode	encoding and decoding
5	synchronization	decoding only
4	clock OK	encoding and decoding
3 and 2	transparent bits	encoding and decoding
1 and 0	emphasis indication	encoding and decoding
16	first channel identification	–
17 to 31	first channel peak level; LSB first	–
32	second channel identification	–
33 to 47	second channel peak level; LSB first	–

Average current consumption

The average current consumption is shown in Fig.16.

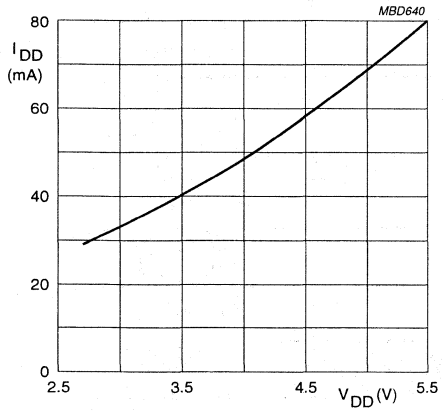


Fig.16 Average current consumption.

Timing diagrams

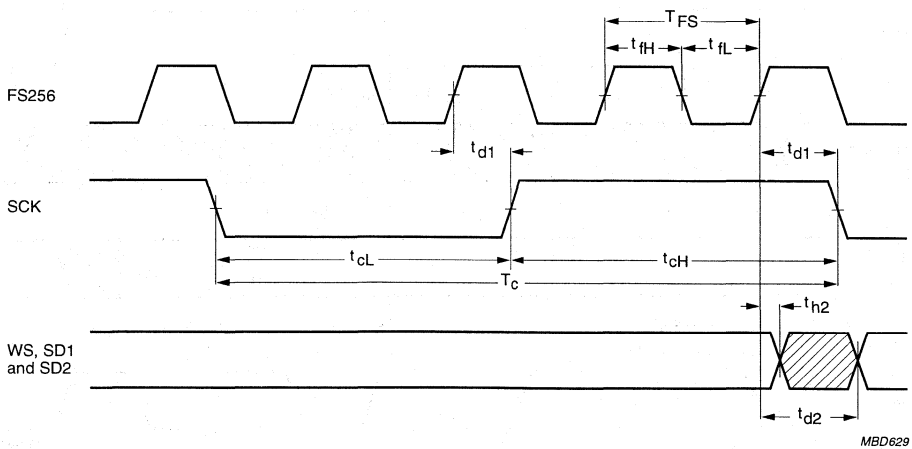


Fig.17 Serial audio interface timing in decode; master mode.

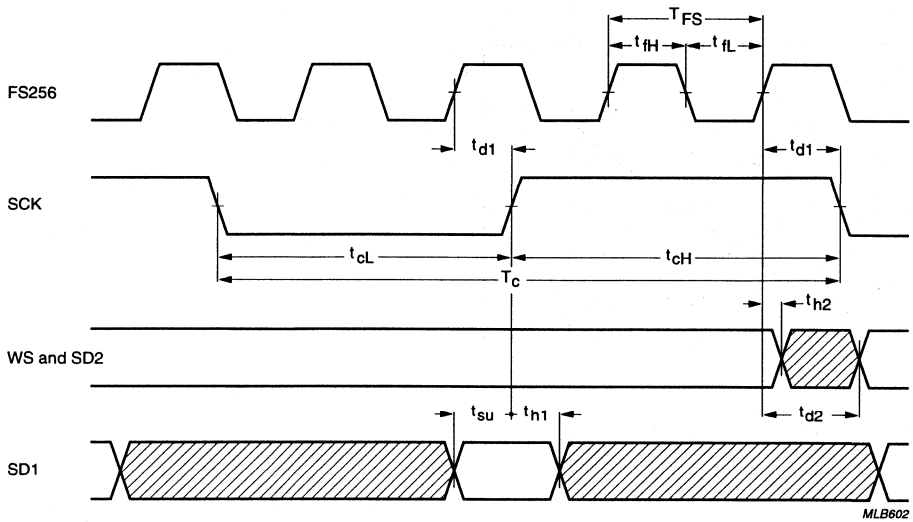


Fig.18 Serial audio interface timing in encode; master mode.

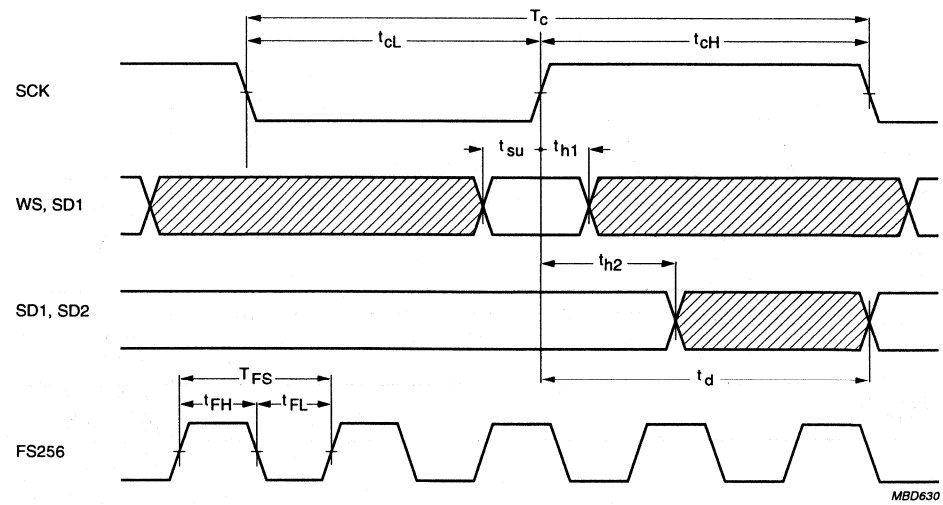


Fig.19 Serial audio interface timing; slave mode.

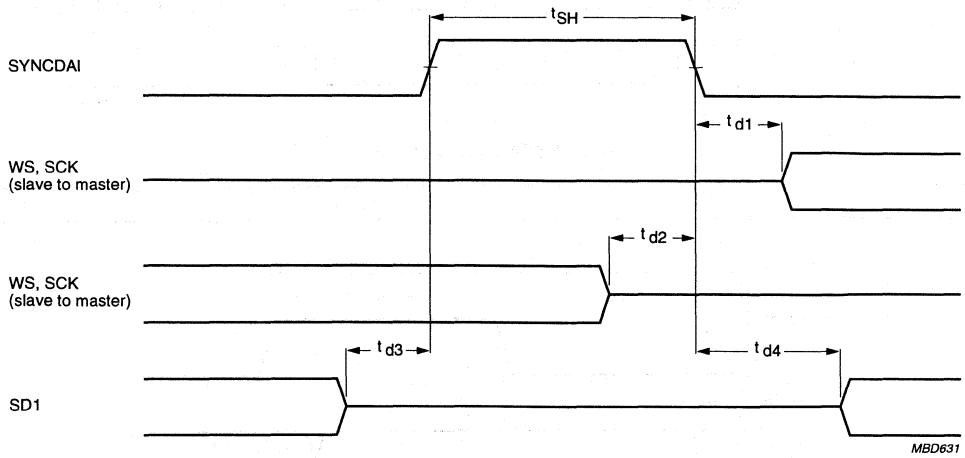


Fig.20 Serial audio master/slave timing.

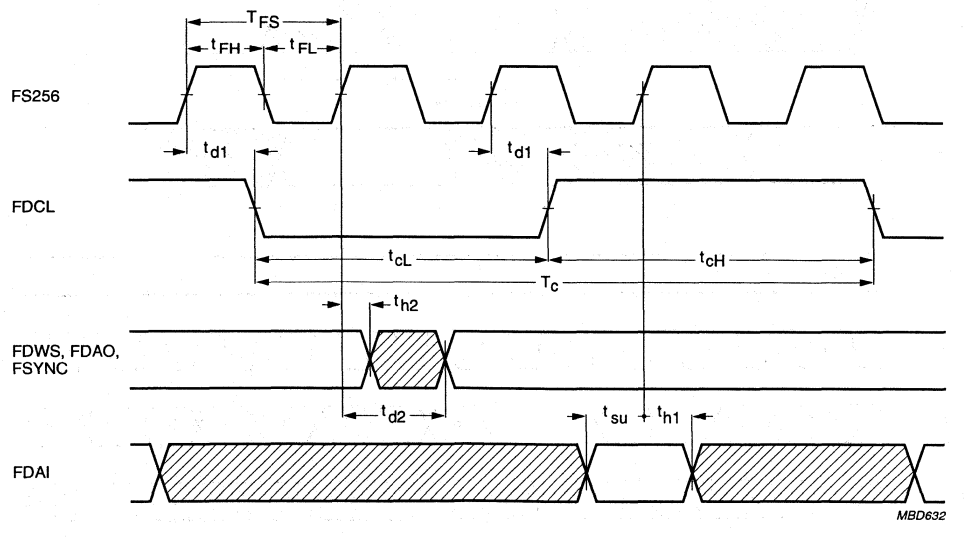


Fig.21 Filtered data interface timing.

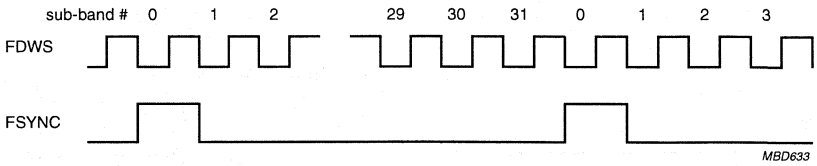


Fig.22 FSYNC output timing.

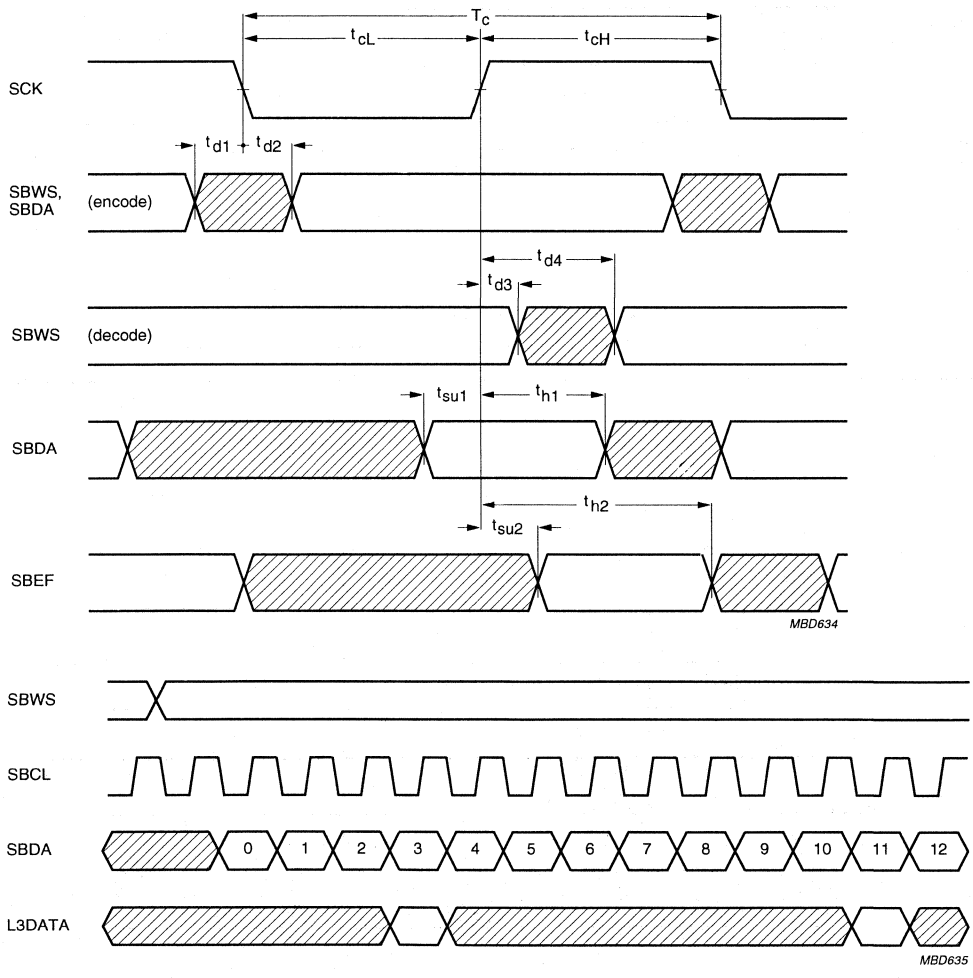


Fig.23 Sub-band PASC interface timing.

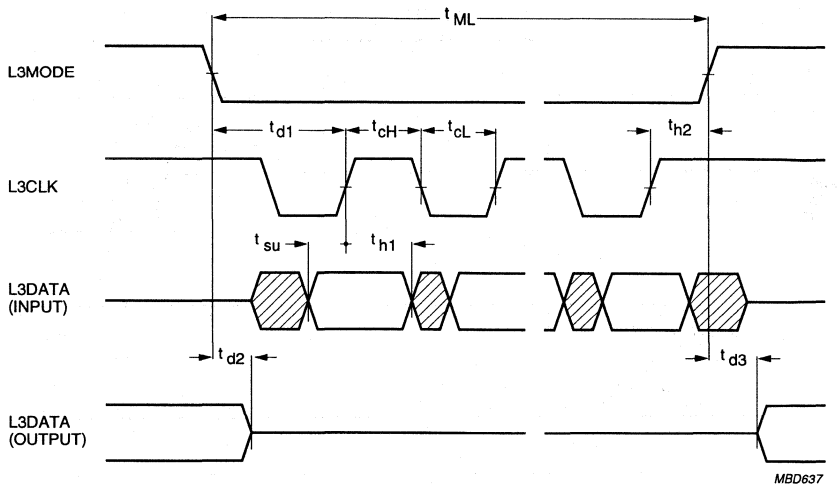


Fig.24 L3 bus timing; addressing mode.

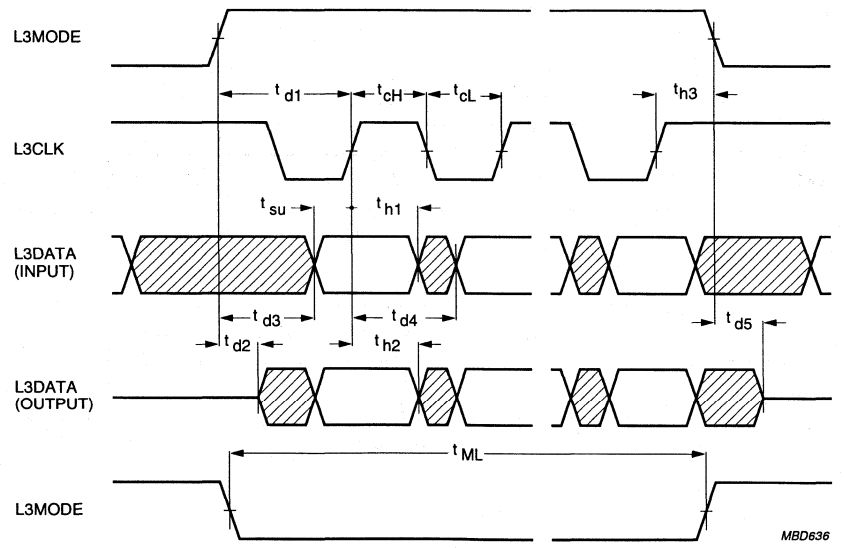


Fig.25 L3 bus timing; data transfer mode.

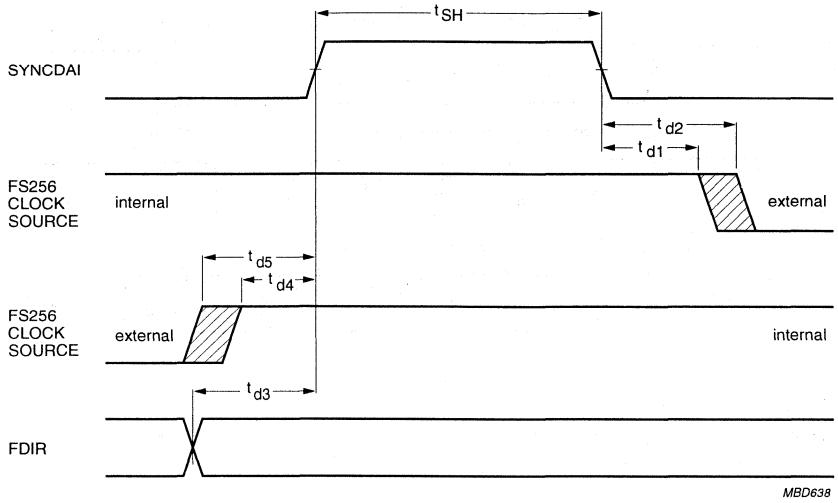


Fig.26 Internal/external clock source transition timing.

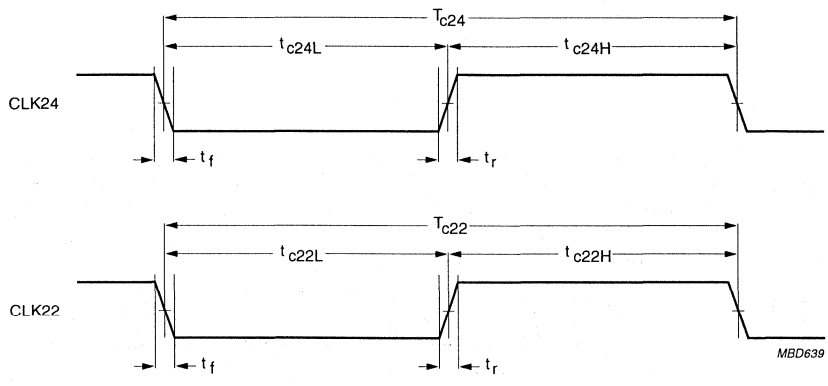


Fig.27 CLK22 and CLK24 timing.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+6.5	V
V_I	input voltage	note 1	−0.5	V_{DD} + 0.5	V
I_I	input current		−	20	mA
V_O	output voltage		−0.5	+6.5	V
I_O	output current		−	20	mA
I_{DDQ}	quiescent supply current	clocks stopped	−	100	µA
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{es1}	electrostatic handling	note 2	−2000	+2000	V
V_{es2}	electrostatic handling	note 3	−200	+200	V

Notes

1. The input voltage (V_I) may not exceed 6.5 V.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
3. Equivalent to discharging a 200 pF capacitor through a 2.5 µH inductor.

CHARACTERISTICS

T_{amb} = −40 to 85 °C; V_{DD} = 2.7 to 5.5 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.7	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 3.0 V	−	32.5	35.0	mA
		V_{DD} = 5.0 V	−	68.8	75.0	mA
		sleep mode; V_{DD} = 5.0 V	−	−	400	µA
Inputs FDAI, L3CLK, URDA, SBDIR, SBEF, X256, SLEEP and L3MODE						
V_{IL}	LOW level input voltage		0	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD}	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	−	+10	µA
C_I	input capacitance		−	−	10	pF
Inputs TEST0 and TEST1						
V_{IL}	LOW level input voltage		0	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD}	V
$R_{I(pd)}$	input pull-down resistance	$V_I = V_{DD}$	−	50	−	kΩ
C_I	input capacitance		−	−	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs LTCNT0 and LTCNT1						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
$R_{I(pu)}$	input pull-up resistance	V_I = 0 V	–	50	–	kΩ
C_I	input capacitance		–	–	10	pF
Input RESET						
V_{tLH}	threshold voltage LOW-to-HIGH		–	–	$0.8V_{DD}$	V
V_{tHL}	threshold voltage HIGH-to-LOW		$0.2V_{DD}$	–	–	V
V_{hys}	hysteresis voltage		–	$0.33V_{DD}$	–	V
C_I	input capacitance		–	–	10	pF
Outputs FDCL, FDWS, FDIR, FSYNC, FDAO, MUTEDAC, ATTDAC and DEEMDAC						
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	30	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 30 pF	–	–	20	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 30 pF	–	–	20	ns
Output CLK22						
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	30	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 30 pF	–	–	7	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 30 pF	–	–	7	ns
Output CLK24						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –6 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 50 pF	–	–	7	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 50 pF	–	–	7	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output SYNCDAI						
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	40	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 40 pF	–	–	20	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 40 pF	–	–	20	ns
Output FS256						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –6 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	60	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 60 pF	–	–	7	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 60 pF	–	–	7	ns
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
Output SD2						
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	30	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 30 pF	–	–	20	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 30 pF	–	–	20	ns
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
Output IECOP						
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 50 pF	–	–	20	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 50 pF	–	–	20	ns
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs/outputs SBDA, SBCL and SBWS						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
$R_{I(pd)}$	input pull-down resistance	$V_I = V_{DD}$	–	50	–	kΩ
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –4 mA	$V_{DD} - 0.4$	–	V_{DD}	V
C_L	load capacitance		–	–	30	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 30 pF	–	–	20	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 30 pF	–	–	20	ns
Inputs/outputs SD1, SCK and WS						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
$R_{I(pd)}$	input pull-down resistance	$V_I = V_{DD}$	–	50	–	kΩ
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –4 mA	$V_{DD} - 0.4$	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 50 pF	–	–	20	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 50 pF	–	–	20	ns
Input/output L3DATA						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –4 mA	$V_{DD} - 0.4$	–	V_{DD}	V
C_L	load capacitance		–	–	60	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 60 pF	–	–	20	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 60 pF	–	–	20	ns
Input X22IN (external clock)						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current		–10	–	+10	μA
C_I	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output X22OUT						
f_{xtal}	crystal frequency	note 1	–	22.5792	–	MHz
g_m	transconductance		1.5	–	–	mS
G_v	small signal voltage gain	$G_v = g_m \times R_O$	3.5	–	–	
C_{fb}	feedback capacitance		–	–	5	pF
C_O	output capacitance		–	–	10	pF
Input X24IN (external clock)						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current		–10	–	+10	μA
C_I	input capacitance		–	–	10	pF
Output X24OUT						
f_{xtal}	crystal frequency	note 1	–	24.567	–	MHz
g_m	transconductance		1.5	–	–	mS
G_v	small signal voltage gain	$G_v = g_m \times R_O$	3.5	–	–	
C_{fb}	feedback capacitance		–	–	5	pF
C_O	output capacitance		–	–	10	pF
Input X256						
f_i	input frequency	f_s = 48 kHz	–	12.288	–	MHz
		f_s = 44.1 kHz	–	11.2896	–	MHz
		f_s = 32 kHz	–	8.192	–	MHz
t_{cH}	HIGH time		35	–	–	ns
t_{cL}	LOW time		35	–	–	ns
CLK22 and CLK24 timing; Fig.27						
OUTPUT CLK24						
f_o	output frequency	C_L = 50 pF	–	24.576	–	MHz
t_{c24H}	HIGH time	C_L = 50 pF	12	–	–	ns
t_{c24L}	LOW time	C_L = 50 pF	12	–	–	ns
t_r	rise time	C_L = 50 pF	–	–	7	ns
t_f	fall time	C_L = 50 pF	–	–	7	ns
OUTPUT CLK22						
f_o	output frequency	C_L = 30 pF	–	22.5792	–	MHz
t_{c22H}	HIGH time	C_L = 30 pF	11	–	–	ns
t_{c22L}	LOW time	C_L = 30 pF	11	–	–	ns
t_r	rise time	C_L = 30 pF	–	–	7	ns
t_f	fall time	C_L = 30 pF	–	–	7	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drive processing interface timing; see Fig.23						
t_{cy}	SCK cycle time		–	1302	–	ns
t_{cH}	SCK HIGH time		460	651	–	ns
t_{cL}	SCK LOW time		460	651	–	ns
t_{d1}	SBWS and SBDA delay time until SCK LOW		20	–	–	ns
t_{d2}	SCK delay time until SBWS and SBDA valid		–	–	20	ns
t_{su1}	SBDA input set-up time before SCK HIGH		235	–	–	ns
t_{h1}	SBDA input hold time after SCK HIGH		30	–	–	ns
t_{su2}	set-up time from SCK HIGH until SBEF valid		–	–	90	ns
t_{h2}	SBEF input hold time after SCK HIGH		380	–	–	ns
Filtered data interface timing; see Fig.21						
FDCL, FDWS, FDAI AND FDAO						
f_{256}	FS256 frequency	f_s = 48 kHz	–	12.288	–	MHz
		f_s = 44.1 kHz	–	11.2896	–	MHz
		f_s = 32 kHz	–	8.192	–	MHz
T_c	FDCL cycle time	f_s = 48 kHz	–	325.6	–	ns
t_{FH}	FS256 HIGH time	f_s = 48 kHz; note 2	35	–	–	ns
		f_s = 44.1 kHz; note 2	38	–	–	ns
		f_s = 32 kHz; note 2	75	–	–	ns
t_{FL}	FS256 LOW time	f_s = 48 kHz; note 2	35	–	–	ns
		f_s = 44.1 kHz; note 2	38	–	–	ns
		f_s = 32 kHz; note 2	35	–	–	ns
t_{d1}	FS256 delay time until FDCL transition		0	–	50	ns
t_{cH}	FDCL HIGH time	f_s = 48 kHz	143	–	–	ns
t_{cL}	FDCL LOW time	f_s = 48 kHz	143	–	–	ns
t_{h2}	FDWS, FDAO and FSYNC hold time after FS256 HIGH		0	–	–	ns
t_{d2}	FS256 HIGH delay time until FDWS, FDAO and FSYNC valid		0	–	50	ns
t_{su}	FDAI input set-up time before FS256 HIGH		20	–	–	ns
t_{h1}	FDAI input hold time after FS256 HIGH		30	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing characteristics FDIR and SYNCDAI; see Fig.26						
t_{sH}	SYNCDAI HIGH time		1280	–	–	ns
t_{d1}	internal clock delay time after SYNCDAI LOW		0	–	–	ns
t_{d2}	external clock delay time after SYNCDAI LOW		–	–	320	ns
t_{d3}	FDIR delay time before SYNCDAI HIGH		280	–	–	ns
t_{d4}	external clock delay time before SYNCDAI HIGH		–	–	320	ns
t_{d5}	internal clock delay time before SYNCDAI HIGH		0	–	–	ns
Baseband data interface timing characteristics						
MASTER MODE; SEE FIGS 17 AND 18						
T_c	SCK cycle time	f_s = 48 kHz	–	325.6	–	ns
t_{cH}	SCK HIGH time	f_s = 48 kHz	143	–	–	ns
t_{cL}	SCK LOW time	f_s = 48 kHz	143	–	–	ns
t_{d1}	FS256 HIGH delay time until SCK transition		0	–	50	ns
t_{h2}	WS, SD1 and SD2 hold time after FS256 HIGH		0	–	–	ns
t_{d2}	FS256 delay time until WS, SD1 and SD2 valid		0	–	50	ns
t_{su}	SD1 input set-up time before SCK HIGH		30	–	–	ns
t_{h1}	SD1 input hold time after SCK HIGH		0	–	–	ns
SLAVE MODE; SEE FIG.19						
T_c	SCK cycle time	f_s = 48 kHz	325.6	–	651.2	ns
t_{cH}	SCK HIGH time	f_s = 48 kHz	116	–	–	ns
t_{cL}	SCK LOW time	f_s = 48 kHz	116	–	–	ns
t_{su}	WS and SD1 inputs set-up time before SCK HIGH		30	–	–	ns
t_{h1}	WS and SD1 inputs hold time after SCK HIGH		0	–	–	ns
t_{h2}	SD1 and SD2 outputs hold time after SCK HIGH		66	–	–	ns
t_d	SCK delay time until SD1 and SD2 outputs valid		–	–	223	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing characteristics master/slave mode transition; see Fig.20						
t_{sH}	SYNCDAI HIGH time		1280	–	–	ns
t_{d1}	WS and SCK outputs enabled after SYNCDAI LOW		140	–	–	ns
t_{d2}	WS and SCK outputs disabled before SYNCDAI LOW		140	–	–	ns
t_{d3}	SD1 output disabled before SYNCDAI HIGH		250	–	–	ns
t_{d4}	SD1 output enabled after SYNCDAI LOW		790	–	–	ns
Timing L3 interface; see Fig.24						
ADDRESSING MODE						
t_{cH}	L3CLK HIGH time		210	–	–	ns
t_{cL}	L3CLK LOW time		210	–	–	ns
t_{d1}	L3MODE LOW delay time until L3CLK HIGH		190	–	–	ns
t_{su}	L3DATA input set-up time before L3CLK HIGH		190	–	–	ns
t_{h1}	L3DATA input hold time after L3CLK HIGH		30	–	–	ns
t_{h2}	L3CLK HIGH hold time before L3MODE HIGH		190	–	–	ns
t_{d2}	L3MODE LOW delay time until L3DATA disabled		0	–	50	ns
t_{d3}	L3MODE HIGH delay time until L3DATA enabled		0	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DATA MODE; SEE FIG.25						
t_{cH}	L3CLK HIGH time		210	–	–	ns
t_{cL}	L3CLK LOW time		210	–	–	ns
t_{d1}	L3MODE delay time until L3CLK HIGH		190	–	–	ns
t_{d2}	L3MODE delay time until L3DATA enabled		0	–	50	ns
t_{d3}	L3MODE delay time until L3DATA valid		–	–	380	ns
t_{su}	L3DATA set-up time before L3CLK HIGH		190	–	–	ns
t_{h1}	L3DATA input hold time after L3CLK HIGH		30	–	–	ns
t_{h2}	L3DATA output hold time after L3CLK HIGH		120	–	–	ns
t_{d4}	L3CLK delay time until L3DATA output valid	not between data bits 7 and 8	–	–	360	ns
		between data bits 7 and 8	–	–	530	ns
t_{h3}	L3CLK HIGH hold time before L3MODE LOW		190	–	–	ns
t_{d5}	L3MODE LOW delay time until L3DATA output disabled		0	–	50	ns
t_{ML}	L3MODE LOW time	between data words	190	–	–	ns

Notes

1. The crystal frequencies 22.5792 MHz $\pm 200 \times 10^{-6}$ MHz and 24.5760 MHz $\pm 200 \times 10^{-6}$ MHz must track each other in frequency with an accuracy of 200×10^{-6} MHz. For example if the 24.5760 MHz clock is 150×10^{-6} MHz fast, then the range of the 22.5792 MHz clock becomes -50×10^{-6} MHz and $+350 \times 10^{-6}$ MHz
2. Timing values only valid for internally generated FS256.

Adaptive allocation and scaling for record processing in DCC systems

SAA2012

FEATURES

- Stereo or 2-channel mono encoding
- Status may be read continuously
- Microcontroller interface
- I^2S interfaces
- Allocation algorithm including optional emphasis correction (for 44.1 kHz)
- Reduced power consumption
- 4 V nominal operating voltage capability.

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

Performing the Adaptive Allocation and Scaling function in the Precision Adaptive Sub-band Coding (PASC) system, the SAA2012 is intended for use in conjunction with the stereo filter and codec (SAA2002).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2012GP	44	QFP; note 1	plastic	SOT205AG

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the "*Quality Reference Pocketbook*" are followed. The pocketbook can be ordered using the code 9398 510 34011.

BLOCK DIAGRAM

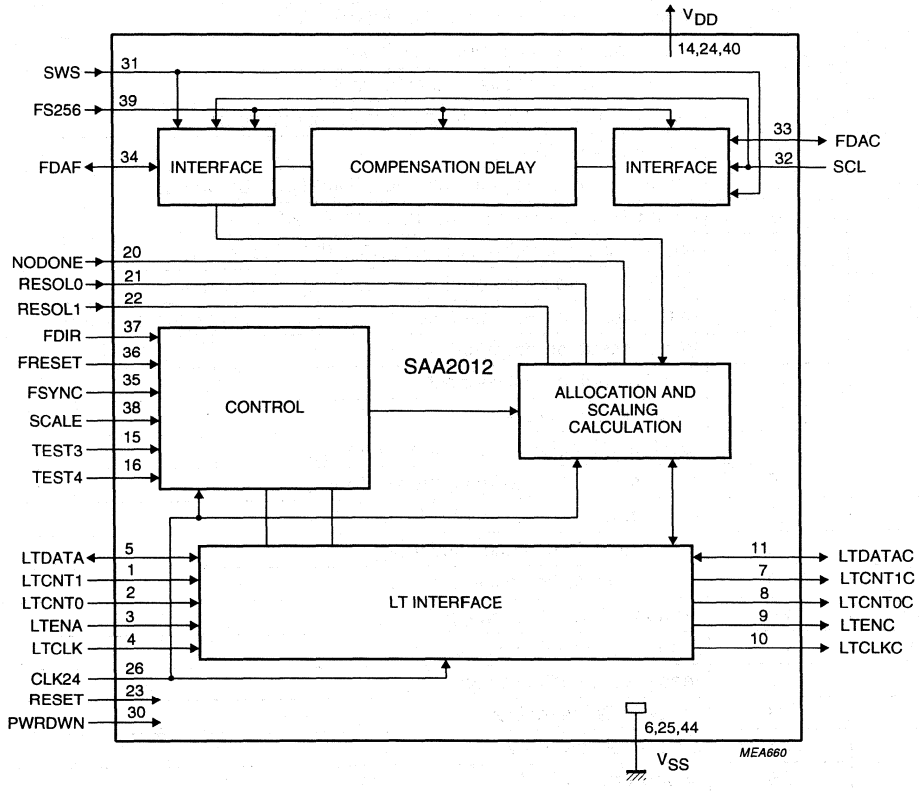


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LTCNT1	1	mode control 1, microcontroller interface input
LTCNT0	2	mode control 0, microcontroller interface input
LTENA	3	enable microcontroller interface input
LTCLK	4	bit clock microcontroller interface input
LTDATA	5	data, microcontroller interface (3-state input/output)
V_{SS}	6	supply ground (0 V)
LTCNT1C	7	control 1, microcomputer interface, SAA2002 side output
LTCNT0C	8	control 0, microcomputer interface, SAA2002 side output
LTENC	9	enable microcontroller interface, SAA2002 side output
LTCLKC	10	bit clock; microcontroller interface, SAA2002 side output
LTDATAC	11	data; microcontroller interface, SAA2002 side (3-state input/output)
TEST1	12	test 1 output; do not connect
TEST2	13	test 2 output; do not connect
V_{DD}	14	supply voltage (+5 V)
TEST3	15	test 3 mode input; to be connected to V_{DD}
TEST4	16	test 4 mode input; to be connected to V_{DD}
TEST5	17	test 5 input; to be connected to V_{SS}
TEST6	18	test 6 input; to be connected to V_{SS}
TEST7	19	test 7 input; to be connected to V_{SS}
NODONE	20	no done state selection input
RESOL0	21	resolution selection 0 input
RESOL1	22	resolution selection 1 input
RESET	23	active HIGH reset input
V_{DD}	24	supply voltage (+5 V)
V_{SS}	25	supply ground (0 V)
CLK24	26	24.576 MHz processing clock input
TEST8	27	test 8 input; to be connected to V_{SS}
TEST9	28	test 9 input; to be connected to V_{SS}
TEST10	29	test 10 input; to be connected to V_{SS}
PWRDWN	30	SLEEP mode input
SWS	31	word selection input; filtered - I^2S-interface
SCL	32	bit clock input; filtered - I^2S-interface
FDAC	33	filtered data - I^2S-interface; SAA2002 side (3-state input/output)
FDAF	34	filtered data - I^2S-interface; SAA2002 side (3-state input/output)
FSYNC	35	sub-band synchronization on input; filtered - I^2S-interface
FRESET	36	reset signal input from SAA2002
FDIR	37	direction input of the I^2S-interface
SCALE	38	scale factor index select (note 1)
FS256	39	system clock input; sample frequency × 256
V_{DD}	40	supply voltage (+5 V)

SYMBOL	PIN	DESCRIPTION
n.c.	41	not connected
n.c.	42	not connected
n.c.	43	not connected
V_{SS}	44	supply ground (0 V)

Note

1. The SCALE input must be set LOW for use with the SAA2002. If operation with the SAA2001/2021 combination is required the SCALE input must be set HIGH.

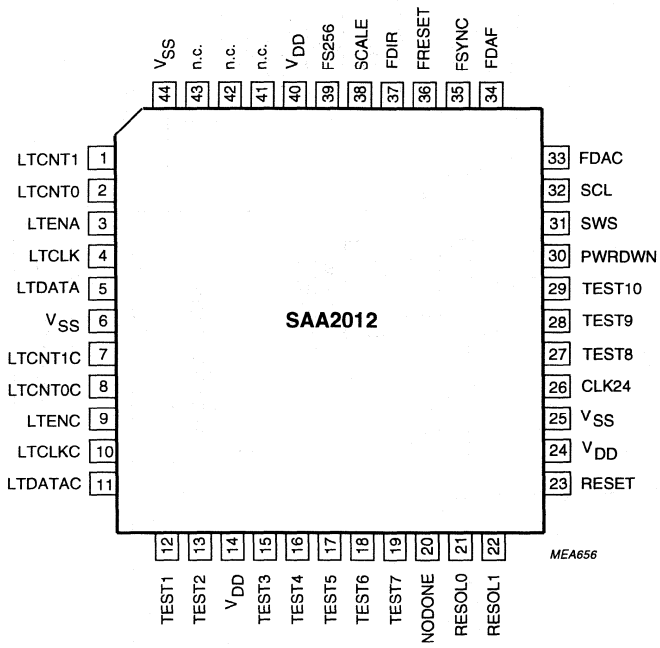


Fig.2 Pin configuration.

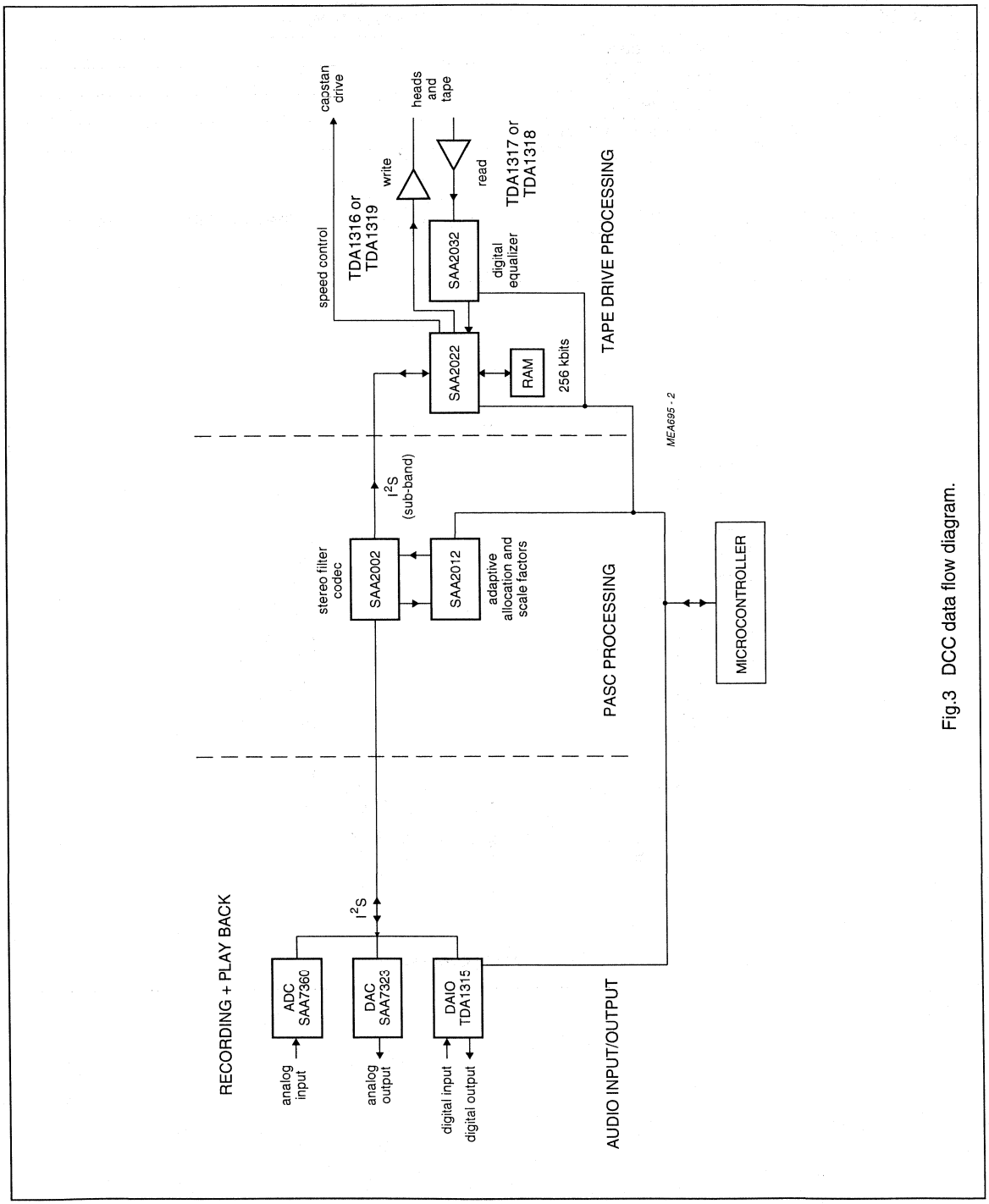


Fig.3 DCC data flow diagram.

FUNCTIONAL DESCRIPTION

PASC

Precision Adaptive Sub-band Coding achieves highly efficient digital encoding with a bit-rate of 384 kbits/s. It utilizes a system producing sub-band samples from an incoming digital audio signal. This relies upon the audibility of signals above a given level and upon high amplitude signals masking those of lower amplitude. Although each sub-band signal is of approximately 750 Hz bandwidth, it possesses considerable overlap with those adjacent to it.

During the process of encoding, the PASC processor analyses the broadband audio signal at sampling frequency (f_s) by splitting it into 32 sub-band signals at a sampling frequency ($f_s/32$).

The PASC signal consists of frames conveying the information corresponding to 384 sub-band samples. These also include a synchronization pattern identifying the start of each new frame. The allocation information for the 32 sub-bands is transferred as 4-bit values. If the amplitude of a sub-band signal is below the masking threshold it will be omitted from the PASC signal.

The duration of a PASC frame depends upon sampling frequency and is adjusted to 384 divided by f_s.

Adaptive Allocation and Scaling

The PASC system calculates the masking power of the sub-band signals and adds the masking threshold. Sub-band signals with power below this threshold denote information to be discarded. Non-masked signals are coded using floating point notation in which a mantissa corresponds in length to the difference between peak power and masking threshold. The process is repeated for every PASC frame and is known as the Adaptive Allocation of the available capacity.

Encoding mode

Signal FDIR sets the data flow direction on the Filtered-I²S-interface. In the encoding mode (FDIR = LOW) the device will accept samples from FDAF. These will be delayed by a number of sample periods depending upon the setting of the SCALE input. In the event of operation with the SAA2002 (SCALE = 0) this delay will be 480 SWS periods. This will ensure alignment of the data with the computed allocations.

After the delay the samples will be presented on FDAC (pin 33). The circuit also performs all the calculations required to build the allocation table which is used in the codec (SAA2002).

When used with the SAA2002 the calculated scale factor indices are sent via the LT interface. These operations are performed for every frame of the sub-band codec.

In order to synchronize with the codec and utilize the correct tables for the calculations the SAA2012 frequently requests the status of the codec. It monitors the bit-rate, sample frequency, operation mode and the emphasis information and uses the 'ready-to-receive' bit of the codec to determine the moment of the transfer of allocation information.

Decoding Mode

In the decoding mode (FDIR = HIGH) the SAA2012 will take samples from FDAC which will be presented on the FDAF after a delay of 160 SWS periods. The LT interface between microcontroller and codec (SAA2002) will only be affected by the 'ready-to-receive' bit from the codec (SAA2002).

Microcontroller Interface Operation

Information on the interface between microcontroller and codec (SAA2002) will flow in a regular sequence synchronized with the codec (SAA2002):

- With every FSYNC the SAA2012 will read the status of the codec (SAA2002).
- Following the calculation of the allocation and scale factors the SAA2012 will send the first allocation information unit (16-bits). It will then continuously read the codec (SAA2012) status to ascertain when it is able to receive further allocation information units. When the transfer of these units is complete the SAA2012 will send settings and (for SCALE = 0) scale factor indices.
- The extended settings will be sent to the codec as soon as possible after reception from the microcontroller.

The microcontroller communicates with the SAA2012 in a similar fashion:

- Status can be read continuously. The SAA2012 will output a copy of the codec (SAA2002) status on the LTDATA line except for the 'ready-to-receive' bits which are generated by the SAA2012. These indicate whether the SAA2012 is ready to receive the next settings or extended settings.
- Settings can be sent following every occasion that the 'ready-to-receive' bit 'S' changes to logic 1.
- Extended settings can be sent following each occasion that the 'ready-to-receive' bit 'E' changes to logic 1.

Mode Control

Operation is controlled by the FRESET and FDIR signals. FRESET causes a general reset. The FDIR signal is sampled at the falling edge of the FRESET signal to determine the operation mode:

- FDIR = logic 1 decoding mode, SAA2012 in feed-through mode
- FDIR = logic 0 encoding mode, SAA2012 in calculation mode.

Figure 4 shows the timing diagram for FRESET and FDIR.

Resolution Selection

The (SAA2012) is designed for operation with input devices (ADCs) which may possess a different sample resolution capability, i.e. audio sample inputs into the sub-band filters. RESOL0 (pin 21) and RESOL1 (pin 22) may be utilized to adjust the allocation information calculation to the resolution of the samples.

With the instance of NODONE (pin 20) being HIGH, all available bits in the bit-pool will be allocated. If NODONE is LOW, no bits will be allocated to the sub-bands with energy levels below the theoretical threshold for the selected resolution. For encoding in accordance with the DCC standard NODONE must be HIGH.

Table 1 Resolution selection.

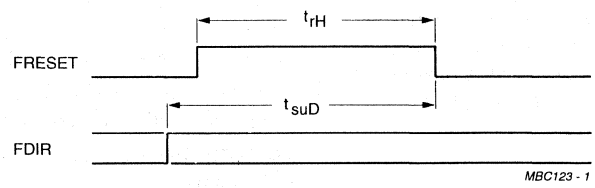
RESOL1	RESOL0	RESOLUTION
0	0	16 bits
0	1	18 bits
1	0	14 bits
1	1	15 bits

Sleep mode switching

When the potential on the RESET pin (pin 23) is held HIGH for at least $5T_{clk24}$ clock periods, the device will be reset after which it will operate in its decoding mode.

The sleep mode is activated when the PWRDWN pin (pin 30) is held HIGH. The 3-state buffers will be set to a high impedance while the normal outputs will retain the state attained prior to this mode being entered. This mode can only be used if other associated circuits react accordingly. The sleep mode is de-activated by a reset action.

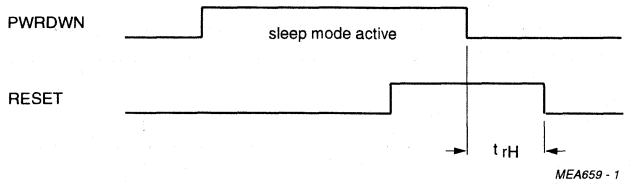
Operation for the sleep mode switching is shown in Fig.5.



$t_{rH} > 5T_{clk24}$ = 210 ns (for CLK = 24.576 MHz) minimum time; FRESET = HIGH.

$t_{suD} < 0$ ns minimum set-up time; FDIR to FRESET = LOW.

Fig.4 Timing of FRESET and FDIR.



$t_{rH} > 5T_{clk24}$ = 210 ns (for CLK = 24.576 MHz) minimum time; RESET = HIGH.

Fig.5 Sleep mode switching.

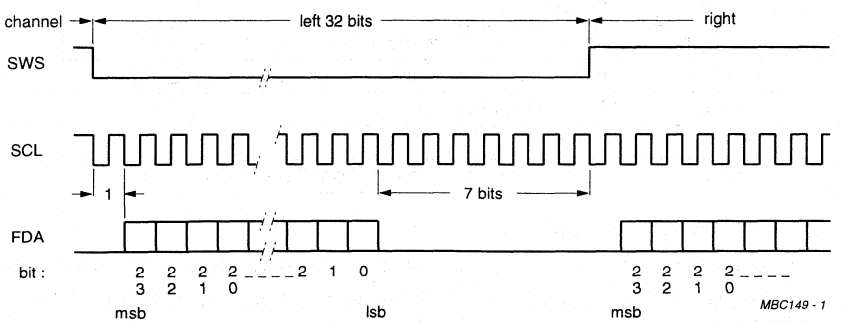


Fig.6 Format for transferring filtered data.

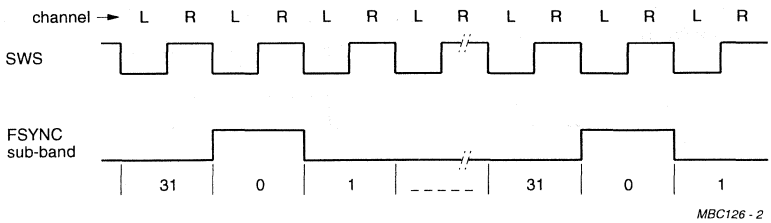


Fig.7 FSYNC relative to SWS.

Filtered-I²S-Interfaces

Interfaces with the sub-band filter and codec (SAA2002) consist of the signals shown in Table 2.

Table 2 The filtered-I²S-interface.

SIGNAL	TYPE	DESCRIPTION	FREQUENCY
SWS	input	word selection	f_s
SCL	input	bit clock	$64f_s$
FDAF	bi-directional	filtered data to/from the filter section of SAA2002	–
FDAC	bi-directional	filtered data to/from the codec section of SAA2002	–
FSYNC	input	filter synchronization	$f_s/32$
FRESET	input	reset	–
FDIR	input	filtered - I²S-interface direction of data flow	–

The format for transferring filtered data is shown in Fig.6.

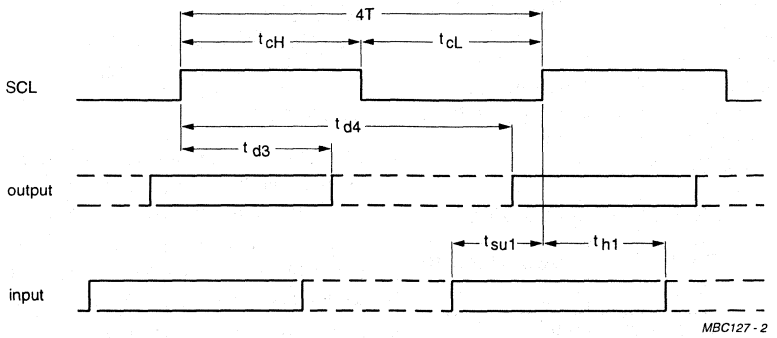
Input frequency (f_i) must be provided as system clock. This frequency is used by the interfaces with the SAA2002.

The frequency of the SWS signal (pin 31) is equal to the sample frequency (f_s). Bit clock SCL (pin 32) is 64 times f_s; thus each SWS period contains 64 data bits, 48 of which are actually used in data transfer. The half period when SWS is logic 0 is used to transfer left-channel information, when SWS is logic 1 transfer of right-channel data is allowed.

The 24-bit samples are transferred with the most significant bit first. This bit is transferred during the bit clock period, one bit time after the change in SWS.

FSYNC signal is provided for the purposes of synchronization and indicates the portion of the SWS period during which the samples of sub-band 0 are transferred.

The relationship between FSYNC and the SWS is logic 0 data transfer period is shown in Fig.7



OUTPUT applies to FDAF and FDAC in the output mode.

INPUT applies to FDAF and FDAC in the input mode, SWS and FSYNC.

T = 1 f_s 256 cycle time.

$t_{Hc} \geq T + 35$ ns minimum HIGH time SCL.

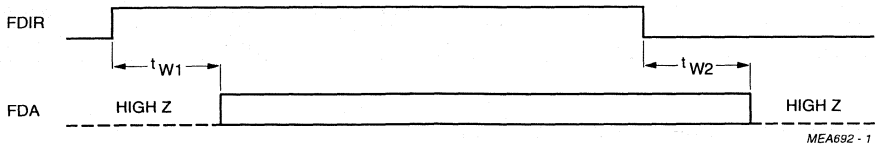
$t_{Lc} \geq T + 35$ ns minimum LOW time SCL.

$t_{d3} \geq 2T - 10$ ns hold time output after SCL HIGH.

$t_{d4} \leq 3T + 60$ ns delay time output after SCL HIGH.

$t_{su1} \geq 20$ ns set-up time input before SCL HIGH.

$t_{h1} \geq T + 35$ ns hold time input after SCL HIGH.



$t_{W1} \geq 3T$ minimum time high impedance to FDA enabled.

$t_{W2} \geq 2T + 35$ ns maximum time FDA enabled to high impedance.

Fig.8 Filtered-I²S interface timing.

Microcontroller Interface

Two microcontroller interfaces are provided; one for connection to the microcontroller interface of the SAA2002, the other to connect to the system controller. Information is conveyed via the SAA2012 which executes monitoring and extracts signals (e.g. settings and synchronization) essential to its operation. It also sends allocation information to the SAA2002. However, the SAA2012 does not monitor the external settings bits from the microcontroller (see "Extended settings (LTCNT1(C) = LTCNT0(C) = logic 0)").

Table 3 SAA2012 Interface with microcontroller.

SIGNAL	TYPE	DESCRIPTION
LTCLK	input	bit clock
LTDATA	bi-directional	data
LTCNT0	input	control line 0
LTCNT1	input	control line 1
LTENA	input	enable

The SAA2012 is a slave on this interface which is active only when the enable signal LTENA (pin 3) is logic 1. This allows connection of this interface to other devices. Only the enable signal is not common to all devices.

Table 4 SAA2012 Interface with SAA2002.

SIGNAL	TYPE	DESCRIPTION
LTCLK	output	bit clock
LTDATAC	bi-directional	data
LTCNT0C	output	control line 0
LTCNT1C	output	control line 1
LTENC	output	enable

The SAA2012 is master on this interface and provides all signals with the exception of the data in the instance of status transfer from SAA2002 to SAA2012.

Information conveyed via these interfaces is transferred in 8 or 16-bit serial units with the type of information designated by the control lines LTCNT1C and LTCNT0C.

A transfer of information begins when the master sets the control lines for the required action. It then sets the LTENA/C line to logic 1. Once this signal is established the slave determines the kind of action required and prepares for the transfer of data.

When the master supplies the LTCLK/C signals, data is transferred either to or from the slave in units of 8-bits; the least significant bit (LSB) is always transferred first. A transfer of 16-bits is made in two, 8-bit units with the most significant 8-bit (MSB) unit first. In between the two 8-bit units the LTENA/C signals remain logic 1.

An example of information transfer via SAA2012 interfaces is shown in Fig.9.

Table 5 SAA2012 interface control lines functions.

LTCNT1(C)	LTCNT0(C)	MODE	FROM	TO	TRANSFER OF
0	0	extended settings	microcontroller	SAA2002	8 bits
0	1	allocation; note 1	SAA2012	SAA2002	16/48 × 16 bits
1	0	settings	microcontroller	SAA2002	16 bits
1	1	status	codec	microcontroller	8 or 16 bits

Note

1. This mode only on the interface between SAA2012 and SAA2002.
   If SCALE = logic 1 then 16 × 16-bits.
   If SCALE = logic 0 then 48 × 16-bits.

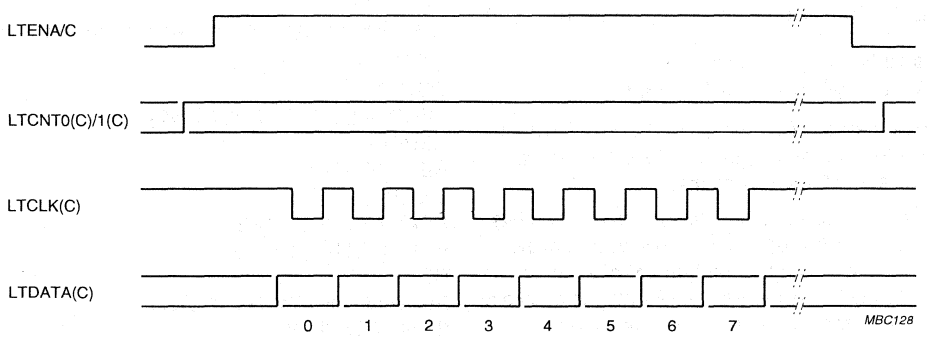
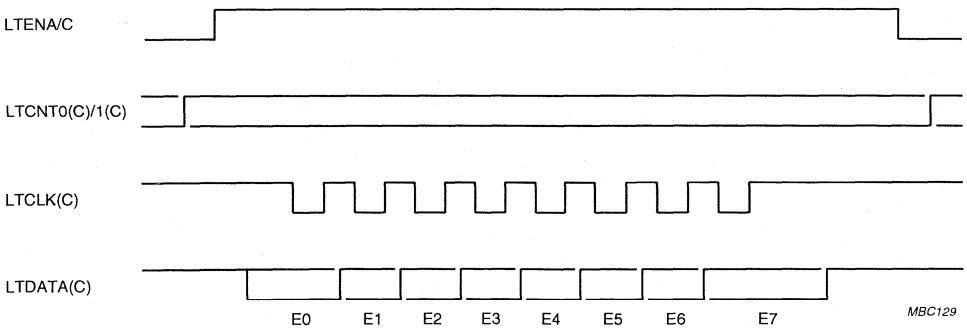


Fig.9 Example of information transfer via SAA2012 interfaces.



Refer to the SAA2002 description for the meaning of these bits as they pass SAA2012 unchanged.

Fig.10 Extended settings LTCNT1(C) and LTCNT0(C).

Extended settings (LTCNT1(C) = LTCNT0(C) = logic 0)

Eight information bits, generated by the microcontroller, are transferred in this mode. The SAA2012 will transfer these bits to the SAA2002 as soon as possible but does not monitor this information.

The relationship of the extended settings is shown in Fig.10.

Allocation and SCALING information (LTCNT1(C) = logic 0, LTCNT0(C) = logic 1)

In the encoding mode (FDIR = logic 0) the SAA2012 will transfer allocation information to the SAA2002. This will occur once for every SAA2002 frame.

The information will consist of 16 transfers each of 16-bits. To synchronize the SAA2012 operation with that of the SAA2002, following the first 16-bit transfer of allocation data the SAA2012 checks the SAA2002 status to ensure it is ready to receive the remainder of the allocation information. Transfer of allocation data is completed by sending settings. Between 16-bit transfers the LTENC line returns to logic 0 as shown in Fig.11.

The order in which the bits occur on the interface during allocation information transfer is shown in Fig.12.

The 4-bit sub-band allocation unit contains the number of bits allocated to the sub-band minus 1. A value of 0000 indicates no bits allocated to that sub-band.

With stereo encoding, left and right channels are designated **L** and **R**. This changes to channels I or II for 2-channel mono mode. If SCALE = logic 0 the transfer of allocation information will be followed by the transfer of scale factors. Each 16-bit transfer contains two scale factor indices.

The following algorithm shows the process of information transfer:

```
COUNT = 0
SEND ALLOCATION (COUNT)
REPEAT
READ STATUS
UNTIL
READY-TO-RECEIVE
FOR COUNT = 1 to 15
DO
SEND ALLOCATION (COUNT)
SEND SETTINGS
IF SCALE = 0
THEN
FOR COUNT = 0 to 31
DO
SEND SCALE FACTORS (COUNT)
```

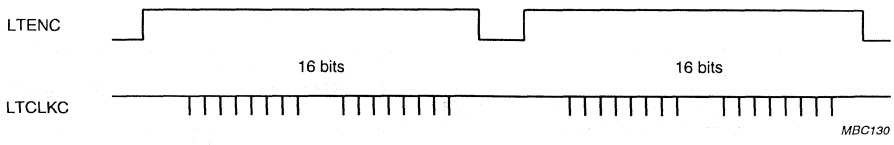


Fig.11 LTENC behaviour for 16-bit transfers.

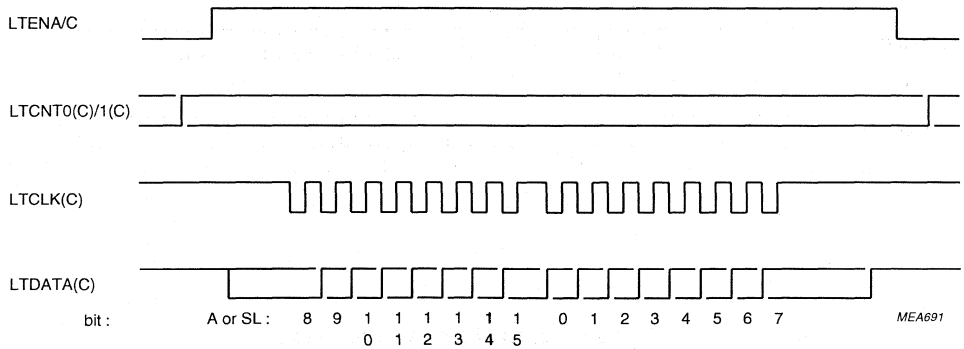


Fig.12 The order of interface bits during allocation information transfer.

Table 6

BITS				CHANNEL	SUB-BAND
MSB			LSB		
A15	A14	A13	A12	L	2 × COUNT
A11	A10	A9	A8	R	2 × COUNT
A7	A6	A5	A4	L	(2 × COUNT) + 1
A3	A2	A1	A0	R	(2 × COUNT) + 1

Table 7

BITS			CHANNEL	CONTENTS
MSB		LSB		
SL15	SL14	–	–	00
SL13	SL12 - SL11 - SL10 - SL9	SL8	L	SCALE FACTOR (COUNT)
SL7	SL6	–	–	00
SL5	SL4 - SL3 - SL2 - SL1	SL0	R	SCALE FACTOR (COUNT)

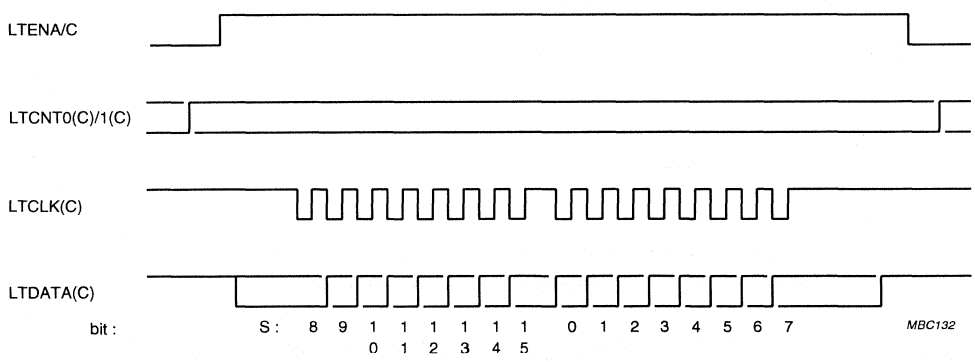


Fig.13 The order of bits on the interface.

Settings (LTCNT1(C) = logic 1, LTCNT0(C) = logic 0)

Without using the information, the SAA2012 transfers microcontroller settings to the SAA2002.

Prior to sending settings, the microcontroller would utilize the SAA2012 status readings to ensure its readiness to accept and convey the data.

Following reception of the settings the SAA2012 will cause the ready-to-receive bit to be logic 0 until the settings have been sent to the SAA2002. The microcontroller can only send this data when this bit is logic 1.

The order of bits on the interface is shown in Fig.13.

Table 8 Microprocessor settings applied to the SAA2002 via the SAA2012.

BITS				NAME	FUNCTION	VALID IN
MSB			LSB			
S15	S14	S13	S12	bit-rate index	bit-rate indication	encode
S11	–	–	S10	sample frequency	44.1, 48 or 32 kHz indication	encode
S9	–	–	–	DECODE	1 = decode; 0 = encode	encode/decode
S8	–	–	–	external 256f_s	1 = external; 0 = internal	encode/decode
S7	–	–	–	2-channel mono	1 = (2-channel mono); 0 = stereo	encode
S6	–	–	–	MUTESFC	1 = mute; 0 = no mute	encode/decode
S5	–	–	–	not used	–	encode/decode
S4	–	–	–	CH I	1 = channel I; 0 = channel II	decode
S3	–	–	S2	Tr0 - Tr1	transparent bits	encode
S1	–	–	S0	EMPHASIS	emphasis indication	encode

Status (LTCNT1(C) = LTCNT0(C) = logic 1)

The SAA2002 and SAA2012 operation may be checked by reading these bits. All, except the ready-to-receive bits, are generated by the SAA2002.

The bit rate index shows the bit rate of the sub-band signal in units of 32 kbits/s. The SAA2012 is designed for bit rates of 384, 256, 192 and 128 kbits/s only.

Table 9 Order of SAA2002 bits as they appear on the interface (see also Fig.14).

BITS				NAME	FUNCTION	VALID IN
MSB			LSB			
T15	T14	T13	T12	bitrate index	bit-rate indication	encode/decode
T11	–	–	T10	sample frequency	44.1, 48 or 32 kHz indication	encode/decode
T9	–	–	–	ready-to-receive S	1 = ready; 0 = not ready	encode/decode
T8	–	–	–	ready-to-receive E	1 = ready; 0 = not ready	encode/decode
T7	–	–	T6	MODE	sub-band signal mode ID	encode/decode
T5	–	–	–	SYNC	synchronization indicator	decode
T4	–	–	–	CLKOK	1 = OK; 0 = not OK	encode/decode
T3	–	–	T2	Tr0 - Tr1	transparent bits	encode/decode
T1	–	–	T0	EMPHASIS	emphasis indication	encode/decode

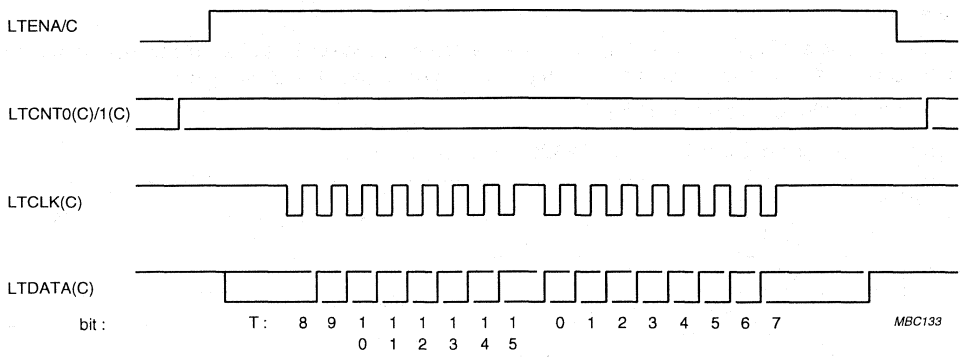


Fig.14 The order of appearance of bits on the interface.

Table 10 Sample frequency indication.

MSB	LSB	f_s	REMARK
0	0	44.1 kHz	default value
0	1	48 kHz	
1	0	32 kHz	
1	1	–	do not use

Table 11 MODE indication.

MSB	LSB	MODE	OUTPUT
0	0	stereo	L and R
0	1	joint stereo	L and R
1	0	2-channel mono	I or II as selected
1	1	1-channel mono	mono, no selection

With EMPHASIS activated (S1 = T1 = logic 0 and S0 = T0 = logic 1) only bit rates 384 and 256 kbits/s can be used.

A ready-to-receive **S** or **E** indicates whether or not the SAA2012 can receive new settings or extended settings respectively from the microcontroller and should be checked prior to sending new information.

The SAA2012 can only be used to encode stereo (mode 00) signals and 2-channel mono (mode 10) signals.

During the decoding mode this bit indicates if the operation of the SAA2002 is in synchronization with the PASC signal. If not the SAA2002 cannot perform the decoding.

CLKOK indicates whether or not the f_{s256} clock corresponds with the specified sample frequency.

EMPHASIS indication may be used to apply correct de-emphasis. During the encoding 50/15 μs mode the SAA2012 will correct the calculated allocation if emphasis is applied for a 44.1 kHz sampling frequency.

Frequency Range Limitation

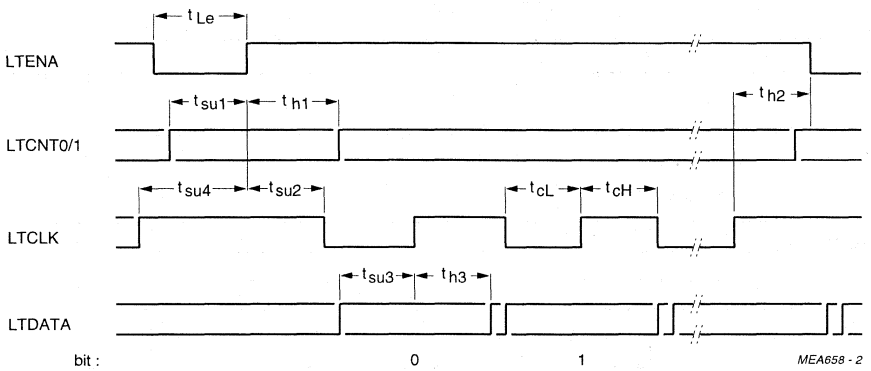
In encode mode the frequency range will be limited at lower rates. This is implemented by making the samples of higher frequency sub-bands equal to 0 before the allocation calculation. This automatically ensures that these sub-bands do not get any bits allocated.

Table 12 shows the sub-bands affected and the resulting frequency range.

The transfer of either 8-bits or 16-bits is permitted for the transfer of status information. When only 8-bits are transferred, these will always form the first byte and may be used in checking the ready-to-receive bit.

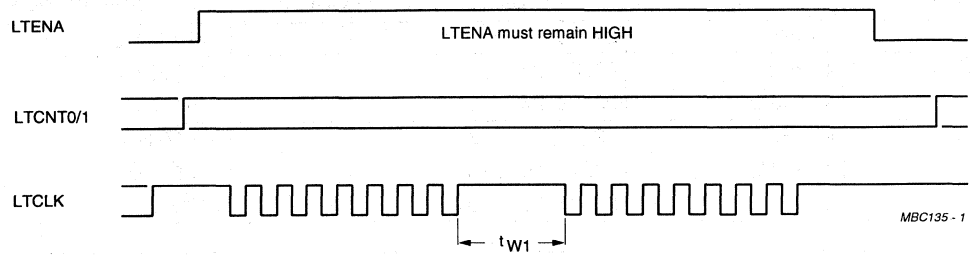
Table 12 The sub-bands affected and the resulting frequency range.

BIT RATE	f_s	SUB-BANDS SET TO LOGIC 0	FREQUENCY
256 kbits/s	48 kHz	29, 30, 31	>21750 Hz
192 kbits/s	48 kHz	20, 21, 22, ..., 31	>15000 Hz
	44.1 kHz	22, 23, 24, ..., 31	>15159 Hz
128 kbits/s	48 kHz	12, 13, 14, ..., 31	>9000 Hz
	44.1 kHz	13, 14, 15, ..., 31	>8957 Hz
	32 kHz	20, 21, 22, ..., 31	>10000 Hz



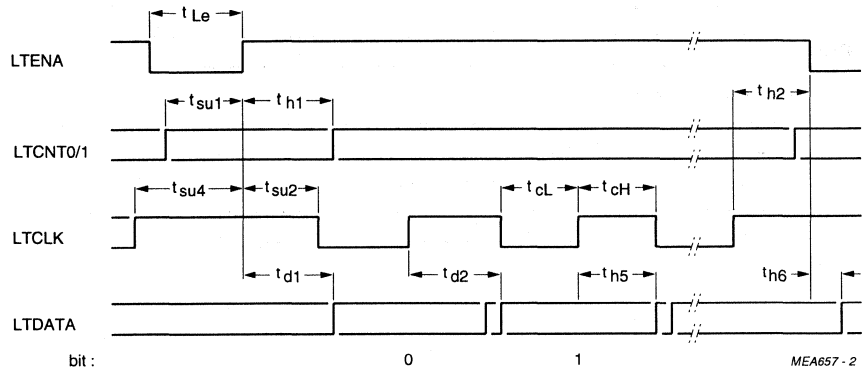
t_{Le} > 210 ns minimum LOW time LTENA prior to transfer.
t_{su1} > 50 ns set-up time LTCNT0, 1 before LTENA HIGH.
t_{h1} > 210 ns hold time LTCNT0/1 after LTENA HIGH.
t_{su2} > 210 ns set-up time LTENA before LTCLK LOW.
t_{h2} > 210 ns hold time LTENA after LTCLK HIGH.
t_{cL} > 210 ns minimum LOW time LTCLK.
t_{cH} > 210 ns minimum HIGH time LTCLK.
t_{su3} > 210 ns set-up time LTDATA before LTCLK HIGH.
t_{h3} > 50 ns hold time LTDATA after LTCLK HIGH.
t_{su4} > 210 ns set-up time LTCLK before LTENA HIGH.

Fig.15 Microcontroller to SAA2012 timing.



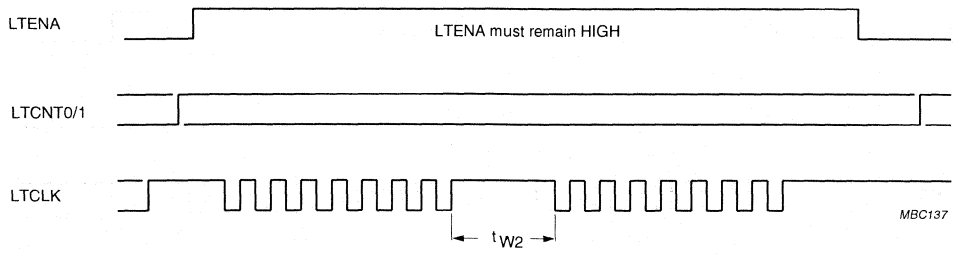
t_{W1} > 550 ns minimum time between two 8-bit transfers.

Fig.16 16-bit transfers.



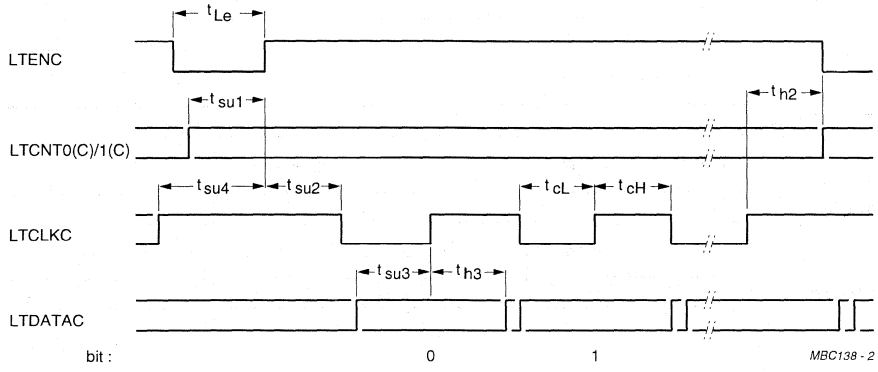
t_{Le} > 210 ns minimum LOW time LTENA prior to transfer.
t_{su1} > 50 ns set-up time LTCNT0/1 before LTENA HIGH.
t_{h1} > 210 ns hold time LTCNT0(C)/1(C) after LTENA HIGH.
t_{su2} > 210 ns set-up time LTENA before LTCLK LOW.
t_{h2} > 210 ns hold time LTENA before LTCLK HIGH.
t_{cL} > 210 ns minimum LOW time LTCLK.
t_{cH} > 210 ns minimum HIGH time LTCLK.
t_{d1} < 385 ns maximum delay LTDATA after LTENA HIGH.
t_{d2} < 385 ns maximum delay LTDATA after LTCLK HIGH.
t_{h5} > 145 ns hold time LTDATA after LTCLK HIGH.
t_{su4} > 210 ns set-up time LTCLK before LTENA HIGH.
t_{h6} > 0 ns hold time LTDATA after LTENA LOW.

Fig.17 SAA2012 to microcontroller timing.



t_{W2} > 550 ns minimum time between two 8-bit transfers.

Fig.18 16-bit transfers.



t_{Le} > 400 ns minimum LOW time LTENA prior to transfer.

t_{su1} > 400 ns set-up time LTCNT0(C)/1(C) before LTENC HIGH.

t_{su2} > 200 ns set-up time LTENC before LTCLKC LOW.

t_{h2} > 400 ns hold time LTENC before LTCLK HIGH.

t_{cL} > 210 ns minimum LOW time LTCLKC.

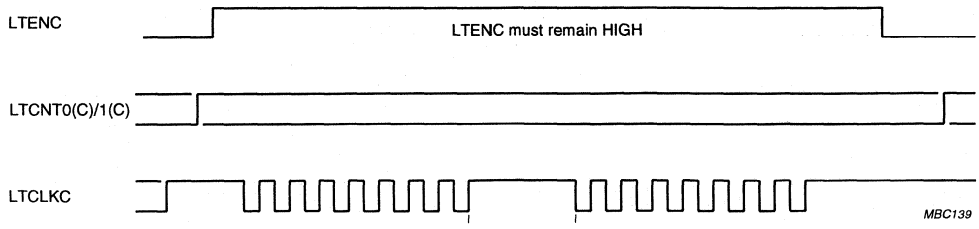
t_{cH} > 210 ns minimum HIGH time LTCLKC.

t_{su3} > 210 ns set-up time LTDATAC before LTCLKC HIGH.

t_{h3} > 160 ns hold time LTDATAC after LTCLKC HIGH.

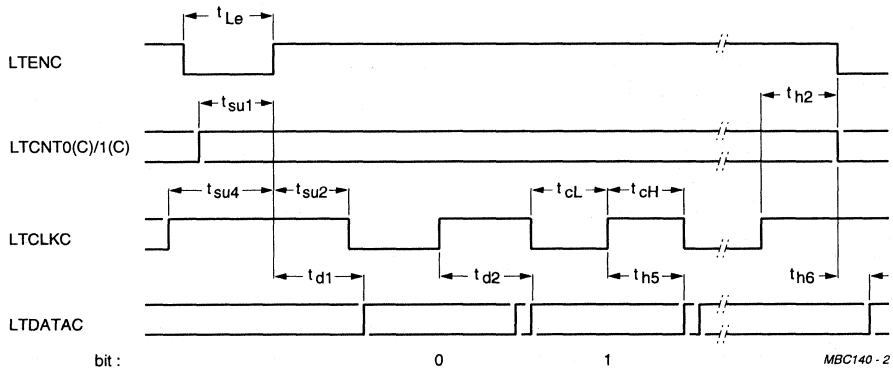
t_{su4} > 900 ns set-up time LTCLKC before LTENC HIGH.

Fig.19 SAA2012 to SAA2002 timing.



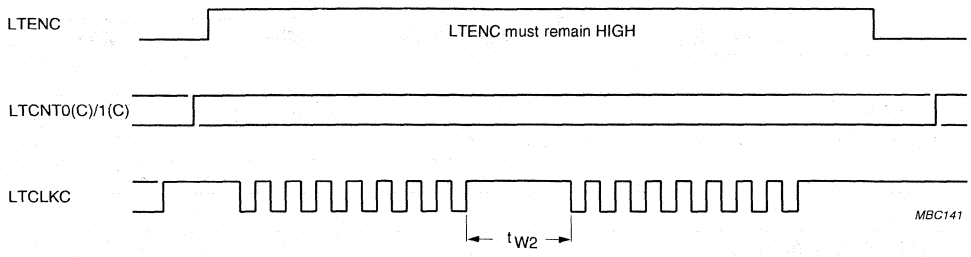
t_{W2} > 600 ns minimum time between two 8-bit transfers.

Fig.20 16-bit transfers.



t_{Le} > 400 ns minimum LOW time LTENC prior to transfer.
t_{su1} > 400 ns set-up time LTCNT0(C)/1(C) before LTENC HIGH.
t_{su2} > 200 ns set-up time LTENC before LTCLKC LOW.
t_{h2} > 400 ns hold time LTENC before LTCLKC HIGH.
t_{cL} > 210 ns minimum LOW time LTCLKC.
t_{cH} > 210 ns minimum HIGH time LTCLKC.
t_{d1} < 300 ns maximum delay LTDATAC after LTENC HIGH.
t_{d2} < 300 ns maximum delay LTDATAC after LTCLKC HIGH.
t_{su4} > 900 ns set-up time LTCLKC before LTENC HIGH.
t_{h5} > 160 ns hold time, after LTCLKC HIGH.
t_{h6} > 0 ns hold time LTDATAC after LTENC LOW.

Fig.21 SAA2002 to SAA2012 timing.



t_{W2} > 600 ns minimum time between two 8-bit transfers.

Fig.22 16-bit transfers.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+6.5	V
V_I	input voltage	note 1	−0.5	V_{DD} + 0.5	V
I_{DD}	supply current		–	100	mA
I_I	input current		–	±10	mA
I_O	output current		–	±40	mA
P_{tot}	total power dissipation		–	550	mW
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{es1}	electrostatic handling	note 2	−1500	+1500	V
V_{es2}	electrostatic handling	note 3	−70	+70	V

Notes

1. Input voltage should not exceed 6.5 V unless otherwise specified.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

DC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		3.8	5.0	5.5	V
I_{DD}	operating supply current	V_{DD} = 3.8 V	–	15	17	mA
		V_{DD} = 5 V	–	23	25	mA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_I	input current		–	–	10	µA
Outputs						
V_{OL}	LOW level output voltage	note 1	–	–	0.4	V
V_{OH}	HIGH level output voltage	note 1	V_{DD} − 0.5	–	–	V
3-state outputs						
I_{OZ}	3-state OFF state current	V_I = 0 to 5.5 V	–	–	10	µA

Note

1. Maximum load current for LTDATA, LTCNT1C, LTCNT0C, LTENC, LTCLKC, TEST1, TEST2, FDAC and FDAF = 2 mA; for LTDATAC = 3 mA.

AC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock CLK24						
f_s	sample frequency		23	24.576	26	MHz
Clock FS256						
f_s	sample frequency		–	–	13	MHz
Inputs FSYNC, SWS, LTCNT1, LTCNT0, LTENA, LTCLK, LTDATA, LTDATAC, FDAF, FDAC, SCL and SWS						
C_I	input capacitance		–	–	10	pF
INPUT SET-UP TIME						
t_{su}	set-up time of inputs referenced to CLK24 rising edge	note 1	15	–	–	ns
t_{su}	set-up time of inputs referenced to $256f_s$ rising edge	note 2	15	–	–	ns
INPUT HOLD TIME						
t_h	hold time of inputs referenced to CLK24 rising edge	note 1	20	–	–	ns
t_h	hold time of inputs referenced to $256f_s$ rising edge	note 2	10	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs LTDATA, LTDATAC, LTCNT1C, LTCNT0C, LTENC, LTCLKC, FDAF and FDAC						
C_o	output capacitance		–	–	10	pF
t_d	output delay referenced to CLK24 rising edge	C_L = 25 pF; note 3	–	–	45	ns
t_d	output delay referenced to $256f_s$ rising edge	C_L = 25 pF; note 4	–	–	30	ns
3-state outputs						
t_{PHZ}	disable time HIGH-to-Z	C_L = 25 pF	–	–	65	ns
t_{PLZ}	disable time LOW-to-Z	C_L = 25 pF	–	–	65	ns
t_{PZH}	enable time Z-to-HIGH	C_L = 25 pF	–	–	65	ns
t_{PZL}	enable time Z-to-LOW	C_L = 25 pF	–	–	65	ns

Notes

1. Inputs FSYNC, SWS, LTCNT1, LTCNT0, LTENA, LTCLK, LTDATA and LTDATAC.
2. Inputs FDAF, FDAC, SCL and SWS.
3. Outputs LTDATA, LTDATAC, LTCNT1C, LTCNT0C, LTENC and LTCLK.
4. Outputs FDAF and FDAC.

Adaptive allocation and scaling for PASC coding in DCC systems

SAA2013

FEATURES

- Wide operating voltage range: 2.7 to 5.5 V
- Low power consumption: 13 mW; 3.0 V
- Low power decode mode: 1 mW; 5.0 V
- Sleep mode for low power and low Electromagnetic Interference (EMI)
- Sophisticated allocation algorithm
- Optimum sound quality
- Three-wire L3 bus microcontroller interface
- Stereo or 2-channel mono recording
- Small surface mounted package (QFP; SOT307).

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

The SAA2013 performs the adaptive allocation and scaling function in the Precision Adaptive Sub-band Coding (PASC) system. It is not required in playback only applications, and is only used during recording. To complete the PASC processor, a SAA2003 stereo filter and codec is required.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2013H	44	QFP[1]	plastic	SOT307-2

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* are followed. The pocketbook can be ordered using the code 9398 510 34011.

BLOCK DIAGRAM

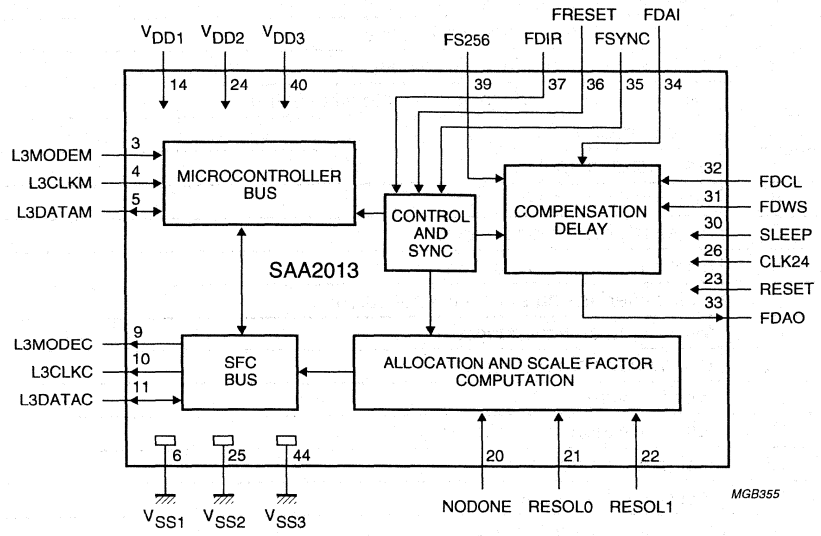


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
TEST10	1	test input; connect to V_{SS}	I
TEST11	2	test input; connect to V_{SS}	I
L3MODEM	3	microcontroller interface mode input	I
L3CLKM	4	microcontroller interface clock input	I
L3DATAM	5	microcontroller interface data 3-state input/output	I/O
V_{SS1}	6	supply ground	–
TEST12	7	test output; do not connect	O
TEST13	8	test output; do not connect	O
L3MODEC	9	codec interface mode output	O
L3CLKC	10	codec interface clock output	O
L3DATAC	11	codec interface data 3-state input/output	I/O
TEST1	12	test output; do not connect	O
TEST2	13	test output; do not connect	O
V_{DD1}	14	supply voltage	–
TEST3	15	test mode input; connect to V_{DD}	I
TEST4	16	test mode input; connect to V_{DD}	I
TEST5	17	test input; connect to V_{SS}	I
TEST6	18	test input; connect to V_{SS}	I
TEST7	19	test input; connect to V_{SS}	I
NODONE	20	nodone state selection input; connect to V_{DD}	I
RESOL0	21	resolution selection 0 input	I
RESOL1	22	resolution selection 1 input	I
RESET	23	reset input; active HIGH	I
V_{DD2}	24	supply voltage	–
V_{SS2}	25	supply ground	–
CLK24	26	24.576 MHz clock input	I
LOWPWR	27	low power decode select input	I
POR	28	power on reset input	I
TEST8	29	test input; connect to V_{SS}	I
SLEEP	30	sleep mode select input	I
FDWS	31	filtered data word select	I
FDCL	32	filtered data clock	I
FDAO	33	filtered data output	O
FDAI	34	filtered data input	I
FSYNC	35	sub-band synchronization on filtered I^2S bus	I
FRESET	36	reset signal input from SAA2003	I
FDIR	37	filtered data direction input	I
TEST9	38	test input; connect to V_{SS}	I
FS256	39	system clock input; 256 × sample frequency (f_s)	I
V_{DD3}	40	supply voltage	–

SYMBOL	PIN	DESCRIPTION	TYPE
n.c.	41	not connected	–
n.c.	42	not connected	–
n.c.	43	not connected	–
V_{SS3}	44	supply ground	–

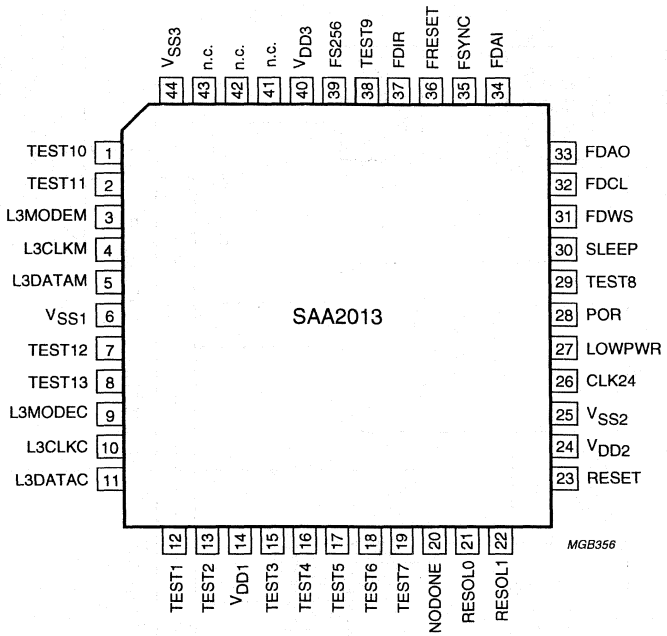


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

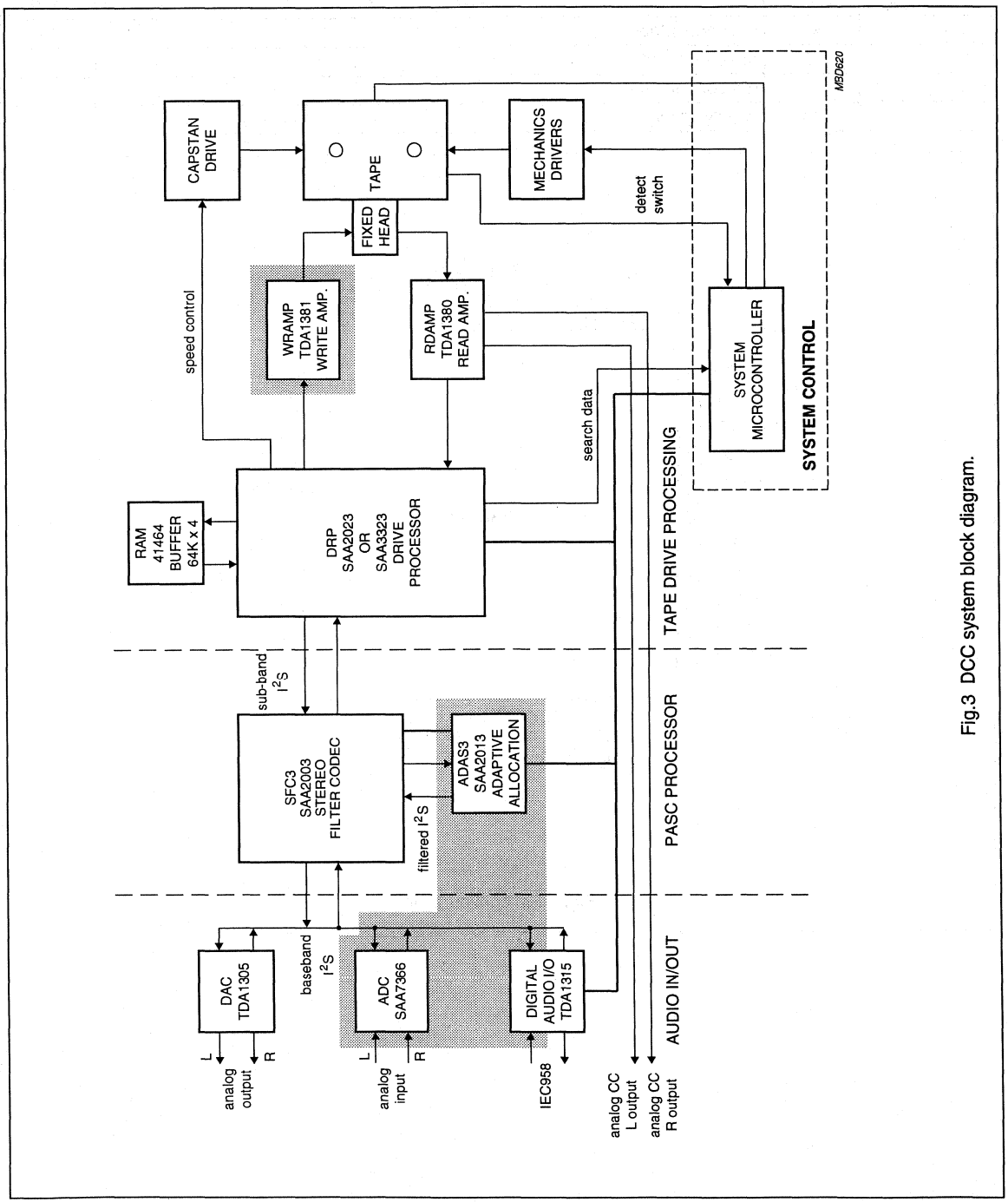


Fig.3 DCC system block diagram.

PASC processor

The PASC processor is a dedicated Digital Signal Processor (DSP) engine which efficiently codes digital audio data at a bit rate of 384 kbits/s without affecting the sound quality. This is achieved using an efficient adaptive data notation and by only encoding the audio information which can be heard by the human ear.

The audio data is split into 32 equal sub-bands during encoding. For each of the sub-bands a masking threshold is calculated. The samples from each of the sub-bands are included in the PASC data with an accuracy that is determined by the available bit-pool and by the difference between the signal power and the masking threshold for that sub-band. In decode, the sub-band signals are reconstructed into the full bandwidth audio signal.

The stereo filter codec performs the splitting (encoding) and reconstruction (decoding), including the necessary formatting functions. During encoding, the adaptive allocation and scaling circuit calculates the required accuracy (bit allocation) and scale factors of the sub-band samples.

Decode/encode control

Selection of decode or encode is controlled using FRESET and FDIR. FRESET causes a general reset. The FDIR signal is sampled at the falling edge of the FRESET signal to determine the operation mode. When FDIR is HIGH, SAA2013 is in decode mode. When FDIR is LOW the SAA2013 is in encode mode. See Fig.4.

Reset

When used with low-power mode disabled (LOWPWR = V_{SS}), and with the SLEEP input LOW, SAA2013 is reset if the RESET pin is held HIGH for at least 5 periods of the CLK24 clock, see Fig.5. SAA2013 defaults to decode mode. When in low-power mode, the RESET pin is disabled.

Sleep mode

Sleep mode is entered by taking the SLEEP input HIGH with the LOWPWR pin connected to V_{SS}; CLK24 and FS256 are stopped internally to the SAA2013, the 3-state buffers will have a high impedance, and outputs will freeze in the same state as just before the sleep mode became active (clocks stopped). To come out of sleep mode, the SLEEP input must be taken LOW again. To clear data present from before sleep was entered, this should be followed by a reset, see Fig.5.

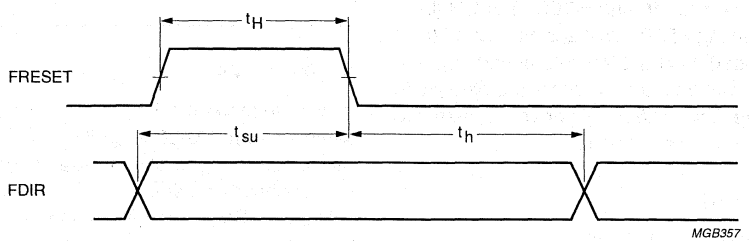


Fig.4 FDIR and FRESET timing.

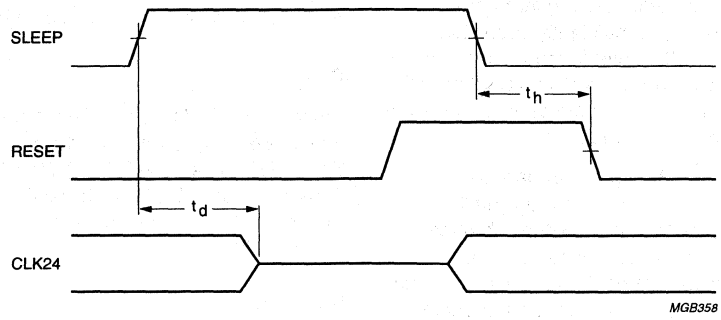


Fig.5 SLEEP and RESET timing.

Low-power decode mode

Low-power decode mode is made available by connecting the LOWPWR pin to V_{DD}. With LOWPWR = V_{DD}, low-power decode mode is entered 9 cycles of CLK24 after the SLEEP input is taken HIGH. In low-power decode mode, the L3 bus connections are connected straight trough the SAA2013, which is effectively bypassed. The compensation delay connection between pins FDAI and FDAO is no longer needed by the SAA2003, and CLK24 and FS256 are stopped internally to the SAA2013.

To get out of low-power decode mode, it is necessary to take SLEEP LOW, FDIR LOW, and FRESET HIGH (in a normal application taking FDIR LOW and FRESET HIGH can be achieved by setting SAA2003 into encode mode), SAA2013 then performs an internal reset, and defaults to normal decode mode. The RESET pin does not reset the circuit from low-power decode mode.

Power-On Reset (POR)

When low-power decode mode is enabled (LOWPWR = V_{DD}), a power-on reset circuit is required to ensure that the internal clocks are connected correctly at power-on. A suitable circuit is shown in Fig.6. This circuit will correctly reset the internal clock connection provided that the nominal value of the V_{DD} supply is reached within 40 ms at power-on.

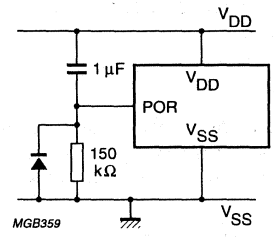


Fig.6 POR circuit.

Encode mode

In encode mode the SAA2013 receives sub-band filtered samples from SAA2003 on the FDAI pin. The SAA2013 has to collect a complete frame of sub-band data before the allocation and scale factor information can be calculated. So that the allocation and scale factor information is available in the same time frame as the audio samples at the output, the sub-band filtered samples are delayed by 480 FDWS periods.

One FDWS period is equal to $\frac{1}{f_s}$ where f_s is the audio sample rate of 32, 44.1 or 48 kHz. The delayed samples are passed to the codec part of SAA2003 on the FDAO pin.

For each sub-band frame, SAA2013 calculates the allocation and scale factor index information required by the SAA2003. In order to synchronize the codec part of SAA2003, SAA2013 frequently requests status information from the codec. It monitors sample frequency, emphasis information and stereo mode, and uses the ready-to-receive bit of the codec to determine when to transfer information.

Decode mode

In decode the SAA2003 will transfer samples from FDAI to FDAO with a delay of 480 FDWS periods. Settings and status information can be sent to SAA2003 via SAA2013, but the SAA2013 does not itself act on this information. Transfer of this information is automatically synchronized to the ready-to-receive bit of SAA2003 by SAA2013.

Filtered data interface

The filtered data interface signals are given in Table 2.

Table 2 Filtered data interface signals.

PIN	INPUT/OUTPUT	FUNCTION	FREQUENCY
FDWS	input	filtered data interface word select	f_s
FDCL	input	filtered data interface bit clock	$64f_s$
FDAI	input	filtered data input	–
FDAO	output	filtered data output	–
FSYNC	input	filtered data sub-band synchronization	–

The filtered data interface transfers sub-band filtered samples between the stereo filter codec SAA2003 and SAA2013. The interface is similar to a normal I²S interface, consisting of clock (FDCL), data (FDAI/FDAO) and word select lines (FDWS), except that the samples sent represent signals divided into 32 sub-bands. One frame of data consists of 12 samples from 32 sub-bands for both left and right channels, i.e.: 768 audio samples. Each audio sub-band sample is represented by a 24-bit two's complement number.

The order in which the samples are sent is shown in Table 3.

For two channel mono, the order is the same, but with Channel 1 samples in the place of left and Channel 2 samples in place of right.

Audio sample resolution section

The SAA2013 is designed for operation with audio input sources of 14, 15, 16 or 18-bit resolution.

For optimum audio performance the bit allocation algorithm of the SAA2013 can be varied to suit the bit resolution of the audio source. This is done with the pins RESOL0 and RESOL1 as shown in Table 1.

Table 1 Resolution set by pins RESOL0 and RESOL1.

RESOLUTION	RESOL0	RESOL1
16 bits	0	0
18 bits	0	1
14 bits	1	0
15 bits	1	1

Table 3 Order of samples.

SUB-BAND	0	0	1	1	2	2	...	31	31
Channel	L	R	L	R	L	R	...	L	R
Sample	0	0	0	0	0	0	...	0	0
	1	1	1	1	1	1	...	1	1
	2	2	2	2	2	2	...	2	2
	.	.	.	.	.	.	...	.	.
	.	.	.	.	.	.	...	.	.
	11	11	11	11	11	11	...	11	11

The signal FSYNC is used between each PASC frame to indicate the sending of samples for sub-band 0 (Fig.7).

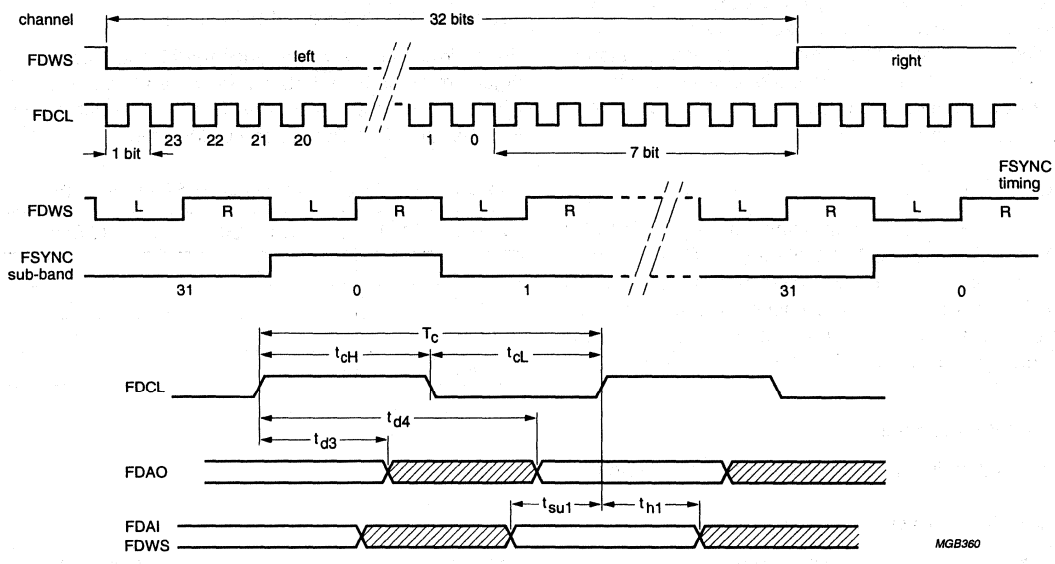


Fig.7 Filtered interface format.

Control interfaces

Two 3-wire control interfaces are provided (referred to as 'L3' interfaces). One is connected to the system microcontroller (L3MODEM, L3CLKM, L3DATAM where 'M' represents microcontroller), the other to SAA2003 (L3MODEC, L3CLKC, L3DATAC where 'C' represents codec). In general, control data is passed between SAA2003 and the microcontroller via SAA2013. This ensures that the microcontroller is buffered from the time-critical SAA2013 to SAA2003 interface during encode.

The SAA2013 does not interpret the data from the microcontroller interface.

Status information from the codec is interpreted to ensure that SAA2013 quickly acts upon the status of SAA2003.

The L3 bus operation is shown in Fig.8. There are three modes:

1. Address.
2. Data.
3. Halt.

Each interface operates as either a master or a slave, where the master provides L3CLK and L3MODE. For the microcontroller to SAA2013 interface, the microcontroller is the master. For the SAA2013 to SAA2003 interface, SAA2013 is the master.

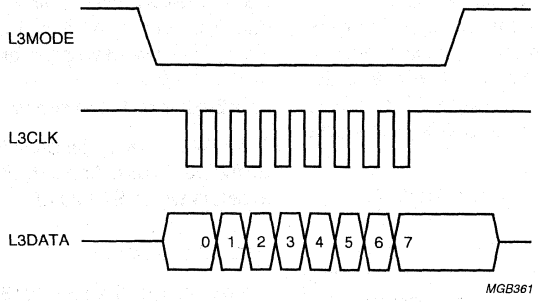


Fig.8 L3 bus operation; address mode.

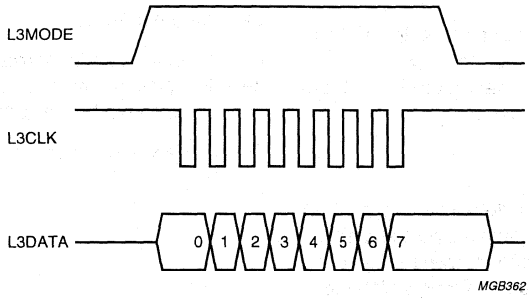


Fig.9 L3 single byte transfer.

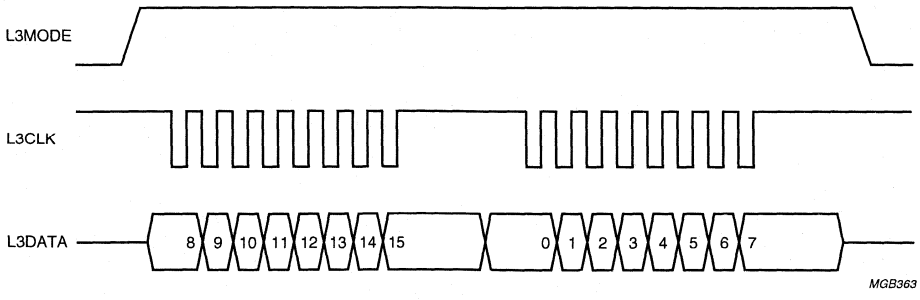


Fig.10 L3 bus two byte transfer.

ADDRESS MODE

Address mode is entered by the master pulling L3MODE LOW. This causes the L3DATA line to act as an input on the slave, and 8 bits of address data are clocked into the slave. If the slave recognizes the address, it will set-up its internal state based on the 2 Least Significant Bits (LSBs) of the address. The slave than expects to send status data or receive control data.

The addresses for SAA2013 are shown in Table 4.

Table 4 SAA2013 addresses.

MSB	LSB	L3 OPERATION MODE	FUNCTION
0010	0000	WDAT	extended settings
0010	0001	RDAT	allocation information
0010	0010	WCMD	settings
0010	0011	RSTAT	status/peak read

The interface may be reset by sending an address of all zeros ('00000000'). This may be used to allow inter-operation with other devices sharing the L3CLK and L3DATA lines (e.g. SAA7345 CD decoder).

DATA MODE

In data mode, bytes of data are clocked into (e.g. control) or out of (e.g. status) the slave. A single byte transfer is shown in Fig.9. A two byte transfer is shown in Fig.10, between bytes there must be a pause during which the clock remains HIGH.

HALT MODE

Halt mode consists of pulling L3MODE LOW after sending data. It is used for marking the end of a data transfer mode which does not have an internal bit counter.

SAA2013 interface modes

The SAA2013 may be used to read and write from or to SAA2003. Information is transferred via a set of transit registers within SAA2013.

DECODE OPERATION

During decode, the SAA2013 does not perform allocation. Therefore no allocation and scale factor indices are sent to SAA2003. Settings and extended settings may still be sent to SAA2003, and SAA2013 monitors the status of the codec by reading status from it after every occurrence of FSYNC. Peak level data can also be transferred from SAA2003.

ENCODE OPERATION

In encode, the same information may be sent as for decode, and in addition, allocation/scale factor indices are sent to the codec by SAA2013.

The interface modes are shown in Table 5.

Table 5 Interface modes.

MODE	ADDRESS		INTERFACE MODE	LENGTH (BITS)	DIRECTION
	BIT 1	BIT 0			
Decode	0	0	extended settings	8	microcontroller to SAA2003
	0	1	–	–	–
	1	0	settings	16	microcontroller to SAA2003
	1	1	status/peak	16 or 48	SAA2003 to microcontroller
Encode	0	0	extended settings	8	microcontroller to SAA2003
	0	1	allocation/scale	48 × 16	SAA2013 to SAA2003
	1	0	settings	16	microcontroller to SAA2003
	1	1	status/peak	16 or 48	SAA2003 to microcontroller

PRIORITY

Each type of transfer has a priority. The priorities are:

1. Allocation/scale/settings (highest priority).
2. Status read.
3. Peak read.
4. Extended settings (lowest priority).

ALLOCATION AND SCALE FACTOR TRANSFER

The allocation and scale factor information sent from SAA2013 to SAA2003 during encode has the highest priority. The other types of transfer interleaved with the allocation/scale information.

SETTINGS TRANSFER

This is a 16-bit transfer. The microcontroller sends settings to SAA2003. SAA2013 only transfers these without taking notice of the contents. In encode, the settings are held in the transit registers, and sent next time that allocation is being sent. In decode, settings are sent as soon as possible subject to the RTRC flag from SAA2003.

Before sending settings the microcontroller should read the status of SAA2013 to examine the Ready-To-Receive bit Settings (RTRS). After the settings have been received by SAA2013, RTRS will be made logic 0, until the settings have been sent to SAA2003. Only after RTRS is logic 1 again may the microcontroller send new settings.

STATUS READ

Status and peak information may be read from SAA2003 by the microcontroller. The status bits are defined in Table 6.

Table 6 Status bits.

BIT	NAME	FUNCTION	VALID IN
B15 to B12	bit rate index	bit rate indication	encode/decode
B11 and B10	sample frequency indication	44.1, 48, 32 kHz indication	encode/decode
B9	RTRS (settings)	1 = ready; 0 = not ready	encode/decode
B8	RTRE (external settings)	1 = ready; 0 = not ready	encode/decode
B7 and B6	MODE	sub-band signal mode identification	encode/decode
B5	SYNC	synchronization indication	encode/decode
B4	CLKOK	1 = OK; 0 = not OK	encode/decode
B3 and B2	Tr0 and Tr1	transparent bits	encode/decode
B1 and B0	EMPHASIS	emphasis indication	encode/decode

Since the two bytes of status information are sampled separately, the bytes may result from different sub-band frames.

The only valid bit rate code for the SAA2013 is 1100.

The sample frequency indication is shown in Table 7.

Table 7 Sample frequency indication.

BIT 11	BIT 10	SAMPLE FREQUENCY
0	0	44.1 kHz; default
0	1	48.0 kHz
1	0	32.0 kHz
1	1	do not use

Ready-to-receive S or E indicates whether the SAA2013 is ready-to-receive new settings or extended settings from the microcontroller. This should be checked before sending new information.

For details of the MODE, SYNC, CLKOK and transparent bits, refer to the *"SAA2003 data sheet"*.

The emphasis indication can be used to apply the correct de-emphasis. In encode SAA2013 will correct the calculated allocation if $^{50}/_{15}$ µs emphasis is applied. When "CCITT J.17" emphasis is applied, the bit allocation remains the same as when no emphasis is applied.

The 2 bytes of the status are 'sampled' at different moments. So the information may not result from the same sub-band frame.

When making repeated status reads (for instance reading the RTRS/RTRE flags before sending settings or extended settings), the microcontroller **must** send an address before each status read, to ensure that the byte counter in the interface is reset to logic 0. If this is not done, then the peak data will be read. Conversely, it is important **not** to send a new address after a status read if the peak data is required.

PEAK READ

Peak information is read by clocking a further 4 bytes of data after a status read. The data format is shown in Figs 11 and 12. Bits B17 to B31 contain a 15-bit unsigned peak, LSB first, channel indicated by bit B16. Bits B33 to B47 contain a 15-bit unsigned peak, channel indicated by bit B32.

The peak data is delayed by 1 read period. If for example the microcontroller reads peak level data every 50 ms, the peak data sourced by SAA2013 will be 50 ms old. Also it is possible that peak data may contain an additional delay of 1 column (667 µs minimum at 48 kHz, 1 ms maximum at 32 kHz). If the microcontroller attempts to read peak level data with a delay of less than 1 column, the peak level data from the previous reading will be repeated. Normally the microcontroller should allow at least 1 ms between reads. There is also a delay required between peak data words (Fig.13).

If the SAA2013 does not have peak data available (for instance the microcontroller attempts two reads in very quick succession), it will return all peak data bits set to logic 0. The microcontroller can detect if valid peak data has been returned by inspecting bits T16 and T32. If both bits are set to logic 0 the data is not valid.

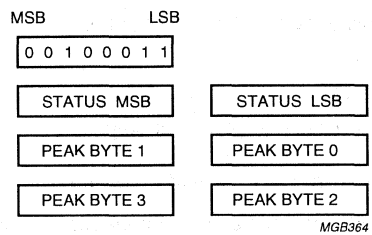


Fig.11 Peak level read format; SAA2013 to microcontroller.

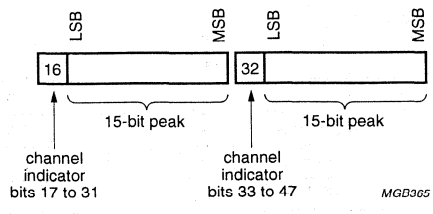


Fig.12 Peak level format.

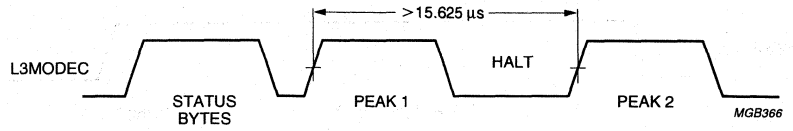


Fig.13 Peak data timing.

EXTENDED SETTINGS

This is a single byte transfer, valid during decode and encode. The sequence of operations is:

1. Microcontroller reads status from SAA2013, waiting for the flag RTRE to be set.
2. When RTRE is logic 1, the microcontroller writes address bit 0 is logic 0, bit 1 is logic 0.
3. One byte of extended settings is clocked into the transit register (SAA2013).
4. When it is possible (i.e. subject to RTRC being HIGH, and assuming that allocation or status is not waiting), the byte is transferred from the transit register to the SAA2003.

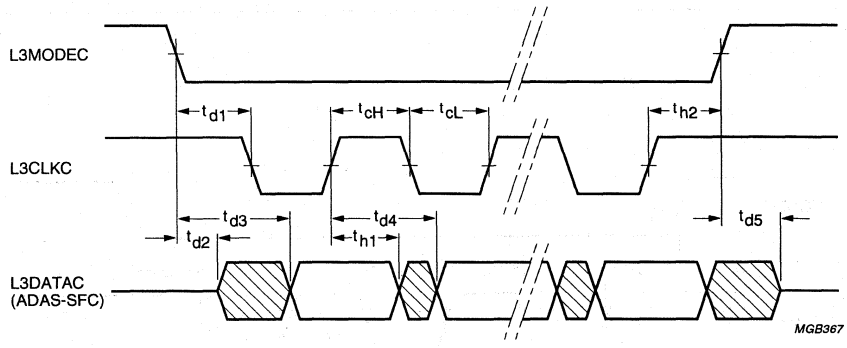


Fig.14 L3 interface timing; SAA2013 to SAA2003 (address mode).

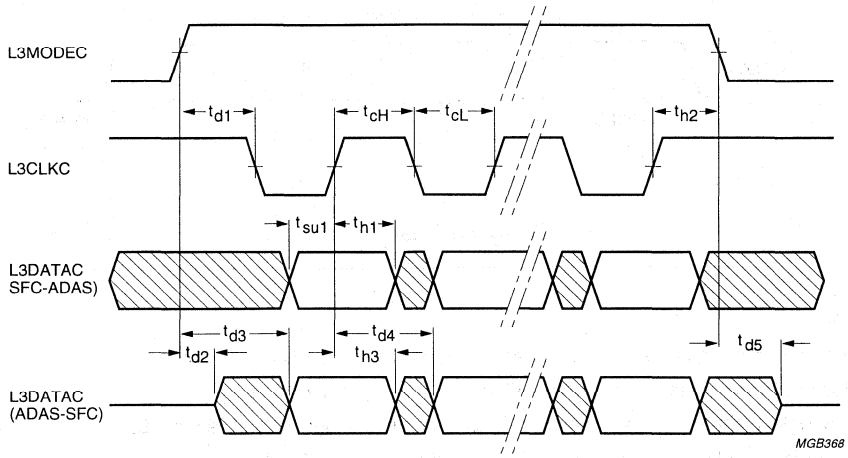


Fig.15 L3 interface timing; SAA2013 to SAA2003 (data mode).

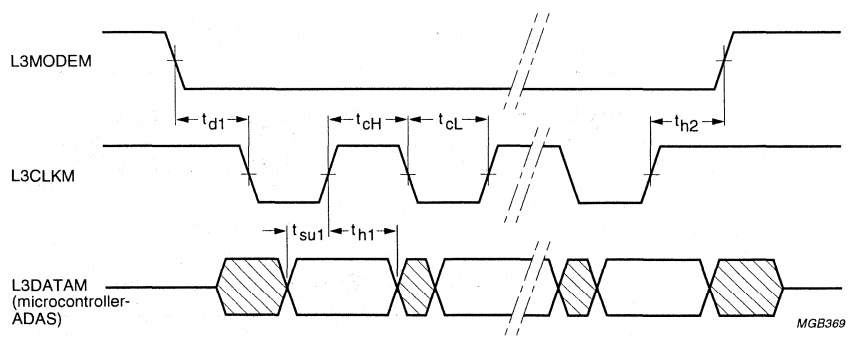


Fig.16 L3 interface timing; microcontroller to SAA2013 (address mode).

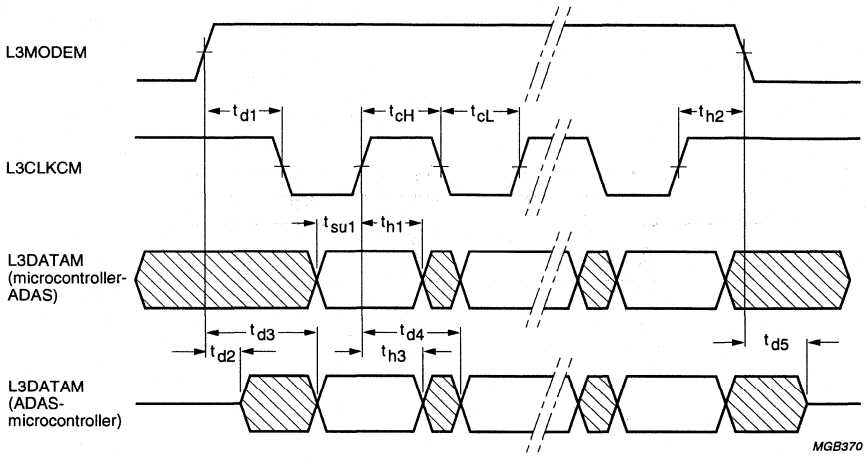


Fig.17 L3 interface timing; microcontroller to SAA2013 (data mode).

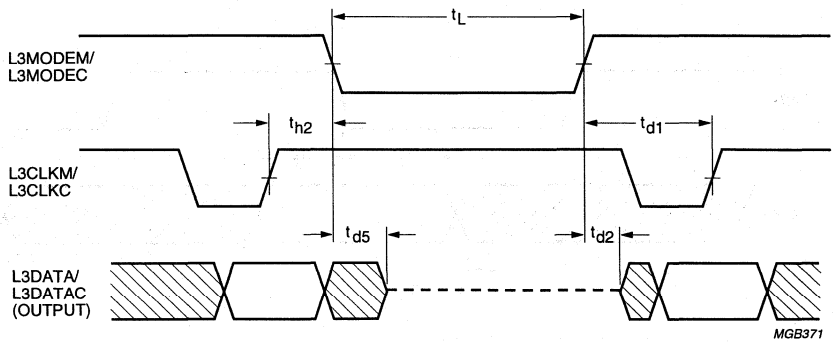


Fig.18 L3 interface timing; microcontroller to SAA2013 and SAA2013 to SAA2003 (halt mode).

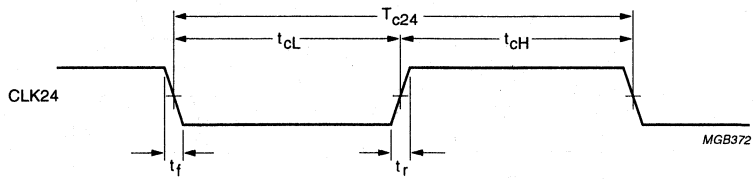


Fig.19 Input timing CLK24.

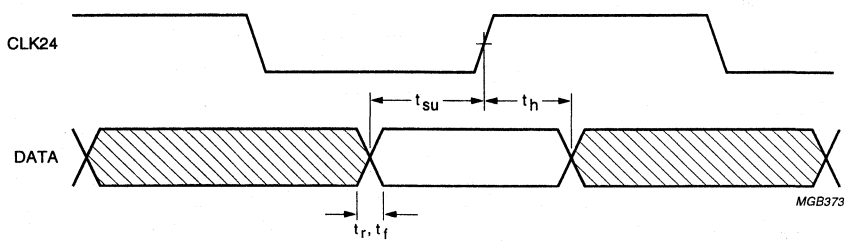


Fig.20 Input signal timing for FSYNC, FRESET, FDIR, FDWS, L3MODEM, L3CLKM, L3DATAM and L3DATAC.

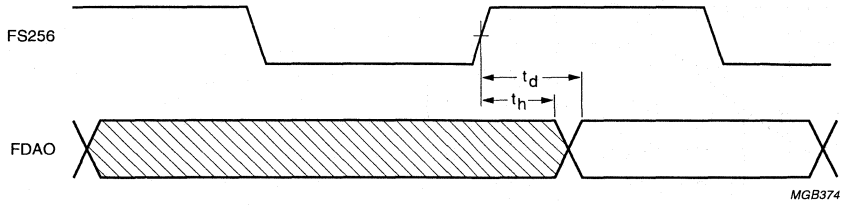


Fig.21 Output signal timing FDAO.

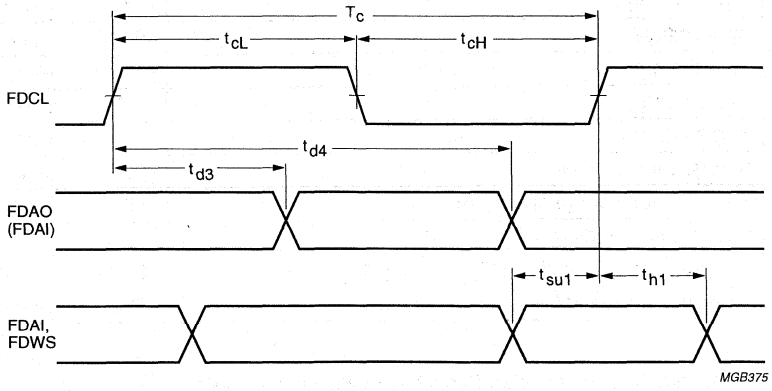
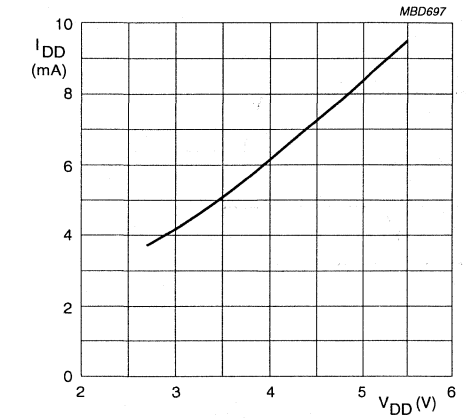


Fig.22 Filtered data interface timing.

Current consumption

The typical current consumption is shown in Fig.23.



T_{amb} = 25 °C.

Fig.23 Typical current consumption.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+6.5	V
V_I	input voltage		−0.5	V_{DD} + 0.5	V
I_I	input current		−	20	mA
V_O	output voltage		−0.5	+6.5	V
I_O	output current		−	20	mA
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{es}	electrostatic handling				
	Human Body Model (HBM)	note 1	−2000	+2000	V
	Machine Model (MM)	note 2	−200	+200	V

Notes

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
2. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_{DD} = 2.7 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to 85 °C; unless otherwise specified; I_{OL} and I_{OH} derated by 75% for V_{DD} < 4.5 V.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.7	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 3.0 V	4	5	6	mA
		V_{DD} = 5.0 V	7	10	12	mA
I_{stb}	standby current	V_{DD} = 5.0 V	–	–	400	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
Outputs						
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −4 mA	V_{DD} − 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	30	pF
Inputs/outputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −4 mA	V_{DD} − 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	30	pF
Clock input CLK24						
f_i	input frequency	see Fig.19	–	24.576	–	MHz
t_r	rise time		–	–	7	ns
t_f	fall time		–	–	7	ns
t_{cH}	HIGH time		10	–	–	ns
t_{cL}	LOW time		10	–	–	ns
Clock input FS256						
f_i	input frequency	f_s = 48 kHz	–	12.288	–	MHz
		f_s = 44.1 kHz	–	11.2896	–	MHz
		f_s = 32 kHz	–	8.192	–	MHz
t_r	rise time		–	–	7	ns
t_f	fall time		–	–	7	ns
t_{cH}	HIGH time		35	–	–	ns
t_{cL}	LOW time		35	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs FSYNC, FRESET, FDIR, FDWS, L3MODEM, L3CLKM, L3DATAM and L3DATAC; referenced to CLK24 rising edge; see Fig.20; SLEEP = RESET = POR = logic 0						
t_{su}	set-up time		15	–	–	ns
t_h	hold time		20	–	–	ns
t_r	rise time		–	–	200	ns
t_f	fall time		–	–	200	ns
Inputs FDAI, FDCL, FDWS, FRESET and FDIR; referenced to FS256 rising edge; SLEEP = RESET = POR = logic 0						
t_{su}	set-up time		15	–	–	ns
t_h	hold time		20	–	–	ns
t_r	rise time		–	–	200	ns
t_f	fall time		–	–	200	ns
Output FDAO; referenced to FS256 rising edge; see Fig.21; SLEEP = RESET = POR = logic 0						
t_h	hold time	C_L = 7.5 pF	0	–	–	ns
t_d	delay time	C_L = 30 pF	–	–	30	ns
t_{d3}	output delay time after FDCL HIGH	see Fig.22	$2T_{c256} - 10^{(1)}$	–	–	ns
t_{d4}	output delay time after FDCL HIGH	see Fig.22	–	–	$3T_{c256} + 60^{(1)}$	ns
Input FDCL; see Fig.22						
T_c	FDCL period		280	$4T_{c256}^{(1)}$	–	ns
t_{cH}	FDCL HIGH time		$T_{c256} + 35^{(1)}$	–	–	ns
t_{cL}	FDCL LOW time		$T_{c256} + 35^{(1)}$	–	–	ns
Inputs FDAI and FDWS; see Fig.22						
t_{su1}	set-up time before FDCL HIGH		$3T_{c256} + 60^{(1)}$	–	–	ns
t_{h1}	hold time after FDCL HIGH		$T_{c256} + 20^{(1)}$	–	–	ns
Input FRESET; see Fig.4						
t_H	FRESET HIGH time		1280	–	–	ns
t_{su}	FDIR set-up time before FRESET LOW		0	210	–	ns
t_h	FDIR hold time after FRESET LOW		$9T_{c24}^{(2)}$	370	–	ns
SLEEP and RESET timing; see Fig.5; LOWPWR = logic 1						
t_h	RESET hold time after SLEEP LOW		$5T_{c24}^{(2)}$	210	–	ns
t_d	CLK24 disable after SLEEP HIGH		$9T_{c24}^{(2)}$	370	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L3 interface timing; microcontroller to SAA2013						
ADDRESS MODE; SEE FIG.16						
t_{d1}	L3MODEM LOW to L3CLKM LOW		190	–	–	ns
t_{cH}	L3CLKM HIGH time		250	–	–	ns
t_{cL}	L3CLKM LOW time		250	–	–	ns
t_{su1}	L3DATAM input set-up time before L3CLKM HIGH		190	–	–	ns
t_{h1}	L3DATAM input hold time after L3CLKM HIGH		30	–	–	ns
t_{h2}	L3CLKM HIGH before L3MODEM HIGH		190	–	–	ns
DATA MODE; SEE FIG.17						
t_{d1}	L3MODEM HIGH to L3CLKM LOW delay time		190	–	–	ns
t_{cH}	L3CLKM HIGH time		250	–	–	ns
t_{cL}	L3CLKM LOW time		250	–	–	ns
t_{su1}	L3DATAM input set-up time before L3CLKM HIGH		190	–	–	ns
t_{h1}	L3DATAM input hold time after L3CLKM HIGH		30	–	–	ns
t_{h2}	L3CLKM HIGH before L3MODEM LOW		190	–	–	ns
t_{d3}	L3MODEM HIGH to L3DATAM output valid		–	–	380	ns
t_{h3}	L3DATAM output hold time after L3CLKM HIGH		120	–	–	ns
t_{d4}	L3CLKM HIGH to L3DATAM output valid delay time		–	–	360	ns
		between bits 7 and 8; no halt mode used	–	–	530	ns
t_{d2}	L3MODEM HIGH to L3DATAM output enabled delay time		0	–	50	ns
t_{d5}	L3MODEM LOW to L3DATAM output disabled delay time		0	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HALT MODE; SEE FIG.18						
t_L	L3MODEM LOW time		190	–	–	ns
t_{d1}	L3MODEM HIGH to L3CLKM HIGH delay time		190	–	–	ns
t_{h2}	L3CLKM HIGH before L3MODEM LOW		190	–	–	ns
t_{d2}	L3MODEM HIGH to L3DATAM output enabled delay time		0	–	50	ns
t_{d5}	L3MODEM LOW to L3DATAM output disabled delay time		0	–	50	ns
L3 interface timing; SAA2013 to SAA2003						
ADDRESS MODE; SEE FIG.14						
t_{d1}	L3MODEC LOW to L3CLKC LOW delay time		190	–	–	ns
t_{cH}	L3CLKC HIGH time		210	–	–	ns
t_{cL}	L3CLKC LOW time		210	–	–	ns
t_{h2}	L3CLKC HIGH time before L3MODEC HIGH		190	–	–	ns
t_{d3}	L3MODEC LOW to L3DATAC output valid delay time		–	–	380	ns
t_{h1}	L3DATAC output hold time after L3CLKC HIGH		120	–	–	ns
t_{d4}	L3CLKC HIGH to L3DATAC output valid delay time		–	–	360	ns
t_{d2}	L3MODEC LOW to L3DATAC output enabled delay time		0	–	50	ns
t_{d5}	L3MODEC HIGH to L3DATAC output disabled delay time		0	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DATA MODE; SEE FIG.15						
t_{d1}	L3MODEC HIGH to L3CLKC LOW		190	–	–	ns
t_{cH}	L3CLKC HIGH time		210	–	–	ns
t_{cL}	L3CLKC LOW time		210	–	–	ns
t_{su1}	L3DATAC input set-up time before L3CLKC HIGH		100	–	–	ns
t_{h1}	L3DATAC input hold time after L3CLKC HIGH		30	–	–	ns
t_{h2}	L3CLKC HIGH time before L3MODEC LOW		190	–	–	ns
t_{d3}	L3MODEC HIGH to L3DATAC output valid		–	–	380	ns
t_{h3}	L3DATAC output hold time after L3CLKC HIGH		120	–	–	ns
t_{d4}	L3CLKC HIGH to L3DATAC output valid		–	–	360	ns
		between bits 7 and 8; no halt mode used	–	–	530	ns
HALT MODE; SEE FIG.18						
t_L	L3MODEC LOW time		190	–	–	ns
t_{d1}	L3MODEC HIGH to L3CLKC HIGH delay time		190	–	–	ns
t_{h2}	L3CLKC HIGH time before L3MODEC LOW		190	–	–	ns
L3 interface delays in bypassed mode; LOWPWR = logic 1						
t_{pd1}	propagation delay from L3MODEM to L3MODEC; L3DATAM to L3DATAC; L3CLKM to L3CLKC		–	–	35	ns
t_{pd2}	propagation delay from L3DATAM to L3DATAC; L3CLKM to L3CLKC		–20	–	+4	ns
t_{pd3}	propagation delay from L3DATAM to L3DATAC; L3MODEM to L3MODEC		–20	–	+4	ns

Notes

1. T_{c256} is a clock period of FS256.
2. T_{c24} is a clock period of CLK24.

Tape formatting and error correction for the DCC system

SAA2022

FEATURES

- Integrated error correction encoder/decoder function with Digital Compact Cassette (DCC) optimized algorithms
- Control of capstan servo during recording and after recording by microcontroller
- Frequency and phase regulation of capstan servo during playback
- Choice of two Dynamic Random Access Memory (DRAM) types operating in page mode
- Scratch pad RAM area available to microcontroller in system DRAM
- Low power standby mode
- I^2S interface
- Microcontroller interface for high-speed transfer burst rates up to 170 kbytes per second
- SYSINFO and AUXILIARY data flags on microcontroller interface
- Protection against invalid AUXILIARY data
- +4 V operating voltage capability.

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

Performing the tape formatting and error correction functions for DCC applications, the SAA2022 can be used in conjunction with the PASC (SAA2002/SAA2012), tape equalization (SAA2032), read amplifier (TDA1317 or TDA1318) and write amplifier (TDA1316 or TDA1319) circuits to implement a full signal processing system.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2022GP	64	QFP[1]	plastic	SOT208A

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* are followed. The pocketbook can be ordered using the code 9398 510 34011.

BLOCK DIAGRAM

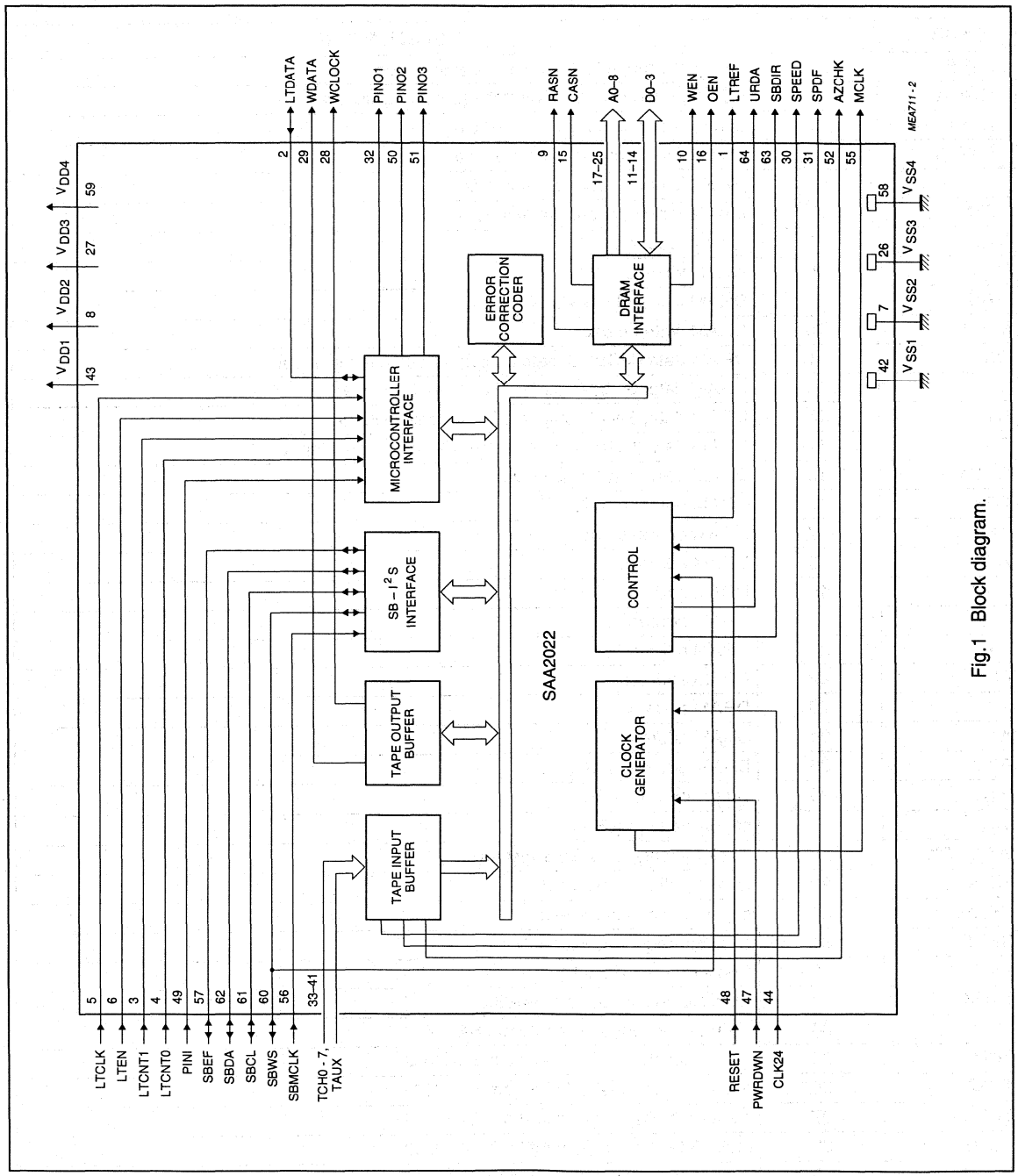


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LTREF	1	timing reference for microcontroller interface
LTDATA	2	data for microcontroller interface (3-state; CMOS levels)
LTCNT1	3	control for microcontroller interface
LTCNT0	4	control for microcontroller interface
LTCLK	5	bit clock for microcontroller interface
LTEN	6	enable for microcontroller interface
V_{SS2}	7	supply ground (0 V)
V_{DD2}	8	supply voltage (+5 V)
RASN	9	DRAM row address strobe
WEN	10	DRAM write enable
D3	11	DRAM data (MSB); 3-state output; TTL compatible input
D2	12	DRAM data; 3-state output; TTL compatible input
D1	13	DRAM data; 3-state output; TTL compatible input
D0	14	DRAM data (LSB); 3-state output; TTL compatible input
CASN	15	DRAM column address strobe
OEN	16	DRAM output enable
A8	17	DRAM address (MSB)
A7	18	DRAM address
A6	19	DRAM address
A5	20	DRAM address
A4	21	DRAM address
A3	22	DRAM address
A2	23	DRAM address
A1	24	DRAM address
A0	25	DRAM address (LSB)
V_{SS3}	26	supply ground (0 V)
V_{DD3}	27	supply voltage (+5 V)
WCLOCK	28	clock for write amplifier transfers
WDATA	29	write amplifier serial data
SPEED	30	capstan phase information
SPDF	31	capstan frequency information
PINO1	32	Port expander output 1
TAUX	33	AUX channel input from SAA2032
TCH7	34	main data channel 7, input from SAA2032
TCH6	35	main data channel 6, input from SAA2032
TCH5	36	main data channel 5, input from SAA2032
TCH4	37	main data channel 4, input from SAA2032
TCH3	38	main data channel 3, input from SAA2032
TCH2	39	main data channel 2, input from SAA2032

SYMBOL	PIN	DESCRIPTION
TCH1	40	main data channel 1, input from SAA2032
TCH0	41	main data channel 0, input from SAA2032
V_{SS1}	42	supply ground (0 V)
V_{DD1}	43	supply voltage (+5 V)
CLK24	44	24.576 MHz clock from SAA2002
TEST0	45	test select LSB; **do not connect**
TEST1	46	test select MSB; **do not connect**
PWRDWN	47	sleep mode selection
RESET	48	reset input with hysteresis and pull-down resistor
PINI	49	Port expander input
PINO2	50	Port expander output 2
PINO3	51	Port expander output 3
AZCHK	52	azimuth check (channels 0 and 7)
TEST2	53	symbol error rate measurement output
TEST3	54	**do not connect**
MCLK	55	master clock output (6.144 MHz)
SBMCLK	56	master clock for SB-I²S-interface
SBEF	57	byte error SB-I²S-interface
V_{SS4}	58	supply ground (0 V)
V_{DD4}	59	supply voltage (+5 V)
SBWS	60	word select SB-I²S-interface; 3-state output; CMOS levels
SBCL	61	bit clock SB-I²S-interface; 3-state output; CMOS levels
SBDA	62	data line SB-I²S-interface; 3-state output; CMOS levels
SBDIR	63	direction SB-I²S-interface
URDA	64	unusable data SB-I²S-interface

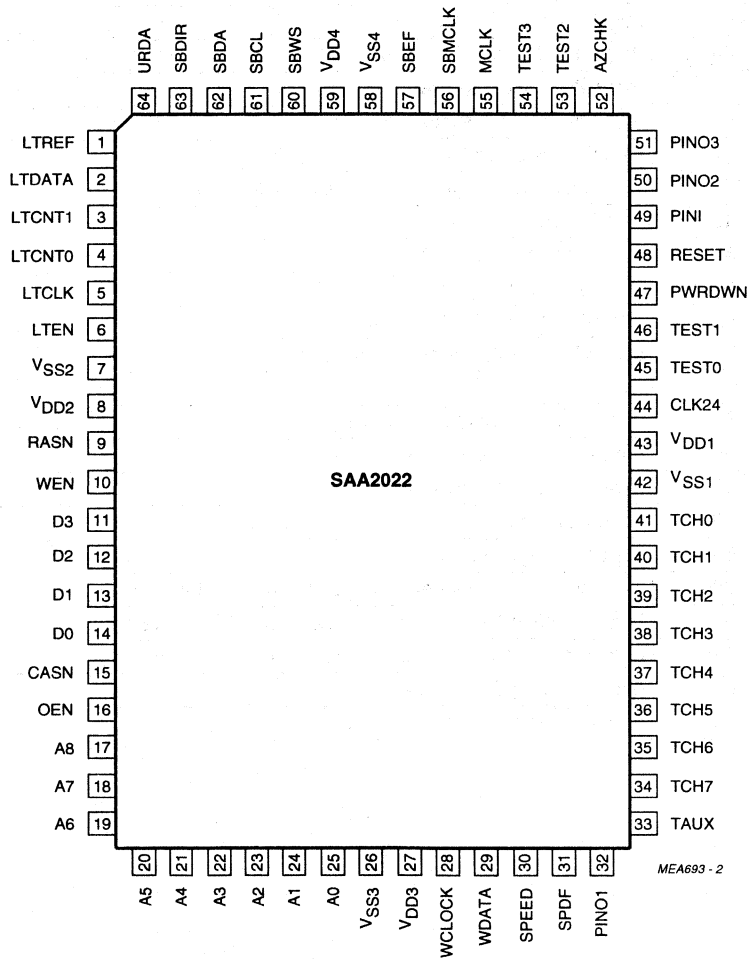


Fig.2 Pin configuration (SOT208A).

FUNCTIONAL DESCRIPTION

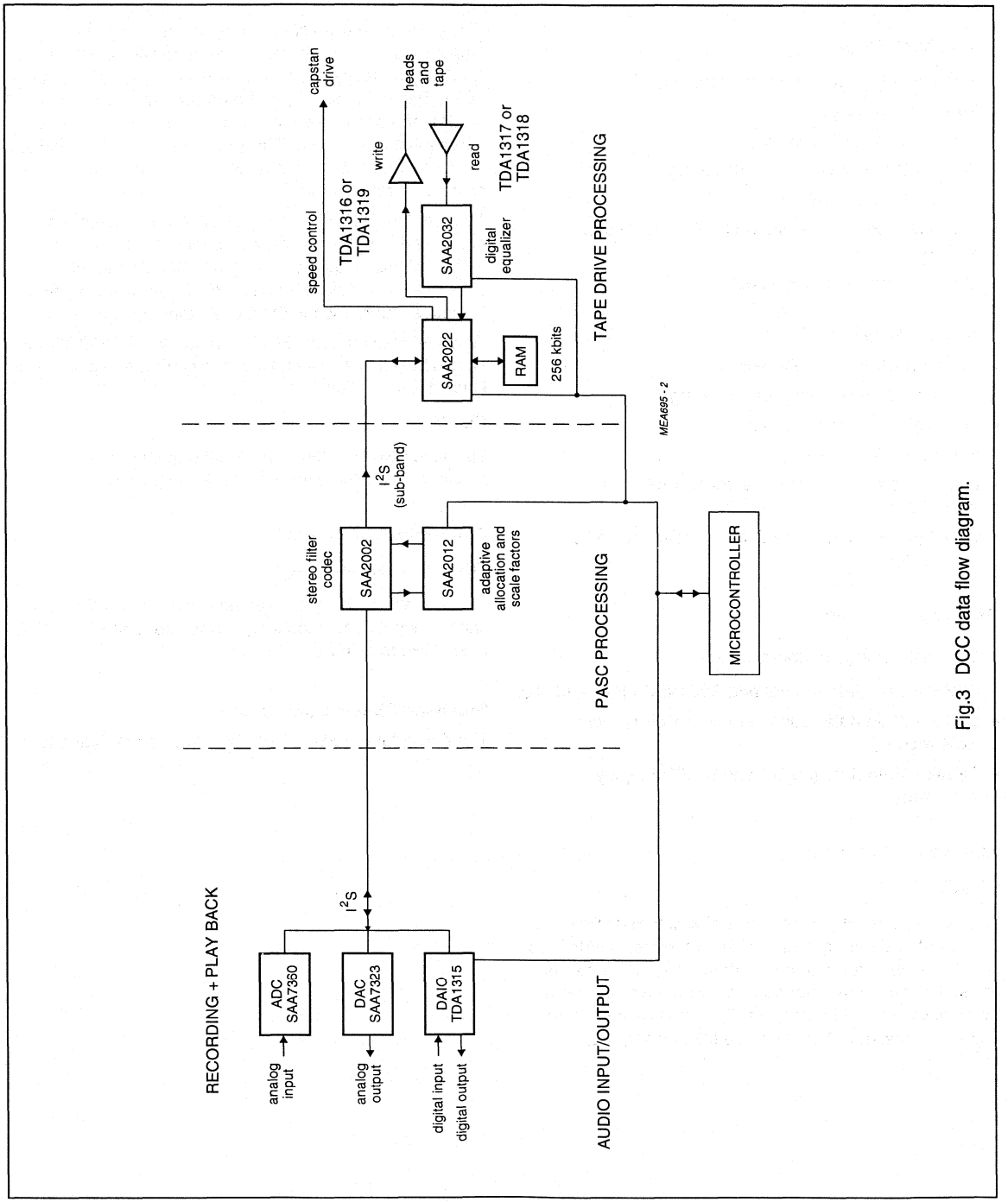


Fig.3 DCC data flow diagram.

Tape formatting and error correction for the DCC system

SAA2022

The SAA2022 provides the following functions:

In Playback Modes

- Tape channel data and clock recovery
- 10 to 8 demodulation
- Data placement in DRAM
- C1 and C2 error correction decoding
- I²S-interfacing to SB-I²S-bus
- Interfacing to microcontroller for SYSINFO and AUX data
- Capstan control for tape deck.

In Record Modes

- I²S-interfacing to SB-I²S-bus
- C1 and C2 error correction encoding
- Formatting for tape transfer
- 8 to 10 modulation
- Interfacing to microcontroller for SYSINFO and AUX data
- Capstan control for tape deck, programmable by microcontroller.

Operational Modes

The 3 basic modes of operation are:

- DPAP - Main data (audio) and SYSINFO play, AUX play
- DRAR - Main data (audio) and SYSINFO record, AUX record
- DPAR - Main data (audio) and SYSINFO play, AUX record.

Hardware Interfacing

RESET

This is an active HIGH input signal which resets the SAA2022 and brings it into its default mode, DPAP. This should be connected to the system reset, which can be driven by the microcontroller. The duration of the reset pulse should be at least 15 μs. This pin has an internal pull-down resistor of between 20 kΩ and 125 kΩ.

PWRDWN

This pin is an active HIGH signal which places the SAA2022 in a "SLEEP" mode. When the SAA2022 is in "SLEEP" mode and the CLK24 is either held HIGH or held LOW, there is no activity in the device, thus resulting in no EMI and a low power dissipation (typically <10% of operational dissipation). This pin should be connected to the DCC power-down signal, which can be driven by the system microcontroller.

To enter the "SLEEP" mode the SAA2022 should reset and hold reset. After a delay of at least 15 μs the PWRDWN pin should be brought HIGH after which the state of the reset pin is "don't care". The power dissipation is reduced further when the CLK24 input signal stops.

When recovering from "SLEEP" mode the PWRDWN pin should be driven LOW and the chip reset with a pulse of at least 15 μs duration.

CLK24

This is the 24.576 MHz clock input and should be connected directly to the SAA2002 CLK24 pin.

Connections to SAA2032

TCH0 TO TCH7 AND TAUX

These lines are the equalized and clipped (to V_{DD}) tape channel inputs and should be connected to the SAA2032 pins TCH0 to TCH7 and TAUX.

Sub-band I²S-bus Connections

The timing for the SB-I²S-interface is given in Figs 4 to 9.

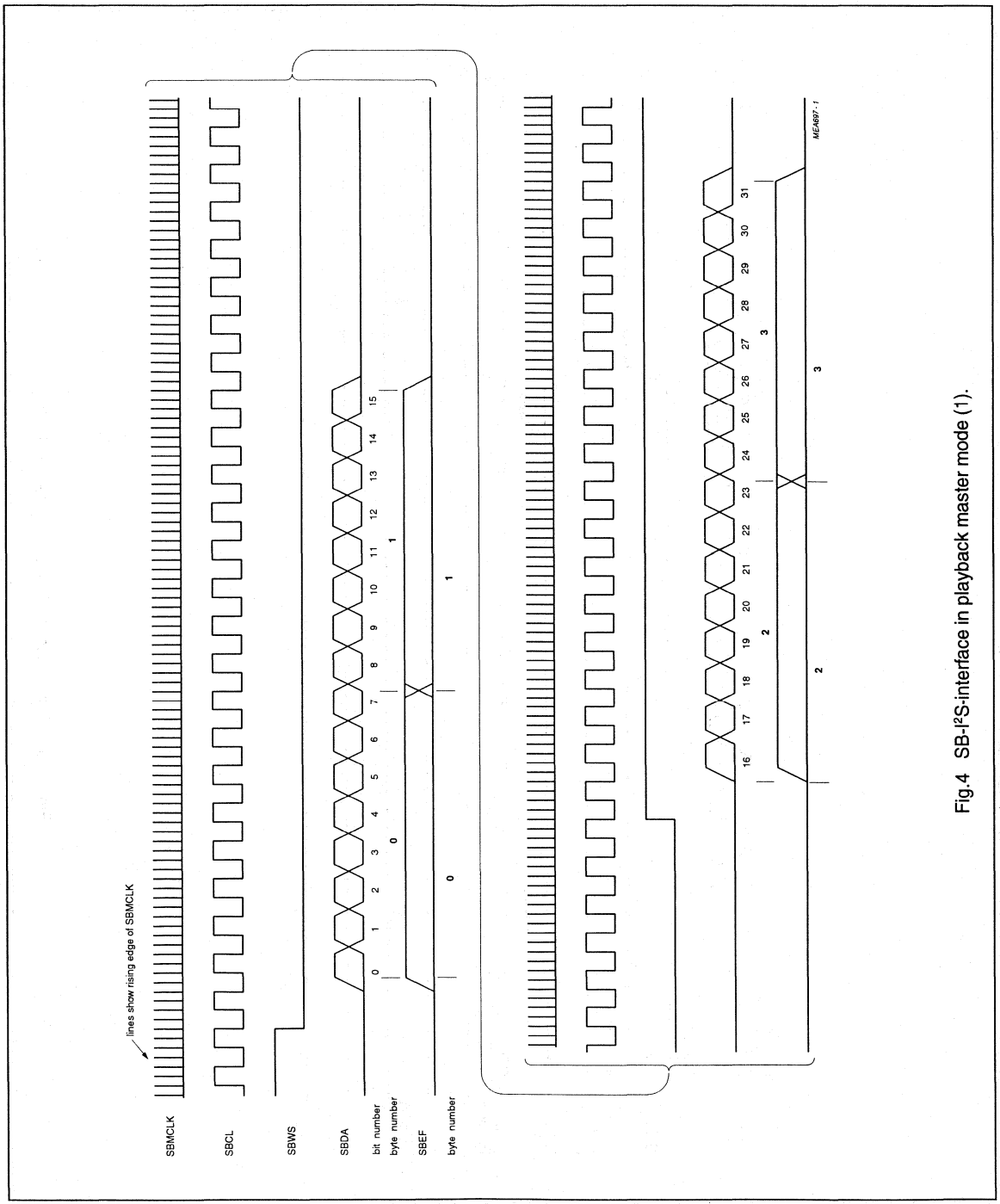


Fig.4 SB-I²S-interface in playback master mode (1).

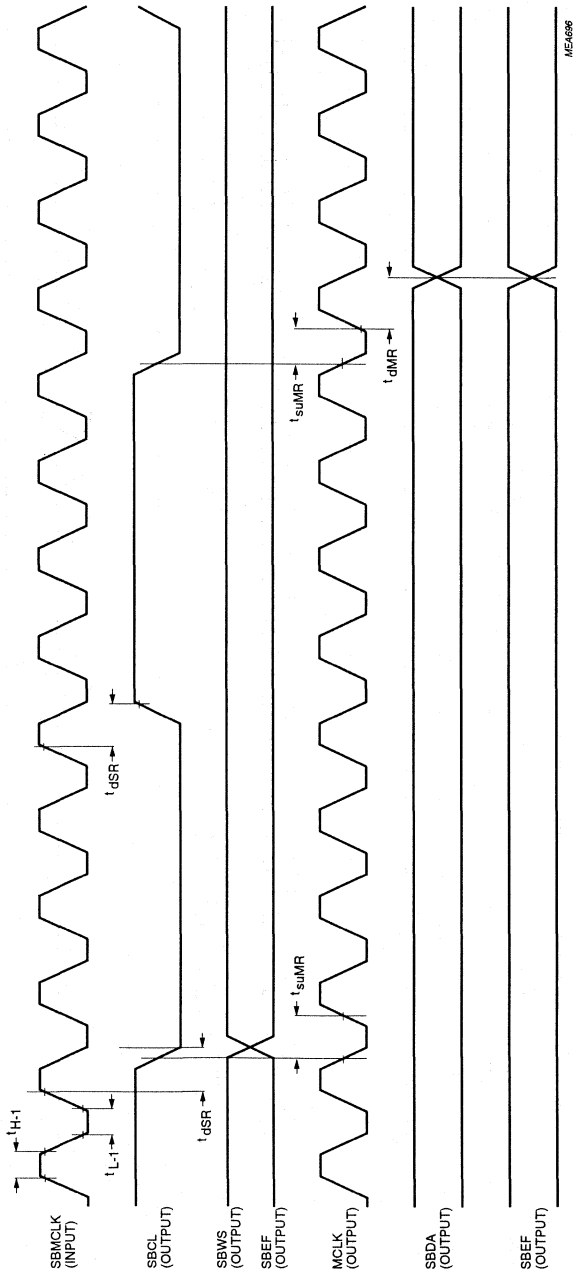


Fig.5 SB-I²S-interface in playback master mode (2).

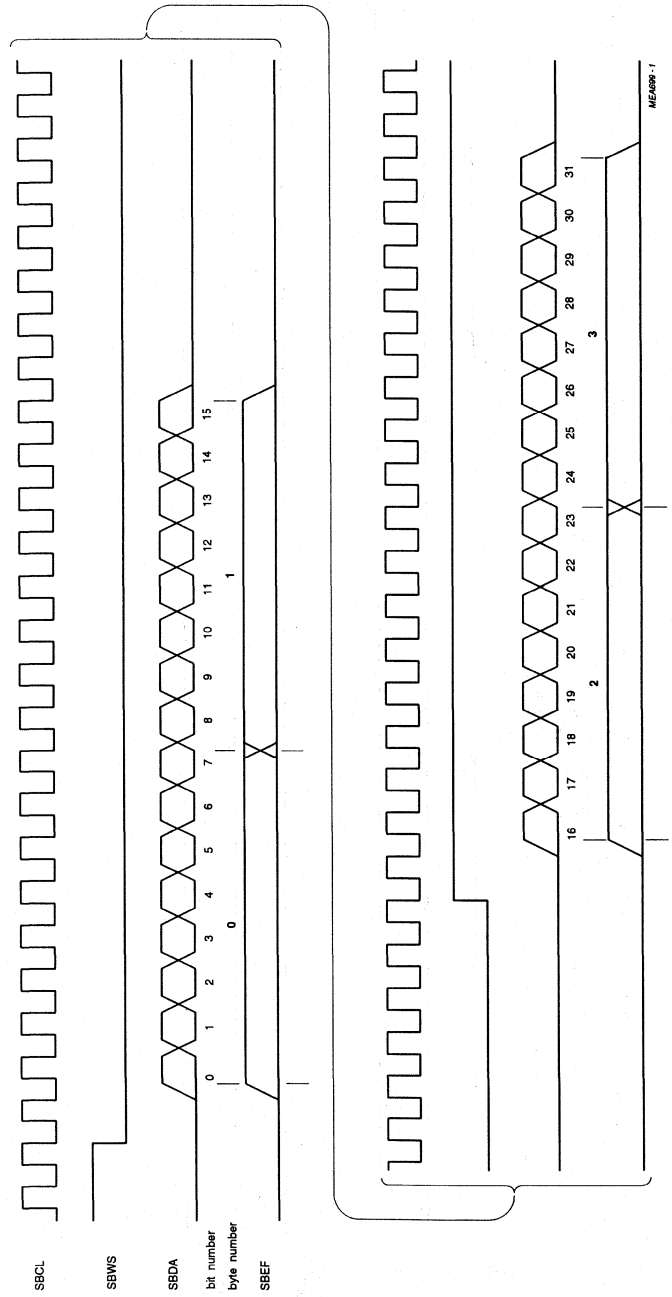


Fig.6 SB-I²S-interface in playback slave mode (1).

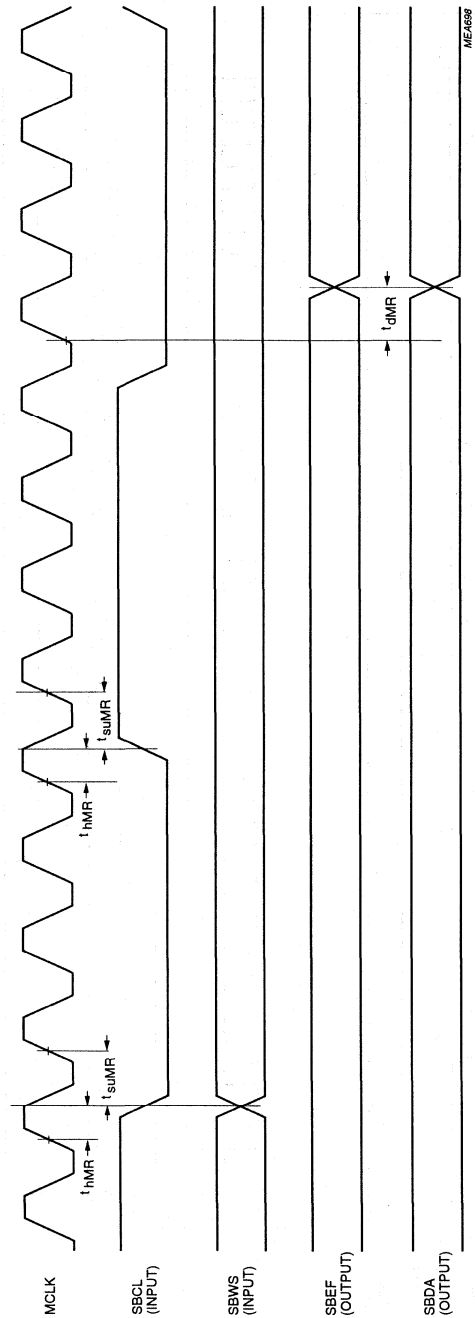


Fig.7 SB-I²S-interface in playback slave mode (2).

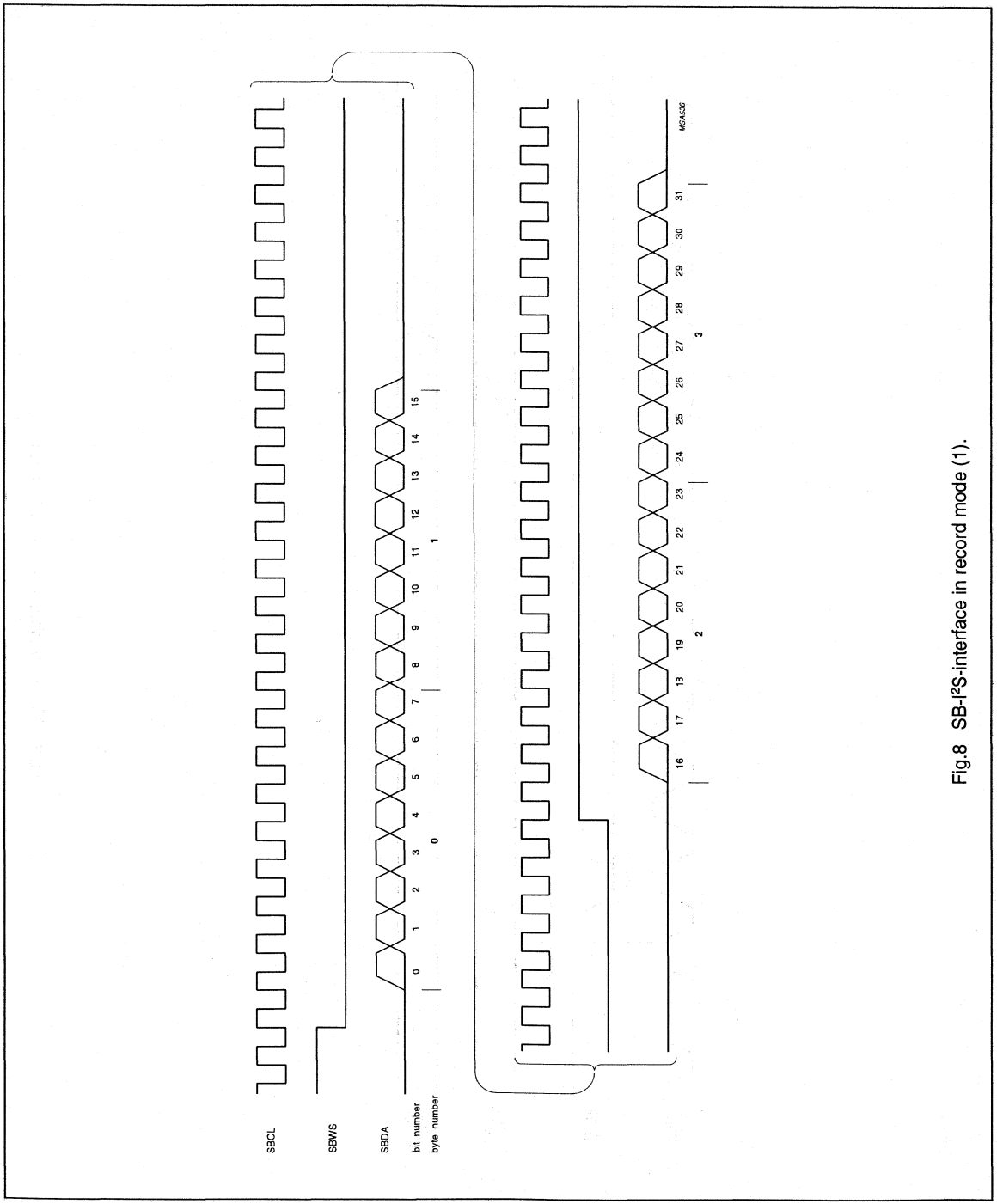


Fig.8 SB-I²S-interface in record mode (1).

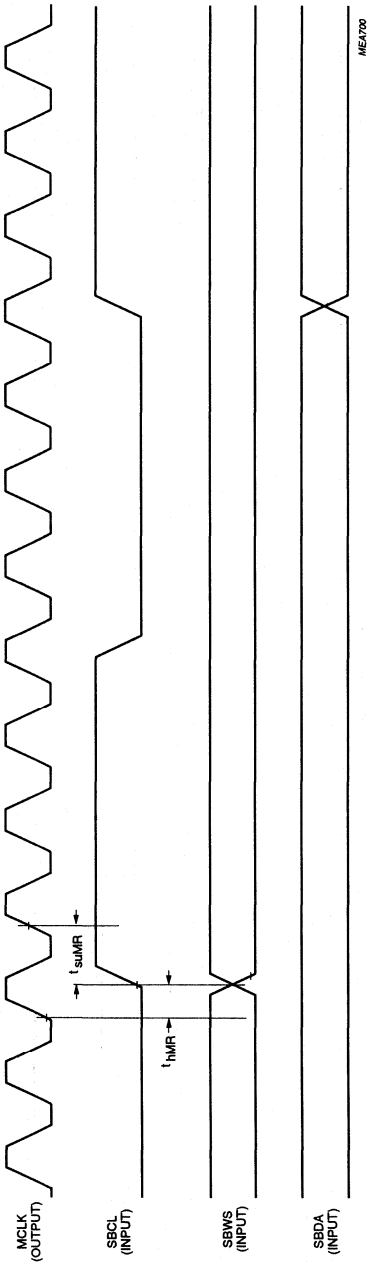


Fig.9 SB-I²S-interface in record mode (2).

SBMCLK

This is the sub-band master clock input for the SB-I²S-interface. The frequency of this signal is nominally 6.144 MHz. This pin should be connected to the SBMCLK pin of the SAA2002.

SBDIR

This output pin is the sub-band I²S-bus direction signal, it indicates the direction of transfer on the SB-I²S-bus. A logic 1 indicates a SAA2022 to SAA2002 transfer (audio play) whilst a logic 0 is output for a SAA2002 to SAA2022 transfer (audio record). This pin connects directly to the SBDIR pin on the SAA2002.

SBCL

This input/output pin is the bit clock line for the SB-I²S-interface to the SAA2002. Is has a nominal frequency of 768 kHz.

SBWS

This input/output pin is the word select line for the SB-I²S-interface to the SAA2002. It has a nominal frequency of 12 kHz.

SBDA

This input/output pin is the serial data line for the SB-I²S-interface to the SAA2002.

SBEF

This active HIGH output pin is the error per byte line for the SB-I²S-interface to the SAA2002.

URDA

This active HIGH output pin indicates that the main data (audio), the SYSINFO and the AUXILIARY data are **not** usable, regardless of the state of the corresponding reliability flags. The state of this pin is reflected in the URDA bit of STATUS byte 0, which can be read by the microcontroller. This pin should be connected directly to the URDA pin of the SAA2002. URDA is activated as a result of a reset, a mode change from DRAR to DPAP, or if the SAA2022 has had to resynchronize with the incoming data from tape.

The position of the first SB-I²S-bytes in a tape frame is shown in Fig.10.

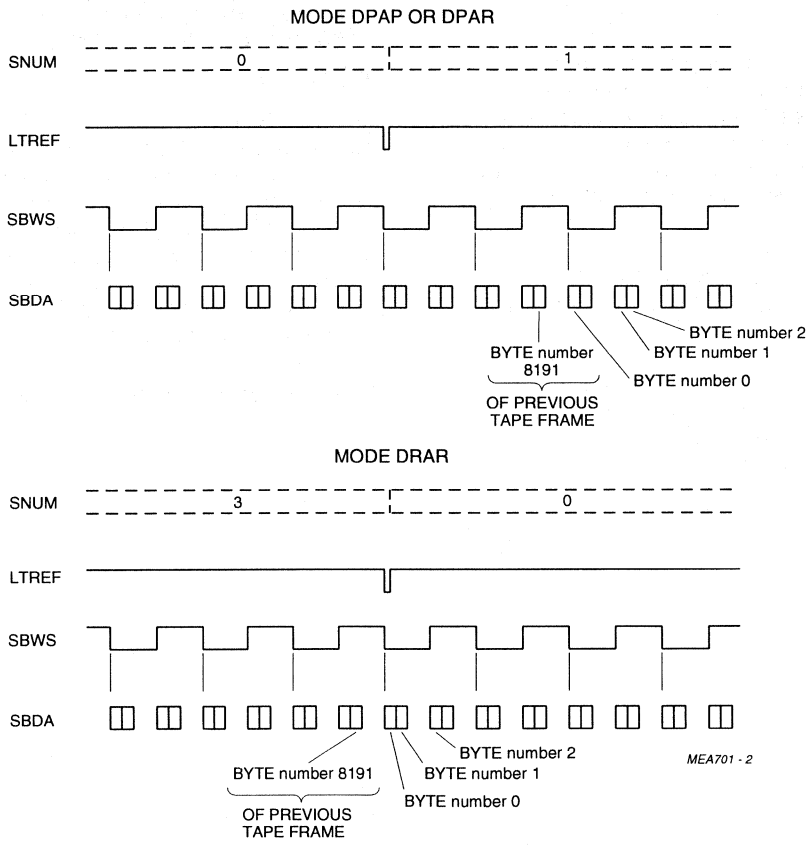


Fig.10 Position of first SB-I²S-bytes in tape frame.

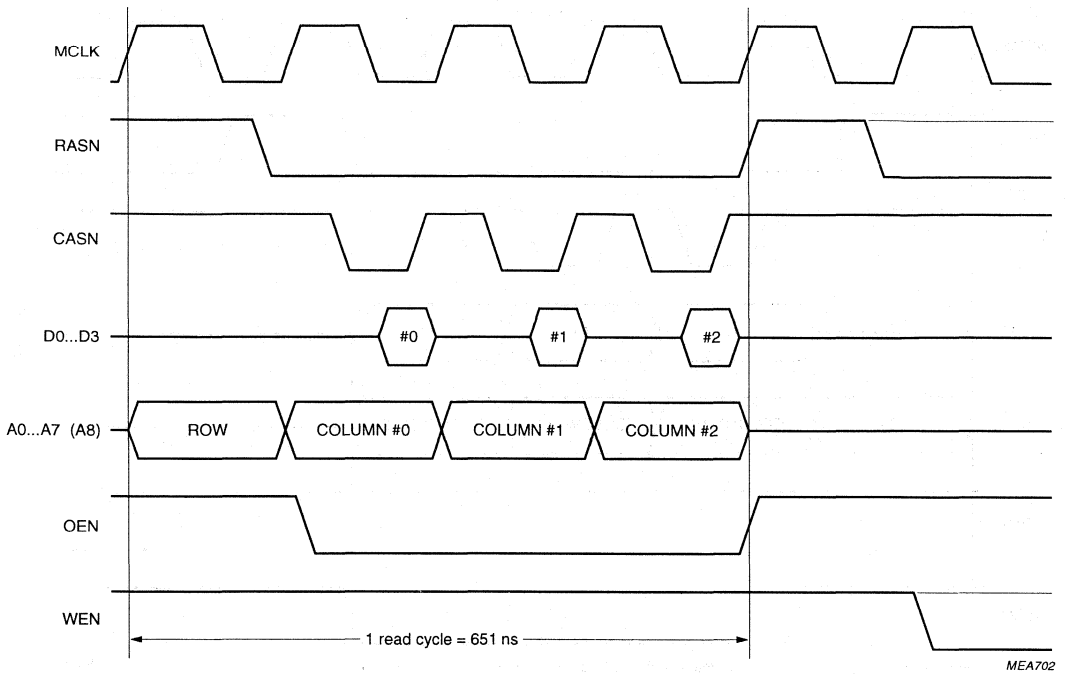


Fig.11 DRAM timing read cycle.

DRAM Interface

The SAA2022 has been designed to operate with 64 k × 4-bit or 256 k × 4-bit DRAMs operating in page mode, with an access time of 80 to 100 ns. The timing for read, write and refresh cycles is shown in Figs 11 to 13.

CASN

This output pin is the column address strobe (active LOW) for the DRAM, it connects directly to the column address strobe pin of the DRAM.

RASN

This output pin is the row address strobe (active LOW) for the DRAM, it connects directly to the row address strobe pin of the DRAM.

OEN

This pin provides the output enable (active LOW) for the DRAM, it connects directly to the output enable pin of the DRAM.

WEN

This output pin provides the write enable (active LOW) for the DRAM, it connects directly to the write enable pin of the DRAM.

A0 TO A8

These output pins are the multiplexed column and row address lines for the DRAM. When the 64 k × 4-bit DRAM is used, pins A0 to A7 should be connected to the DRAM address input pins, and pin A8 should be left unconnected. When using the 256 k × 4-bit DRAM then address pins A0 to A8 should be connected to the address input pins of the DRAM.

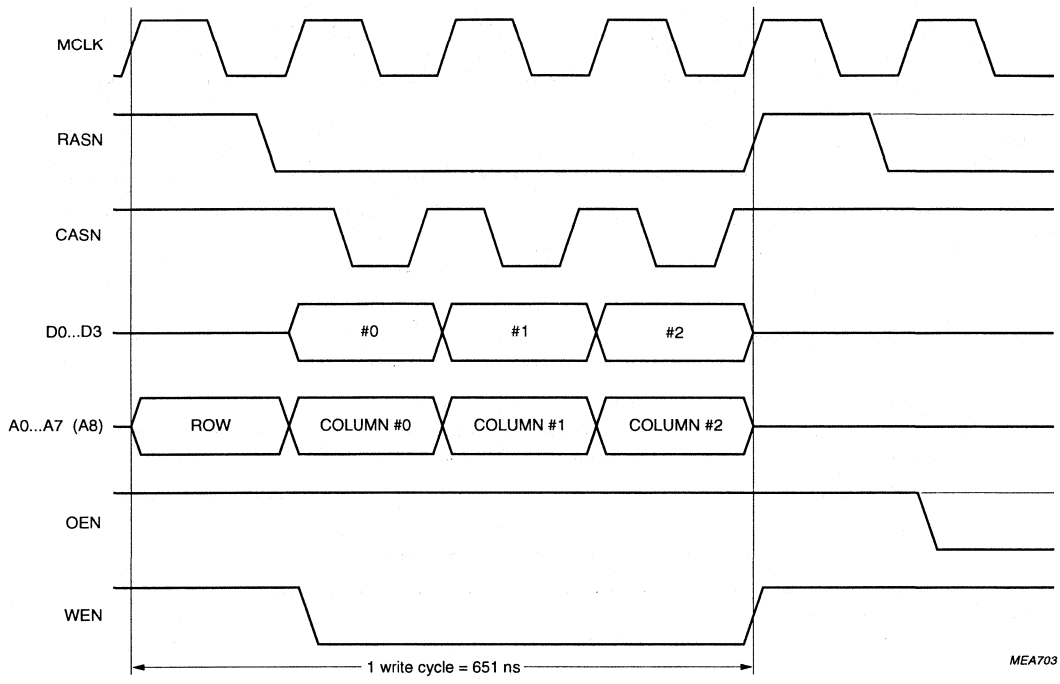


Fig.12 DRAM write cycle.

D0 TO D3

These input/output pins are the data lines for the DRAM, they should be connected directly to the DRAM data I/O pins.

Write amplifier interface

The SAA2022 may be used with either the TDA1316 or TDA1319 write amplifiers.

WCLOCK

This output pin provides the 3.072 MHz clock output for the WRITE AMPLIFIER, it should be connected directly to the WCLOCK pin of the WRITE AMPLIFIER.

WDATA

This output pin is the multiplexed data and control line for the WRITE AMPLIFIER (timing information is shown in Fig.14). The WDATA pin should be connected directly to the WDATA pin of the WRITE AMPLIFIER.

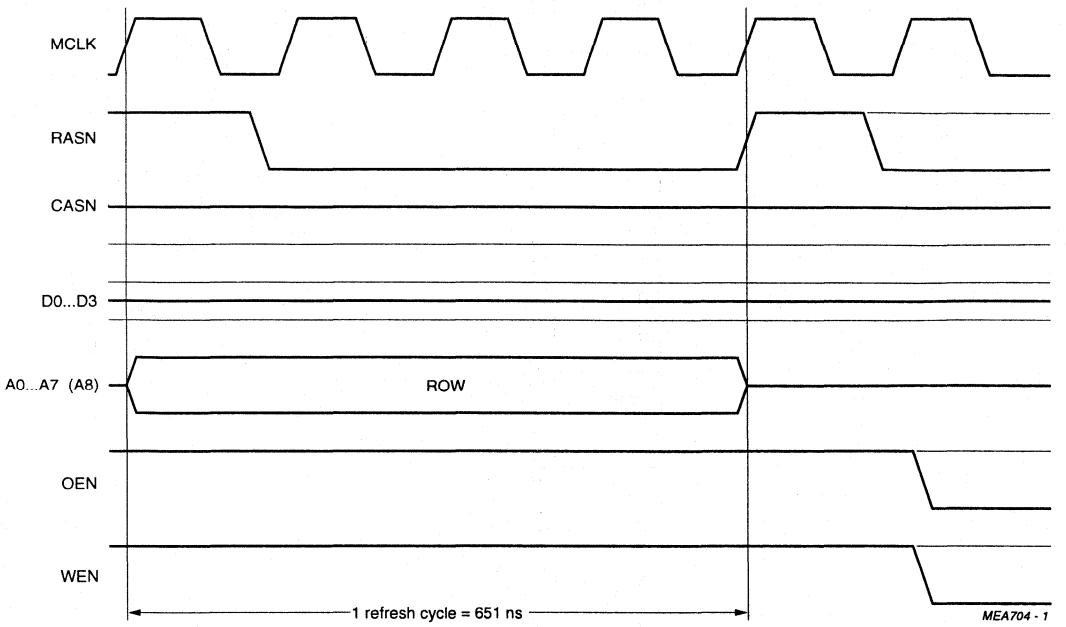


Fig.13 DRAM refresh cycle.

Tape deck capstan control interface

SPEED

This signal is a pulse width modulated output that may be used to control the tape deck capstan. The period of the SPEED signal is 41.66 µs and the nominal duty cycle is 50%.

There are 4 modes of operation for the SPEED signal which can be selected by the programmed settings of µCSPD (microcontroller capstan speed), ENFREG (enable frequency regulation) and ENEFREG (enable extended frequency regulation) flags.

SPDF

If µCSPD = logic 0 this pin outputs a pulse width modulated measurement of the main data channel bit rates and may be used in combination with the SPEED signal to control the tape deck capstan. The period of the SPDF signal is 5.2 µs. The duty cycle of SPDF can vary from 0% at +6.5% deviation to 100% at –6.5% deviation. If the deviation = 0% then the duty cycle of SPDF is 50%.

Microcontroller Interface

LTREF

The SAA2022 divides time into segments of 42.67 ms nominal duration which are counted in modulo 4. The LTREF active LOW output pin can be connected directly to the interrupt input of the microcontroller and indicates the start of a time segment. It goes LOW for 5.2 µs once every 42.66 ms and can be used for generating interrupts. Note if a resync occurs then the time between the occurrences of LTREF can vary. The function and programming of the other interface lines LTCNT0, LTCNT1, LTEN, LTCLK and LTDATA are described in the pinning and programming sections.

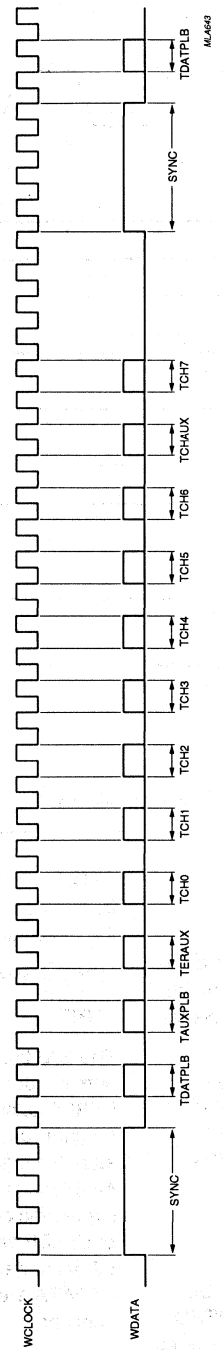


Fig.14 WDATA and WCLOCK timing.

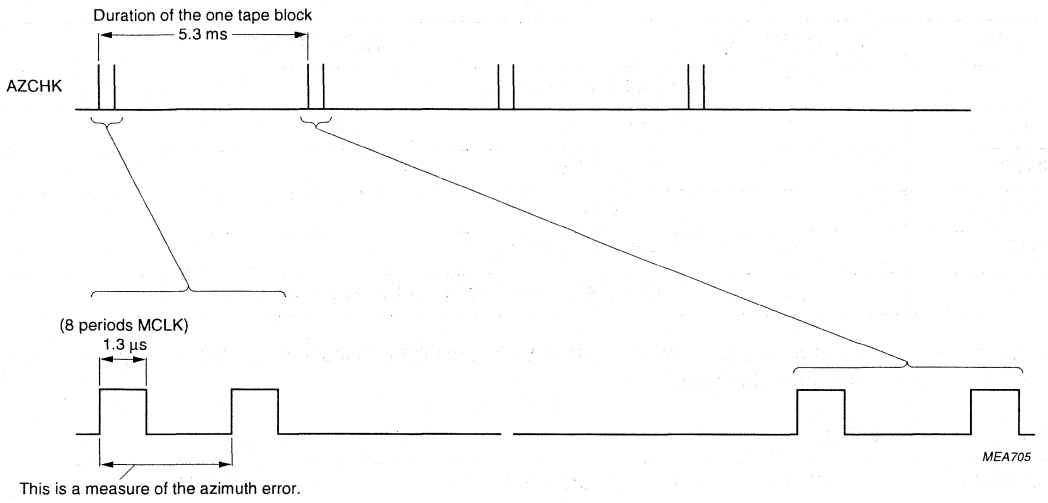


Fig.15 AZCHK timing.

Test Pins

TEST0, TEST1, TEST2 AND TEST 3

These input pins are for test use only and for normal operation should **not** be connected.

AZCHK

This output pin indicates the occurrence of a tape channel sync symbol on tape channels TCH0 and TCH7. The separation between the pulses for the TCH0 and TCH7 channels gives a measure of the azimuth error between the tape and head alignment (see Fig.15).

Port Expansion Pins

PINI

This input pin is connected directly to the PINI bit in the STATUS byte 1, it can be read by the microcontroller, and may be used for any CMOS level compatible input signals.

PINO1

This output pin is connected directly to the PINO1 bit of the SETTINGS byte 1 register and can be set or reset by the microcontroller.

PINO2

This output pin is connected directly to the PINO2 bit of the SETTINGS byte 1 register and can be set or reset by the microcontroller.

PINO3

This output pin is connected directly to the PINO3 bit of the SETTINGS byte 1 register and can be set or reset by the microcontroller.

Power Supply Pins

V_{DD1} TO V_{DD4}

These are the +5 V power supply pins which must all be connected. Decoupling of V_{SS1} to V_{SS4} is recommended.

V_{SS1} TO V_{SS4}

These are the +5 V power supply ground pins, all of which must be connected.

Programming the SAA2022 via the Microcontroller Interface

Table 1 SAA2022 interface connections to the microcontroller.

PIN	INPUT/OUTPUT	DESCRIPTION
LTEN	I	enable active HIGH
LTCLK	I	clock signal
LTCNT0	I	control LSB
LTCNT1	I	control MSB
LTDATA	I/O	bi-directional data
LTREF	O	timing reference 5 µs at start of every segment active LOW

All transfers are in units of 8-bits, registers with less than 8-bits are LSB justified, unless otherwise specified. The four basic types of transfer are shown in Table 2.

Table 2 Types of transfer.

LTCNT1	LTCNT0	TRANSFER	EXPLANATION
0	0	WDAT	write DATA to SAA2022
0	1	RDAT	read DATA from SAA2022
1	0	WCMD	write Command to SAA2022
1	1	RSTAT	read Status from SAA2022

Microcontroller Interface Registers

The SAA2022 microcontroller interface has 7 write and 4 read registers, as shown in Table 3.

Table 3 SAA2022 Microcontroller Interface Registers.

REGISTER	READ/WRITE	NO. OF BITS	COMMENTS
SET0	WRITE	7	primary settings
SET1	WRITE	8	secondary settings
CMD	WRITE	6	microcontroller command
BYTCNT	WRITE	8	byte counter
RACCNT	WRITE	7	random access counter
SPDDTY	WRITE	8	duty cycle for SPEED
AFLEV	WRITE	4	AUXILIARY flag level
STATUS0	READ	8	primary status
STATUS1	READ	7	secondary status
STATUS2	READ	8	SYSINFO/AUX flags
STATUS3	READ	8	channel status flags

Direct Access

Only one write (CMD) and four read (STATUS0 to STATUS3) registers can be directly accessed using the LTCNT lines, all other registers must be accessed by first programming the command register.

The four Status registers can be read by performing 4 RSTAT transfers within the same LTEN = HIGH period.

Indirect Access

To write to or read from the indirect access registers, a command must first be sent to the command register. The transfer of bytes can then occur using WDAT and RDAT type transfers. It is the responsibility of the microcontroller to ensure that the transfer type and the last command are compatible. The same type of transfer can continue until a new command is sent.

Typical transfers on the microcontroller interface are shown in Figs 16 to 19.

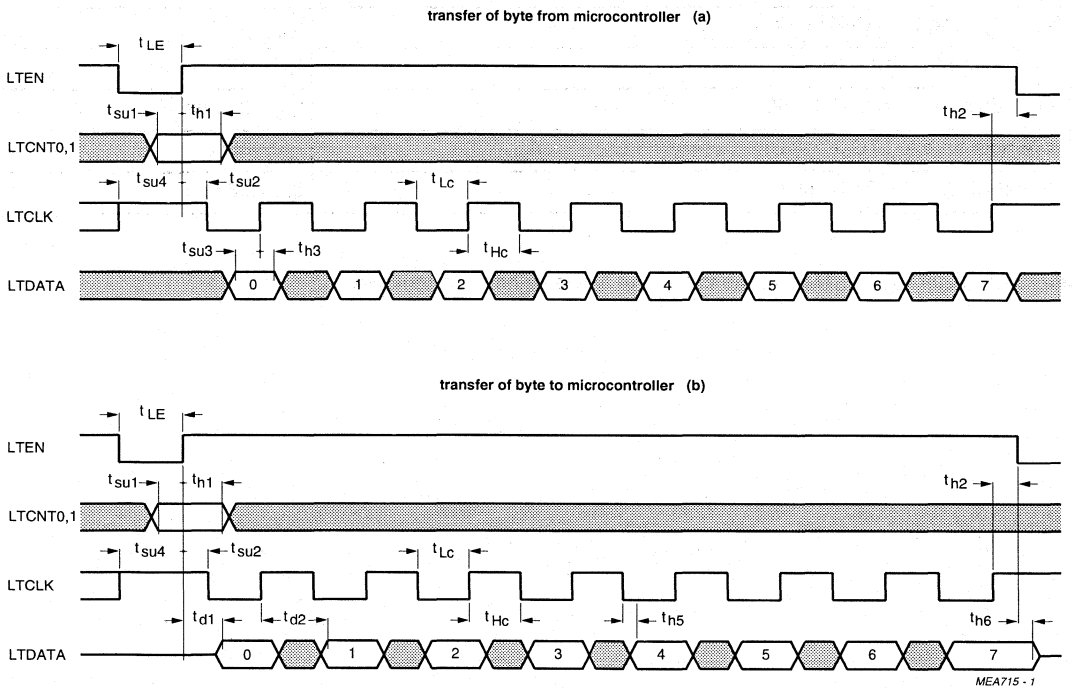


Fig.16 LT interface timing (1).

Notes to Fig.16a.

DESCRIPTION	TIMING
For the timing figures it is assumed that cycle time T_{cy} of MCLK is within the limits	160 ns < T_{cy} < 165 ns
The set-up time t_{su} of LTEN, LTCNT, LTCLK and LTDATA to MCLK HIGH	t_{su} < 40 ns
The hold time t_h of LTEN, LTCNT, LTCLK and LTDATA to MCLK HIGH	t_h = 0 ns
LTEN LOW time before start data transfer	t_{LE} > 535 ns; note 1
LTCLK LOW time	t_{Lc} > 205 ns
LTCLK HIGH time	t_{Hc} > 205 ns
LTCNT0/1 set-up time to LTEN HIGH	t_{su1} > 205 ns
LTCNT0/1 hold time to LTEN HIGH	t_{h1} > 205 ns
LTEN set-up time to LTCLK LOW	t_{su2} > 0 ns
LTEN hold time to LTCLK HIGH	t_{h2} > 205 ns
LTDATA set-up time to LTCLK HIGH	t_{su3} > 205 ns
LTDATA hold time to LTCLK HIGH	t_{h3} > 40 ns
LTCLK set-up time to LTEN HIGH	t_{su4} > 535 ns

Note

1. See interface timing (Fig.16b) for the transfer of a byte to the microcontroller.

Notes to Fig.16b.

DESCRIPTION	TIMING
For the timing figures it is assumed that cycle time T_{cy} of MCLK is within the limits	160 ns < T_{cy} < 165 ns
The set-up time t_{su} of LTEN, LTCNT, LTCLK and LTDATA to MCLK HIGH	t_{su} < 40 ns
The hold time t_h of LTEN, LTCNT, LTCLK and LTDATA to MCLK HIGH	t_h = 0 ns
The delay time t_d of LTDATA from MCLK HIGH is within the limits	0 ns < t_d < 30 ns
The delay time t_d of LTEN to the 3-state control of LTDATA	0 ns < t_d < 50 ns
LTEN LOW time before start data transfer	t_{LE} > 535 ns; note 1
LTCLK LOW time	t_{Lc} > 205 ns
LTCLK HIGH time	t_{Hc} > 205 ns
LTCNT0/1 set-up time to LTEN HIGH	t_{su1} > 205 ns
LTCNT0/1 hold time from LTEN HIGH	t_{h1} > 205 ns
LTEN set-up time to LTCLK LOW	t_{su2} > 0 ns
LTEN hold time from LTCLK HIGH	t_{h2} > 205 ns
LTCLK set-up time to LTEN HIGH	t_{su4} > 535 ns
LTCLK hold time from LTEN LOW	t_{h5} > 160 ns
LTDATA hold time from LTEN LOW	t_{h6} > 0 ns
LTDATA delay time from LTEN HIGH	t_{d1} < 235 ns
LTDATA delay time from LTCLK HIGH	t_{d2} < 400 ns
LTDATA delay time from LTEN (3-state control)	t_{d4} < 50 ns

Note

1. t_{LE} is determined by the longest path from LTEN LOW to LTDATA. This path is via the reset of the internal bit counter. This reset is only necessary when after the last LTEN = LOW, an exact multiple of 8-bits has not been transferred. Otherwise t_{LE} can be T_{cy} = 165 ns less.

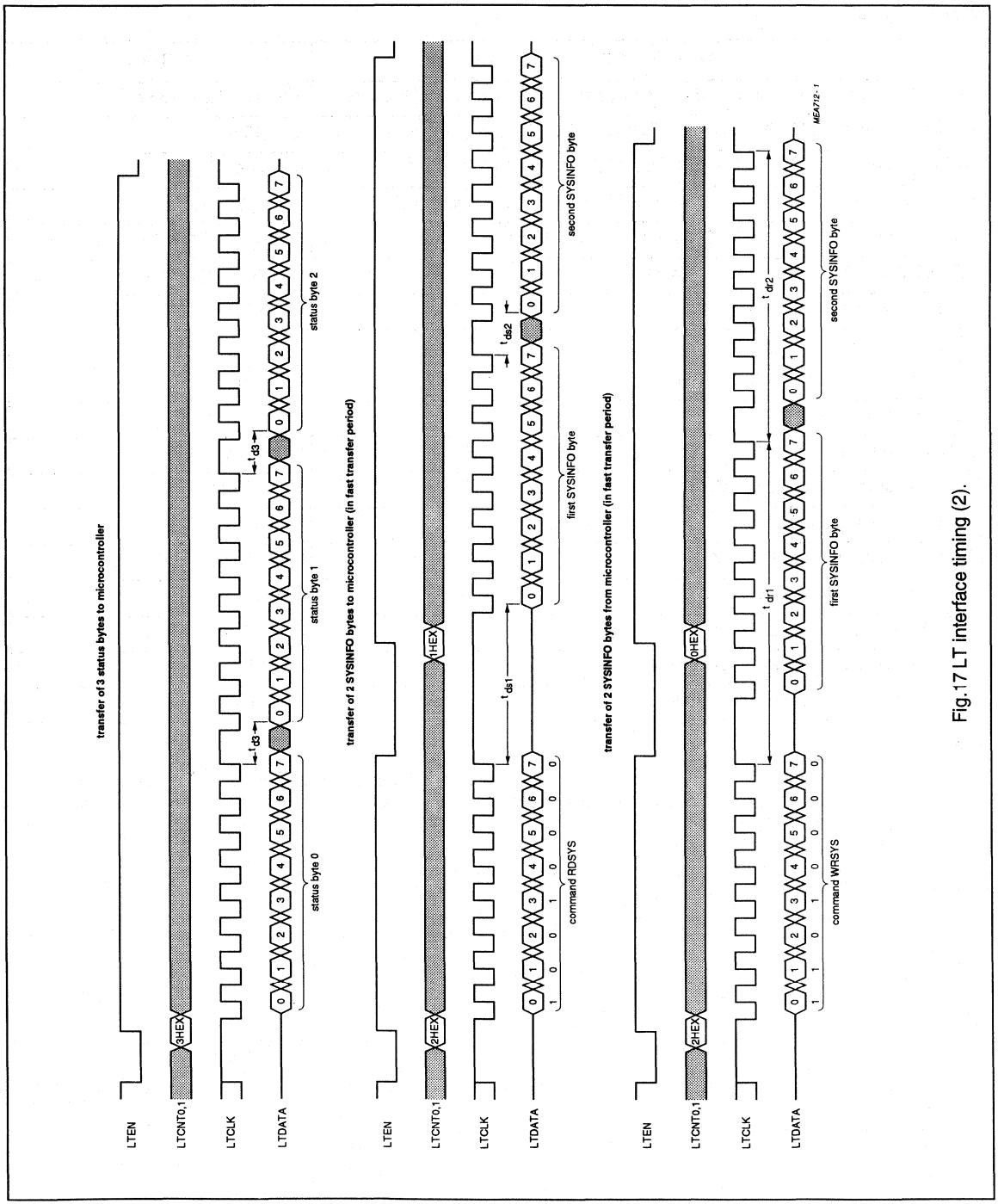


Fig.17 LT interface timing (2).

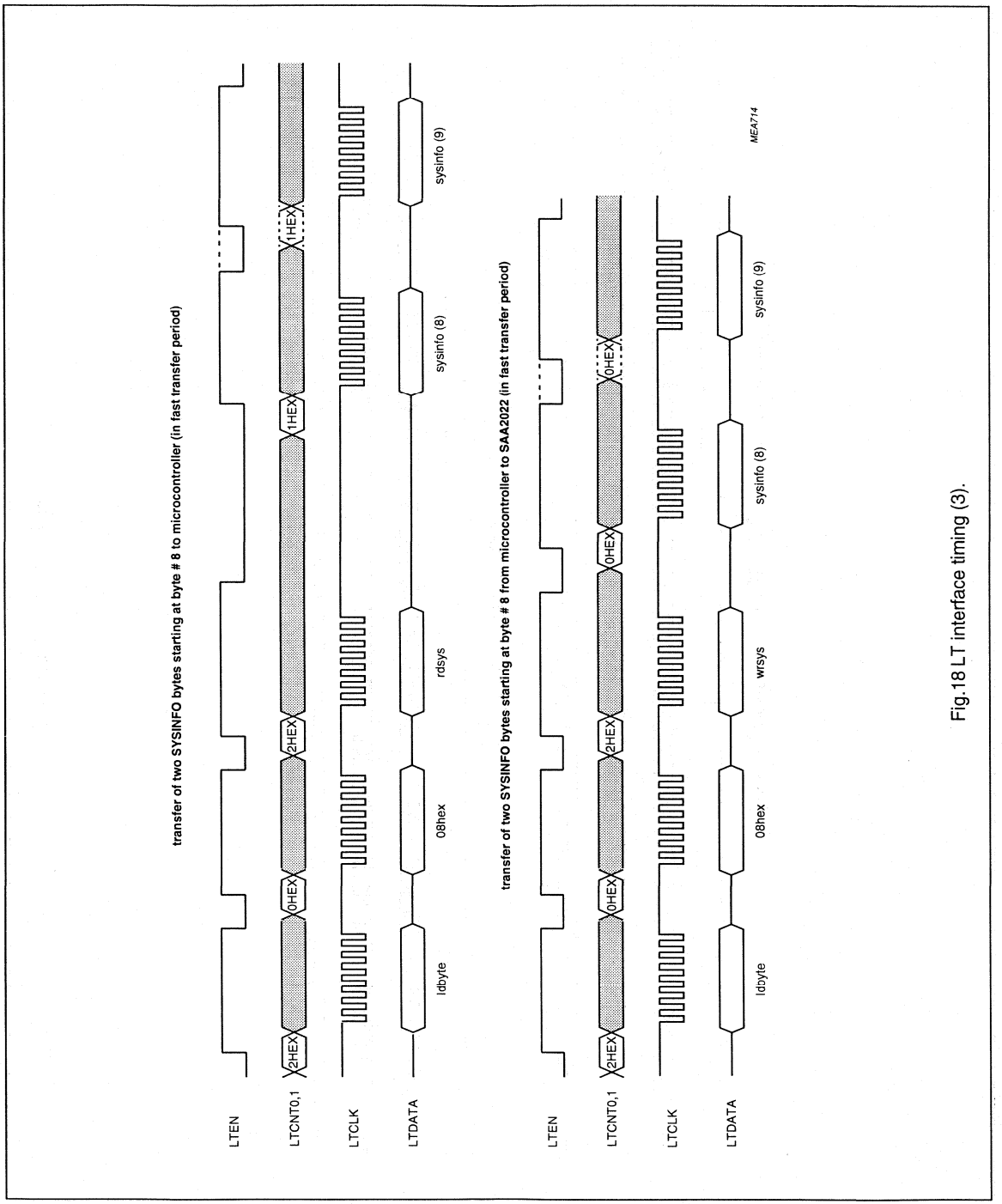


Fig.18 LT interface timing (3).

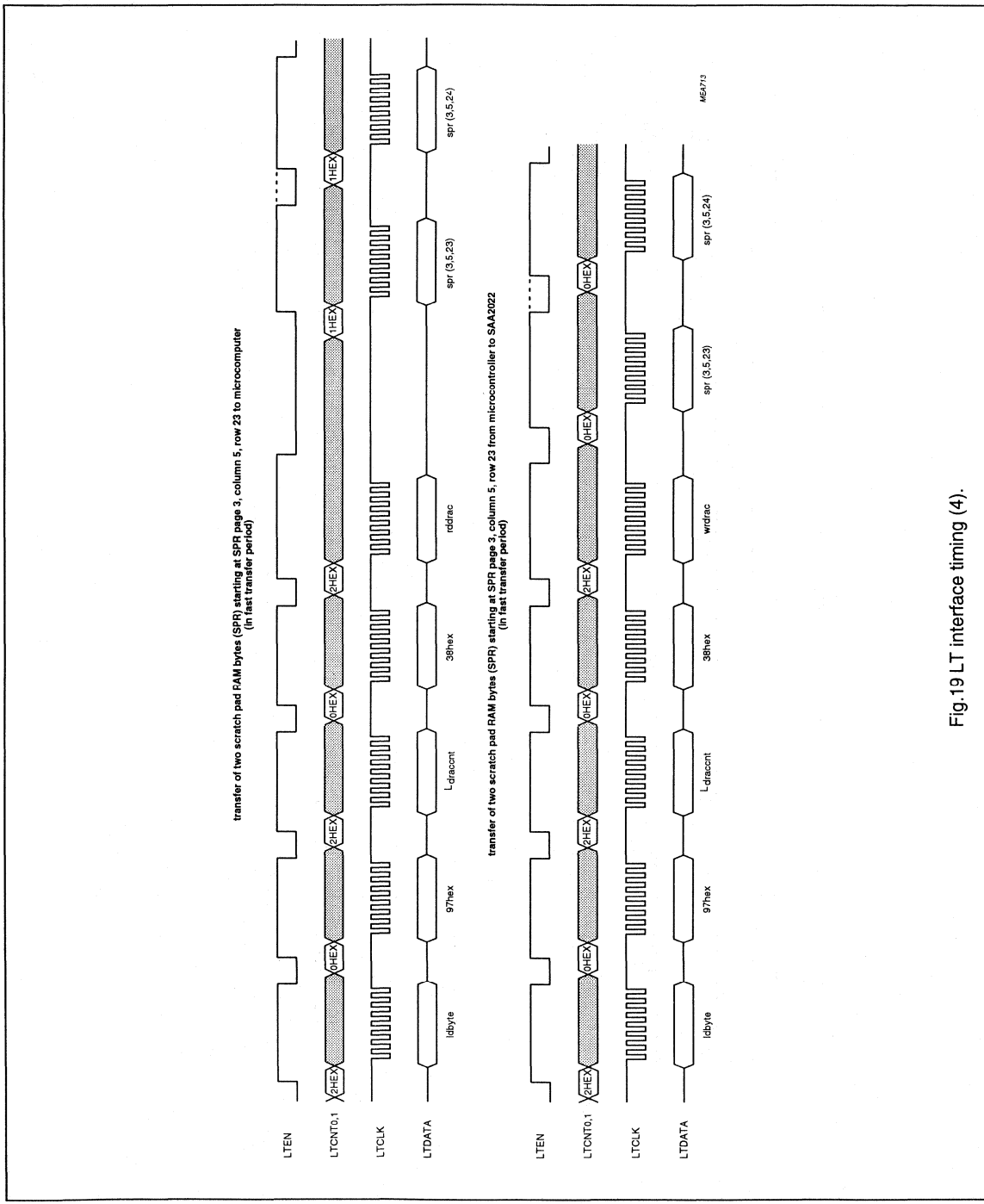


Fig.19 LT interface timing (4).

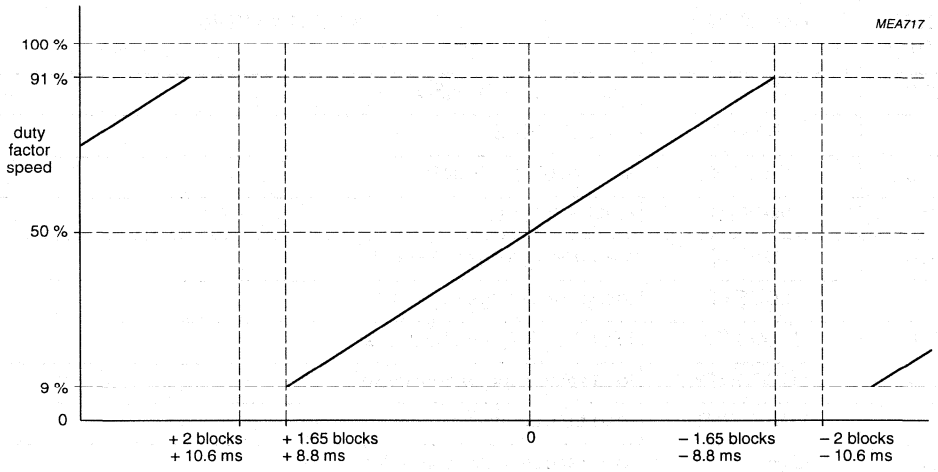


Fig.20 SPEED pulse width as a function of phase error.

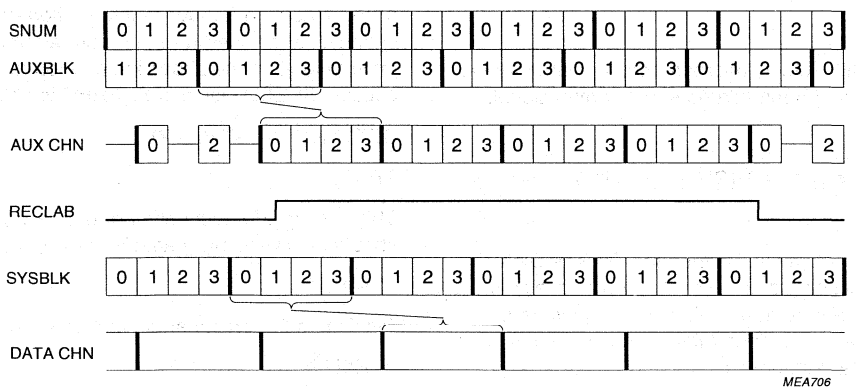


Fig.21 Recording a label.

Table 4 Microcontroller Interface Commands.

CMD REGISTER 76543210	COMMAND	EXPLANATION
XXXX1000	RDAUX	read AUXILIARY INFO
XXXX1001	RDSYS	read SYSINFO
XXXX1010	WRAUX	write AUXILIARY INFO
XXXX1011	WRSYS	write SYSINFO
XXXX0000	LDSET0	load new settings register 0
XXXX0001	LDSET1	load new settings register 1
XXXX0010	LDAFLEV	load AUX flag threshold level
XXXX0011	LDSPDDTY	load record speed duty cycle
XXXX0101	LDBYTCNT	load byte counter
XXXX0110	LDRACCNT	load random access counter
XXYZ1100	RDDRAC	read data in random access mode from RAM quarter YZ
XXYZ1101	RDFDRAC	read flag and data in random access mode from RAM quarter YZ
XXYZ1110	WRDRAC	write data in random access mode to RAM quarter YZ
XXYZ1111	WRFDRAC	write flag and data in random access mode to RAM quarter YZ

Explanation of settings

SET0 REGISTER (TABLE 6)

µCSPD

An active HIGH, selects microprocessor control for the SPEED pulse width modulated servo control signal.

DISRSY

Disable Resyncs active HIGH, is used in after recording.

RECLAB

Record labels active HIGH when in DRAR or DPAR modes; a label being defined as the bodies of all four AUX tape blocks in a tape frame which is being written. This setting has immediate effect and should only be modified in time segment 1.

ENFREG

In modes DPAP and DPAR Enable Frequency Regulation active HIGH, allows frequency information from the data channels to be used with the phase information to generate the capstan SPEED signal.

ENEFREG

Enable Extended Frequency Regulation active HIGH, allows extended frequency information from the data channels to be used with the "normal" frequency information and the phase information to generate the capstan SPEED signal, if ENFREG is active.

SET1 REGISTER (TABLE 7)

TEST1

This setting is for test only. For use in applications this bit should be always programmed to logic 0.

PINO1

Pin Output 1, Port expander output for the microcontroller.

TFEMAS

This allows the SAA2022 to become master of the SB-I²S-bus in modes DPAP and DPAR. In mode DRAR the device always operates as a slave irrespective of the settings bit.

PORTAB

Portable application active HIGH, allows for the data channels clock extraction to track fast variations in tape bit rate. For home use set to inactive.

NOCOS

No Corrected Output Symbol active HIGH, disables the writing of the error corrected output to the DRAM. It is only used for debugging.

TEST2

This setting is for test only. For use in applications this bit should always be programmed to logic 0.

PINO2

Pin output 2, Port expander output for the microcontroller.

PINO3

Pin output 3, Port expander output for the microcontroller.

TAPE PHASE MODE

ENFREG = logic 0, ENEFREG = logic 0 and µCSPD = logic 0

In this mode the SAA2022 performs a new calculation to determine the pulse width for the SPEED signal approximately once every 21.33 ms, giving a sampling rate of approximately 46.9 Hz. This calculation is basically a phase comparison between the incoming main data tape frame and an internally generated reference. The pulse duty cycle increases linearly from approximately 9% when the incoming main data tape frame is 1.65 tape blocks (8.8 ms) too early up to 91% when the incoming main data tape frame is 1.65 tape blocks (8.8 ms) too late, in 256 steps (see Fig.20). Outside ±2 tape blocks range the pulse width characteristic overflows and repeats itself forming a saw-tooth pattern. The SAA2022 has an internal buffer of ±8.8 ms inside which the phase information is valid.

TAPE FREQUENCY MODE

ENFREG = logic 1, ENEFREG = logic 0 and µCSPD = logic 0

The above description is overridden with frequency information. That is if the incoming main data bit rate deviates by more than approximately ±6% from the nominal bit rate of 96000 bits per second, frequency information is mixed with the phase information. In between the limits ±6% the pulse width is determined as above.

EXTENDED TAPE FREQUENCY MODE

ENFREG = logic 1, ENEFREG = logic 1 and µCSPD = logic 0

In this mode there are 3 regions. This provides a more gentle transition from frequency plus phase control to phase only control. Firstly from 0% to ±4.5% deviation, where the operation is as for the tape phase mode. Secondly from ±4.5% to ±6% deviation where the contribution of the frequency information to the servo information is half of that in the region beyond ±6% deviation. Thirdly when the deviation is greater than ±6%, which is the same as for the tape frequency mode.

MICROCONTROLLER MODE

µCSPD = logic 1

In this mode the pulse width is determined by the microcontroller programming of the SPDDTY interface register.

NMODE0, NMODE1

These two bits control the mode change operation in the SAA2022.

Table 5 NMODE1, NMODE0.

NMODE1	NMODE0	OPERATING MODE
0	0	DPAP
1	0	DPAR
1	1	DRAR
0	1	invalid state

SETTINGS REGISTERS

Table 6 SET0.

SETTING	BIT	DEFAULT
ENEFREG	6	0
ENFREG	5	0
RECLAB	4	0
DISRSY	3	0
μCSPD	2	0
NMODE1	1	0
NMODE0	0	0

Table 7 SET1.

SETTING	BIT	DEFAULT
PINO3	7	0
PINO2	6	0
TEST2	5	0
NOCOS	4	0
PORTAB	3	1
TFEMAS	2	1
PINO1	1	0
TEST1	0	0

Table 8 SPEED Source.

MODE	μCSPD	SPEED
DPAP	0	tape(1)
DPAP	1	μC(2)
DPAR	0	tape(1)
DPAR	1	μC(2)
DRAR	0	50%(3)
DRAR	1	μC(2)

Notes

1. "Tape" means that the duty cycle has been calculated from the playback tape signal.
2. "μC" means that the microcontroller programs the duty cycle via the SPDDTY register in the microcontroller interface.
3. "50%" defines that the duty cycle is fixed at 50%.

Table 9 Typical Settings.

SETTING BYTE																WHEN
0								1								
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
X	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	play home machine
X	1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	play portable machine
X	X	X	0	X	0	1	1	0	0	0	0	0	1	0	0	record NO LABEL
X	X	X	1	X	0	1	1	0	0	0	0	0	1	0	0	record LABEL
X	X	X	0	1	1	1	0	0	0	0	0	0	1	0	0	after record NO LABEL
X	X	X	1	1	1	1	0	0	0	0	0	0	1	0	0	after record LABEL

Status Registers

The SAA2022 has 4 status registers all of which are read only. A circular pointer is used to select which of the status registers is addressed. This pointer is reset to point to STATUS0 as result of the rising edge of LTEN while the LTCNT0/1 = RSTAT. Any number of the registers may be read, always starting at STATUS0.

Table 10 STATUS0.

STATUS BIT	BIT
RFBT	7
SYSFLC	6
AUXFLC	5
AUXFLO	4
FLAGI	3
URDA	2
SNUM1	1
SNUM0	0

Table 11 STATUS1.

STATUS BIT	BIT
SLOWTFR	7
TEST4	6
–	5
PINI	4
PAG2	3
PAG1	2
MODE1	1
MODE0	0

Table 12 STATUS2.

STATUS BIT	BIT
NFLG3	7
NFLG2	6
NFLG1	5
NFLG0	4
FLG3	3
FLG2	2
FLG1	1
FLG0	0

Table 13 STATUS3.

STATUS BIT	BIT
CHANS7	7
CHANS6	6
CHANS5	5
CHANS4	4
CHANS3	3
CHANS2	2
CHANS1	1
CHANS0	0

SNUM0, SNUM1

Time segment number.

URDA

Unreliable Data active HIGH, means that regardless of the other flag information **you cannot use the Data, SYSINFO or AUX, because they are unreliable**, this can occur as result of a RESYNC, a mode change from mode DRAR to mode DPAP, or a reset of the SAA2022. When a resync occurs it resynchronizes with the incoming main data tape channel information, with a result that for a period of time, the time that URDA is HIGH all output data is unusable.

FLAGI

Instantaneous flag active HIGH, indicates that the AUXILIARY byte that is about to be transferred to the microcontroller has a flag that is ≥ AFLEV, or that the SYSINFO byte that is about to be transferred is in error.

AUXFLO

Old Aux Flag active HIGH, indicates that AUXILIARY data due to be transferred to the microcontroller in the current segment should not be used.

AUXFLC

AUX Flag active HIGH, indicates that at least one of the AUXILIARY data bytes due to be transferred to the microcontroller in the current segment is in error. This information is provided before the transfer occurs.

SYSFLC

SYSINFO flag active HIGH, indicates that at least one of the SYSINFO bytes in the current segment is in error. This information is provided before the transfer occurs.

RFBT

Ready for byte transfer of SYSINFO, AUX or Scratch pad RAM to or from the microcontroller active HIGH.

MODE0, MODE1

Current mode of operation of the SAA2022.

PAG1, PAG2

Two most significant bits of the modulo 6 internal page counter, the least significant bit is equal to SNUM0.

PINI

Pin input, Port expander input for the microcontroller.

TEST4

This is for test purposes only.

SLOWTFR

Indicates that LT data transfers of SYSINFO, AUX or Scratch Pad RAM can only occur at low speed rate. This occurs only during the second half of time segment 0, therefore the status bit RFBT must be polled to see if a transfer is possible. This bit will be HIGH only during the second half of time segment 0.

FLG 0 to 3

Error flag from the next AUXILIARY/SYSINFO byte which is to be transferred to the microcontroller.

The flags for SYSINFO bytes have only 2 values, logic 0 which implies that the error corrector finds the bytes are good and logic 1 which implies that the bytes are in error.

The flags for AUXINFO bytes can have any one of 16 values, 0 to 15, depending on the type of correction. All of the AUX bytes in the same AUX code word will have the same flag value. The less reliable the data, the higher the flag value. It is recommended that any byte with a flag value of 10 or higher is deemed unreliable.

NFLG 0 to 3

Error flag from the byte after the next AUXILIARY/ SYSINFO byte which will be transferred to the microcontroller.

CHANS 0 to 7

Error Correction Channel status, which indicates if the even C1 code words in the 5th block of the segment for each data tape channel were non correctable. Therefore 1 in every 16 C1 code words from each channel is monitored to see if the C1 error correcting decoding was successful.

Loadable registers

Table 14 AFLev.

3	2	1	0	BIT
1	0	1	0	default value

AUX Flag threshold level. FLAGI goes HIGH for the AUX bytes whose flags are ≥ AFLev. AUXFLC will go HIGH if the flags from either code word in the current segment are ≥ AFLev. The default value is 10.

Table 15 SPDDTY.

7	6	5	4	3	2	1	0	BIT
1	0	0	0	0	0	0	0	default value

SPEED duty cycle register. If μCSPD is active, this register determines the duty cycle of the speed signal.

The duty cycle is given by:

$$Duty\ cycle = \frac{SPDDTY \times 100}{256}\ \%$$

- 0 for 0% duty cycle
- 128 for 50% duty cycle
- 255 for 99.6% duty cycle.

The default value is 128.

Table 16 BYTCNT.

7	6	5	4	3	2	1	0	BIT
0	0	0	0	0	0	0	0	default value

Byte counter for SYSINFO, AUX and Scratch Pad RAM transfers. For SYSINFO:

values 0 to 31 access SYSINFO from the current segment.

values 32 to 63 access SYSINFO from the current +1 segment.

values 64 to 95 access SYSINFO from the current +2 segments.

values 96 to 127 access SYSINFO from the current +3 segments.

In Random access mode the SYSTEM ADDRESS is mapped on to BYTCNT as follows:

Table 17 SYSTEM ADDRES in Random access mode.

7	6	5	4	3	2	1	0	BYTCNT
7	6	5	4	3	2	1	0	ROW

Table 18 RAACNT.

6	5	4	3	2	1	0	BIT
0	0	0	0	0	0	0	default value

Random Access counter is used for generating addresses in the Random access mode, the SYSTEM ADDRESS is mapped on to RACCNT as shown in Table 19.

Table 19 SYSTEM address.

6	5	4	3	2	1	0	RACCNT
–	–	–	–	–	–	8	ROW
–	–	–	2	1	0	–	COL
2	1	0	–	–	–	–	PAG

SYSINFO AND AUX DATA OFFSETS

AUX data consists of 4 blocks of 36 bytes, one block being transferred in each time segment.

Each tape frame contains 128 bytes of SYSINFO, the SYSINFO bytes can for convenience, be considered as being grouped into 4 SYSINFO blocks, with:

SYSBlk0 ==> SI0 to SI31,

SYSBlk1 ==> SI32 to SI63, etc.

In modes DPAP and DPAR SYSINFO transfers may occur in two ways:

1. 4 blocks of 32 bytes, one block being transferred from the SAA2022 in each time segment.
2. 1 block of 128 bytes being transferred in time segment 1.

In mode DRAR SYSINFO must be transferred to the SAA2022 as 4 blocks of 32 bytes, one block in each segment.

Figures 26 to 29 show the offsets between the SYSINFO and AUX and the time segment counter, for the various modes of operation of the SAA2022.

BLOCK OFFSETS WITH RESPECT TO TIME SEGMENT

Mode DPAP

SYSBlk = (SNUM + 3) MOD 4;
or read all 4 SYSINFO blocks when SNUM = 1.

If AUX and MAIN were recorded simultaneously then AUXBlk = (SNUM + 1) MOD 4; else read and interpret 1 AUX block in each time segment.

Mode DRAR

SYSBlk = SNUM;
AUXBlk = (SNUM + 1) MOD 4.

Mode DPAR

SYSBlk = (SNUM + 3) MOD 4;
or read all 4 SYSINFO blocks when SNUM = 1;
AUXBlk = (SNUM + 1) MOD 4.

THE SCRATCH PAD RAM

The SAA2022 provides the microcontroller with a scratch pad RAM, which it can use for any purpose. The size of the scratch pad depends upon the size of the DRAM used and the locations may be written and read in 8-bit or 12-bit units.

For a 64 k × 4-bit DRAM, the scratch pad is arranged as 6 pages, where each page consists of 7 columns × 64 rows. The pages are numbered 0 to 5, columns 1 to 7 and rows 0 to 63. This gives a total of (6 × 7 × 64) = 2688 locations.

For a 256 k × 4-bit DRAM, the scratch pad is the same as for the 64 k × 4 bit DRAM, plus an additional 3 RAM quarters, each of 6 pages where each page consists of 8 columns × 448 rows. The pages are numbered 0 to 5, columns 0 to 7 and rows 0 to 431. This gives then a total of (2688 + (3 × 6 × 8 × 448)) = 67200 locations. The RAM quarter is chosen by the YZ bits of the microcontroller interface commands.

Use of the scratch pad RAM outside the above ranges will upset the operation of the device.

As with SYSINFO, AUX transfers can occur at high-speed at all times except the second half of time segment 0, that is when the status bit SLOWTFR is HIGH. During this period the microcontroller must poll the status bit RFBT to determine when a transfer can occur.

There are two possible methods for addressing the scratch pad RAM. For random access of the scratch pad the address of each location is sent by the microcontroller to the SAA2022 before each location transfer. Alternatively, the address of the first location can be sent by the microcontroller before the first location transfer. This will automatically increment the row for all subsequent transfers until the end of the column. The RACCNT and BYTCNT registers are used for addressing the scratch pad. For the 64 k × 4-bit DRAM, and first quarter of 256 k × 4 DRAM the mapping of the scratch pad RAM address onto the RACCNT and BYTCNT registers is shown in Tables 20 and 21. For the other three-quarters of the 256 k × 4 DRAM the mapping of the scratch pad RAM address onto the RACCNT and BYTCNT registers is shown in Tables 22 and 23.

Table 20 RACCNT bit.

RACCNT BIT						
6	**5**	**4**	**3**	**2**	**1**	**0**
P2	P1	P0	C2	C1	C0	1

Table 21 BYTCNT bit.

BYTCNT BIT							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	0	R5	R4	R3	R2	R1	R0

Table 22 RACCNT bit.

RACCNT BIT						
6	**5**	**4**	**3**	**2**	**1**	**0**
P2	P1	P0	C2	C1	C0	R8

Table 23 BYTCNT bit.

BYTCNT BIT							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R7	R6	R5	R4	R3	R2	R1	R0

Mode changes

Table 24 Possible mode changes for the SAA2022.

CURRENT MODE	NEW MODE		
	DPAP	DRAR	DPAR
DPAP	–	YES	YES
DRAR	YES	–	–
DPAR	YES	–	–

TIMING FOR MODE CHANGES

Mode change DPAP to DRAR

This mode change occurs at the end of the time segment in which the SAA2022 receives the new settings. Writing of the first MAIN and AUX data commences at the start of the time segment 1 which follows two subsequent end of time segment 3 intervals. The delay to writing to tape is approximately 222 ms, as shown in Fig.22. If "seamless appending" is required the new settings should be sent to the SAA2022 during time segment 2.

Mode change DPAP to DPAR

This mode change occurs at the first end of time segment 2 after the SAA2022 receives the new settings. Output of AUX to tape begins at the start of the following time segment 1, (i.e. ≈85.3 ms after the mode change), as shown in Fig.23.

Mode change DRAR to DPAP

This mode change occurs at the first end of time segment 0 after the SAA2022 receives the new setting. Writing of MAIN and AUX data stops immediately after the mode change. The time segment jumps back to 0, URDA goes HIGH and stays HIGH for 5 time segments (≈213.3 ms) after which it goes LOW, as shown in Fig.24.

Mode change DPAR to DPAP

This mode change occurs at the first end of time segment 0 after the SAA2022 receives the new setting. The writing of AUX data to tape stops immediately after the mode change. The first AUX read from tape can be expected during the following time segment 0 or 1 (i.e. 128 to 170.67 ms after the mode change), as shown in Fig.25.

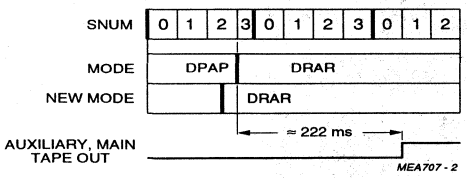


Fig.22 Mode change DPAP to DRAR (AUX and MAIN simultaneously recording).

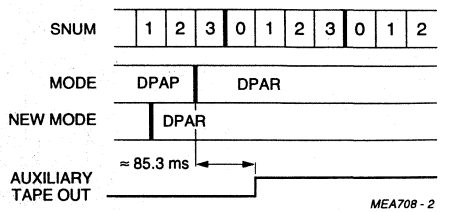


Fig.23 Mode change DPAP to DPAR (AUX after recording).

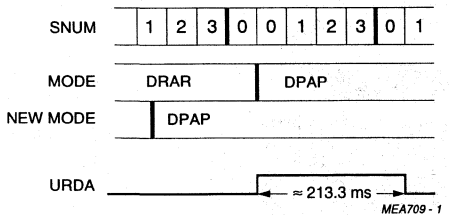


Fig.24 Mode change DRAR to DPAP.

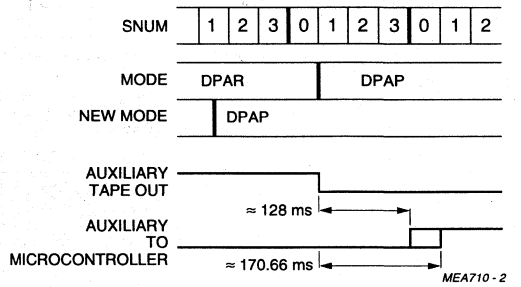


Fig.25 Mode change DPAR to DPAP.

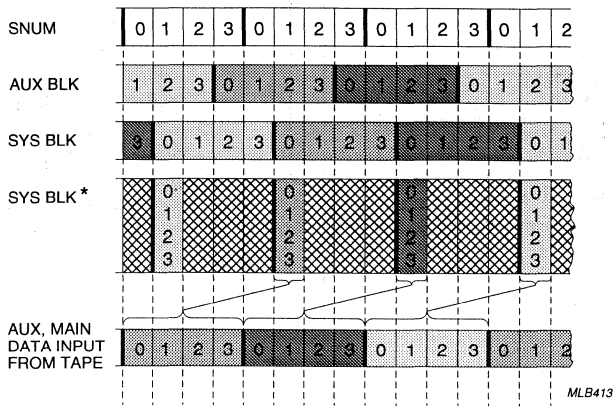


Fig.26 SYSINFO and AUX block delays in DPAP (Audio and AUX simultaneously recorded).

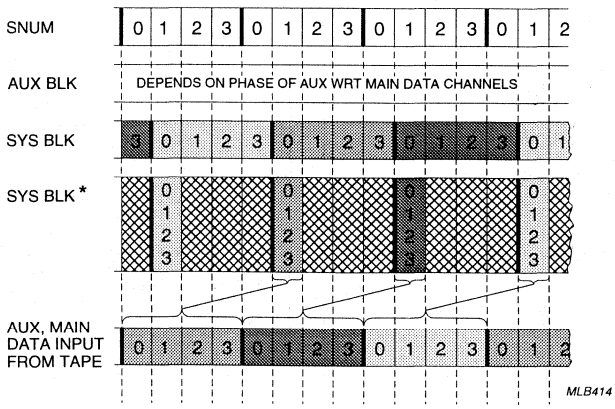


Fig.27 SYSINFO and AUX block delays in mode DPAP (Audio and AUX recorded separately).

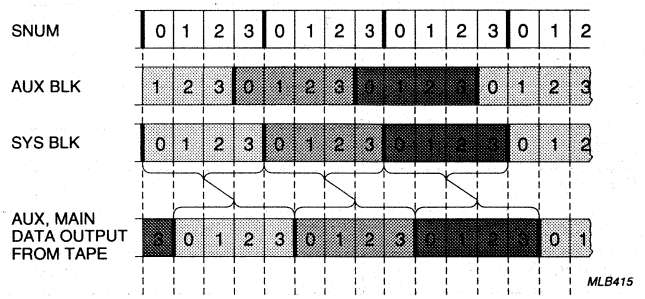


Fig.28 SYSINFO and AUX block delays in mode DRAR.

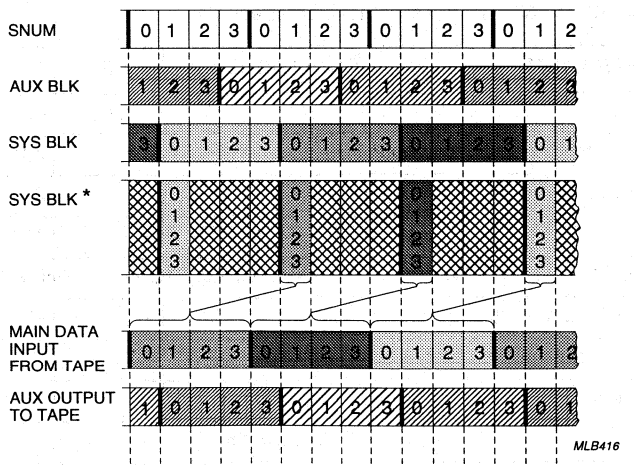


Fig.29 SYSINFO and AUX block delays in mode DPAR.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+6.5	V
V_I	input voltage	note 1	−0.5	V_{DD} + 0.5	V
I_{SS}	supply current in V_{SS}		−	−100	mA
I_{DD}	supply current in V_{DD}		−	100	mA
I_I	input current		−10	+10	mA
I_O	output current		−20	+20	mA
P_{tot}	total power dissipation		−	500	mW
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{es1}	electrostatic handling	note 2	−1500	+1500	V
V_{es2}	electrostatic handling	note 3	−70	+70	V

Notes

1. Input voltage should not exceed 6.5 V unless otherwise specified.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

DC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	note 1	3.8	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V	−	21	30	mA
		V_{DD} = 3.8 V	−	16	25	mA
Inputs CLK24, TCH0 to TCH7, TAUX, PWRDWN, LTCLK, LTCNT0, LTCNT1, LTEN, PINI and SBMCLK						
V_{IL}	LOW level input voltage		−	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	−	V
I_I	input current	V_I = 0 V; T_{amb} = 25 °C	−	−	−10	µA
		V_I = 5.5 V; T_{amb} = 25 °C	−	−	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input RESET						
V_{tLH}	threshold voltage LOW-HIGH		$0.8V_{DD}$	–	–	V
V_{tHL}	threshold voltage HIGH-LOW		–	–	$0.2V_{DD}$	V
V_{hys}	hysteresis	$V_{tLH} - V_{tHL}$	–	1.5	–	V
I_I	input current	$V_I = V_{DD}$	25	–	400	µA
Outputs RASN, CASN, WCLOCK and WDATA						
V_{OL}	LOW level output voltage	$I_O = -3$ mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	$I_O = 3$ mA	$V_{DD} - 0.5$	–	–	V
Outputs LTREF, WEN, OEN, A0 to A8, SPEED, SPDF, PINO1, PINO3, AZCHK, TEST2, TEST3, MCLK, SBEF, SBDIR and URDA						
V_{OL}	LOW level output voltage	$I_O = -2$ mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	$I_O = 2$ mA	$V_{DD} - 0.5$	–	–	V
Inputs/outputs D0 to D3; with outputs in 3-state						
V_{IL}	LOW level input voltage	TTL-level	–	–	0.8	V
V_{IH}	HIGH level input voltage	TTL-level	2	–	–	V
I_I	input leakage current	$V_I = 0$ V; $T_{amb} = 25$ °C	–	–	–10	µA
		$V_I = 5.5$ V; $T_{amb} = 25$ °C	–	–	10	µA
Inputs/outputs D0 to D3						
V_{OL}	LOW level output voltage	$I_O = -3$ mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	$I_O = 3$ mA	$V_{DD} - 0.5$	–	–	V
Inputs/outputs LTDATA, SBCL, SBDA and SBWS; with outputs in 3-state						
V_{IL}	LOW level input voltage	TTL-level	–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	TTL-level	$0.7V_{DD}$	–	–	V
I_I	input leakage current	$V_I = 0$ V; $T_{amb} = 25$ °C	–	–	–10	µA
		$V_I = 5.5$ V; $T_{amb} = 25$ °C	–	–	10	µA
Inputs/outputs LTDATA, SBCL, SBDA and SBWS						
V_{OL}	LOW level output voltage	$I_O = -3$mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	$I_O = 3$ mA	$V_{DD} - 0.5$	–	–	V

Note

1. For applications requiring minimum power dissipation the device may be operated from a nominal +4 V supply.

AC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock inputs						
C_i	input capacitance		–	–	10	pF
CLK24						
f	pulse frequency		23	24.576	26	MHz
t_{L-i}	pulse width LOW		10	–	–	ns
t_{H-i}	pulse width HIGH		10	–	–	ns
SBMCLK						
f	pulse frequency		–	6.144	12.5	MHz
t_{L-i}	pulse width LOW		30	–	–	ns
t_{H-i}	pulse width HIGH		30	–	–	ns
Clock outputs						
C_L	load capacitance		–	–	50	pF
MCLK						
f	pulse frequency		–	6.144	–	MHz
t_{L-i}	pulse width LOW		50	–	–	ns
t_{H-i}	pulse width HIGH		50	–	–	ns
t_{dMFR}	delay time from CLK24	note 1	–	–	45	ns
t_d	delay time from PWRDWN		–	15	–	ns
Clock inputs						
C_i	input capacitance		–	–	10	pF
Inputs LTCLK, LTCNT0, LTCNT1, LTEN, RESET, TCH0 to TCH7 and TAUX						
t_{suMR}	set-up time to MCLK	note 2	40	–	–	ns
t_{hMR}	hold time from MCLK	note 2	0	–	–	ns
Input PINI						
t_{suMR}	set-up time to MCLK	note 1	70	–	–	ns
t_{hMR}	hold time from MCLK	note 1	0	–	–	ns
Outputs						
C_L	load capacitance		–	–	50	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs A0 to A8, AZCHK, TEST2, LTREF, SBDIR, SBEF, SPDF, SPEED, PINO1 to PINO3, URDA, WCLOCK, WDATA, OEN and WEN						
t_{dMR}	delay time from MCLK	note 2	–	–	30	ns
Outputs OEN and WEN						
t_d	delay time from PWRDWN		–	15	–	ns
Output RASN						
t_{dFR}	delay time from CLK24	note 1	–	–	30	ns
t_d	delay time from PWRDWN		–	15	–	ns
Output CASN						
t_{dFR}	delay time from CLK24	note 1	–	–	30	ns
t_d	delay time from PWRDWN		–	15	–	ns
Inputs/outputs						
C_i	input capacitance		–	–	10	pF
C_L	load capacitance		–	–	50	pF
Inputs/outputs D0 to D3						
t_{suCR}	set-up time to CASN	note 3	10	–	–	ns
t_{hCR}	hold time from CASN	note 3	0	–	–	ns
t_{dMR}	delay time from MCLK	note 2	–	–	25	ns
t_d	delay time from PWRDWN		–	15	–	ns
Input/output LTDATA						
t_{suMR}	set-up time to MCLK	note 2	40	–	–	ns
t_{hMR}	hold time from MCLK	note 2	0	–	–	ns
t_{dMR}	delay time from MCLK	note 2	–	–	30	ns
t_d	delay time from PWRDWN		–	15	–	ns
t_d	delay time from LTEN		–	15	–	ns
Inputs/outputs SBCL and SBWS						
t_{suMR}	set-up time to MCLK	note 2	40	–	–	ns
t_{hMR}	hold time from MCLK	note 2	0	–	–	ns
t_{dSR}	delay time from SBMCLK	note 3	–	–	40	ns
t_{dMR}	delay time from MCLK	notes 2 and 5	–	–	30	ns
t_d	delay time from PWRDWN		–	15	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input/output SBDA						
t_{suMR}	set-up time to MCLK	note 2	40	–	–	ns
t_{hMR}	hold time from MCLK	note 2	0	–	–	ns
t_{dMR}	delay time from MCLK	note 2	–	–	30	ns
t_d	delay time from PWRDWN		–	15	–	ns

Notes

1. LOW-to-HIGH transition of CLK24.
2. LOW-to-HIGH transition of MCLK.
3. LOW-to-HIGH transition of CASN.
4. LOW-to-HIGH transition of SBMCLK.
5. 3-state control.

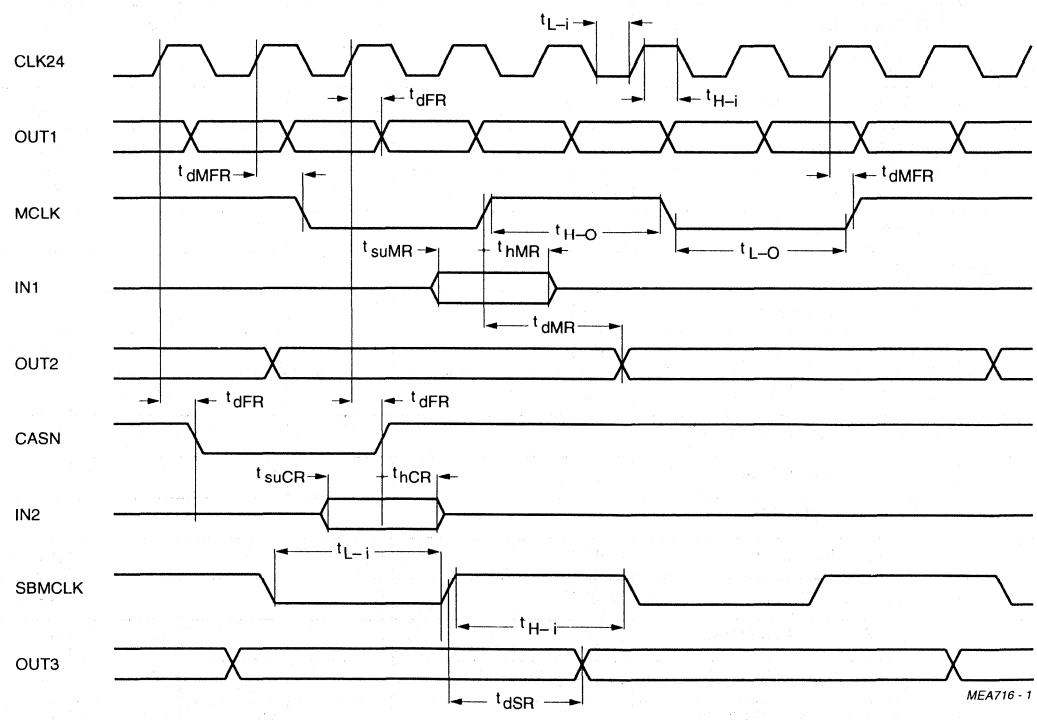


Fig.30 Timing for AC characteristics.

Drive processor for DCC systems SAA2023

FEATURES

- Operating supply voltage: 4.5 to 5.5 V
- Low power dissipation: 260 mW at 5.0 V
- Single chip digital equalizer, tape formatting and error correction
- 8-bit flash analog-to-digital converter (ADC) for low symbol error rate
- Two switchable Infinite Impulse-Response (IIR) filter sections
- 10-tap Finite Impulse-Response (FIR) filter per main data channel, with 8 bit coefficients, identical for all main channels
- 10-tap FIR filter for the AUX channel
- Analog and digital eye outputs
- Interrupt line triggered by internal auxiliary envelope processing e.g. label, counter, and others
- Robust programmable digital PLL clock extraction unit
- Low power SLEEP mode
- Slew rate limited Electromagnetic Compatibility (EMC) friendly output
- Digital Compact Cassette (DCC) optimized error correction
- Programmable symbol synchronization strategy for tape input data
- Microcontroller control of capstan servo possible during playback and recording

DIGITAL dcc COMPACT CASSETTE

- Frequency and phase regulation of capstan servo during playback
- Choice of Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM) types for system Random Access Memory (RAM)
- Scratch pad RAM for microcontroller in system RAM
- Integrated interface for Precision Adaptive Sub-band Coding (PASC) data bus
- Three wire microcontroller 'L3' interface
- Protection against invalid auxiliary data
- Seamless joins between recordings.

GENERAL DESCRIPTION

The SAA2023 performs the drive processor function in the DCC system. This function is built up of digital equalizer, error correction and tape formatting functions. The digital equalizer is intended for use with DCC read amplifiers TDA1318 or TDA1380. The tape formatting and error correction circuit is intended for use with PASC ICs SAA2003 and SAA2013, and write amplifiers TDA1319 or TDA1381.

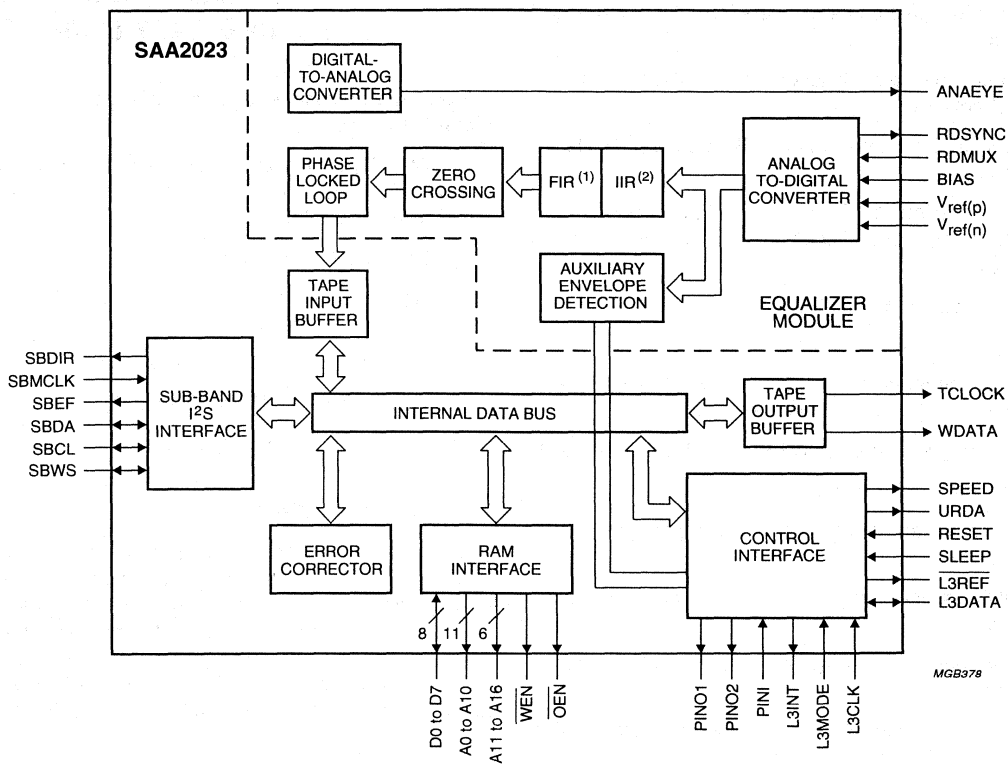
ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2023H	80	TQFP80[1]	plastic	SOT315-1
SAA2023GP	80	QFP80[1]	plastic	SOT318-2

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* are followed. The pocketbook can be ordered using the code 9398 510 34011.

BLOCK DIAGRAM



(1) FIR = Finite Impulse-Response.
(2) IIR = Infinite Impulse-Response.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION	TYPE[1]
	QFP80	TQFP80		
SBWS	1	79	word select for sub-band PASC interface	I/O (1 mA)
SBCL	2	80	bit clock for sub-band PASC interface	I/O (1 mA)
SBDA	3	1	data line for sub-band PASC interface	I/O (1 mA)
SBDIR	4	2	direction line for sub-band PASC interface	O (1 mA)
SBMCLK	5	3	master clock for sub-band PASC interface	I
URDA	6	4	unreliable data	O (1 mA)
L3MODE	7	5	mode line for L3 interface	I
L3CLK	8	6	bit clock line for L3 interface	I
L3DATA	9	7	serial data line for L3 interface	I/O (2 mA)
L3INT	10	8	L3 interrupt output	O (1 mA)
V_{DD1}	11	9	digital supply voltage	S
V_{SS1}	12	10	digital ground	S
$\overline{L3REF}$	13	11	L3 bus timing reference	O (1 mA)
RESET	14	12	reset SAA2023	I
SLEEP	15	13	sleep mode selection of SAA2023	I
CLK24	16	14	24.576 MHz clock input	I
AZCHK	17	15	channel 0 and channel 7 azimuth monitor	O (1 mA)
MCLK	18	16	6.144 MHz clock output	O (1 mA)
TEST3	19	17	TEST3 output; do not connect	O (1 mA)
ERCOSTAT	20	18	ERCO status, for symbol error rate measurements	O (1 mA)
$\overline{OEN}$	21	19	output enable for RAM	O (2 mA)
A10/$\overline{RAS}$	22	20	address SRAM; $\overline{RAS}$ DRAM	O (2 mA)
V_{DD2}	23	21	digital supply voltage	S
V_{SS2}	24	22	digital ground	S
D7	25	23	data SRAM	I/O (4 mA)
D6	26	24	data SRAM	I/O (4 mA)
D5	27	25	data SRAM	I/O (4 mA)
D4	28	26	data SRAM	I/O (4 mA)
D3	29	27	data SRAM; data DRAM	I/O (4 mA)
D2	30	28	data SRAM; data DRAM	I/O (4 mA)
D1	31	29	data SRAM; data DRAM	I/O (4 mA)
V_{DD7}	32	30	digital supply voltage for RAM	S
V_{SS7}	33	31	digital ground for RAM	S
D0	34	32	data SRAM; data DRAM	I/O (4 mA)
A0	35	33	address SRAM; address DRAM	O (2 mA)
A1	36	34	address SRAM; address DRAM	O (2 mA)
A2	37	35	address SRAM; address DRAM	O (2 mA)
A3	38	36	address SRAM; address DRAM	O (2 mA)

SYMBOL	PIN		DESCRIPTION	TYPE[1]
	QFP80	TQFP80		
A4	39	37	address SRAM; address DRAM	O (2 mA)
V_{SS3}	40	38	digital ground	S
V_{DD3}	41	39	digital supply voltage	S
A5	42	40	address SRAM; address DRAM	O (2 mA)
A6	43	41	address SRAM; address DRAM	O (2 mA)
A7	44	42	address SRAM; address DRAM	O (2 mA)
A12/PINO5	45	43	address SRAM; Port expander output 5	O (2 mA)
A14/PINO1	46	44	address SRAM; Port expander output 1	O (2 mA)
A16/PINO3	47	45	address SRAM; Port expander output 3	O (2 mA)
A15/PINO4	48	46	address SRAM; Port expander output 4	O (2 mA)
$\overline{WEN}$	49	47	write enable for RAM	O (2 mA)
A13/PINO2	50	48	address SRAM; Port expander output 2	O (2 mA)
A8	51	49	address SRAM; address DRAM	O (2 mA)
V_{DD4}	52	50	digital supply voltage	S
V_{SS4}	53	51	digital ground	S
A9/$\overline{CAS}$	54	52	address SRAM; $\overline{CAS}$ for DRAM	O (2 mA)
A11	55	53	address SRAM	O (2 mA)
SPEED	56	54	Pulse Width Modulation (PWM) capstan control output for deck	O_t (1 mA)
PINO2	57	55	Port expander output 2	O_t (1 mA)
WDATA	58	56	serial output to write amplifier	O (1 mA)
TCLOCK	59	57	3.072 MHz clock output for tape I/O	O (1 mA)
V_{SS5}	60	58	digital ground	S
V_{DD5}	61	59	digital supply voltage	S
TEST2	62	60	TEST mode select; do not connect	I_{pd}
RDMUX	63	61	analog multiplexed input from read amplifier	I_A
$V_{ref(p)}$	64	62	ADC positive reference voltage	I_A
$V_{ref(n)}$	65	63	ADC negative reference voltage	I_A
SUBSTR	66	64	substrate connection	I_A
BIAS	67	65	bias current for ADC	I_A
V_{SSA}	68	66	analog ground	S
V_{DDA}	69	67	analog supply voltage	S
ANAEYE	70	68	analog eye pattern output	O_A
RDSYNC	71	69	synchronization output for read amplifier	O (1 mA)
V_{DD6}	72	70	digital supply voltage	S
V_{SS6}	73	71	digital ground	S
CHTST1	74	72	channel test pin 1	O (1 mA)
CHTST2	75	73	channel test pin 2	O (1 mA)
TEST0	76	74	TEST mode select; do not connect	I_{pd}
TEST1	77	75	TEST mode select; do not connect	I_{pd}

SYMBOL	PIN		DESCRIPTION	TYPE(1)
	QFP80	TQFP80		
PINI	78	76	Port expander input	I
PINO1	79	77	Port expander output 1	O (1 mA)
SBEF	80	78	sub-band PASC error flag line	O (1 mA)

Note

1. I = input; I_A = analog input; I_{pd} = input with pull-down resistance; I/O = bidirectional; O = output; O_A = analog output; O_t = 3-state output; S = supply.

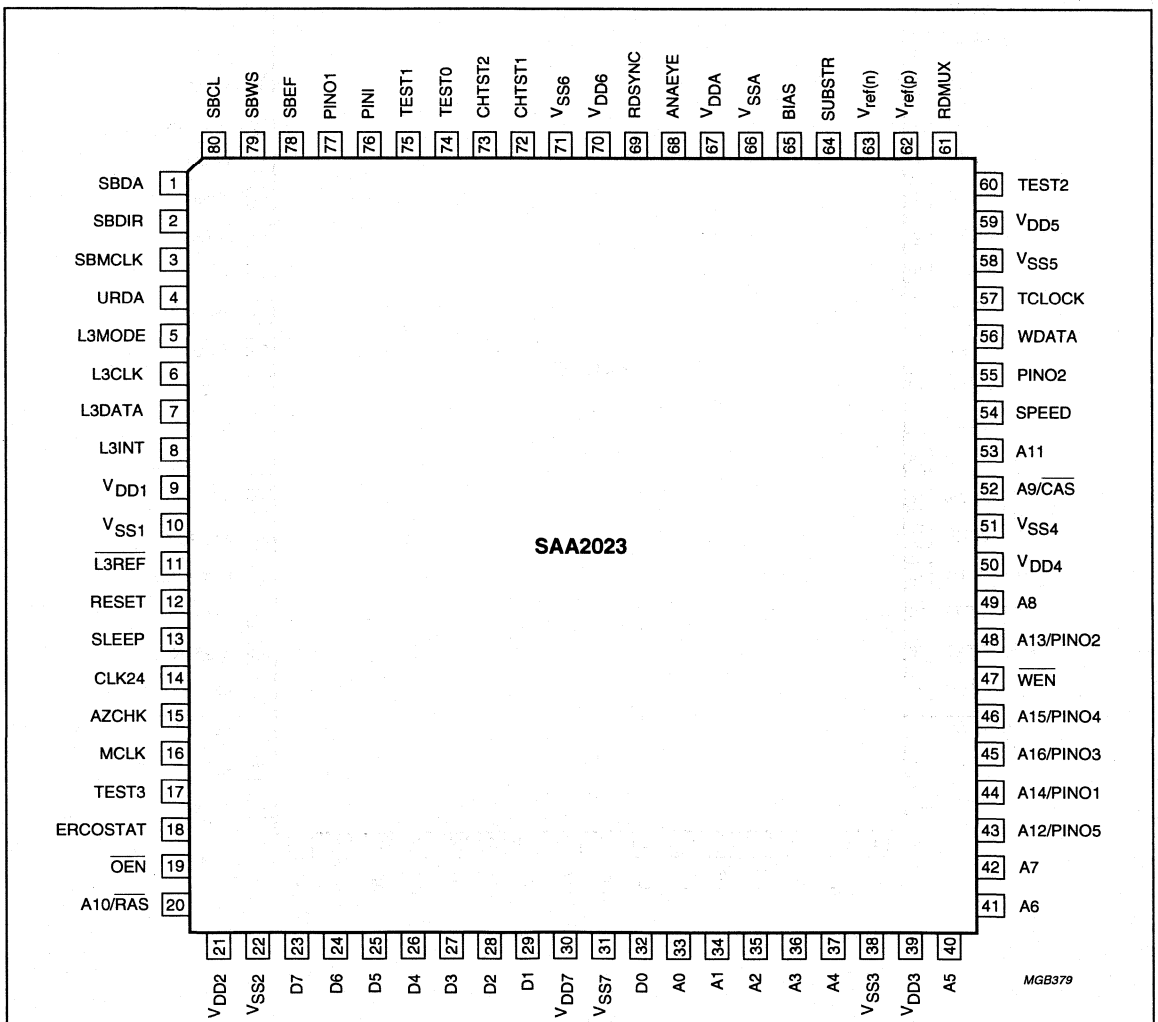


Fig.2 Pin configuration (SOT315-1; TQFP80).

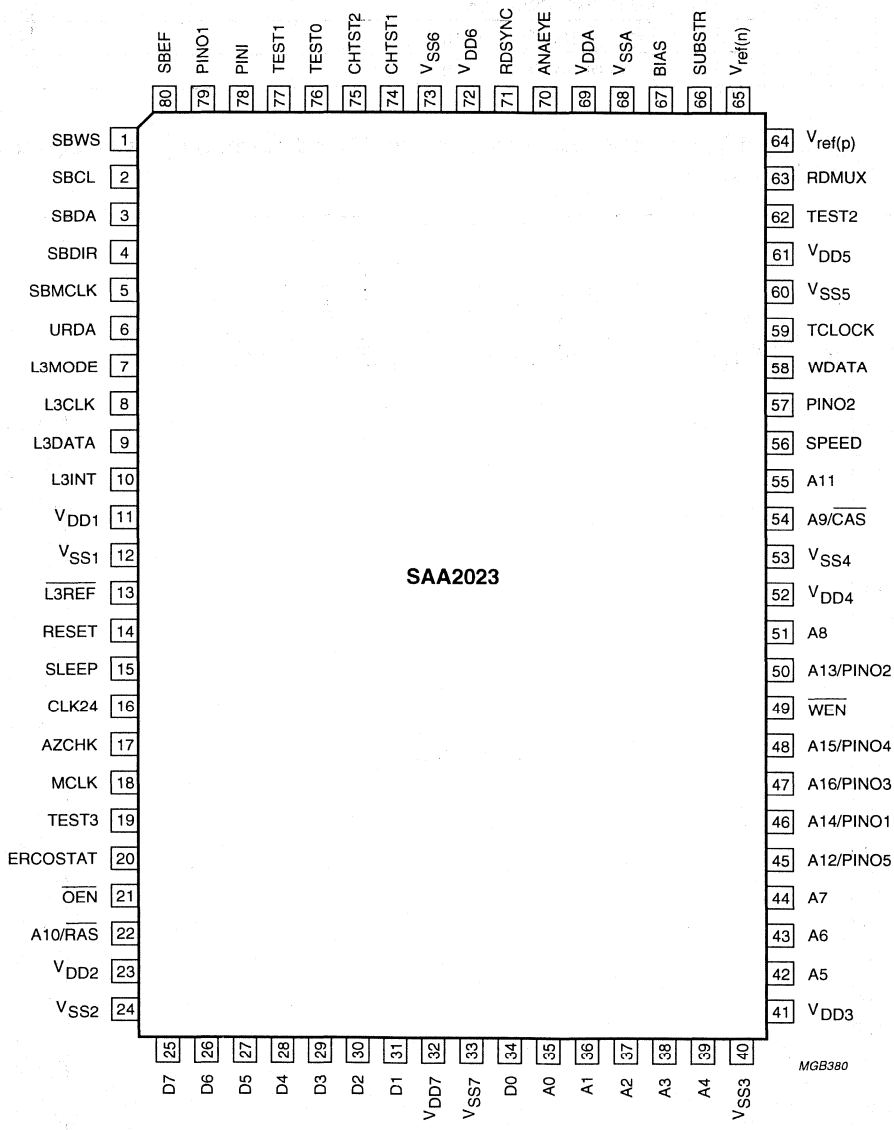


Fig.3 Pin configuration (SOT318-2; QFP80).

FUNCTIONAL DESCRIPTION

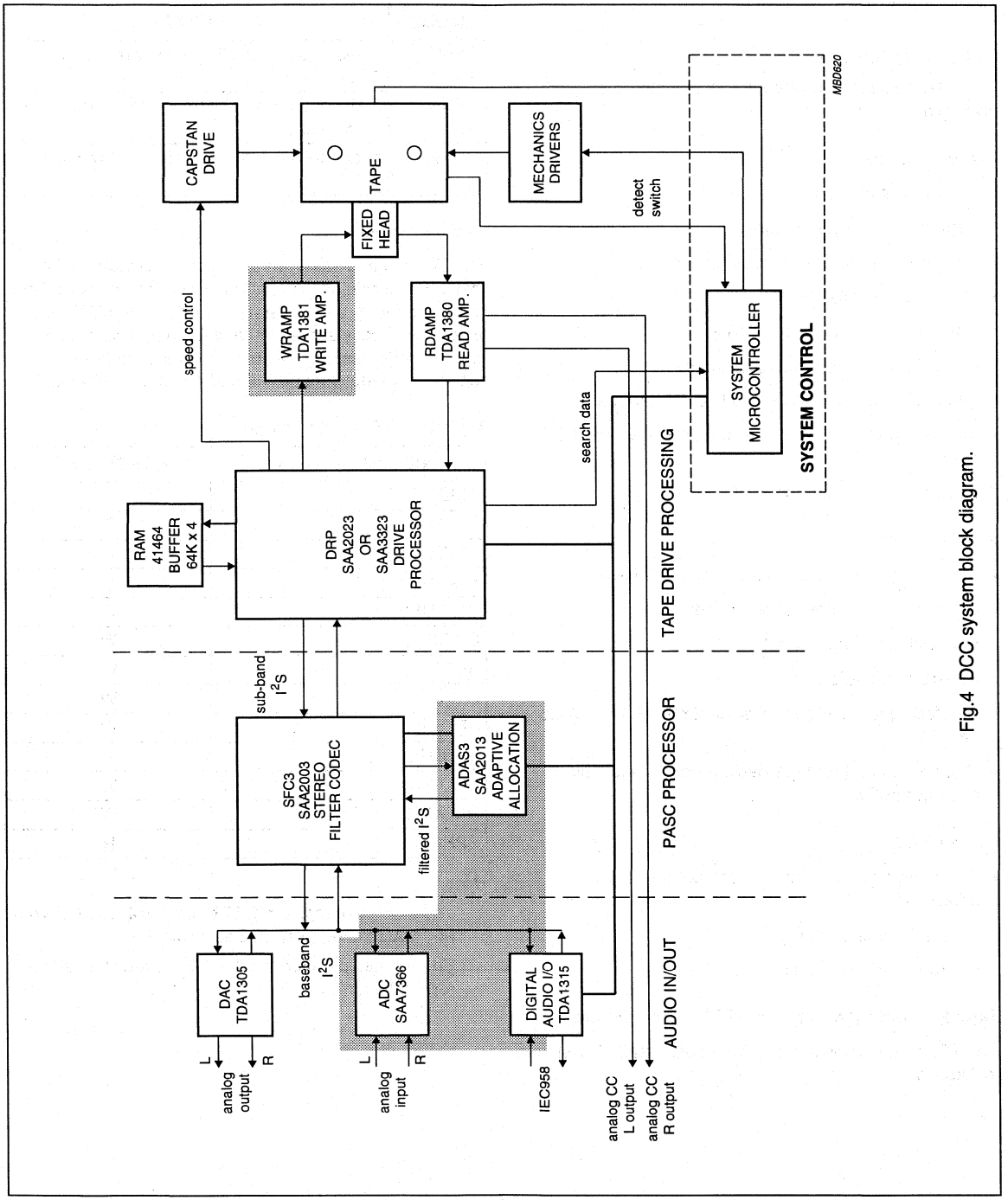


Fig.4 DCC system block diagram.

A simplified block diagram of the SAA2023 is shown in Fig.1.

DCC drive processing

The SAA2023 provides the following functions for the DCC drive processing.

PLAYBACK MODES

- Analog-to-digital conversion
- Tape channel equalization
- Tape channel data and clock recovery
- 10-to-8 demodulation
- Data placement in system RAM
- C1 and C2 error correction decoding
- Interfacing to sub-band serial PASC interface
- Interfacing to microcontroller for SYSINFO and AUX data
- Capstan control for tape deck.

RECORD MODES

- Interfacing to sub-band serial PASC interface
- C1 and C2 error correction encoding
- Formatting for tape transfer
- 8-to-10 modulation
- Interfacing to microcontroller for SYSINFO and AUX data
- Capstan control for tape deck, programmable by microcontroller.

SEARCH MODE

- Detection and interpretation of AUX envelope information
- AUX envelope counting
- Search speed estimation.

Tape Formatting and Error (TFE) correction module

The TFE module has 3 basic modes of operation as shown in Table 1.

Table 1 Basic modes of TFE module.

MODE	EXPLANATION
DPAP	audio and SYSINFO (main data) play; AUX play
DPAR	audio and SYSINFO (main data) play; AUX record
DRAR	audio and SYSINFO (main data) record; AUX record

TFE REGISTERS

The TFE module has 8 writable and 5 readable registers that are accessible via the L3 interface, one write register (CMD) and four read registers (STATUS0 to STATUS3) which are directly addressable, the other registers are indirectly addressable via commands sent to the CMD register. The registers are named as shown in Table 2.

Table 2 TFE register names.

REGISTER NAME	READ/WRITE
CMD	W
STATUS0	R
STATUS1	R
STATUS2	R
STATUS3	R
SET0	W
SET1	W
SET2	W
SET3[1]	W
SPDDTY	W
BYTCNT	W
RACCNT	W
SPEED	R

Note

1. The 4 LSBs of register 'SET3' set RAM type (RType) and RAM timing (RTim). See Table 3.

   For normal operation the 4 MSBs of register 'SET3' should be logic 0.

Table 3 RAM settings by register SET3.

RAM	REGISTER SET3
RTYPE 0	bit 0
RTYPE 1	bit 1
RTim 0	bit 2
RTim 1	bit 3

TFE DATA STREAMS

The TFE module has three read/write data streams that are accessible via the L3 interface and they are shown in Table 4.

Table 4 TFE data streams.

DATA STREAM NAME	READ/WRITE
SYSINFO	R/W
AUXINFO	R/W
Scratch pad RAM	R/W

TFE 'COMMANDS'

These are the commands that need to be sent to the TFE in order to access the indirectly accessible registers and the data streams, see Table 5.

Table 5 TFE commands.

NAME	COMMAND BYTE								EXPLANATION
	7	6	5	4	3	2	1	0	
RDSPEED	0	0	0	0	0	0	0	0	read SPEED register
LDSET0	0	0	0	1	0	0	0	0	load new TFE settings register 0
LDSET1	0	0	0	1	0	0	0	1	load new TFE settings register 1
LDSET2	0	0	0	1	0	0	1	0	load new TFE settings register 2
LDSET3	0	0	0	1	0	0	1	1	load new TFE settings register 3
LDSPDDTY	0	0	0	1	0	1	0	1	load SPDDTY register
LDBYTCNT	0	0	0	1	0	1	1	1	load BYTCNT register
LDRACCNT	0	0	0	1	1	0	0	0	load RACCNT register
RDAUX	0	0	1	0	0	0	0	0	read AUXILIARY information
RDSYS	0	0	1	0	0	0	0	1	read SYSINFO
RDDRAC	Y	Z	1	0	0	0	1	0	read RAM data bytes (8 bits) from quarter YZ
RDWDRAC	Y	Z	1	0	0	0	1	1	read RAM data words (12 bits) from quarter YZ
WRAUX	0	0	1	1	0	0	0	0	write AUXILIARY information
WRSYS	0	0	1	1	0	0	0	1	write SYSINFO
WRDRAC	Y	Z	1	1	0	0	1	0	write RAM data bytes (8 bits) to quarter YZ
WRWDRAC	Y	Z	1	1	0	0	1	1	write RAM data words (12 bits) to quarter YZ

Digital equalizer module

The digital equalizer module has 2 basic modes of operation as shown in Table 6.

Table 6 Basic modes of equalizer module.

MODE	EXPLANATION
Play	main data and AUX channels are equalized
Search	only AUX channel is processed; AUX envelope information is processed

DIGITAL EQUALIZER REGISTERS

The digital equalizer module has 9 write only, 3 read only and 1 read/write register(s) that are accessible via the L3 interface, one write register (CMD) and 2 read registers (STATUS0 and STATUS1) which are directly addressable, the other registers are indirectly addressable via commands sent to the CMD register. The registers are named as shown in Table 7.

Table 7 Digital equalizer register names.

REGISTER NAME	READ/WRITE
CMD	W
STATUS0	R
STATUS1	R
COEFCNT	W
FCTRL	W
CHT1SEL	W
CHT2SEL	W
ANAEYE	W
AEC	R/W
SSPD	R
INTMASK	W
DEQ2SET	W
CLKSET	W

DATA STREAMS

The digital equalizer module has one write only and one read only data stream that are accessible via the L3 interface and they are shown in Table 8.

Table 8 Digital equalizer data streams.

DATA STREAM NAME	READ/WRITE
FIR coefficients to buffer bank	W
FIR coefficients from active bank	W

DIGITAL EQUALIZER "COMMANDS"

These are the commands that need to be sent to the digital equalizer in order to access the indirectly accessible registers and the data streams.

Table 9 Digital equalizer commands.

NAME	COMMAND BYTE								EXPLANATION
	7	6	5	4	3	2	1	0	
WRCOEF	0	0	1	1	0	0	0	0	write FIR coefficients to the digital equalizer buffer bank
RDCOEF	0	0	1	0	0	0	0	0	read FIR coefficients from the digital equalizer active bank
LDCOEFCNT	0	0	0	1	0	0	1	1	load FIR coefficient counter
LDFCTRL	0	0	0	1	0	1	0	0	load filter control register
LDT1SEL	0	0	0	1	0	1	1	0	load CHTST1 pin selection register
LDT2SEL	0	0	0	1	0	1	1	1	load CHTST2 pin selection register
LDTAEYE	0	0	0	1	1	0	0	0	load ANAEYE channel selection register
LDAEC	0	0	0	1	1	0	0	1	load AEC counter
RDAEC	0	0	1	0	0	0	1	0	read AEC counter
RDSSPD	0	0	1	0	0	1	0	0	read SEARCH speed register
LDINTMSK	0	0	0	1	0	0	1	0	load interrupt mask register
LDDEQ3SET	0	0	0	1	0	0	0	0	load digital equalizer settings register
LDCLKSET	0	0	0	1	0	0	0	1	load PLL clock extraction settings register

Table 10 Filter control register.

BIT	7	6	5	4	3	2	1	0
Meaning	–	–	–	µCS(1)	SH1	SH0	Reserved	
Default	0	0	0	0	1	0	1	1

Note

1. µCS is a microcontroller controlled coefficient bank switch. This causes the filter coefficients to be activated at a time that is safe for the digital equalizer, i.e. at the end of the FIR program and that the complete value of coefficient number 9 has been received.

Table 11 SH1 and SH2 (FIR output scaling).

SH		EFFECT ON FIR OUTPUT
1	0	
0	0	FIR mod 256
0	1	$\frac{FIR}{2}$ mod 256
1	0	$\frac{FIR}{4}$ mod 256
1	1	$\frac{FIR}{8}$ mod 256

Transfer of FIR coefficients

For the main data channels (tracks 0 to 7) there are 10 coefficients (taps) each of 8 bits, where all of the data channels make use of the same coefficients. The addresses for the main data coefficients 0 to 9 are 0 to 9_{dec} respectively.

There are ten coefficients (taps) each of 8 bits for the aux channel (CHAUX). The addresses for the auxiliary coefficients 0 to 9 are 16 to 25_{dec} respectively.

There are 2 banks of coefficients for both the aux and the main data channels, namely the 'buffer', and the 'active' banks. The microcontroller writes only to the 'buffer' banks, and reads only from the 'active' banks.

The microcontroller can poll the digital equalizer status bit BKSW to see when the switch occurs. BKSW starts life LOW, goes HIGH as a result of the bank switching and goes LOW as result of the complete value of a main data coefficient being received by the digital equalizer.

The microcontroller sets μCS HIGH before sending the new set of aux or main data coefficients, the digital equalizer resets it once the bank switch occurs.

The actual FIR coefficients that are used are a function of the tape head, read amplifier and type of tape (i.e. pre-recorded or own recorded) used, such information is outside of the scope of this data sheet.

Coefficient address counter (COEFCNT)

This 5 bit counter is used to point to the FIR coefficient to be transferred to or from the digital equalizer.

Table 12 Coefficient address counter.

BIT	7	6	5	4	3	2	1	0
Meaning	–	–	–	CC4	CC3	CC2	CC1	CC0
Default	0	0	0	0	0	0	0	0

Pin explanations and interfacing to other hardware

RESET

This is an active HIGH input which resets the SAA2023 and brings it into its default mode, DPAP. This reset does not affect the contents of the FIR filter coefficients in the digital equalizer. This should be connected to the system reset, which can be driven by the microcontroller. The duration of the reset pulse should be at least 15 μs.

SLEEP

This pin is an active HIGH input which puts the SAA2023 in a low power consumption SLEEP mode. This pin should be connected to the DCC SLEEP signal, which can be driven by the microcontroller. The CLK24 clock may be stopped and the VREFP and VREFN inputs brought to ground while the SAA2023 is in 'sleep' mode to further reduce power consumption. When recovering from sleep mode, the SLEEP pin should be taken LOW and the SAA2023 reset.

CLK24

This is the 24.576 MHz clock input and should be connected directly to the SAA2003 (pin CLK24).

Sub-band serial PASC interface connections

The timing for the sub-band serial PASC interface is given in Figs 5 to 7.

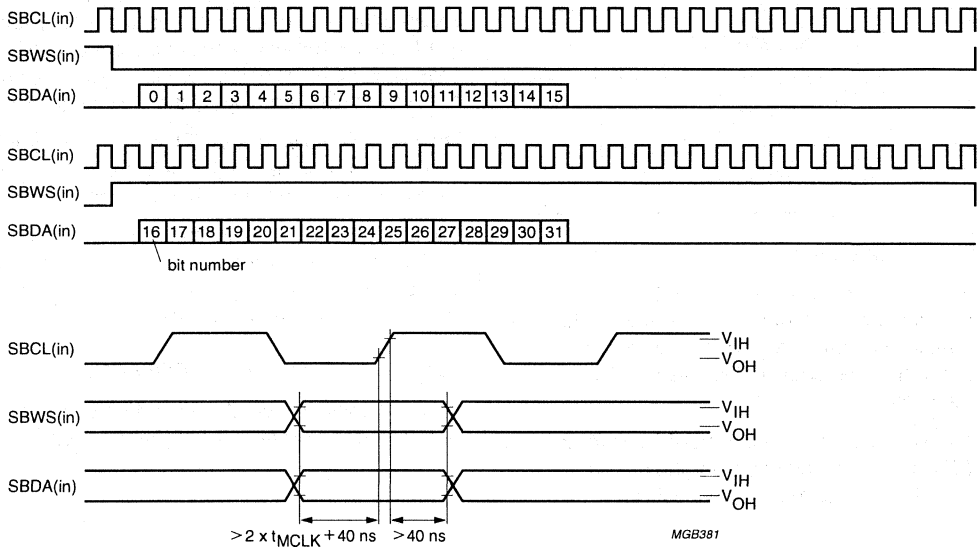


Fig.5 Sub-band serial PASC interface timing; DRAR mode.

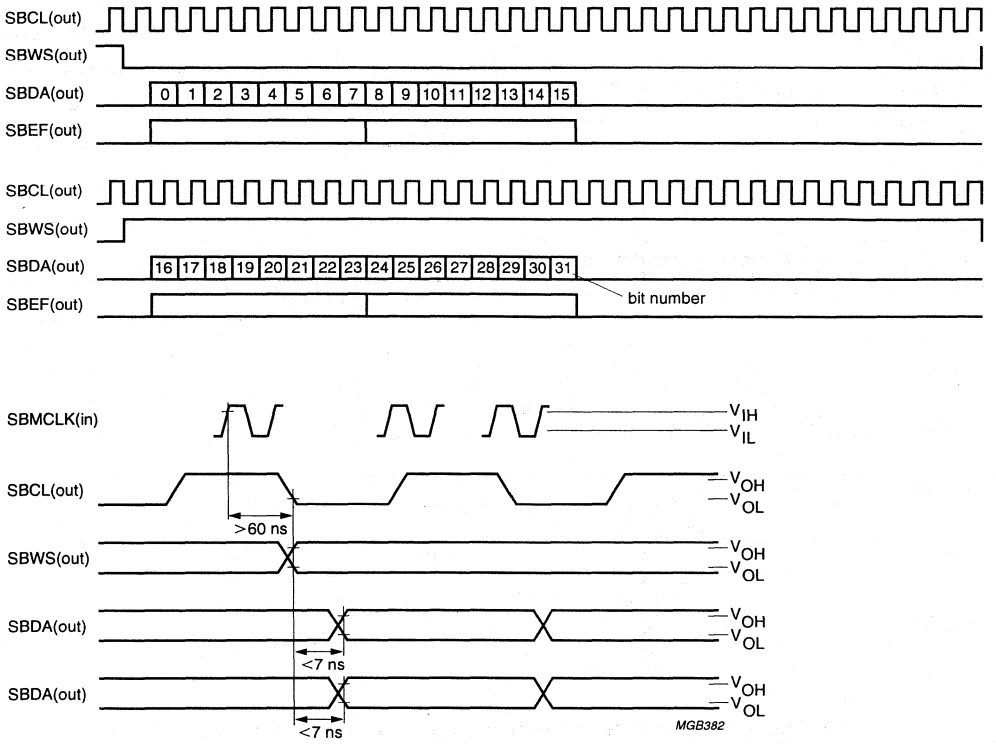


Fig.6 Sub-band serial PASC interface timing in play modes; DRPMAS = logic 1.

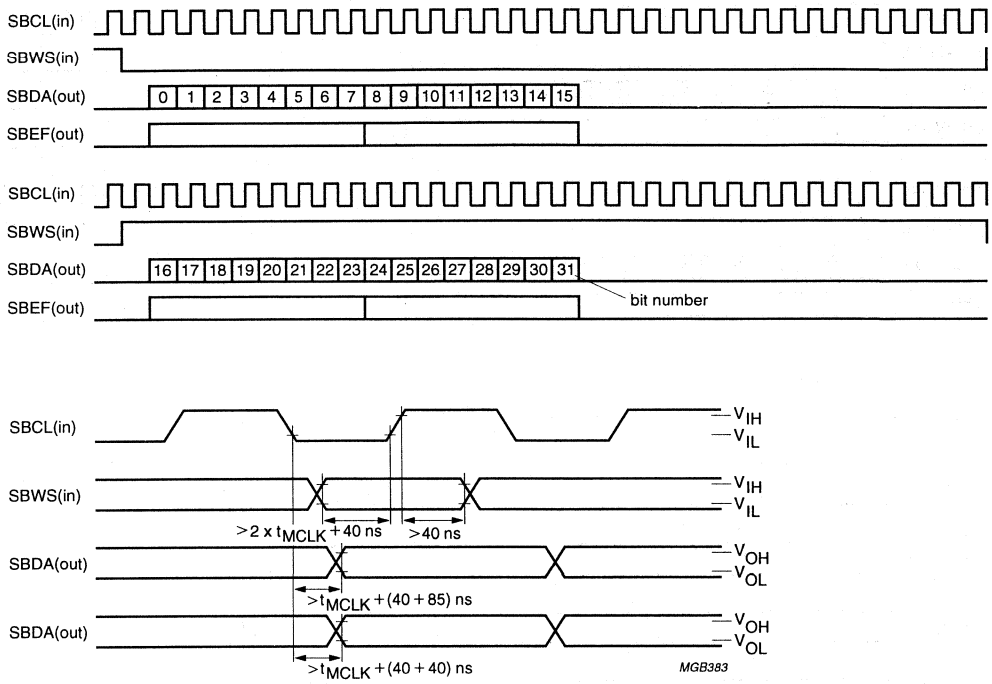


Fig.7 Sub-band serial PASC interface timing in play modes; DRPMAS = logic 0.

SBMCLK

This is the sub-band master clock input for the sub-band serial PASC interface. The frequency of this signal is nominally 6.144 MHz. When the SAA2023 is used with SAA2003 this pin is tied to ground, and the TFE settings bit 'DRPMAS' set to logic 1.

SBDIR

This output pin is the sub-band serial PASC bus direction signal, it indicates the direction of transfer on the sub-band serial PASC bus. This pin connects directly to the SBDIR pin on the SAA2003. The transfer directions are shown in Table 13.

Table 13 PASC bus transfer directions.

SBDIR	DIRECTION
1	SAA2023 to SAA2003 transfer (audio play)
0	SAA2003 to SAA2023 transfer (audio record)

SBCL

This input/output pin is the bit clock line for the sub-band serial PASC interface to the SAA2003. When used with SAA2003 this pin is input only. It has a nominal frequency of 768 kHz.

SBWS

This input/output pin is the word select line for the sub-band serial PASC interface to the SAA2003. When used with SAA2003 this pin is input only. It has a nominal frequency of 12 kHz.

SBDA

This input/output pin is the serial data line for the sub-band serial PASC interface to the SAA2003.

SBEF

This active HIGH output pin is the error-per-byte line for the sub-band serial PASC interface to the SAA2003.

URDA

This active HIGH output pin indicates that the main data (audio), the SYSINFO and the AUXILIARY data are NOT usable, regardless of the state of the corresponding reliability flags. The state of this pin is reflected in the URDA bit of STATUS byte 0, which can be read by the microcontroller. This pin should be connected directly to the URDA pin of the SAA2003. URDA goes active as a result of a reset, a mode change from mode DRAR to DPAP, or if the SAA2023 has had to re-synchronize with the incoming data from tape.

The position of the first sub-band serial PASC bytes in a tape frame is shown in Figs 8 and 9.

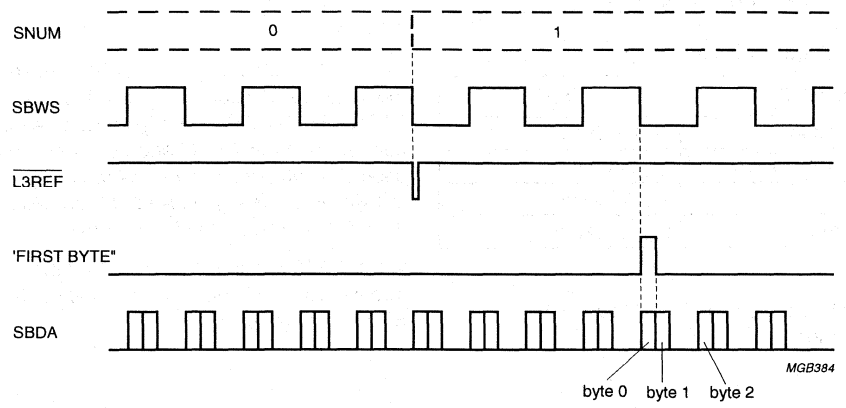


Fig.8 Position of first sub-band serial PASC bytes in a tape frame in DPAP/DPAR mode.

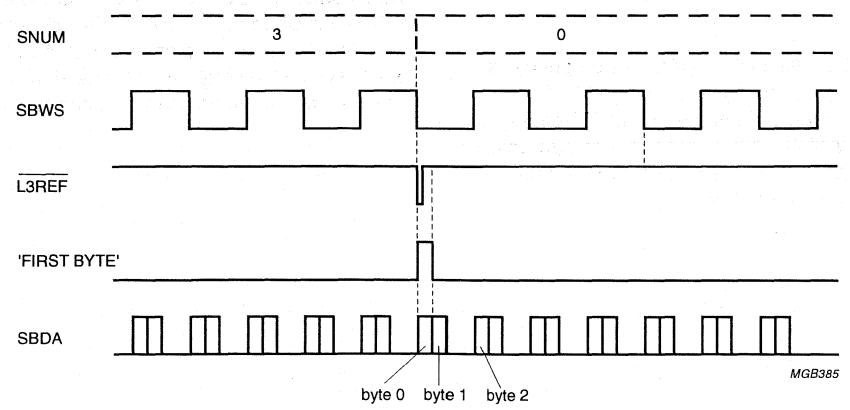


Fig.9 Position of first sub-band serial PASC bytes in a tape frame in DRAR mode.

RAM connections

The SAA2023 has been designed to operate with DRAMs and SRAMs. Suitable DRAMs are 64K × 4-bit or 256K × 4-bit configurations operating in page mode, with an access time of 80 to 100 ns. The timing for read, write and refresh cycles for DRAMs is shown in Figs 10 to 12. The timing for SRAMs is shown in Figs 13 to 19.

For fast SRAMs: (these values are subject to verification during characterization). The conditions (most critical at the required V_{DD}) are shown in Table 14.

Table 14 Fast SRAM conditions.

CONDITION[1]	TIME
Write pulse duration	$t_W \leq 140$ ns
Data set-up to rising $\overline{WEN}$	$t_{su} \leq 72$ ns
Write cycle time	$T_{cy} \leq 200$ ns
Read access time	$t_{ACC} \leq 240$ ns

Note

1. The SAA2023 should work in: RType = '01'; RTim = '00' mode.

A9/$\overline{CAS}$

When SAA2023 is used with SRAM this output pin is Address line 9, and should be connected directly to the corresponding address pin on the SRAM. When SAA2023 is used with DRAM this output pin is the column address strobe (active LOW), it connects directly to the column address strobe pin of the DRAM.

A10/$\overline{RAS}$

When SAA2023 is used with SRAM this output pin is Address line 10, and should be connected to the corresponding address pin of the SRAM. When SAA2023 is used with DRAM this output pin is the row address strobe (active LOW), it connects directly to the row address strobe pin of the DRAM.

$\overline{OEN}$

This output pin is the output enable (active LOW) for the RAM, it connects directly to the output enable pin of the RAM.

$\overline{WEN}$

This output pin is the write enable (active LOW) for the RAM, it connects directly to the write enable pin of the RAM.

A0 TO A8

When SAA2023 is used with DRAM these output pins are the multiplexed column and row address lines. When the 64K × 4-bit DRAM is used, pins A0 to A7 should be connected to the DRAM address input pins, and pin A8 should be left unconnected. When using the 256K × 4-bit DRAM the address pins A0 to A8 should be connected to the address input pins of the DRAM.

When SAA2023 is used with SRAM these are the lower address pins and should be connected directly to the SRAM address pins.

A11

This output pin is the an address pin for the SRAM and when SRAM is used they should be connected directly to the address pins of the SRAM. When DRAM is used this pin should not be connected.

A10 AND A12 TO A16

These output pins are the upper address pins for the SRAM and when SRAM is used they should be connected directly to the address pins of the SRAM. When DRAM is used or when the small SRAM is used all or some of these pins become available as Port expander outputs.

Table 15 Port expander outputs.

PIN NAME	PIN		PORT EXPANDER OUTPUT	CONDITIONS
	QFP80	TQFP80		
A14/PINO1	46	44	PINO1	RType = 00
A13/PINO2	50	48	PINO2	RType = 00
A16/PINO3	47	45	PINO3	RType = 00 or RType = 01
A15/PINO4	48	46	PINO4	RType = 00 or RType = 01
A12/PINO5	45	43	PINO5	RType = 00

D0 TO D3

When SAA2023 is used with SRAM these I/O pins form the lower nibble of the data bus connection to the RAM, and should be connected to the corresponding data I/O pins of the SRAM. When SAA2023 is used with DRAM these input/output pins are the data lines for the RAM, they should be connected directly to the DRAM data I/O pins.

D4 TO D7

These input/output pins are the upper nibble of the data bus for use with SRAM, and when SRAM is being used they should be connected directly to the corresponding SRAM I/O pins.

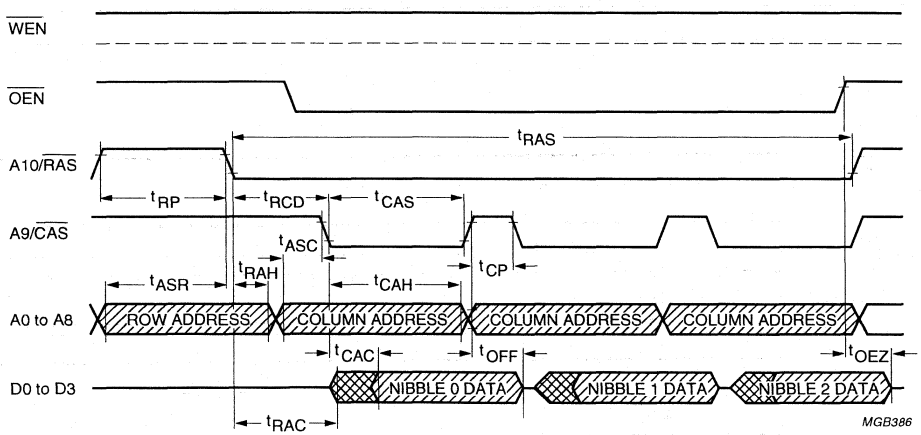


Fig.10 DRAM read cycle timing.

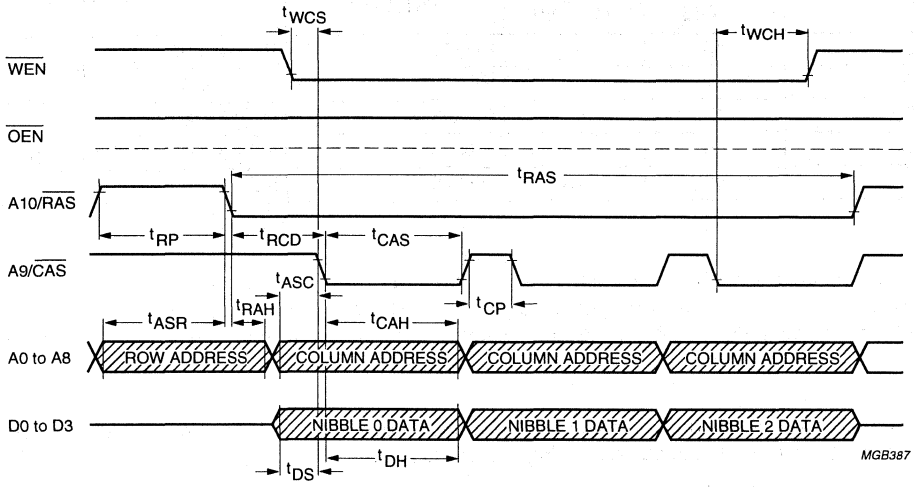


Fig.11 DRAM write cycle timing.

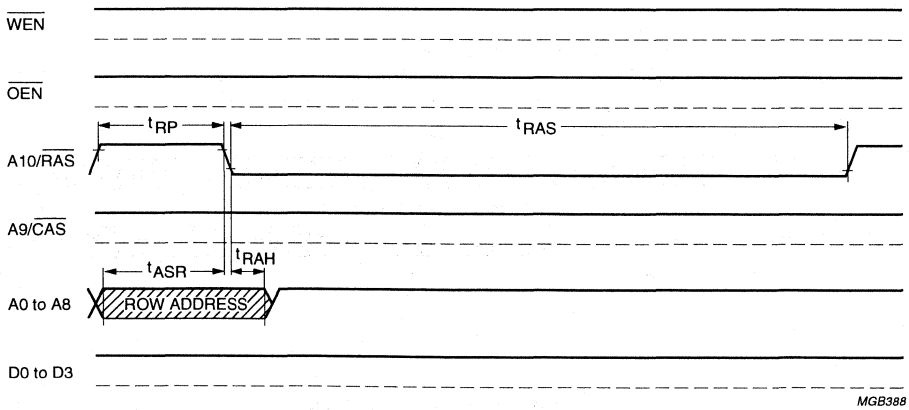


Fig.12 DRAM refresh cycle timing.

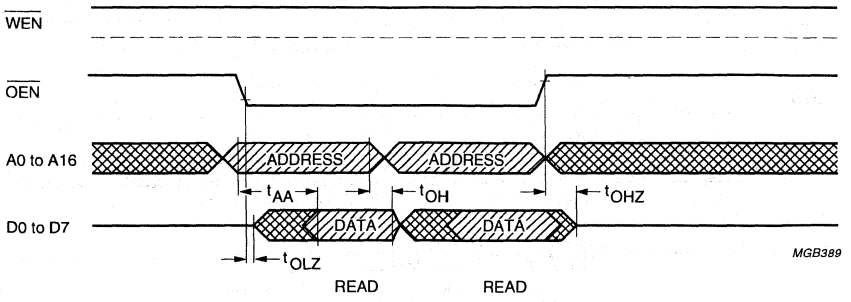


Fig.13 Fast SRAM read cycle timing.

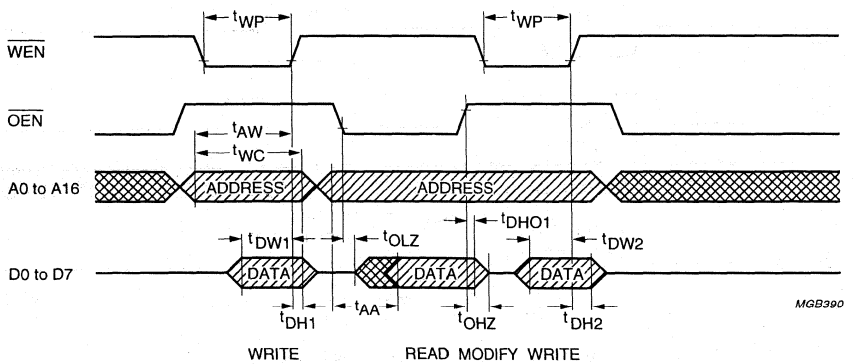


Fig.14 Fast SRAM write cycle timing; RTim = "00".

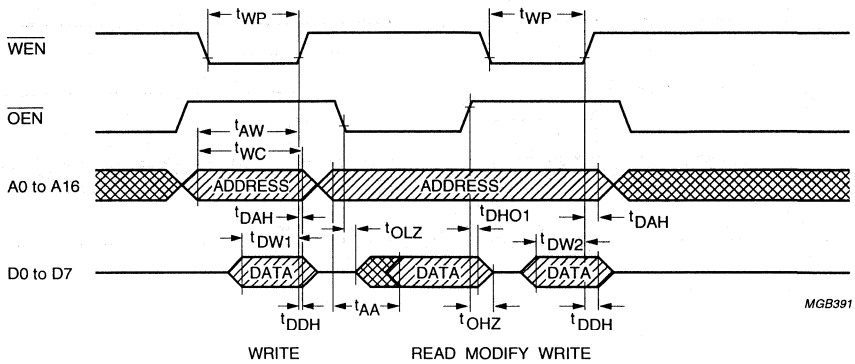


Fig.15 Fast SRAM write cycle timing; RTim = "01".

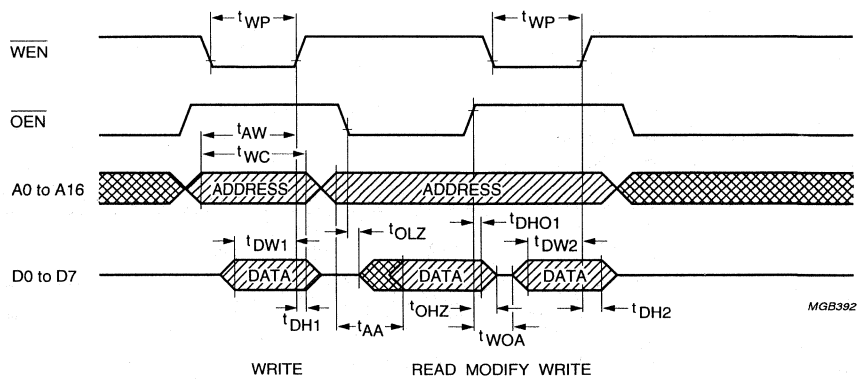


Fig.16 Fast SRAM write cycle timing; RTim = "10".

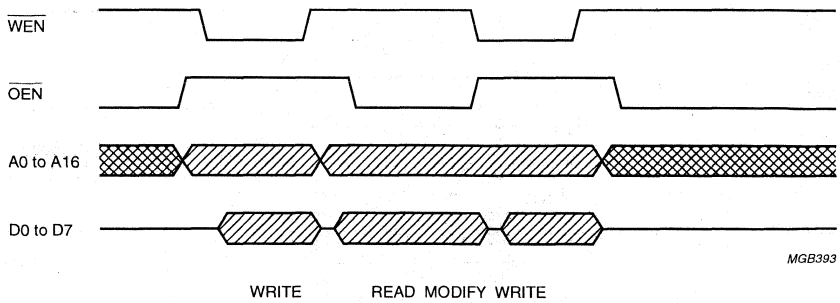


Fig.17 Fast SRAM write cycle timing; RTim = "11".

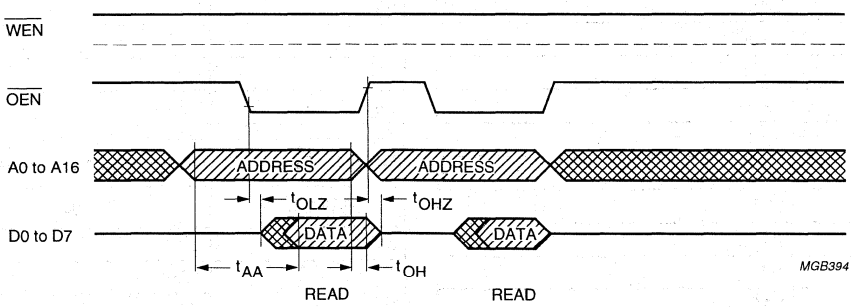


Fig.18 Slow SRAM read cycle timing.

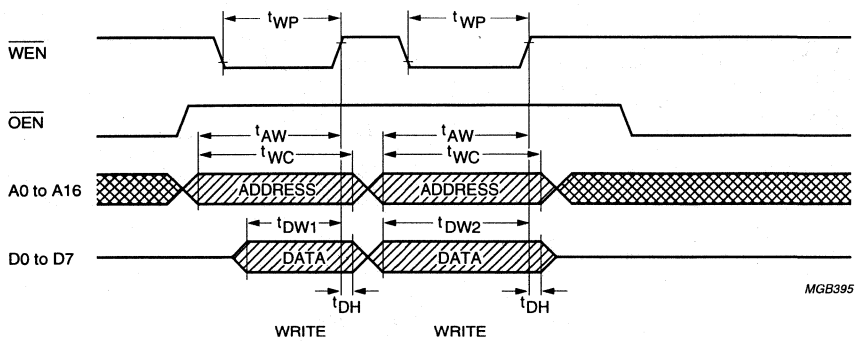


Fig.19 Slow SRAM write cycle timing.

Table 16 Timing values for Figs 10 to 12.

SYMBOL	VALUE (ns)
t_{RP}	≥110
t_{RAS}	≥510
t_{RCD}	≥70
t_{CP}	≥30
t_{CAS}	≥100
t_{ASR}	≥100
t_{RAH}	≥25
t_{ASC}	≥30
t_{CAM}	≥100
t_{DS}	≥25
t_{DH}	≥100
t_{WCS}	≥30
t_{WCH}	≥100
t_{RAC}	≤160
t_{CAC}	≤80

Table 17 Timing values for Figs 13 to 17.

SYMBOL	VALUE (ns)
t_{WP}	≥140
t_{AW}	≥180
t_{WC}	≥200
t_{DW}	≥72
t_{DM}	≥25
t_{AA}	≤240
t_{HC}	≥250

Table 18 Timing values for Figs 18 and 19.

SYMBOL	VALUE (ns)
t_{WP}	≥225
t_{AW}	≥260
t_{WC}	≥300
t_{DW}	≥140
t_{DM}	≥25
t_{AA}	≤280

Read/write connections

TCLOCK

This output pin is the 3.072 MHz clock output for the read and write amplifiers, it should be connected directly to the WCLOCK pin of the write amplifier and to the RDCLK pin of the read amplifier.

RDMUX

This input pin carries the time multiplexed analog tape channel signals from the read amplifier.

$V_{ref(n)}$ AND $V_{ref(p)}$

These are the lower and upper voltage reference inputs for the ADC in the digital equalizer part of SAA2023.

BIAS

This pin defines a bias current for the ADC. It should be connected to the analog supply voltage V_{DDA} via a 47 kΩ resistor.

RDSYNC

This output line provides synchronization information for the read Amplifier data transfers. The relationship between TCLOCK, RDSYNC and the channel information carried by the RDMUX line is given in Fig.20. This pin should be connected directly to the RDSYNC pin of the read amplifier. When the digital equalizer in SAA2023 is in search mode this pin will be HIGH ensuring that only the AUX channel is processed by the SAA2023.

WDATA

This output pin is the multiplexed data and control line for the write amplifier. Figure 21 shows the manner in which this information is multiplexed onto WDATA. The WDATA pin should be connected directly to the WDATA pin of the write amplifier.

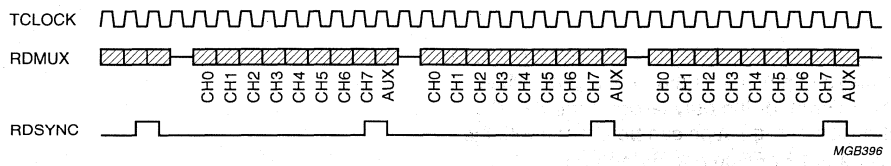


Fig.20 RDMUX, RDSYNC and TCLOCK timing.

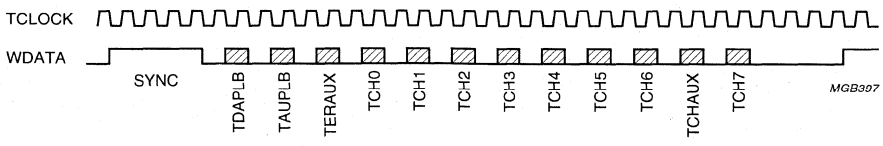


Fig.21 WDATA and TCLOCK timing.

Tape deck capstan control connections

SPEED

This pin outputs a pulse width modulated signal that may be used for controlling the tape capstan of the deck.

Operation of the SPEED control signal

Table 19 gives the sources that determine the duty factor of the SPEED signal. Note that the 3-state SPEED output may be put into high-impedance state by programming the TFE setting by bit HiZSpd.

Table 19 SPEED signal duty factor.

MODE	µCSPD	SOURCE FOR SPEED DUTY FACTOR
DPAP	0	tape(1)
DPAP	1	µC(2)
DPAR	0	tape(1)
DPAR	1	µC(2)
DRAR	0	50%(3)
DRAR	1	µC(2)

Notes

1. "Tape" means that the duty factor has been calculated from the played back main data tape signal. When tape is the source for the duty factor of the SPEED signal, the type of regulation can be chosen with the TFE settings bits EnFReg and SelNBand.
2. "µC" means that the microcontroller programs the duty factor via the SPDDTY register.
3. "50%" means that the duty factor is fixed at 50%.

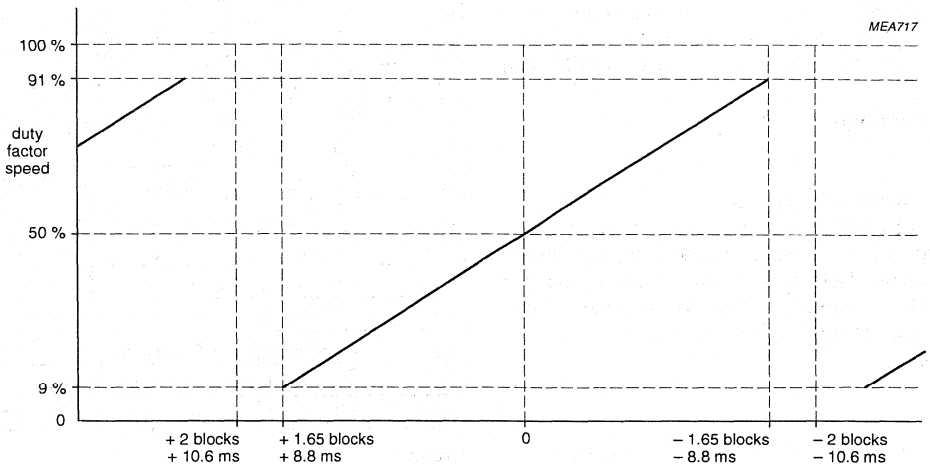


Fig.22 SPEED regulation duty factor as a function of phase characteristic.

If EnFReg is programmed 'LOW' then there is phase regulation of the capstan speed. The period of the pulse width modulated SPEED signal is 41.66 µs. The SAA2023 performs a new calculation to determine the duty factor of SPEED once every 21.33 ms, giving a sampling rate of approximately 46.9 Hz. This calculation is basically a phase comparison between the incoming Main Data tape frame and an internally generated reference. The SPEED duty factor as a function of phase characteristic is shown in Fig.22. As shown the duty factor increases monotonously from approximately 9% when the incoming Main Data tape frame is 1.65 tape blocks (8.8 ms) too early up to 91% when it is 1.65 tape blocks (8.8 ms) too late. Outside of a ±2 tape blocks range the pulse width characteristic overflows and repeats itself forming a sawtooth pattern. The SAA2023 has an internal buffer of ±8.8 ms outside of which the phase information is invalid.

If EnFReg is programmed 'HIGH' then the above description is over-ridden with frequency information. If the incoming main data bit rate deviation from the nominal 96000 bits/s rate is less than the Phase Only Threshold (POT) then the control is as described above in the phase control description. If the deviation is more than the Frequency Only Threshold (FOT) then the SPEED information is gated with the phase information resulting in the SPEED signal being continuously HIGH or LOW while the condition continues. If the deviation is between the POT and the FOT then the frequency information is gated with the Phase information for 50% of the time.

The deviation thresholds POT and FOT are programmable via the TFE settings bit SelNBand.

Table 20 POT and FOT deviation thresholds.

SelNBand	POT (DEVIATION FROM NOMINAL)	FOT (DEVIATION FROM NOMINAL)
0	±6%	±9%
1	±3%	±4.5%

If SLEEP is 'HIGH' then the state of the SPEED signal will be the state that it was in just before the SAA2023 went into sleep. Thus if SPEED was HIGH just before sleep it will stay HIGH during sleep. The same applies if it was LOW or if it was in 'high-Z' state. Note that a reset of the SAA2023 will take the SPEED signals out of 'high-Z' state.

Microcontroller connections

$\overline{\text{L3REF}}$

This active LOW output pin indicates the start of a time segment, it goes LOW for 5.2 µs once every 42.66 ms approximately and can be used for generating interrups for the microcontroller. If a re-synchronization occurs then the time between the occurrences van vary. This pin can be connected directly to the interrupt input of the microcontroller.

L3CLK

This input pin is the clock line for the microcontroller interface.

L3DATA

This input/output pin is the serial data line for the microcontroller interface.

L3MODE

This input determines the type of transfer that is occurring between the microcontroller and the SAA2023. If L3MODE is LOW then a device address can be sent by the microcontroller. If L3MODE is HIGH then a data transfer may be occurring.

L3INT

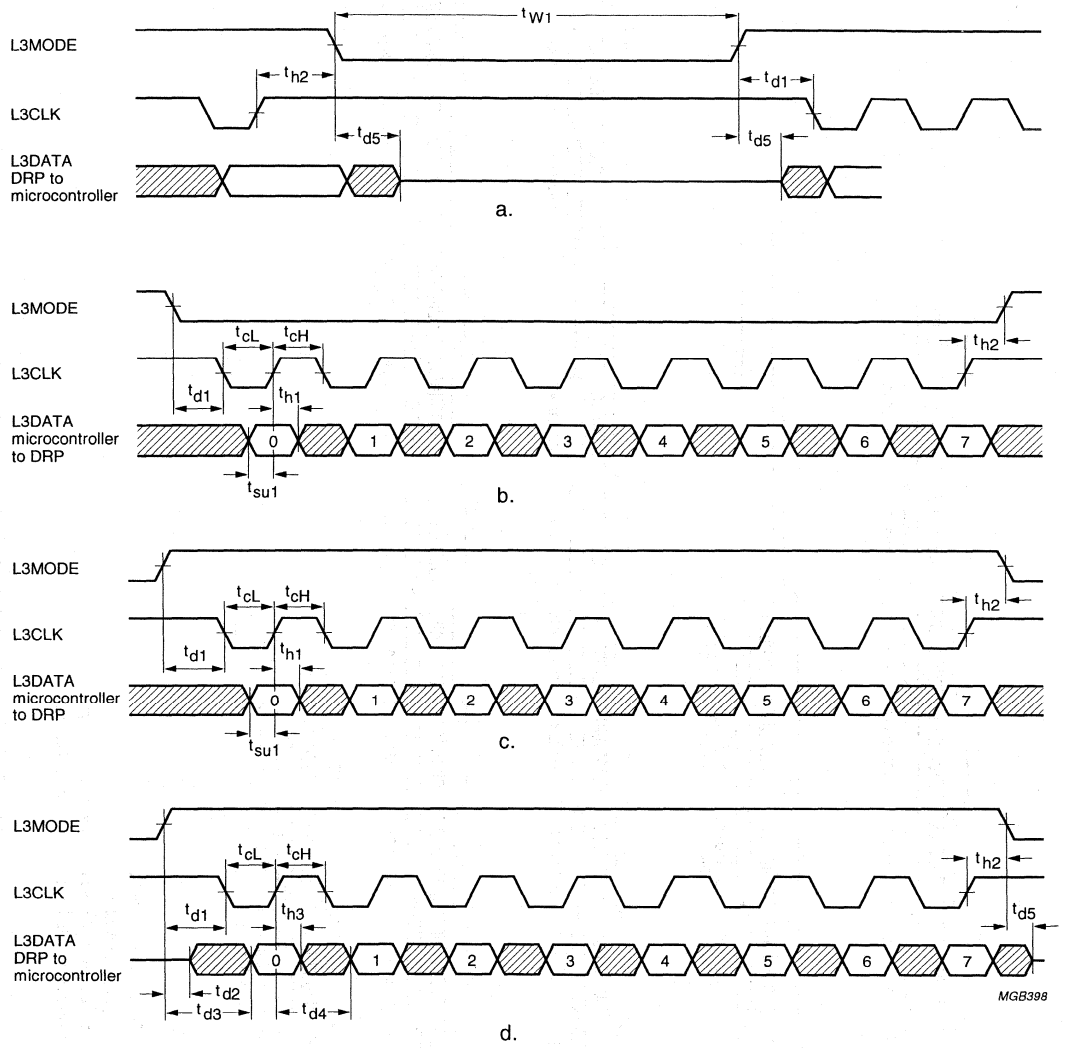
This pin carries interrupts from the digital equalizer module. It can also be programmed to reflect the state of the AENV, LABEL and VIRGIN signals.

Table 21 Timing values for Fig.23.

SYMBOL	TIME[1]
t_{W1}	$T + t_{su\ (L3MODE)} + t_{h\ (L3MODE)}$; $t_{w1} \geq 200$ ns
t_{d1}	$T + t_{su\ (L3MODE)} + t_{h\ (L3CLK)}$; $t_{d1} \geq 200$ ns
t_{h2}	$T + t_{su\ (L3CLK)} + t_{h\ (L3MODE)}$; $t_{h2} \geq 200$ ns
t_{d2}	$T + t_{su\ (L3CLK)} + t_{d\ (L3DATA)}$; $t_{d2} \leq 250$ ns
t_{d5}	$0 \leq t_{d5} \leq 50$ ns
t_{cL}	$T + t_{su\ (L3CLK)} + t_{h\ (L3CLK)}$; $t_{cL} \geq 200$ ns
t_{cH}	$T + t_{su\ (L3CLK)} + t_{h\ (L3CLK)}$; $t_{cH} \geq 200$ ns
t_{su1}	$T + t_{su\ (L3DATA)} + t_{h\ (L3CLK)}$; $t_{su1} \leq 200$ ns
t_{h1}	$T + t_{su\ (L3CLK)} + t_{h\ (L3DATA)}$; $t_{h1} \leq 35$ ns
t_{d3}	$2 \times T + t_{su\ (L3MODE)} + t_{d\ (L3DATA)}$; $t_{d3} \leq 250$ ns
t_{h3}	$T + t_{h\ (L3CLK)} + t_{d\ (L3DATA)}$; $t_{h3} \geq 50$ ns
t_{d4}	$2 \times T + t_{su\ (L3CLK)} + t_{d\ (L3DATA)}$; $t_{d4} \leq 410$ ns
t_{d4}[2]	$3 \times T + t_{su\ (L3CLK)} + t_{d\ (L3DATA)}$; $t_{d4} \leq 575$ ns

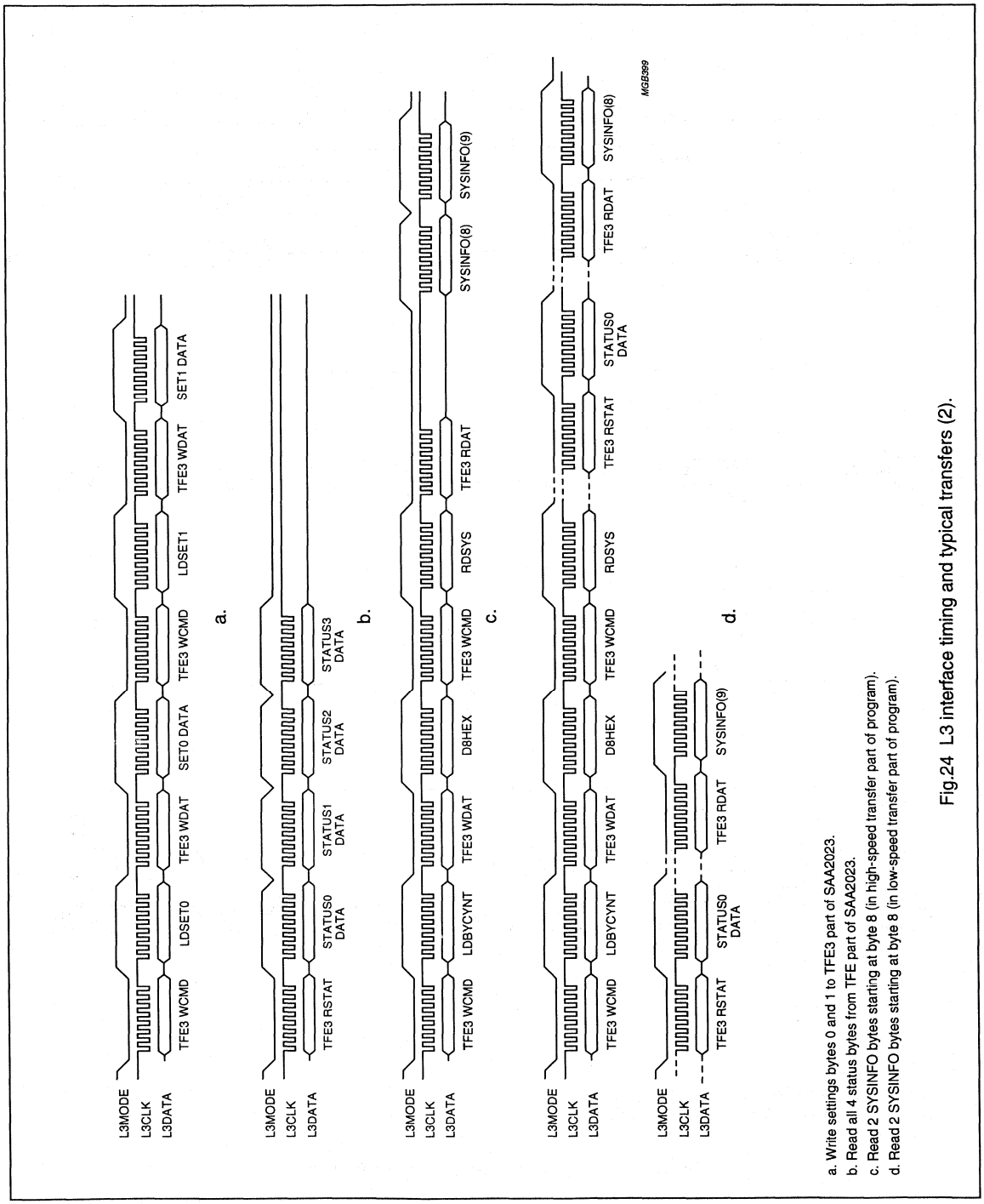
Notes

1. T is the period of the master clock on the chip.
2. t_{d4} is the delay time between the last bit of a byte and first bit of the next byte, if no 'halt' is used.



a. Halt mode.
b. Addressing mode.
c. Data mode (transfer from microcontroller to SAA2023).
d. Data mode (transfer from SAA2023 to microcontroller).

Fig.23 L3 interface timing and typical transfers (1).



a. Write settings bytes 0 and 1 to TFE3 part of SAA2023.
b. Read all 4 status bytes from TFE part of SAA2023.
c. Read 2 SYSINFO bytes starting at byte 8 (in high-speed transfer part of program).
d. Read 2 SYSINFO bytes starting at byte 8 (in low-speed transfer part of program).

Fig.24 L3 interface timing and typical transfers (2).

SAA2023 test pins

TEST0 TO TEST3

These input pins are for test only, **do not connect**.

AZCHK

This output pin indicates the occurrence of a tape channel sync symbol on tape channels TCH0 and TCH7, the distance between the pulses for the TCH0 and TCH7 channels gives a measure of the azimuth error between the tape and head alignment. Figure 25 shows the typical timing for this signal.

ERCOSTAT

This output pin can be connected to a symbol error rate measurement system.

Port expansion pins

PINI

This input pin is connected directly to the PINI bit in the status byte 1, it can be read by the microcontroller, and may be used for any CMOS level compatible input signals.

PINO1

This output pin is connected directly to the PINO1 bit of the TFE settings 0 register. The microcontroller can set or reset this pin.

PINO2 TO PINO5

Depending upon the type and the size of system RAM used, some or all of these Port expander output pins may be available, (please see Section "RAM connections" "A10 and A12 to A16" on interfacing to the RAM pins).

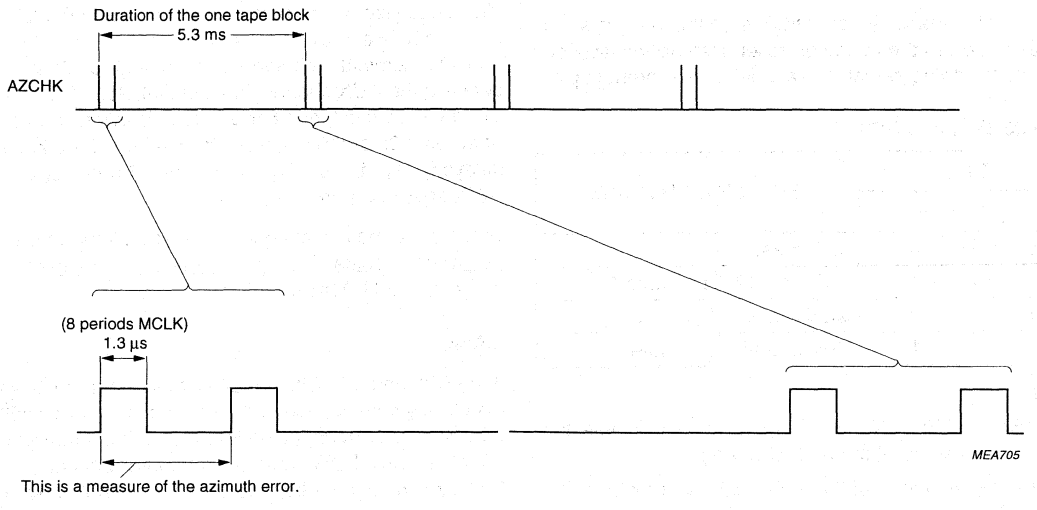
Supply pins

V_{DD1} TO V_{DD6}

These are the supply pins, all of these pins must be connected. We recommend that each power supply pin pair (i.e. V_{DD1} to V_{SS1}, V_{DD2} to V_{SS2}, etc.) be decoupled using a 22 nF capacitor as close as is physically possible to the pins of the SAA2023.

V_{SS1} TO V_{SS6}

These are the supply ground pins, all of which must be connected.



Nominal Inter Frame Gap (IFG) lasts 660 µs.

Fig.25 AZCHK timing.

V_{DD7}

This is the supply pin for the output buffers to the data lines of the system RAM. It should always be connected externally. Decouple this pin with a 22 nF capacitor to the V_{SS7} pin.

V_{SS7}

This is the ground supply pin for the output buffers of the data lines of the system RAM. This pin is connected internally to all the supply ground pins (V_{SS1} to V_{SS6}), however it should always be connected externally.

Auxiliary envelope detection

INTMASK

INTMASK is a interrupt mask register. This register sets the mode of operation for the interrupt interface, and is writable only.

Table 22 Interrupt mask register.

BIT	7	6	5	4	3	2	1	0
Meaning	BP1	BP0	Vup(1)	AEup(2)	AEdn(3)	Lup(4)	Ldn(5)	ECZ(6)
Default	0	0	0	0	0	0	0	0

Notes

1. Vup ≡ rising edge of VIRGIN interrupt.
2. AEup ≡ rising edge of AUX envelope interrupt.
3. AEdn ≡ falling edge of AUX envelope interrupt.
4. Lup ≡ rising edge of LABEL interrupt.
5. Ldn ≡ falling edge of LABEL interrupt.
6. ECZ ≡ AUX envelope counter has just reached zero interrupt.

BP1 AND BP0 (BYPASS)

If any of the bypass bits are HIGH then the interrupts are not passed on to the microcontroller, instead the level of the corresponding signal is available an the interrupt pin.

Table 23 BP1 and BP0.

BP		EFFECT OF BYPASS
1	0	
0	0	no bypass
0	1	LAB on L3INT pin; note 1
1	0	AENV on L3INT pin; note 2
1	1	VIR on L3INT pin; note 3

Notes

1. LAB = LABEL (HIGH if a LABEL condition is detected in the envelope of the AUX channel).
2. AENV = envelope of the AUX channel (1 bit binary).
3. VIR = VIRGIN (indicated by the total [continuous] absence of signal on the AUX channel).

The AUX envelope information is only valid when the digital equalizer is in search mode and when the tape speed is between the values of 3 to 48 × nominal tape speed. The timing relationships between the AUX channel input signal, AENV, LAB and VIR are shown in Figs 26 to 28. The delays t_{d1} and t_{d2} are between 0.25 and $0.5t_{AUX}$ (AUX envelope periods). The delays t_{d3}, t_{d4}, t_{d5} and t_{d6} are between 2 and $6t_{AUX}$ (AUX envelope periods).

When using the digital equalizer in search mode first program the digital equalizer to search mode, then program the INTMASK register.

MASK

If the BP1 and BP0 bits are LOW then the mask bits take effect. Any combination of the mask bits may be HIGH, enabling the corresponding interrupts. The interrupt pin L3INT is active LOW when used for interrupts and active HIGH when used for bypassing. So if it is not in bypass mode and at least one of the interrupts has occurred it will go LOW and stays LOW until DEQ status byte 0 has been read. Extra interrupts that occur after the first interrupt and before the DEQ status byte 0 is read are seen in the status register. Extra interrupts that occur after the status byte

has been read will generate a new interrupt. Interrupts that are already noted in the digital equalizer Status 0 are cleared by reading it.

Table 24 Digital equalizer STATUS0.

BIT	7	6	5	4	3	2	1	0
Meaning	BKSW(1)	TEST	Vup(2)	AEup(3)	AEdn(4)	Lup(5)	Ldn(6)	ECZ(7)

Notes

1. BKSW (filter bank switched) indicates that the last main data coefficients sent to the digital equalizer have been activated.
2. Vup indicates whether an interrupt caused by the rising edge of VIRGIN has occurred.
3. AEup indicates whether an interrupt caused by the rising edge of AUX envelope has occurred.
4. AEdn indicates whether an interrupt caused by the falling edge of AUX envelope has occurred
5. Lup indicates whether an interrupt caused by the rising edge of LABEL has occurred.
6. Ldn indicates whether an interrupt caused by the falling edge of LABEL has occurred.
7. ECZ indicates that the AUX envelope counter has reached zero.

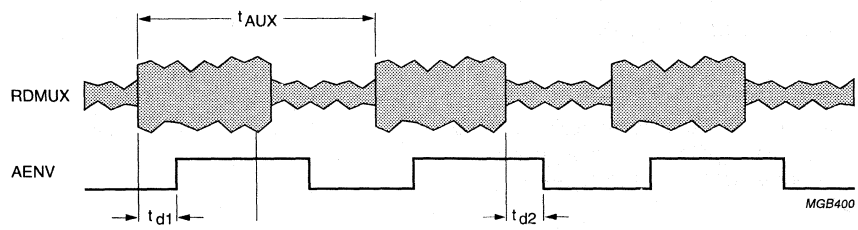


Fig.26 AUX channel envelope to AENV delays.

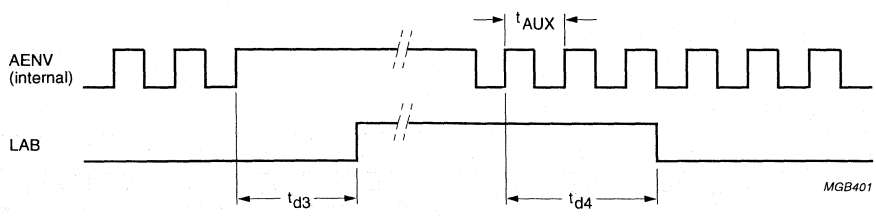


Fig.27 AENV to LAB delays.

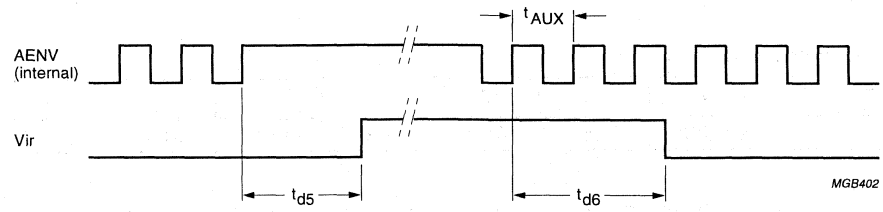


Fig.28 AENV to VIR delays.

Table 25 Digital equalizer STATUS1.

BIT	7	6	5	4	3	2	1	0
Meaning	–	–	–	–	–	VIR(1)	AENV(2)	LAB(3)

Notes

1. VIR gives the state of the VIRGIN signal.
2. AENV represents the state of the AENV signal.
3. LAB gives the state of the LAB signal.

AUX envelope count (AECNT) register

This 16 bit register is used for loading the AUX envelope counter and for reading the state of that counter, it is therefore readable and writable as 2 bytes. Least Significant Byte first.

Table 26 AECNT register.

AECNT	LEAST SIGNIFICANT BYTE								MOST SIGNIFICANT BYTE							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Meaning	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8

Search speed (SSPD) register

$$\text{Search speed} = \left(2^{SR}\right) \times \left(\frac{51.2}{SV}\right) \times \text{normal speed}$$

Table 27 Search speed register.

BIT	7	6	5	4	3	2	1	0
Meaning	SVF(1)	SV4(2)	SV3(2)	SV2(2)	SV1(2)	SV0(2)	SR1(3)	SR0(3)

Notes

1. SVF speed validation flag, if HIGH then the search speed measurement is invalid.
2. SV4 to SV0 search speed value.
3. SR1 and SR0 search speed range.

ANAEYE register

Table 28 ANAEYE register analog eye pattern selection register.

BIT	7	6	5	4	3	2	1	0
Meaning	–	–	–	AEN(1)	ACHN3(2)	ACHN2(2)	ACHN1(2)	ACHN0(2)
Default	0	0	0	0	0	0	0	0

Notes

1. AEN analog eye pattern output enable. If this bit is LOW the Digital-to-Analog Converter (DAC) is switched off and the output is HIGH.
2. ACHN3 to ACHN0 select channel for analog eye output.

Table 29 ACHN3 to ACHN0 channel selections for analog eye output.

ACHN				CHANNEL ON ANAEYE
3	2	1	0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	AUX

T1sel register

Table 30 T1SEL register CHTST1 pin selection register.

BIT	7	6	5	4	3	2	1	0
Meaning	–	T1F2	T1F1	T1F0	T1C3	T1C2	T1C1	T1C0
Default	0	0	0	0	0	0	0	0

Table 31 T1C3 to T1C0 CHTST1 pin channel selections.

T1C				CHANNEL ON CHTST1
3	2	1	0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	AUX

Table 32 T1F2 to T1F0 CHTST1 pin function selections.

T1F			FUNCTION OF CHTST1 PIN
2	1	0	
0	0	0	off; logic 0
0	0	1	digital eye pattern
0	1	0	sliced data
0	1	1	bit clock
1	0	0	clock extraction frequency

The digital eye pattern is in 8 bits two's complement notation, the sliced data and the bit clock give the current binary state of the corresponding signals, and the clock extraction frequency output is in 8 bits offset binary format. The timing diagrams for the digital eye pattern output and the clock extraction frequency output are shown in Fig.29.

T2sel register

Table 33 T2SEL register CHTST2 pin selection register.

BIT	7	6	5	4	3	2	1	0
Meaning	–	T2F2	T2F1	T2F0	T2C3	T2C2	T2C1	T2C0
Default	0	0	0	0	0	0	0	0

Table 34 T2C3 to T2C0 CHTST2 pin channel selections.

T2C				CHANNEL ON CHTST2
3	2	1	0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	AUX

Table 35 T2F2 to T2F0 CHTST2 pin function selections.

T2F			FUNCTION OF CHTST2 PIN
2	1	0	
0	0	0	off; logic 0
0	0	1	digital eye pattern
0	1	0	sliced data
0	1	1	bit clock
1	0	0	clock extraction frequency

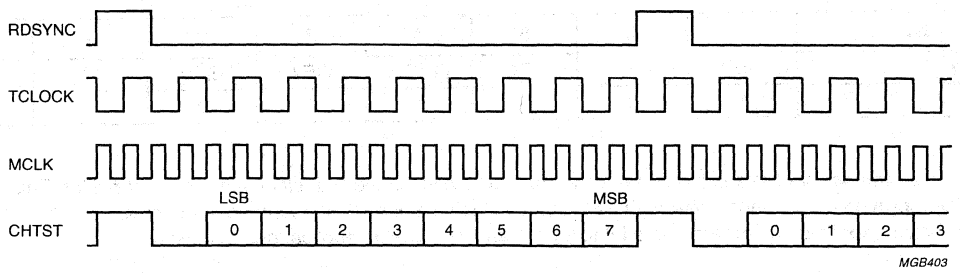


Fig.29 CHTST1 and CHTST2 output timing.

Table 36 DEQSET digital equalizer settings.

BIT	7	6	5	4	3	2	1	0
Meaning	–	–	–	–	–	ACup[1]	DM1	DM0
Default	0	0	0	0	0	0	0	0

Note

1. ACup is the AUX envelope counter direction is up. This setting caused the AUX envelope counter increment or to decrement by 1 every rising edge of the AUX envelope signal AENV.

DM1 and DM0

Table 37 DM1 and DM0 digital equalizer mode of operation.

DM		MODE OF OPERATION OF DIGITAL EQUALIZER
1	0	
0	0	normal[1]
0	1	search[2]
1	0	off[3]
1	1	off[3]

Notes

1. In normal mode the main data channels and the AUX channel are processed (equalized), the AUX channel envelope information is not processed.
2. In search mode only the AUX channel is processed by the digital equalizer.
3. Off means that the digital equalizer is put to sleep (low power), this can be used for example in portable recording equipment. RDSYNC is HIGH if off mode. Also note that the other digital equalizer registers are not addressable while the digital equalizer is in off mode.

CLKSET

Table 38 CLKSET clock extraction settings.

BIT	7	6	5	4	3	2	1	0
Meaning	LEAE(1)	FR1	FR0	GNOR	GE1	GE0	RD1	RD0
Default	1	0	0	1	1	0	1	0

Note

1. LEAE (leakage enable): this setting enables a leakage function in the PLL clock extraction loop filter. This gives a slightly improved performance with high SER tapes at the cost of a slight decrease in dynamic performance. For home (static) applications program this bit to logic 1 and for portable applications to logic 0.

Table 39 FR1 and FR0 clock extraction frequency range control.

FR		EFFECT ON PLL FREQUENCY LOOP
1	0	
0	0	range ±8%
0	1	range ±16%
1	0	range ±22%
1	1	range ±28%

Note that in the (FR = 0) range the clock extraction stays in its normal range only, hence it does not enter the extended range.

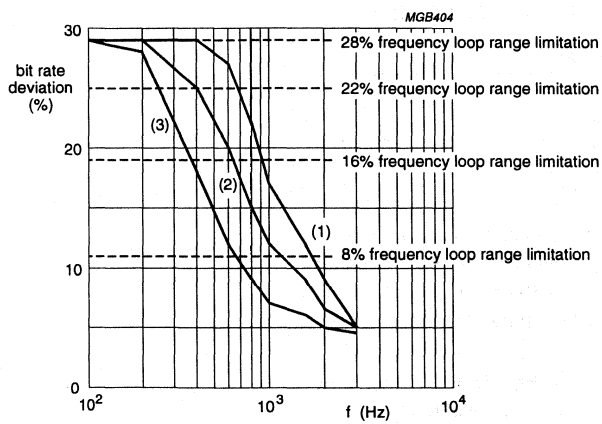
Figure 30 shows the lock characteristic of the clock extraction PLL.

Table 40 GNOR gain in normal frequency range mode of clock extraction.

GNOR	EFFECT ON GAIN IN NORMAL RANGE
0	gain 2; for portable (mobile) applications
1	gain 1; for home (static) applications

Table 41 GE1 and GE0 gain in extended frequency range mode of clock extraction.

GE		EFFECT ON PLL GAIN IN EXTENDED RANGE
1	0	
0	0	gain 2
0	1	gain 3
1	0	gain 4
1	1	gain 5; do not use



(1) Gain 4.
(2) Gain 3.
(3) Gain 2.

Fig.30 Clock extraction PLL lock characteristic.

RD1 and RD0 return delay

This is the delay before returning to normal mode after being in 'extended range mode' (i.e. the number of consecutive channel clock bit periods where the bit clock frequency falls within the normal range before the clock extraction returns to normal frequency mode).

Table 42 RD1 and RD0 return delay.

RD		DELAY IN BITS TO RETURN TO NORMAL MODE
1	0	
0	0	64
0	1	128
1	0	256
1	1	512

SYSINFO and AUX data offsets in the SAA2023

AUX data consists of 4 blocks of 36 bytes, one block being transferred in each (n) time segment.

The 128 bytes in each tape frame contain SYSINFO. The SYSINFO bytes can for convenience, be considered as being grouped into 4 SYSINFO blocks with:
SYSBLK0 → SI0 to SI31, SYSBLK1 → SI31 to SI63, etc.

In modes DPAP and DRAR SYSINFO transfers may occur in two ways:

1. 4 blocks of 36 bytes, one block being transferred to the SAA2023 in each time segment.
2. 1 block of 128 bytes being transferred in time segment 1.

In mode DRAR SYSINFO must be transferred as 4 blocks of 32 bytes, one block in each segment.

Figures 31 to 34 show the offsets between the SYSINFO and AUX and the time segment counter, for the various modes of operation of the SAA2023.

Table 43 Block offsets with respect to time segment.

MODE	DESCRIPTION
DPAP	SYSBLK = (SNUM + 3) MOD4; or read all 4 SYSINFO blocks when SNUM = logic 0; if AUX and main were recorded simultaneously then AUXBLK = (SNUM + 1) MOD4; else read and interpret 1 AUX block in each time segment.
DRAR	SYSBLK = SNUM; AUXBLK = (SNUM + 1) MOD4
DPAR	SYSBLK = (SNUM + 3) MOD4; or read all 4 SYSINFO blocks when SNUM = logic 0

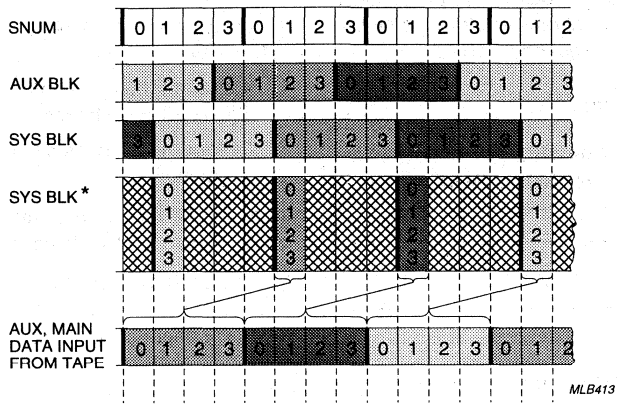


Fig.31 SYSINFO and AUX block delays in DPAP mode; audio and AUX simultaneously recorded.

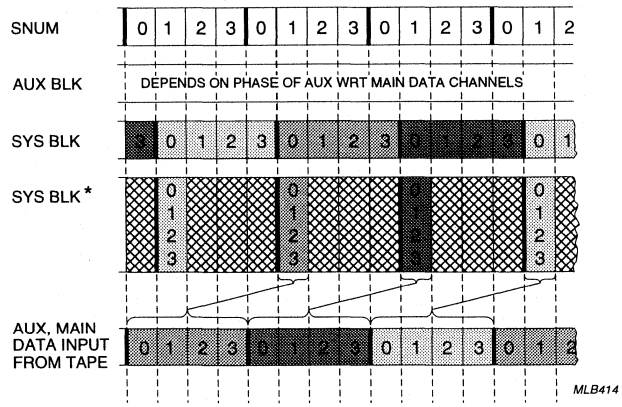


Fig.32 SYSINFO and AUX block delays in DPAP mode; audio and AUX separately recorded.

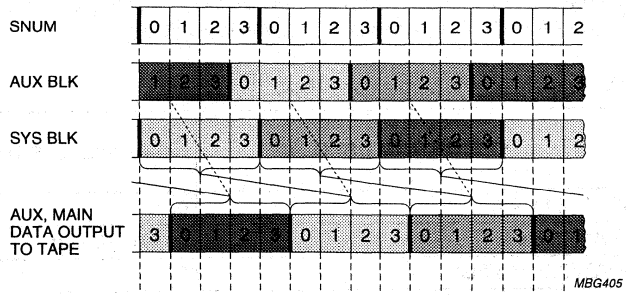


Fig.33 SYSINFO and AUX block delays in DRAR mode.

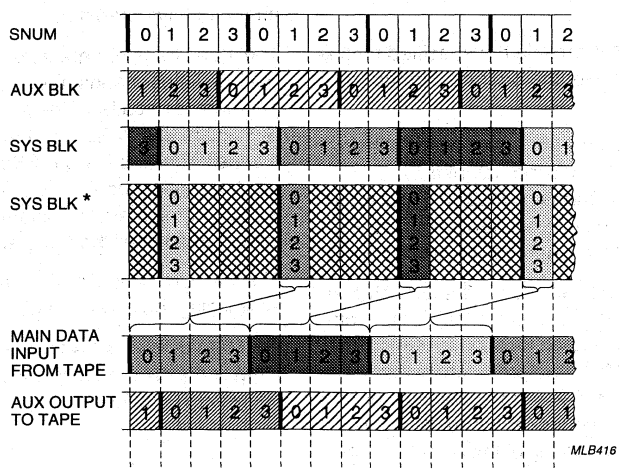


Fig.34 SYSINFO and AUX block delays in DPAR mode.

Scratch pad RAM

The SAA2023 provides the microcontroller with a scratch pad RAM that the microcontroller can use for whatever it likes. The size of the scratch pad depends upon the size and type of RAM used with the SAA2023. The locations in the scratch pad RAM may be written and read in 8 bit or 12 bit units.

The RAM may be viewed as having up to 4 quarters, the availability of these quarters for the scratch pad RAM is given in Table 44.

Table 44 Availability of RAM quarters for the scratch pad RAM.

RTYPE		TYPE OF RAM USED	AVAILABLE RAM QUARTERS YZ[1]
1	0		
0	0	DRAM 64K × 4	00
0	0	DRAM 256K × 4	00, 01, 10 and 11
0	1	SRAM 32K × 8 fast	00
1	0	SRAM 128K × 8 fast	00, 01, 10 and 11
1	1	SRAM (2×) 32K × 8 slow	00
1	1	SRAM 128K × 8 slow	00 and 10

Note

1. In RAM quarter YZ = 00, the scratch pad is arranged as 6 pages, where each page consists of 7 columns × 64 rows. The pages are numbered **0 to 5**, the columns **1 to 7** and the rows **0 to 63**. This gives a total of (6 × 7 × 64) 2688 locations.

   In each of the RAM quarters YZ = 01, 10 and 11 the scratch pad is arranged as 6 pages where each page consists of 8 columns × 448 rows. The pages are numbered **0 to 5**, the columns **0 to 7** and the rows **0 to 447**. This gives then a total of (6 × 8 × 448) 21504 locations per RAM quarter YZ.

During communication with the scratch pad RAM, the RAM quarter YZ is chosen when sending the RDDRAC, RDWDRAC, WRDRAC or WRWDRAC commands to the TFE module.

Use of the scratch pad RAM outside the specified ranges is not allowed and it may upset the operation of the SAA2023.

As with SYSINFO and AUX transfers can occur at high speed at all times except the second half of time segment 0, that is when the status bit SLOWTFR is HIGH. When SLOWTFR is HIGH the microcontroller must poll the status bit RFBT to investigate when a transfer can occur.

Two addressing modes are available for the scratch pad, namely random access and auto-increment. For random access mode the address of each location is sent by the microcontroller to the SAA2023 before each location transfer. For auto-increment mode the address of the first location is sent by the microcontroller before the first location transfer, auto-incrementing of the row occurs then for all transfers until the end of the column.

The 8 bit transfers are initiated by the WRDRAC and RDDRAC commands, these transfers are each 1 byte per memory location, therefore the byte counter will increment after each byte transfer.

The 12 bit transfers are initiated by the WRDRAC and RDDRAC commands, these transfers are each 2 bytes per memory location. The first byte contains the 4 Most Significant Bits (MSBs) of the memory location in its 4 Least Significant Bits (LSBs) positions. The other bit positions being 'don't care'. The second byte contains the 8 LSBs of the memory location. The byte counter is incremented after the transfer of the second byte.

The RACCNT and BYTCNT registers are used for addressing the scratch pad.

For RAM quarter YZ = 00 the mapping of the scratch pad RAM address onto the RACCNT and BYTCNT registers is shown in Table 45.

Table 45 Mapping of scratch pad RAM address for RAM quarter YZ = 00.

REGISTER	RACCNT							BYTCNT							
BIT	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Value	P2	P1	P0	C2	C1	C0	1	1	R6	R5	R4	R3	R2	R1	R0

For The other three quarters of the RAM the mapping of the scratch pad RAM address onto the RACCNT and BYTCNT registers is shown in Table 46.

Table 46 Mapping of scratch pad RAM address for RAM quarter YZ = 01, 10 and 11.

REGISTER	RACCNT							BYTCNT							
BIT	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Value	P2	P1	P0	C2	C1	C0	R8	R7	R6	R5	R4	R3	R2	R1	R0

Mode changes

The possible mode changes for the TFE are shown in Table 47.

Table 47 Mode changes.

CURRENT MODE	NEW MODE		
	DPAP	DRAR	DPAR
DPAP	–	yes	yes
DRAR	yes	–	no
DPAR	yes	no	–

TIMING FOR SAA2023 MODE CHANGES

Mode change DPAP to DRAR

This mode change occurs at the end of the time segment in which the TFE module receives the new settings. Writing of the first Main and AUX data to tape starts at the start of the time segment 1 which occurs 2 'end of time segment 3' s after the mode change. The delay to writing to tape is approximately 222 ms, as shown in Fig.35.

If 'seamless appending' is required the new settings should be sent to the TFE module during time segment 2.

Mode change DPAP to DPAR

This mode change occurs at the first end of time segment 2 after the TFE module receives the new settings. Output of AUX to tape begins at the start of the following time segment 1, (i.e. approximately 85.3 ms after the mode change), as shown in Fig.36.

Mode change DRAR to DPAP

This mode change occurs at the first end of time segment 0 after the TFE module receives the new setting. Writing of Main and AUX data stops immediately after the mode change.The time segment jumps back to logic 0, URDA goes HIGH and stays HIGH for 5 time segments (i.e. approximately 213.3 ms) after which it goes LOW, as shown in Fig.37.

Mode change DPAR to DPAP

This mode change occurs at the first end of time segment 0 after the TFE module receives the new setting. The writing of AUX data to tape stops immediately after the mode change. The first AUX read from tape can be expected during the following time segment 0 or 1 (i.e. approximately 128 to 170.67 ms after the mode change), as shown in Fig.38.

Mode change DPAP to search

This mode change occurs almost instantaneously, program the digital equalizer module in SAA2023 to go to search mode, then program the interrupt mask register to select the required type of interrupt.

Mode change search to DPAP

This mode change occurs almost instantaneously, program the interrupt mask register to disable interrupts program the digital equalizer module of SAA2023 to go to normal mode. A re-synchronization will most likely occur when as result of the data being read from tape, thus causing URDA to go HIGH.

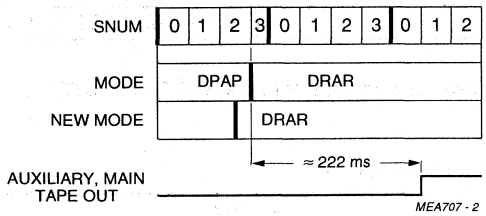


Fig.35 Mode change to DRAR.

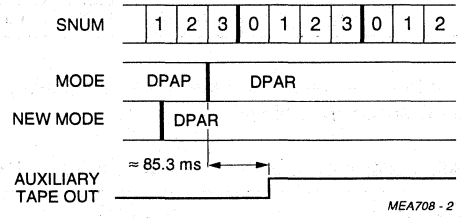


Fig.36 Mode change to DPAR.

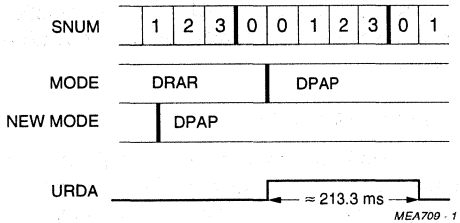


Fig.37 Mode change from DRAR.

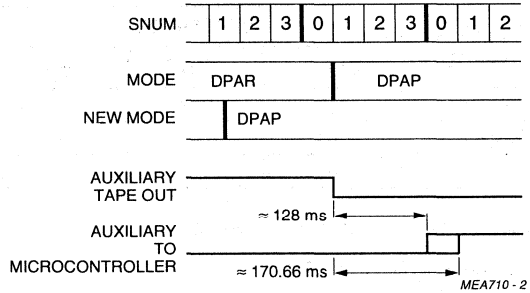


Fig.38 Mode change from DPAR.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		tbf	tbf	V
V_I	input voltage	note 1	−0.5	V_{DD} + 0.5	V
I_I	input current		−10	+10	mA
V_O	output voltage		tbf	tbf	V
I_O	output current		−20	+20	mA
I_{DD}	supply current		−	100	mA
I_{SS}	supply current		−100	−	mA
P_{tot}	total power dissipation		−	500	mW
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{es1}	electrostatic handling	note 2	−2000	+2000	V
V_{es2}	electrostatic handling	note 3	−200	+200	V

Notes

1. The input voltage must not exceed maximum supply voltage unless otherwise specified.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

DC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DD}	supply current	digital plus analog; see Fig.39	−	52	−	mA
		inputs with internal pull-down to V_{SS}; all other inputs to V_{SS} or V_{DD}	−	−	100	µA
Inputs CLK24, L3CLK, L3MODE, PINI, SLEEP and SBMCLK						
V_{IL}	LOW level input voltage		−	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	−	V
I_I	input current	V_I = 0 V to V_{DD}; T_{amb} = 25 °C	−10	−	+10	µA
Inputs TEST0, TEST1 and TEST2						
V_{IL}	LOW level input voltage		−	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	−	V
I_I	input current	$V_I = V_{DD}$; T_{amb} = 25 °C	25	−	400	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input RESET						
V_{tLH}	positive-going threshold		–	–	$0.8V_{DD}$	V
V_{tHL}	negative-going threshold		$0.2V_{DD}$	–	–	V
V_{hys}	hysteresis (V_{tLH} to V_{tHL})		–	$0.3V_{DD}$	–	V
Outputs AZCHK, CHTST1, CHTST2, ERCOSTAT, L3INT, $\overline{\text{L3REF}}$, MCLK, PINO3, RDSYNC, SBDIR, SBEF, URDA, TCLOCK and WDATA						
V_{OH}	HIGH level output voltage	I_O = 1 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = –1 mA	–	–	0.4	V
Outputs A0 to A8, A9/$\overline{\text{CAS}}$, A10/$\overline{\text{RAS}}$, $\overline{\text{OEN}}$ and $\overline{\text{WEN}}$						
V_{OH}	HIGH level output voltage	I_O = 2 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = –2 mA	–	–	0.4	V
Outputs SPEED and PINO2						
V_{OH}	HIGH level output voltage	I_O = 1 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = –1 mA	–	–	0.4	V
I_{OZ}	3-state leakage current	V_I = 0 V to V_{DD}; T_{amb} = 25 °C	–10	–	+10	µA
Inputs/outputs SBCL, SBDA and SBWS						
V_{OH}	HIGH level output voltage	I_O = 1 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = –1 mA	–	–	0.4	V
V_{IL}	LOW level input voltage	outputs in 3-state	–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	outputs in 3-state	$0.7V_{DD}$	–	–	V
I_{OZ}	3-state leakage current	V_I = 0 V to V_{DD}; T_{amb} = 25 °C	–10	–	+10	µA
Inputs/outputs A11 to A16 and L3DATA						
V_{OH}	HIGH level output voltage	I_O = 2 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = –2 mA	–	–	0.4	V
V_{IL}	LOW level input voltage	outputs in 3-state	–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	outputs in 3-state	$0.7V_{DD}$	–	–	V
I_{OZ}	3-state leakage current	V_I = 0 V to V_{DD}; T_{amb} = 25 °C	–10	–	+10	µA
Inputs/outputs D0 to D7						
V_{OH}	HIGH level output voltage	I_O = 4 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = –4 mA	–	–	0.4	V
V_{IL}	LOW level input voltage	outputs in 3-state	–	–	0.8	V
V_{IH}	HIGH level input voltage	outputs in 3-state	2	–	–	V
I_{OZ}	3-state leakage current	V_I = 0 V to V_{DD}; T_{amb} = 25 °C	–10	–	+10	µA

Average current consumption

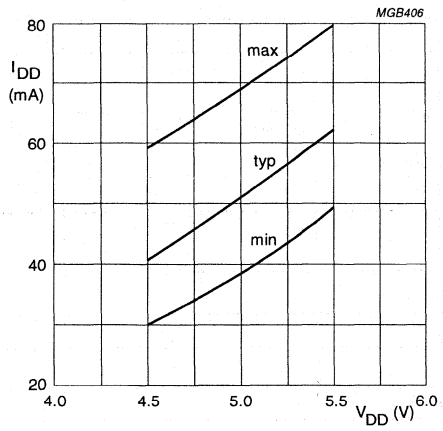


Fig.39 Average current consumption.

AC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = −40 to +85 °C; C_L = 10 pF on all outputs; see Fig.40; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock inputs						
C_I	input capacitance		–	–	10	pF
CLK24						
f_{CLK24}	clock frequency		24	24.576	25	MHz
t_{24L}	pulse width LOW		12	–	–	ns
t_{24H}	pulse width HIGH		12	–	–	ns
SBMCLK						
f_{SBMCLK}	clock frequency			6.144	12.5	MHz
t_{SCL}	pulse width LOW		30	–	–	ns
t_{SCH}	pulse width HIGH		30	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock output MCLK						
C_L	load capacitance		–	–	20	pF
t_d	delay time from SLEEP HIGH to SLEEP active		–	20	–	ns
f_{MCLK}	clock frequency			6.144	6.25	MHz
t_{MCL}	MCLK pulse width LOW		50	–	–	ns
t_{MCH}	MCLK pulse width HIGH		50	–	–	ns
t_{pd}	propagation delay time from rising edge of CLK24		–	–	65	ns
Inputs						
C_I	input capacitance		–	–	10	pF
L3CLK, L3MODE AND RESET						
t_{su}	set-up time to rising edge of MCLK		35	–	–	ns
t_h	hold time from rising edge of MCLK		0	–	–	ns
PINI						
t_{su}	set-up time to rising edge of MCLK		60	–	–	ns
t_h	hold time from rising edge of MCLK		0	–	–	ns
Outputs						
C_L	load capacitance		–	–	20	pF
A0 TO A8						
t_{pd}	propagation delay time from falling edge of CLK24		–	–	50	ns
A9/$\overline{\text{CAS}}$, A10/$\overline{\text{RAS}}$ AND $\overline{\text{OEN}}$						
t_{pd}	propagation delay time from falling edge of CLK24		–	–	50	ns
t_d	delay time from SLEEP HIGH to SLEEP active		–	20	–	ns
$\overline{\text{WEN}}$						
t_{pd}	propagation delay time					
	from falling edge of CLK24		–	–	50	ns
	from falling edge of $\overline{\text{WEN}}$ to rising edge of CLK24	long write pulse mode	–	–	50	ns
t_d	delay time from SLEEP HIGH to SLEEP active		–	20	–	ns
AZCHK, CHTST1, CHTST2, L3INT, PINO3, RDSYNC, SBEF AND WDATA						
t_{pd}	propagation delay time from rising edge of MCLK		–	–	45	ns
ERCOSTAT, $\overline{\text{L3REF}}$, SBDIR, SPEED, PINO2, URDA AND TCLOK						
t_{pd}	propagation delay time from rising edge of MCLK		–	–	55	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs/outputs						
C_I	input capacitance		–	–	10	pF
C_L	load capacitance		–	–	20	pF
A11 TO A16						
t_d	delay time from SLEEP HIGH to SLEEP active		–	25	–	ns
t_{pd}	propagation delay time from falling edge of CLK24		–	–	55	ns
D0 TO D3						
t_d	delay time from SLEEP HIGH to SLEEP active		–	20	–	ns
t_{su}	set-up time to falling edge of CLK24		5	–	–	ns
t_h	hold time from falling edge of CLK24		15	–	–	ns
t_{pd}	propagation delay time					
	from falling edge of CLK24		–	–	50	ns
	from rising edge of CLK24	early write mode	–	–	50	ns
D4 TO D7						
t_d	delay time from SLEEP HIGH to SLEEP active		–	25	–	ns
t_{su}	set-up time to falling edge of CLK24		5	–	–	ns
t_h	hold time from falling edge of CLK24		15	–	–	ns
t_{pd}	propagation delay time					
	from falling edge of CLK24		–	–	50	ns
	from rising edge of CLK24	early write mode	–	–	50	ns
L3DATA						
t_d	delay time from SLEEP HIGH to SLEEP active		–	25	–	ns
t_{su}	set-up time to rising edge of MCLK		35	–	–	ns
t_h	hold time from rising edge of MCLK		0	–	–	ns
t_{pd}	propagation delay time					
	from rising edge of MCLK		–	–	50	ns
	from L3MODE		–	–	45	ns
SBCL AND SBWS						
t_d	delay time from SLEEP HIGH to SLEEP active		–	25	–	ns
t_{su}	set-up time to rising edge of MCLK		40	–	–	ns
t_h	hold time from rising edge of MCLK		0	–	–	ns
t_{pd}	propagation delay time					
	from rising edge of SBMCLK		–	–	60	ns
	from rising edge of MCLK (3-state control)		–	–	55	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SBDA						
t_d	delay time from SLEEP HIGH to SLEEP active		–	25	–	ns
t_{su}	set-up time to rising edge of MCLK		35	–	–	ns
t_h	hold time from rising edge of MCLK		0	–	–	ns
t_{pd}	propagation delay time from rising edge of MCLK		–	–	55	ns

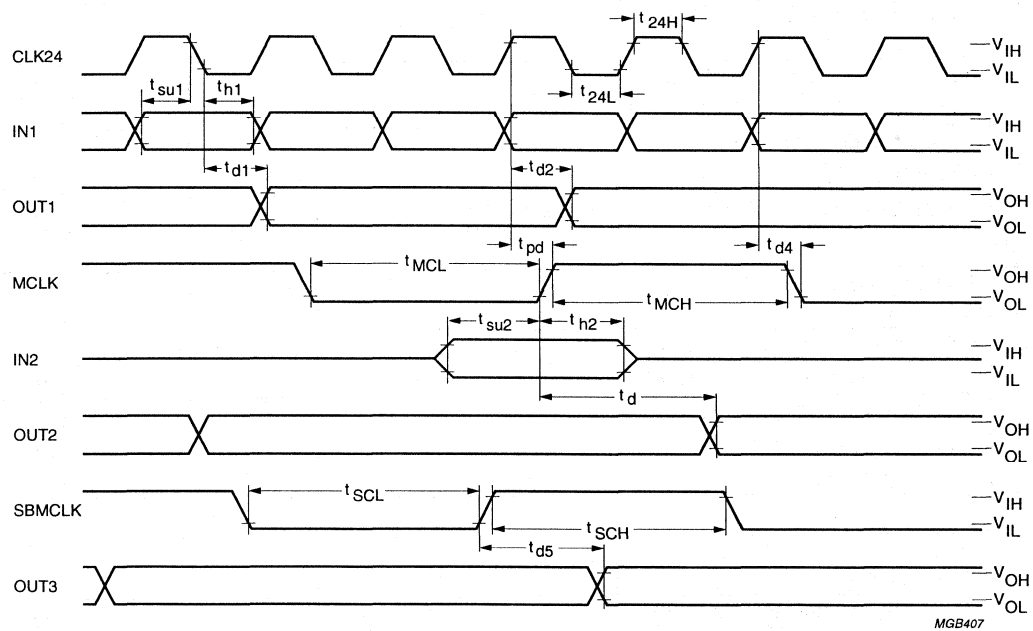


Fig.40 Timing for AC characteristics.

ADC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = −40 to +85 °C; C_L = 10 pF on TCLOCK output; see Fig.41; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	AC RDMUX ADC resolution		–	8	–	bits
$V_{ref(p)}$	positive reference voltage		–	–	V_{DD} − 0.5	V
$V_{ref(n)}$	negative reference voltage		0	–	–	V
ΔV_{ref}	$V_{ref(p)}$ to $V_{ref(n)}$		2.0	–	–	V
Z_i	input impedance	$V_{ref(p)}$ to $V_{ref(n)}$	700	1200	1500	Ω
		$V_{ref(n)}$ to V_{SS}	–	650	–	Ω
C_I	input capacitance (RDMUX)		–	–	15	pF
I_I	input current		–	–	90	μA
DNL	differential non-linearity		–	–	±0.99	LSB
S/(THD+N)	signal-to-total harmonic distortion plus noise ratio	−20 dB (FS); 100 to 500 kHz	24	–	–	dB
Timing						
T_{cy}	cycle time of CLK24		40	–	–	ns
t_{d1}	TCLOCK delay time from rising edge of CLK24	C_L = 10 pF	–	–	80	ns
t_{su}	RDMUX set-up time to falling edge of CLK24	Z_{source} < 150 Ω	60	–	–	ns
t_h	RDMUX hold time from falling edge of CLK24		40	–	–	ns

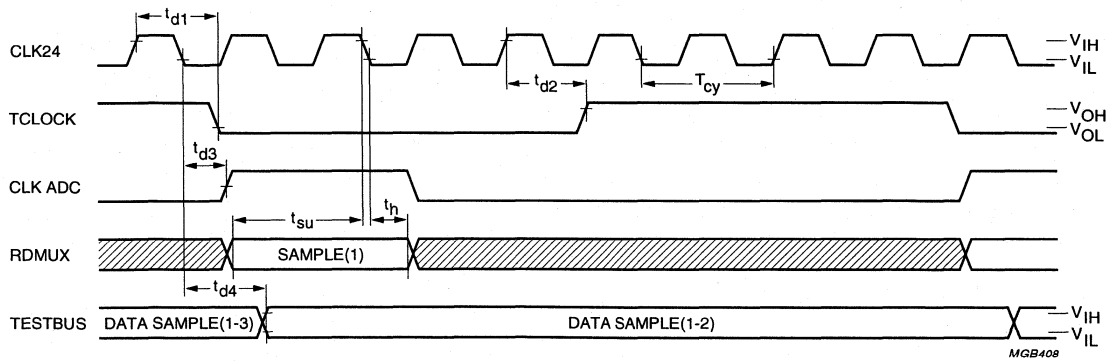


Fig.41 ADC timing.

DAC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	DIGEYE/ANAEYE resolution		–	6	–	bits
V_o	ANAEYE output voltage	Z_L > 1 MΩ	–	(V_{DD} − 1.1) to V_{DD}	–	V

Digital equalization for the tape drive processing of the DCC system

SAA2032

FEATURES

- Analog-to-digital conversion, demultiplexing, equalization and zero crossing of time multiplexed analog read amplifier signal
- Microcontroller interface
- Search mode envelope, label and virgin detection of the AUX channel
- Search mode tape speed measurement
- Simplified external biassing
- Reduced power consumption
- Analog eye output
- 4 V nominal operating voltage capability.

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

Performing the Digital Equalizing function in the Digital Compact Cassette (DCC) system, the SAA2032 is intended for use in conjunction with the SAA2022, read amplifier TDA1317 or TDA1318.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2032GP	44	QFP 1	plastic	SOT205AG

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *Quality Reference Pocketbook* are followed. The pocketbook can be ordered using the code 9398 510 34011.

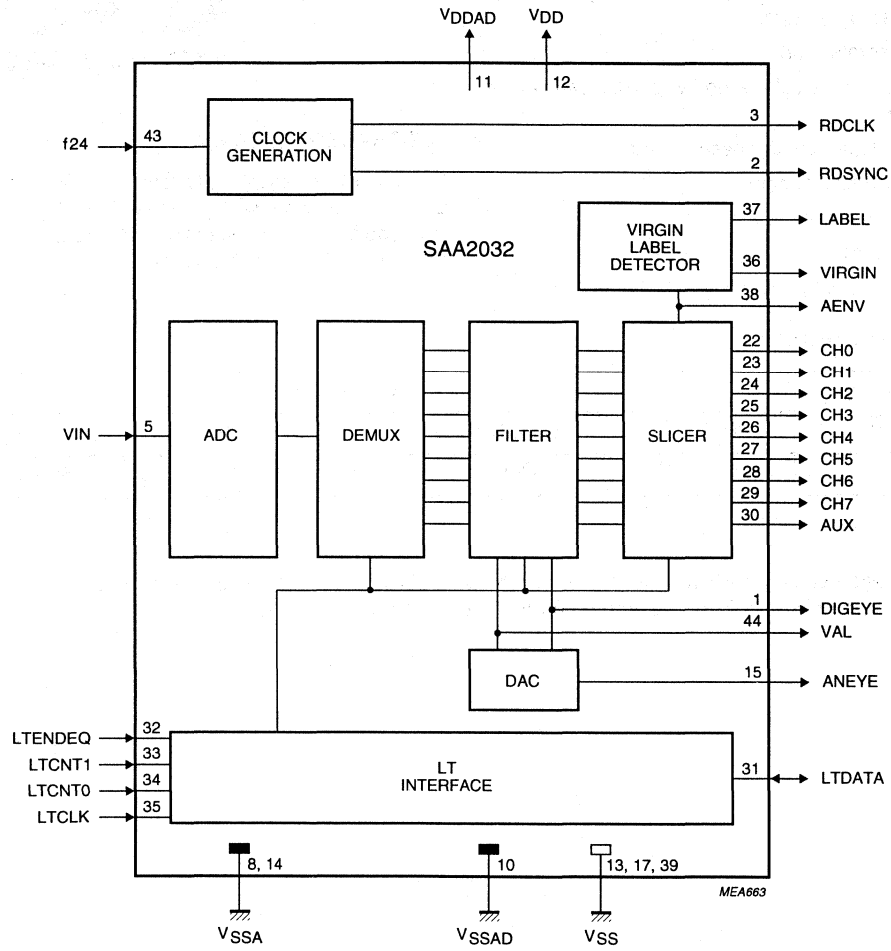


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DIGEYE	1	serial data output for eye pattern
RDSYNC	2	SYNC data for Read Amplifier (push-pull output)
RDCLK	3	data clock for Read Amplifier (push-pull output)
TEST1	4	test 1; to be connected to V_{SS}
VIN	5	analog time multiplexed input from Read Amplifier
REFN	6	lower reference voltage (+1 V) for ADC
REFP	7	upper reference voltage (+3.1 V) for ADC
V_{SSA}	8	analog ground (0 V)
BIASA	9	bias current for ADC (sinks current from V_{DDAD} via 33 kΩ)
V_{SSAD}	10	supply ground (0 V) for ADC
V_{DDAD}	11	supply voltage (+5 V) for ADC
V_{DD}	12	supply voltage (+5 V)
V_{SS}	13	supply ground (0 V)
V_{SSA}	14	supply ground (0 V)
ANEYE	15	analog eye voltage output
n.c.	16	not connected
V_{SS}	17	supply ground (0 V)
TEST4	18	test 4; do not connect
TEST5	19	test 5; do not connect
TEST6	20	test 6; do not connect
TEST7	21	test 7; do not connect
CH0	22	channel 0 output for SAA2022 (DCC Drive Signal Processing) (push-pull output)
CH1	23	channel 1 output for SAA2022 (push-pull output)
CH2	24	channel 2 output for SAA2022 (push-pull output)
CH3	25	channel 3 output for SAA2022 (push-pull output)
CH4	26	channel 4 output for SAA2022 (push-pull output)
CH5	27	channel 5 output for SAA2022 (push-pull output)
CH6	28	channel 6 output for SAA2022 (push-pull output)
CH7	29	channel 7 output for SAA2022 (push-pull output)
AUX	30	AUX channel output for SAA2022 (push-pull output)
LTDATA	31	microcontroller I/O data interface (3-state push-pull output and input; CMOS levels)
LTENDEQ	32	microcontroller interface enabling (CMOS input levels)
LTCNT1	33	microcontroller interface; mode control 1 (CMOS input levels)
LTCNT0	34	microcontroller interface; mode control 0 (CMOS input levels)
LTCLK	35	microcontroller bit-clock interface (CMOS input levels)
VIRGIN	36	search mode virgin detection output
LABEL	37	search mode label detection output
AENV	38	search mode auxiliary detection output
V_{SS}	39	supply ground (0 V)

SYMBOL	PIN	DESCRIPTION
TEST8	40	test 8 input; to be connected to V_{SS}
TEST9	41	test 9 input; to be connected to V_{SS}
TEST10	42	test 10 input; to be connected to V_{SS}
f24	43	clock input; typical frequency 24.576 MHz (CMOS input)
VAL	44	synchronization output for DIGEYE

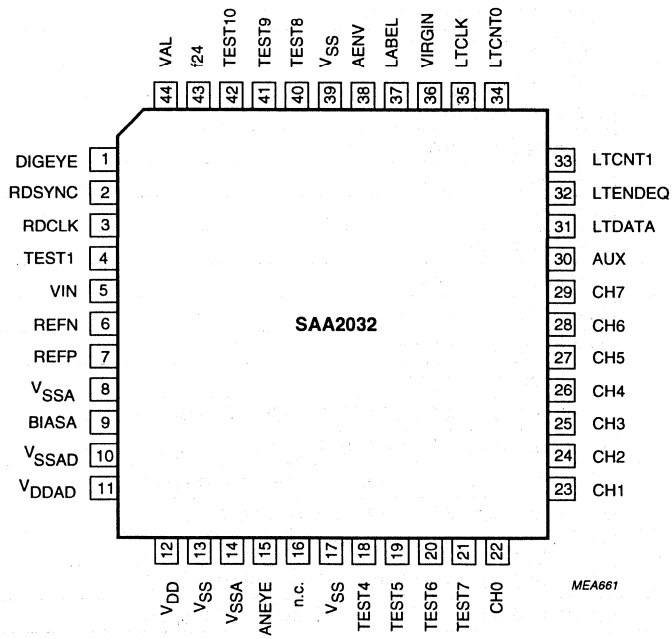


Fig.2 Pin configuration.

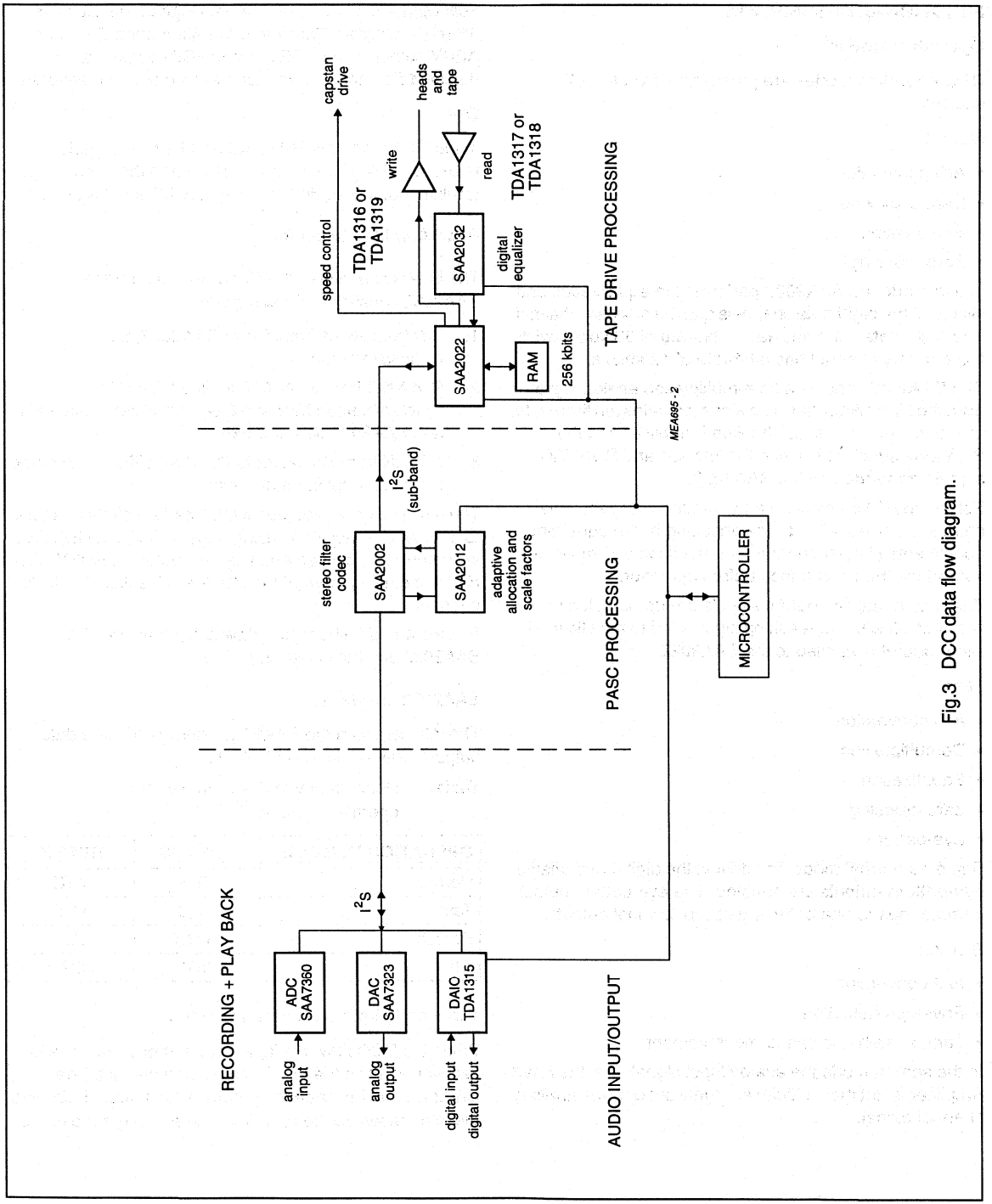


Fig.3 DCC data flow diagram.

FUNCTIONAL DESCRIPTION

Operating Modes

DEQ operating modes are programmed via the LT interface:

NORMAL

- A/D conversion
- Demultiplexing
- Equalization
- Zero crossing.

in this mode the SAA2032 performs the equalization and slicing of the eight data channels and the auxiliary channel. The eight data channels have a bit-rate of 96 kbits/s while the auxiliary channel has a bit-rate of 12 kbits/s.

The SAA2032 input is a time-multiplexed analog signal from the Read Amplifier. The signal contains ten time slots, of which nine are used. The Read Amplifier and the SAA2032 synchronize with the RDCLK and RDSYNC signals generated by the SAA2032.

Following A/D conversion and demultiplexing the nine channels are equalized. The encoding of the equalizing coefficients (12 per channel) are not fixed and must be loaded via the LT interface before operation.

The nine equalized output signals are up-sampled by a factor of 10 with the resulting signals fed to the slicer. The slicer output is applied to the SAA2022.

TEST

- A/D conversion
- Demultiplexing
- Equalization
- Zero crossing
- Eye-pattern.

Same as normal mode. In addition the digital and analog eye-pattern outputs are enabled. The eye-pattern output corresponds to one of the equalized channel outputs.

SEARCH

- A/D conversion
- Envelope detection
- Tape search and speed measurement.

In the search mode the analog input signal from the Read Amplifier is not the multiplexed signal but only the auxiliary channel signal.

Following A/D conversion the envelope of this signal is filtered and sliced. This forms the Alternating Envelope AENV output. The LABEL and VIRGIN outputs are detected from this and the tape search speed measured.

OFF

In the OFF mode the RDSYNC and RDCLK signals are HIGH, the EYE outputs are disabled and the channel and auxiliary outputs (CH0 to CH7 and AUX) are 3-stated.

Read Amplifier interface

The interface between the Read Amplifier and the SAA2032 consists of three signals:

1. VIN from Read Amplifier to SAA2032; time multiplexed data.
2. RDSYNC from SAA2032 to Read Amplifier; synchronization between Read Amplifier multiplexer and SAA2032 demultiplexer.
3. RDCLK from SAA2032 to Read Amplifier; data clock for Read Amplifier multiplexer.

The multiplexed VIN output of the Read Amplifier changes to another channel at the rising edge of RDCLK. RDSYNC synchronizes the Read Amplifier VIN output: if RDSYNC is HIGH, the rising edge of the RDCLK will select the AUX channel.

Figures 4 and 5 show the relationship between the SAA2032 and the Read Amplifier.

SAA2022 interface

The interface with the SAA2022 consists of the 9 data output signals CH0 to CH7, AUX.

Table 1 Dependency of Read Amplifier on operational mode.

OPERATIONAL MODE	RDSYNC	RDCLK
Normal	YES	YES
Test	YES	YES
Search	HIGH	YES
Off	HIGH	HIGH

Label and virgin detection interface

When the DCC player is in its search mode, the tape is fast-wound while the head retains tape contact. The SAA2032 can be made to operate in the search mode and the information will be read from the auxiliary tape track.

The following three signals are generated:

1. LABEL: label detection (HIGH if label is detected).
2. VIRGIN: virgin tape detection (HIGH if virgin tape is detected).
3. AENV: alternating envelope (sliced envelope).

AENV, LABEL and VIRGIN are disabled in normal or off modes. LABEL, VIRGIN and AENV are LOW.

AENV, LABEL and VIRGIN are enabled when the SAA2032 is in search mode.

The device detects the envelope AENV of the auxiliary track at search speeds between 3 and 50 times normal speed. If AENV is continuously HIGH (label detection), LABEL will be HIGH.

When AENV is continuously LOW (virgin tape detection) VIRGIN will be HIGH.
Figures 6, 7 and 8 show the relationship between AENV, VIRGIN and LABEL.

Labelled tape-speed calculation

When the DCC player is in its search mode, the tape speed increases. LABEL information is encoded throughout its length. To examine the length of a label, the tape speed must be known. In search mode the SAA2032 assesses the speed of labelled tapes. The microcontroller obtains this information via the LT-interface.

The speed information is encoded in 3 variables:

1. SVF Speed Validation Flag (HIGH if invalid).
2. SC (4..0) Speed counter.
3. SR (1..0) Speed Range.

Search speed = $2^{SR} \times \frac{51.2}{SC}$ x normal speed.

If SC = 0 then search speed > 51.2.

With SR = 0, 1, 2 or 3 and SC = 0 to 31.

If SVF = 1 then SR and SC values are invalid.

Appendix 1 gives a table of the search mode speed control.

Microcontroller (LT) Interface

The SAA2032 is able to exchange information with the microcontroller via the LT-interface. The microcontroller performs as master, the SAA2032 as slave.

Figure 9 gives the operation of the LT-interface.

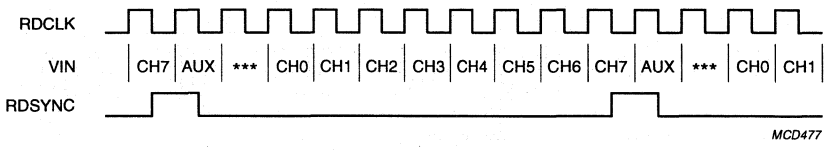
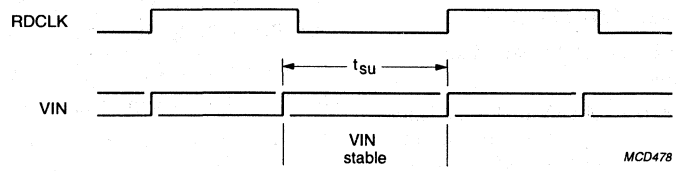
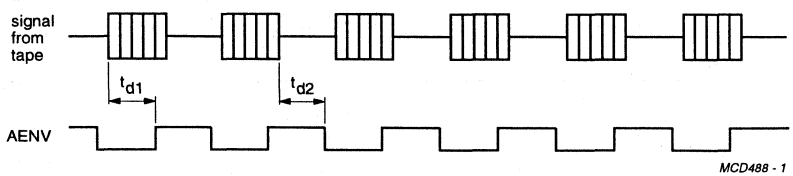


Fig.4 Signals on interface between Read Amplifier and SAA2032.



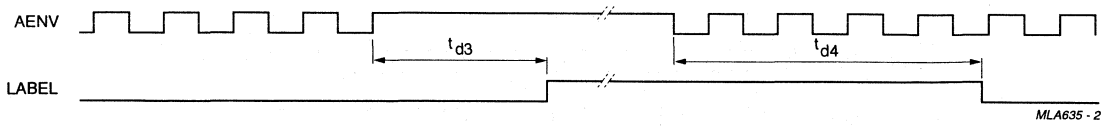
t_{su} > 80 ns; set-up time VIN before RDCLOCK HIGH.
Typical frequency for RDCLK = 3.072 MHz.
Typical frequency for RDSYNC = 307.2 kHz.

Fig.5 Timing.



$t_{d1} = t_{d2}$ = between 0.5 and 1.0 auxiliary block lengths.

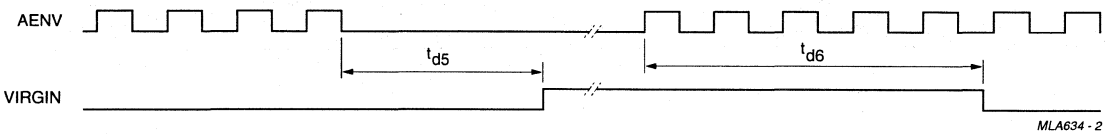
Fig.6 Diagram of AENV signal.



t_{d3} = between 4 and 12 auxiliary blocks.

t_{d4} = between 4 and 12 auxiliary blocks.

Fig.7 AENV and LABEL signals.



t_{d5} = t_{d6} = between 4 and 12 auxiliary blocks.

Fig.8 AENV and VIRGIN signals.

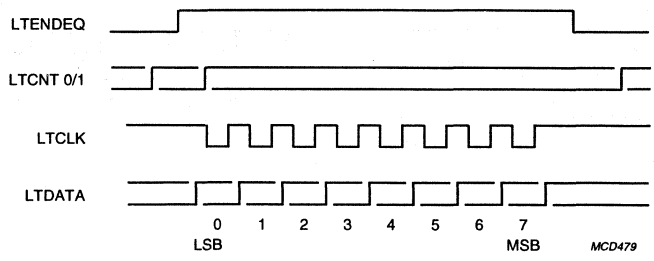


Fig.9 Typical operation of the LT-interface.

LTCNT specification

Table 2 Four types of data exchange performed on the interface.

LTCNT1	LTCNT0	LT DATA EXCHANGE MODE		FROM	TO
0	0	data	write	µC	DEQ
0	1	data	read	DEQ	µC
1	0	address	write	µC	DEQ
1	1	mode settings	write	µC	DEQ

Mode Settings Load (LTCNT = 11) (See Fig.10)

The 8-bits transmitted under 'mode settings load' control both the 'operation mode' and the 'data exchange type'.

Table 3 Mode settings; 'operation mode'.

a1	a0	OPERATION MODE
0	0	normal
0	1	test
1	0	search
1	1	off

Table 4 Mode settings; 'data exchange type'.

b1	b0	DATA	EXCHANGE	TYPE
0	0	write	coefficient	data
0	1	read	coefficient	data
1	1	read	envelope	data

Remark post condition: after every communication sequence the data exchange type must be set to "read coefficient data".

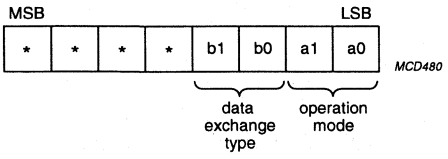


Fig.10 Mode settings load (LTCNT = 11).

Address Information Load (LTCNT = 10) (See Fig.11)

A channel/tap combination can be selected through this type of data exchange.

Co-efficient Data Load (LTCNT = 00) (See Fig.12)

This type of data exchange will overwrite the equalizer tap coefficient of the **current selected** channel/tap combination.

The coefficient data for tap <0000> of the auxiliary channel should always be zero.

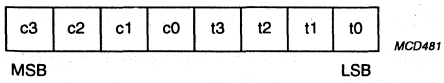
Data Read (LTCNT = 01) (See Fig.13)

This type of data exchange will send information from the LTDATA register in the SAA2032 to the microcontroller. Data in the LTDATA register depends upon the current data exchange type.

LTDATA interpretation:

- coefficient data: two's complement coefficient data
- tape speed data
  - d7 = SVF flag
  - d6 to d2 = SC4 to SC0
  - d1, d0 = SR1, SR0.

Tape speed data format is shown in Fig.14.



c3 to c0 --> channel number <0000 to 0111>
+ auxiliary channel <1000>
t3 to t0 --> tap number <0000 .. 1011>

Fig.11 Address information load (LTCNT = 10).

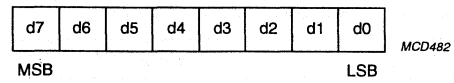


Fig.12 Coefficient data load (LTCNT = 00).

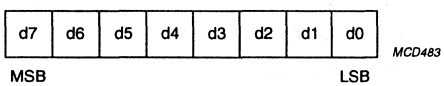


Fig.13 Read data (LTCNT = 01).

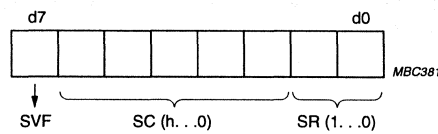
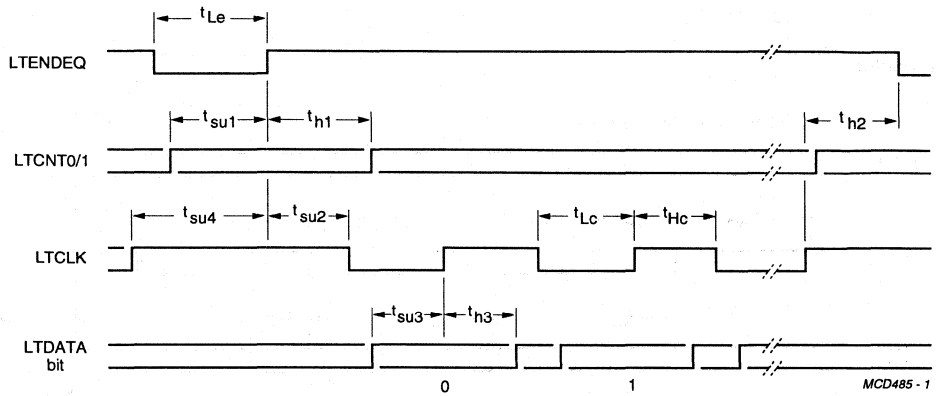


Fig.14 Tape speed data format.



t_{Le} > 120 ns; minimum LOW time LTENDEQ before transfer.

t_{su1} > 20 ns; set-up time LTCNT0/1 before LTENDEQ HIGH.

t_{h1} > 100 ns; hold time LTCNT0/1 after LTENDEQ HIGH.

$t_{su2} \geq 0$ ns; set-up time LTCNT0/1 before LTCLK LOW.

t_{h2} > 20 ns; hold time LTENDEQ after LTCLK HIGH.

t_{Lc} > 120 ns; minimum LOW time LTCLK.

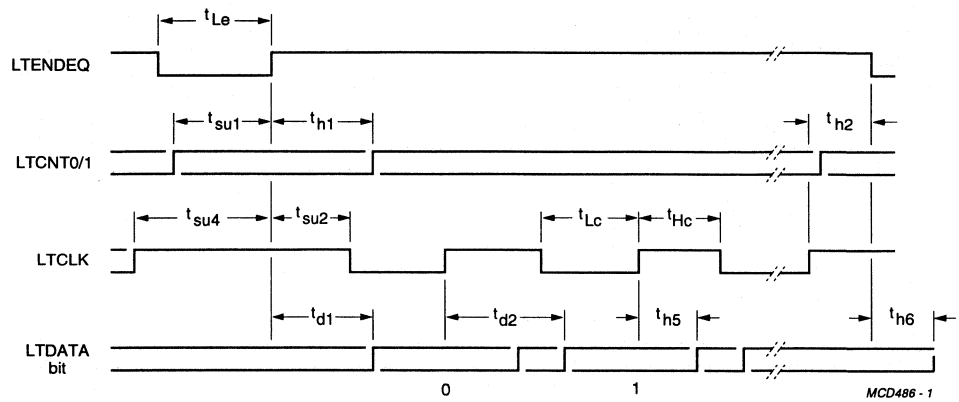
t_{Hc} > 120 ns; minimum HIGH time LTCLK.

t_{su4} > 200 ns; set-up time LTCLK before LTENDEQ HIGH.

t_{su3} > 100 ns; set-up time LTDATA before LTCLK HIGH.

t_{h3} > 20 ns; hold time LTDATA after LTCLK HIGH.

Fig.15 Microcontroller to SAA2032 timing.



t_{Le} > 120 ns; minimum LOW time LTENDEQ before transfer.

t_{su1} > 20 ns; set-up time LTCNT0/1 before LTENDEQ HIGH.

t_{h1} > 100 ns; hold time LTCNT0/1 after LTENDEQ HIGH.

$t_{su2} \geq 0$ ns; set-up time LTCNT0/1 before LTCLK LOW.

t_{h2} > 20 ns; hold time LTENDEQ after LTCLK HIGH.

t_{Lc} > 120 ns; minimum LOW time LTCLK.

t_{Hc} > 120 ns; minimum HIGH time LTCLK.

t_{su4} > 200 ns; set-up time LTCLK before LTENDEQ HIGH.

t_{d1} > 300 ns; maximum delay LTDATA after LTENDEQ HIGH.

t_{d2} > 400 ns; maximum delay LTDATA after LTCLK HIGH.

t_{h5} > 160 ns; hold time LTDATA after LTCLK HIGH.

t_{h6} > 0 ns; hold time LTDA after LTENDEQ LOW.

Fig.16 SAA2032 to Microcontroller timing.

Eye pattern output

To test equalization performance it is possible to output the equalized channels. For this purpose one analog and two digital output signals are provided. Selection of the EYE pattern output is determined by the last channel address sent to the SAA2032.

- DIGEYE: serial data line for 8-bits output value
- VAL: validation signal for data bits
- ANEYE: analog eye voltage output.

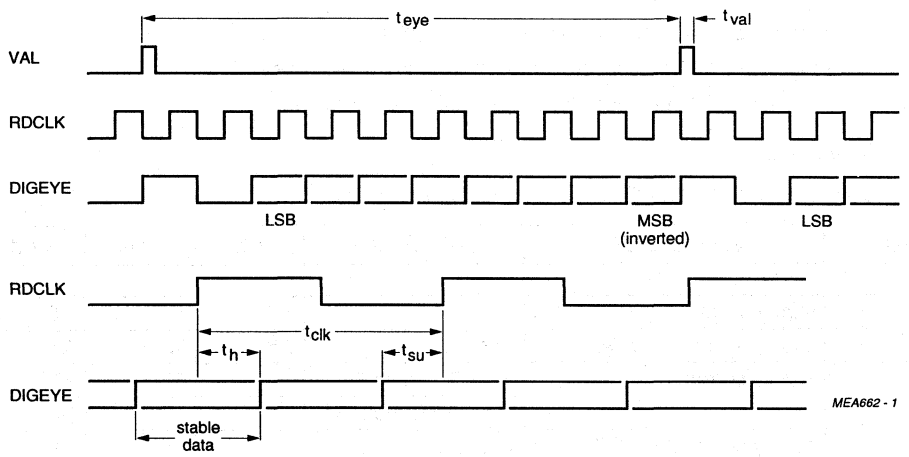
The eye outputs are enabled in test mode.

Table 5 Eye outputs.

OPERATION MODE	DIGEYE	ANEYE
Normal	LOW	HIGH
Test	ENABLED	ENABLED
Search	LOW	HIGH
Off	LOW	HIGH

The internal number representation in the SAA2032 is in two's complement. The format of the selected 8-bits will be converted to the off-set-binary format. This means that the MSB of the two's complement number has been inverted. This 8-bit number is shifted out via the DIGEYE output.

Figure 17 gives the eye pattern output timing.



t_{val} = 1/4 clock period; pulse width HIGH.

t_{su} > 60 ns; minimum set-up time data before clock.

t_h > 5 ns; minimum hold time data after clock.

$t_{clk} = 1/f_{clk}$.

f_{clk} = 3.072 MHz; nominal DIGEYE clock frequency.

$t_{eye} = 1/f_{eye}$.

f_{eye} = 307.2 kHz; nominal DIGEYE clock frequency.

Fig.17 Timing diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+6.5	V
V_I	input voltage	note 1	−0.5	V_{DD} + 0.5	V
I_{SS}	supply current in V_{SS}		−	−100	mA
I_{DD}	supply current in V_{DD}		−	100	mA
I_I	input current		−10	10	mA
I_O	output current		−20	20	mA
P_{tot}	total power dissipation		−	550	mW
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{es1}	electrostatic handling	note 2	−1500	+1500	V
V_{es2}	electrostatic handling	note 3	−70	+70	V

Notes

1. Input voltage should not exceed 6.5 V unless otherwise specified.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

DC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		3.8	5.0	5.5	V
V_{DDAD}	supply voltage for ADC	note 1	3.8	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V; note 2	−	22	26	mA
		V_{DD} = 3.8 V; note 2	−	12	14	mA
I_{DDAD}	supply current for ADC	V_{DDAD} = 5 V	−	11	13	mA
		V_{DDAD} = 3.8 V	−	5	7	mA
I_{OP}	operating current	note 3	1.3	1.9	3.4	mA
Inputs f24, LTCLK, LTCNT0, LTCNT1 and LTENDEQ						
V_{IL}	LOW level input voltage		0	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD}	V
I_I	input current	V_I = 0 V; T_{amb} = 25 °C	−	−	−10	µA
		V_I = V_{DD}; T_{amb} = 25 °C	−	−	10	µA
Input REFP						
V_{refp}	reference voltage		2.7	3.1	3.4	V
Input REFN						
V_{refn}	reference voltage		0.7	1.0	1.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs REFP and REFN						
ΔV_{ref}	reference voltage difference between REFP and REFN		2	2.1	2.7	V
Input VIN						
$V_{I(p-p)}$	input voltage (peak-to-peak)		V_{refn}	–	V_{refp}	V
I_I	input current		–	–	100	μA
Digital outputs						
V_{OL}	LOW level output voltage	note 4	–	–	0.4	V
V_{OH}	HIGH level output voltage	note 4	$V_{DD} - 0.5$	–	–	V
Output ANEYE						
V_O	output voltage	note 4	–	–	V_{DDAD}	V
V_O	output voltage range	note 4	–	1.1	–	V
Input/output LTDATA						
V_{OL}	LOW level output voltage	$I_O = -3$ mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	$I_O = 2$ mA	$V_{DD} - 0.5$	–	–	V
I_{OZ}	leakage current with outputs in 3-state	$V_I = 0$ V; $T_{amb} = 25$ °C	–	–	10	μA
		$V_I = V_{DD}$; $T_{amb} = 25$ °C	–	–	10	μA
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V

Notes

1. V_{DDAD} should never be lower than $V_{DD} - 0.2$ V.
2. For load impedances in a typical application circuit.
3. Operating reference current for the specified range of V_{refp} allowing for the tolerance on the internal resistor.
4. For outputs DIGEYE, RDSYNC, RDCLK, CH0 to CH7, AUX and VAL the maximum load current is 1 mA. For ANEYE output the maximum load current is 10 μA. For VIRGIN, LABEL and AENV the maximum load current is 2 mA.

AC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = −40 to 85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIN						
C_i	input capacitance		–	–	15	pF
All digital inputs						
C_i	input capacitance		–	–	10	pF
Clock input f24						
f	clock frequency		23	24.576	26	MHz
t_p	pulse width LOW or HIGH		10	–	–	ns
Inputs LTCLK, LTENDEQ, LTCNT0 and LTCNT1						
t_{su}	set-up time to f24	note 1	10	–	–	ns
t_h	hold time from f24	note 1	30	–	–	ns
All outputs						
C_i	input capacitance		–	–	10	pF
C_L	load capacitance		–	–	50	pF
t_d	propagation delay time from f24	note 1	–	–	80	ns
Input/output LTDATA						
C_i	input capacitance		–	–	10	pF
C_L	load capacitance		–	–	50	pF
t_d	propagation delay time from f24		–	–	80	ns
t_{su}	set-up time to f24	note 1	10	–	–	ns
t_h	hold time from f24	note 1	30	–	–	ns

Note

1. LOW-to-HIGH transition.

CONVERTER CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = −40 to 85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-Digital Converter; VIN						
	resolution		–	7	–	bits
	conversation data available after		–	$2 \times t_{cy}$	–	
	effective input bandwidth	6-bit resolution at f_s = 3.1 MHz	0.5	–	–	MHz
	differential non-linearity		–	–	±0.99	LSB
V_{refn}	reference voltage at VREFN	note 1	0.7	1.0	1.4	V
V_{refp}	reference voltage at VREFP		2.7	3.1	3.4	V
ΔV_{ref}	reference voltage difference between REFP and REFN		2	2.1	2.7	V
V_i	input voltage		V_{refn}	–	V_{refp}	V
S+THD/N	signal-to-total harmonic distortion and noise ratio	note 2	21	–	–	dB
C_i	input capacitance		–	–	15	pF
I_I	input current (DC)	note 3	–	–	100	µA
Digital-to-analog converter; output ANEYE						
	resolution		–	6	–	bits
V_O	output voltage	note 4	–	–	V_{DDAD}	V
V_O	output voltage range	note 4	–	1.1	–	V

Notes

1. V_{refp} is supplied externally.
   V_{refn} is derived internally and set to $^1/_3 V_{refp}$.
   V_{refn} must be decoupled externally at pin 6 via a 100 nF capacitor.
2. Signal level (f_s) −20 dB, at any DC level within the input voltage range.
3. The output impedance of the analog input signal source must be <150 Ω.
4. Load impedance ≥1 MΩ.

APPENDIX 1

Search Mode Speed Control Interface

In search mode the SAA2032 measures the tape speed. The tape speed is encapsulated in the variables:

- SVF Speed Validation Flag; is HIGH if NOT valid
- SC Speed Counter
- SR Speed Range.

The values in Table 6 represent the speed in multiples of the nominal tape speed of 4.76 cm/s.

Table 6 Speed in multiples of nominal tape speed.

SC[4 .. 0]	SR[1 .. 0]				REMARKS
	0	1	2	3	
0	>51.20	>102.40	>204.80	>409.60	shift to higher speed range
1	51.20	102.40	204.80	409.60	
2	25.60	51.20	102.40	204.80	
3	17.07	34.13	68.27	136.53	
4	12.80	25.60	51.20	102.40	
5	10.24	20.48	40.96	81.92	
6	8.53	17.07	34.13	68.27	
7	7.31	14.63	29.26	58.51	
8	6.40	12.80	25.60	51.20	normal working area
9	5.69	11.38	22.76	45.51	
10	5.12	10.24	20.48	40.96	
11	4.65	9.31	18.62	37.24	
12	4.27	8.53	17.07	34.13	
13	3.94	7.88	15.75	31.51	
14	3.66	7.31	14.63	29.26	
15	3.41	6.83	13.65	27.31	
16	3.20	6.40	12.80	25.60	
17	3.01	6.02	12.05	24.09	

SC[4 .. 0]	SR[1 .. 0]				REMARKS
	0	1	2	3	
18	2.84	5.69	11.38	22.76	shift to lower speed range
19	2.69	5.39	10.78	21.56	
20	2.56	5.12	10.24	20.48	
21	2.44	4.88	9.75	19.50	
22	2.33	4.65	9.31	18.62	
23	2.23	4.45	8.90	17.81	
24	2.13	4.27	8.53	17.07	
25	2.05	4.10	8.19	16.38	
26	1.97	3.94	7.88	15.75	
27	1.90	3.79	7.59	15.17	
28	1.83	3.66	7.31	14.63	
29	1.77	3.53	7.06	14.12	
30	1.71	4.41	6.83	13.65	
31	1.65	3.30	6.61	13.21	

MPEG Audio Source Decoder SAA2500

FEATURES

- Advanced error protection
- Integrated audio post processing for control of signal level and inter-channel crosstalk
- Demultiplexing of ancillary data in the input bitstream
- Automatic digital de-emphasis of the decoded audio signal
- Separate master and slave inputs
- Automatic sample frequency and bit-rate switching in master input mode
- Automatic synchronization of input and output interface clocks in master input mode
- Selectable audio output precision; 16, 18, 20 or 22 bit
- Low power consumption.

APPLICATIONS

- Cable and satellite digital radio decoders
- Video CD
- Compact Disc Interactive (CD-I)
- Sold-state audio
- Multimedia Personal Computer (PC).

GENERAL DESCRIPTION

The SAA2500 supports all audio modes (joint stereo, stereo, single channel and dual channel) bit rates and sample frequencies of ISO/MPEG-1 layers I and II, as standardized in *"ISO/IEC 11172-3"*.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA2500H	QFP44[1]	Plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Pocketbook"* (order number 9398 510 34011) are followed.

Supply of this *"ISO/IEC 11172-3"* audio standard Layer I or layer II compatible IC does not convey a licence nor imply a right under any patent, or any Industrial or Intellectual Property Right, to use this IC in any ready-to-use electronic product.

BLOCK DIAGRAM

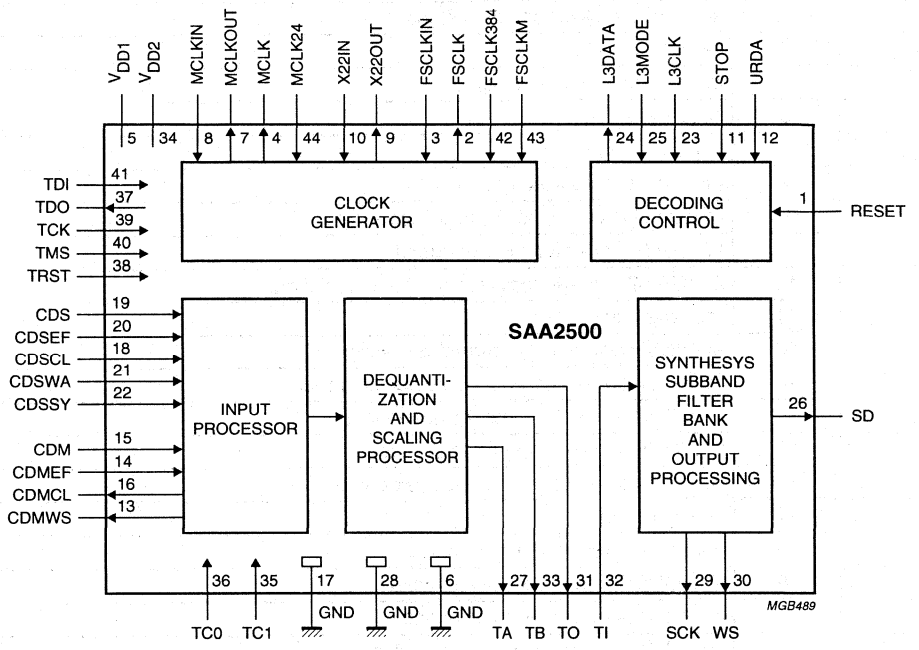


Fig.1 Functional block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
RESET	1	master reset	I
FSCLK	2	sample rate clock; buffered signal	O
FSCLKIN	3	sample rate clock input	I
MCLK	4	master clock; buffered signal	O
V_{DD1}	5	supply voltage	–
GND	6	supply ground	–
MCLKOUT	7	master clock oscillator output	O
MCLKIN	8	master clock oscillator input or signal input	I
X22OUT	9	22.579 MHz clock oscillator output	O
X22IN	10	22.579 MHz clock oscillator input or signal input	I
STOP	11	stop decoding	I
URDA	12	unreliable data input; interrupt decoding	I
CDMWS	13	coded data (master input) word select output	O
CDMEF	14	coded data (master input) error flag input	I
CDM	15	ISO/MPEG coded data (master input)	I
CDMCL	16	coded data (master input) bit clock output	O
GND	17	supply ground	–
CDSCL	18	coded data (slave input) bit clock	I
CDS	19	ISO/MPEG coded data (slave input)	I
CDSEF	20	coded data (slave input) error flag	I
CDSWA	21	coded data (slave input) window signal	I
CDSSY	22	coded data (slave input) frame sync	I
L3CLK	23	L3 interface bit clock	I
L3DATA	24	L3 interface serial data	I/O
L3MODE	25	L3 interface address/data select input	I
SD	26	baseband audio I^2S data output	O
TA	27	do not connect; reserved	O
GND	28	supply ground	–
SCK	29	baseband audio data I^2S clock output	O
WS	30	baseband audio data I^2S word select output	O
TO	31	connect to TI (pin 32)	O
TI	32	connect to TO (pin 31)	I
TB	33	do not connect; reserved	O
V_{DD2}	34	supply voltage	–
TC1	35	do not connect; factory test control 1 input, with integrated pull-down resistor	I
TC0	36	do not connect; factory test control 0 input, with integrated pull-down resistor	I
TDO	37	boundary scan test data output	O
TRST	38	boundary scan test reset input; this pin should be connected to ground for normal operation	I
TCK	39	boundary scan test clock input	I

SYMBOL	PIN	DESCRIPTION	TYPE
TMS	40	boundary scan test mode select input	I
TDI	41	boundary scan test data input	I
FSCLK384	42	sample rate clock frequency indication input	I
FSCLKM	43	sample rate clock source selection for the master input	I
MCLK24	44	master clock frequency indication	I

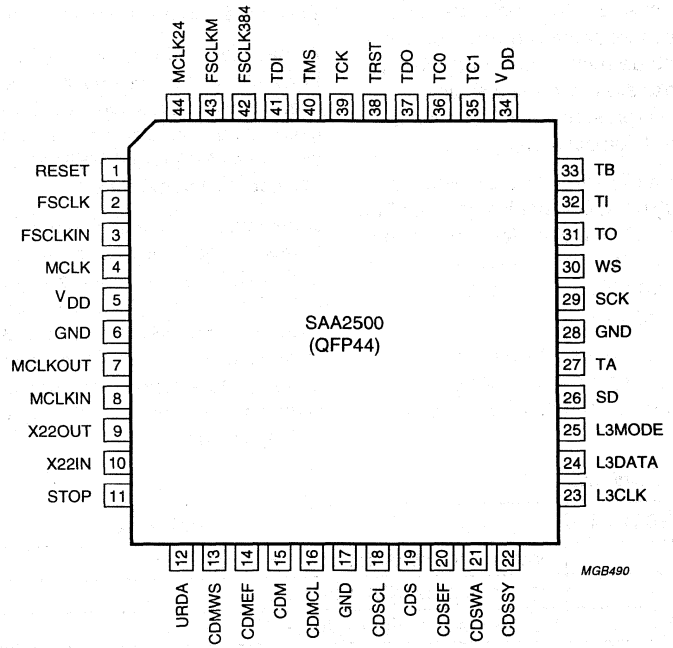


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Coding system

The perceptual audio encoding/decoding scheme defined within the *"ISO/IEC 11172-3 MPEG Standard"* allows for a high reduction in the amount of data needed for digital audio whilst maintaining a high perceived sound quality. The coding is based upon a psycho-acoustic model of the human auditory system. The coding scheme exploits the fact that the human ear does not perceive weak spectral components that are in the proximity (both in time and frequency) of loud components. This phenomenon is called masking.

For layers I and II of ISO/MPEG the broadband audio signal spectrum is split into 32 sub-bands of equal bandwidth. For each sub-band signal a masking threshold is calculated. The sub-band samples are then re-quantized to such an accuracy that the spectral distribution of the re-quantization noise does not exceed the masking threshold. It is this reduction of representation accuracy which yields the data reduction. The re-quantized sub-band signals are multiplexed, together with ancillary information regarding the actual re-quantization, into a MPEG audio bitstream.

During decoding, the SAA2500 de-multiplexes the MPEG audio bitstream, and with knowledge of the ancillary information, reconstructs and combines the sub-band signals into a broadband audio output signal.

Basic functionality

From a functional point of view, several blocks can be distinguished in the SAA2500. A clock generator section derives the internally and externally required clock signals from its clock inputs. The SAA2500 can switch between a master and a slave input interface to receive the coded input data. The input processor parses and de-multiplexes the input data stream. The de-quantization and scaling processor performs the transformation and scaling operations on the sample representations in the input bitstream to yield sub band domain samples.

The sub band samples are transferred via an external detour to the synthesis sub band filter bank processor. The detour can be used to process the decoded audio in the sub band domain. The baseband audio samples, reconstructed by the sub band filter bank, can be processed before being output.

The decoding control block houses the L3 control interface, and handles the response to external control signals. The L3 control interface enables the application to configure the SAA2500, to read its decoding status, to read Ancillary Data, and so on.

Several pins are reserved for Boundary Scan Test and Scan Test purposes.

SAA2500 clocks

The SAA2500 clock interfacing is designed for application versatility. It consists of 10 signals (see Table 1).

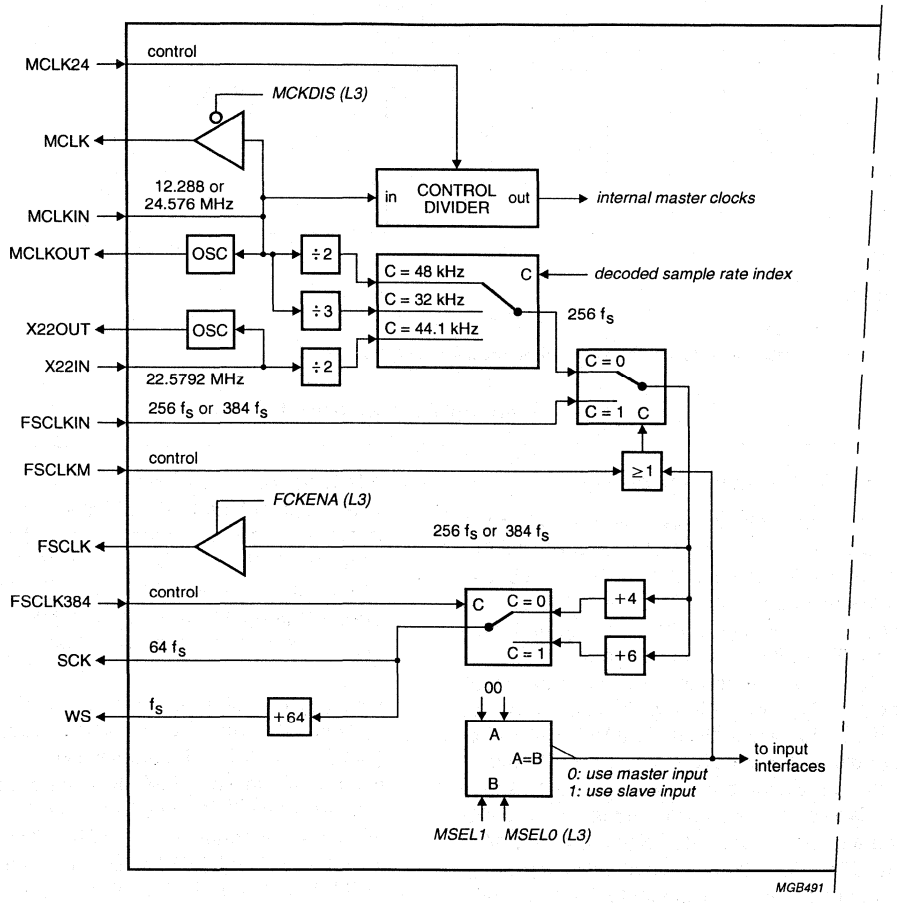
From a functional point of view, the clock generator inside the device can be represented as shown in Fig.3.

As described above, the SAA2500 incorporates a master input interface on which it requests for coded input data itself, as well as a slave input interface for an imposed coded data input bitstream. The input interface is selected with flags MSEL0 and MSEL1, controlled via the L3 microcontroller interface.

Depending on the selected input interface, only a limited number of the three possible input clocks (MCLKIN, X22IN and FSCLKIN) is actually required. The various clock options are selected with the 3 external control signals MCLK24, FSCLKM and FSCLK384. These control signals must be stationary while the device reset signal RESET is de-activated; changing any of these 3 signals without simultaneously resetting the SAA2500 can result in malfunctioning.

Table 1 Clock interfacing signals.

SIGNAL	DIRECTION	FUNCTION
MCLKIN	input	master clock oscillator input or signal input
MCLKOUT	output	master clock oscillator output
MCLK	output	master clock; buffered signal
MCLK24	input	master clock frequency indication: MCLK24 = 0; MCLKIN frequency is 12.288 MHz (256 × 48 kHz) MCLK24 = 1; MCLKIN frequency is 24.576 MHz (512 × 48 kHz)
X22IN	input	22.5792 MHz (512 × 44.1 kHz) clock oscillator input or signal input
X22OUT	output	22.5792 MHz (512 × 44.1 kHz) clock oscillator output
FSCLKIN	input	sample rate clock signal input
FSCLK	output	sample rate clock signal; buffered signal
FSCLK384	input	sample rate clock signal frequency indication: FSCLK384 = 0; FSCLKIN frequency is 256 times the sample rate FSCLK384 = 1; FSCLKIN frequency is 384 times the sample rate
FSCLKM	input	sample rate clock source selection when using the master input: FSCLKM = 0; use MCLKIN or X22IN as source FSCLKM = 1; use FSCLKIN as source

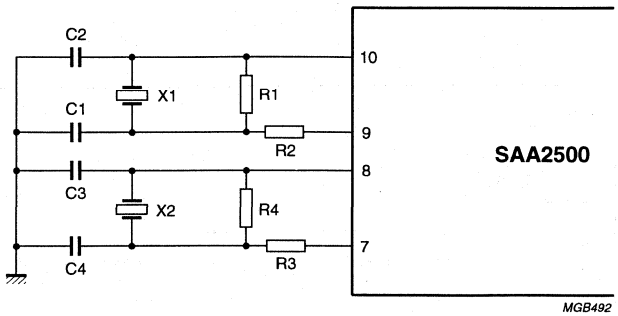


Italics: internal signal designation.

Fig.3 SAA2500 clock generator.

Crystal oscillator

The recommended crystal oscillator configuration is shown in Fig.4. The specified component values only apply to crystals with a low equivalent series resistance of <40 Ω.



C1 =C2 = 33 pF;
R1 = R4 = 1 MΩ;
R2 = R3 = 1 kΩ;
X1 = 22.5792 MHz;
X2 = 24.5760 MHz or 12.2880 MHz

The specified component values only apply to crystals with a low equivalent series resistance of <40 Ω.

Fig.4 Crystal oscillator components.

Clock frequencies when using the slave input

If the slave input is used (MSEL1 and MSEL0 = 10 or 11), the SAA2500 clock sources are MCLKIN and FSCLKIN and X22IN is not used. The I²S clocks SCK and WS are generated by the SAA2500 from FSCLKIN. FSCLKIN may be designated to have a frequency of 256 times (indicated by FSCLK384 = 0) or 384 times (indicated by FSCLK384 = 1) the sample frequency of the coded input data. Master clock signal MCLKIN may be chosen to have a frequency of 12.288 MHz (indicated by MCLK24 = 0) or 24.576 MHz (indicated by MCLK24 = 1). MCLKIN and FSCLKIN do not have to be phase or frequency locked. If the application is based on a sample frequency of 48 kHz or 32 kHz, and a sample rate related clock of 12.288 MHz (256 × 48 kHz; 384 × 32 kHz) is available, this can be taken advantage of by using this signal for both MCLKIN and FSCLKIN.

Clock frequencies when using the master input

If the master input is used (MSEL1 and MSEL0 = 00), one out of two configurations is selected with signal FSCLKM with respect to the clock sources:

1. If FSCLKM = 0, MCLKIN and X22IN are the clock sources. FSCLKIN is not used in this configuration. FSCLK384 must be set to 0 for reasons of internal connections in the clock generator circuitry. MCLKIN may have only frequency 24.576 MHz (so mandatory accompanied by MCLK24 = 1), and X22IN must have a frequency of 22.5792 MHz. MCLKIN and X22IN do not have to be phase or frequency locked. The main advantage of this configuration is that the SAA2500 determines automatically which sample rate is active from the sampling rate setting of the input data bitstream, and then selects either MCLKIN or X22IN as the clock source for the I²S clocks SCK and WS. This configuration is therefore particularly suited in applications with more than one possible sample rate setting.
2. If FSCLKM = 1, the configuration is comparable to the configuration when using the slave input (see Section "Clock frequencies when using the slave input"). MCLKIN and FSCLKIN are used as the clock sources, and X22IN is not required. MCLKIN may again have a frequency of 12.288 MHz (indicated by MCLK24 = 0) or 24.576 MHz (indicated by MCLK24 = 1), and FSCLKIN may have a frequency of 256 times (indicated by FSCLK384 = 0) or 384 times (indicated by FSCLK384 = 1) the sample frequency of the input data. MCLKIN and FSCLKIN do not have to be phase or frequency locked.

Target applications; applying the SAA2500 with 2 ISO/MPEG sources

In Table 2 the three target applications of the SAA2500 are summarised. The slave input application is labelled S, and the master input applications are labelled M0 and M1.

Table 2 Target applications.

ATTRIBUTE CONDITIONS		APPLICATION		
		S	M0	M1
INPUT INTERFACE	CONDITIONS	SLAVE INPUT	MASTER INPUT	MASTER INPUT
FSCLKM		X	0	1
MCLKIN	MCLK24 = 1	24.576 MHz	24.576 MHz	24.576 MHz
	MCLK24 = 0	12.288 MHz	illegal	12.288 MHz
X22IN		note 1	22.579 MHz	note 1
FSCLKIN	FSCLK384 = 1	$384f_s$	illegal	$384f_s$
	FSCLK384 = 0	$256f_s$	note 1	$256f_s$
FSCLK	FCKENA = 1 (L3)	copy of FSCLKIN	$256f_s$	copy of FSCLKIN
Remarks		note 2	note 3	–

Notes

1. Must be electrically defined; e.g.: LOW.
2. FSCLKIN must be locked to input data clock CDSCL; see Section "The coded data slave input interface".
3. FSCLKIN is not used, but FSCLK384 must be LOW.

Sections "Clock frequencies when using the slave input" and "Clock frequencies when using the master input" explain which clock sources are activated by the SAA2500 depending on the selected input interface. This automatic clock source selection makes it easy to apply the SAA2500 in systems with two ISO/MPEG coded data sources (one connected to the master input, an one to the slave input), even if these data sources use different clocks.

Buffered clock outputs

The SAA2500 provides a signal MCLK which is a buffered version of MCLKIN. MCLK can be set to 3-state by setting the L3 control interface flag MCKDIS to 1 in applications where MCLK is not needed.

Signal FSCLK is copied from the FSCLKIN input for application types S and M1 or generated with a frequency of $256f_s$ by the SAA2500 for application type M0. After a device reset, FSCLK must be enabled explicitly by setting L3 flag FCKENA, or can alternatively be left 3-stated in applications where it is not needed.

After a device reset, MCLK is enabled; FSCLK is disabled (i.e. both MCKDIS and FCKENA are set to 0).

Functionality issues

The SAA2500 fully complies with ISO/MPEG layer I and II with the slave input. With the master input, the SAA2500 complies with ISO/MPEG layer I and II, excluding the free format bit rate. Several aspects of the decoding process, as well as the audio post-processing features, offered by the SAA2500, are described in more detail below.

Synchronization to input data bitstreams

After a reset, the SAA2500 mutes both sub band and baseband audio data. After data inputting has started, the SAA2500 searches either for a sync pattern or a sync pulse. The speed at which input data is read by the master input to search for synchronisation is described below. If the application is such that the SAA2500 starts at a random moment in time compared to the bitstream, maximal one frame is skipped before a synchronisation pattern or pulse is encountered.

When the SAA2500 has detected the first synchronisation word or pulse, a number of frames are decoded in order to verify synchronisation; the input data for these frames is read and decoded, but meanwhile the audio output is muted. The number of muted frames depends on whether the ISO/MPEG CRC is active, and whether the bit rate is free format. If the synchronisation is found to be false, the SAA2500 resumes the initial synchronisation as described above. If the detected pulse/pattern is concluded to be a real synchronisation pulse/pattern, Table 3 indicates the number of muted frames.

Table 3 Muted frames.

CRC	MINIMUM NUMBER OF MUTED FRAMES DURING SYNCHRONIZATION	
	FREE FORMAT BIT RATE	NON-FREE-FORMAT BIT RATE
No CRC	2	1
CRC	1	0

Master input bit rate selection

As explained above, the SAA2500 can be used to alternate between two applications: one with the slave input, and one with the master input. When using the master input, the SAA2500 should fetch data with the effective bit rate, but cannot know what the bit rate of the input data is until it has established synchronisation. To overcome this paradox, the input requesting is done at the last selected bit rate.

After a device reset, the master input bit rate selection defaults to the value indicated in Table 4.

Table 4 Defaults master input bit rate.

FSCLKM	FSCLK384	FSCLKIN	DEFAULT MASTER INPUT BIT RATE kbits/s
0	0	X[1]	384
1	0	256 × 32 kHz	278.64
	1	384 × 32 kHz	
	0	256 × 44.1 kHz	384
	1	384 × 44.1 kHz	
	0	256 × 48 kHz	417.96
	1	384 × 48 kHz	

Note

1. X = don't care.

When FSCLKM = 0, the default master input bit rate is 384 kbits/s. When FSCLKM = 1, the SAA2500 uses signal FSCLKIN to derive the selected bit rate, but it has no indication concerning the sample rate corresponding to FSCLKIN. Therefore, a bit rate of 384 kbits/s is selected at an assumed sample rate of 44.1 kHz; with other sample rates, the bit rate changes proportionally.

The consequence is that while the SAA2500 synchronises (e.g. after a device reset), the application must at least be able to supply at the given default bit rate the required number of frames plus one additional frame (because of the random decoding start point in the input bitstream). Buffers in the application must thus be chosen sufficiently large to prevent under or overflows.

The speed with which input data is requested by the master input is changed by the SAA2500 in each of the following cases:

1. When input synchronization is established after checking a number of frames and the bit rate index of the newly decoded bitstream indicates a different bit rate than that currently selected. In this case, the bit rate is adapted to the newly decoded index.
2. When the active input interface is changed from the master to the slave input, or the signal STOP is activated; in these cases input requesting stops.
3. When the active input interface is changed from the slave to the master input, or the signal STOP is deactivated; the bit rate is set to the last selected master input bit rate (the last selected master input bit rate is memorised while using the slave input).

In all other cases (e.g. when the SAA2500 goes and stays out of synchronisation), the data requesting speed of the master input is maintained.

Sample rate selection

When using the slave input, or when using the master input with FSCLKM = 1, the application must know the sample rate: FSCLKIN must be applied, which has a frequency which is a multiple of the sample rate; the (sample rate dependent) I^2S timing signals SCK and WS are generated from FSCLKIN. These configurations will normally be used in applications with a fixed sample rate. Should the sample rate change, then the SAA2500 must be reset.

When using the master input with FSCLKM = 0, the SAA2500 selects the active sample rate autonomously, and generates the signals SCK and WS from its crystal clocks. After a device reset, the SAA2500 selects a sample rate of 44.1 kHz by default.

SCK and WS may, and will only, show phase or frequency changes in any of the following 3 situations:

1. When the SAA2500 establishes synchronization with the coded data input bitstream.
2. When the active input interface is changed from the master input with FSCLKM = 0 to the slave input (i.e. the timing source for the generation of SCK and WS is switched from the crystal clocks to FSCLKIN).
3. When the active input interface is changed from the slave input to the master input with FSCLKM = 0 (i.e. the timing source for the generation of SCK and WS is switched from FSCLKIN to the crystal clocks); the sample rate is set to the last selected sample rate that was used with the master input (the last selected sample rate is memorised while using the slave input).

In all other cases, SCK and WS keep on running without phase or frequency changes, and the sample rate selection remains unchanged.

Handling of errors in the coded input data

The SAA2500 can handle errors in the input data. Errors are assumed to be present in 3 cases:

1. If errors are indicated with the coded input data error flag CDSEF and/or CDMEF.
2. On CRC failure if ISO/MPEG error protection is active.
3. If input bitstream syntax errors are detected.

Errors in the input data have an effect on the decoding process if the corrupted data is inside the header, bit allocation or scale factor select information field in a frame (then the SAA2500 will mute) or inside the scale factor field (then the previous scale factor will be copied). Errors in other data fields are not handled explicitly. If the ISO/MPEG CRC is active, only the CRC result is interpreted: CDSEF/CDMEF un-reliability indications for bit allocation and scale factor select information are neglected.

In applications where the ISO/MPEG CRC is always present, the protection bit (which itself is not protected) in the ISO/MPEG header may be overruled by making L3 settings flag CRCACT HIGH. In this manner, the SAA2500 is made robust for data errors on the protection bit.

Subband filter signals

The decoded subband signals are output, so that they can be processed. The optionally processed subband signals are put back into the SAA2500 for synthesis filtering.

Baseband audio processing

The baseband audio de-emphasis as indicated in the ISO/MPEG input data is performed digitally inside the SAA2500. The incorporated 'Audio Processing Unit' (see Fig.5) can be used to apply inter-channel crosstalk or independent volume control per channel. The APU attenuation coefficients LL, LR, RL and RR may be changed dynamically by the host microcontroller, writing their 8 bit indices to the SAA2500 over the L3 control bus. The coefficient changes become effective within one sample period after the coefficient index writing.

To avoid clicks at coefficient changes, the transition from the current attenuation to the next is smoothed. The relation between the APU coefficient index and the actual coefficient (i.e. the gain) is given in Table 5.

Table 5 APU coefficient index and actual coefficient.

APU COEFFICIENT INDEX C		APU COEFFICIENT
BINARY	DECIMAL	
00000000 to 00111111	0 to 63	$2^{-\frac{C}{12}}$
01000000 to 01111110	64 to 126	$2^{-\frac{(C-32)}{6}}$
01111111	127	0
1XXXXXXX	128 to 255	reserved

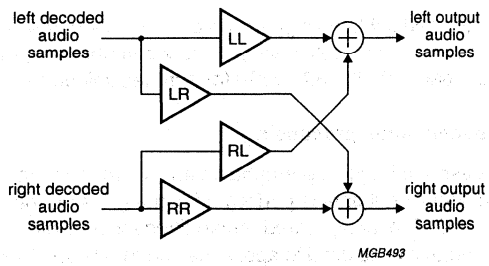


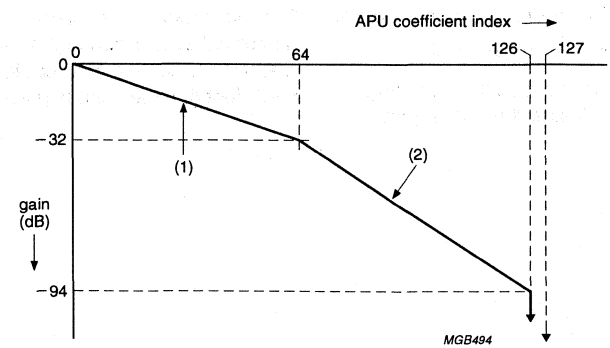
Fig.5 Audio Processing Unit (APU).

From Table 5 we learned that up to coefficient index 64 the step size is approximately –0.5 dB per coefficient increment, and from coefficient index 64 to index 126 the step size is approximately –1 dB per increment.

Note that the APU has no built-in overflow protection, so the application must take care that the output signals of the APU cannot exceed 0 dB level. For an update of the APU coefficients, it may be required to increase some of the coefficients and decrease some others. The APU coefficients are always written sequentially in the fixed sequence LL, LR, RL and RR. Therefore, to prevent internal APU data overflow due to non-simultaneous coefficient updating, the following steps can be followed:

1. Write LL, LR, RL, RR once, but change only those coefficients that must decrease; overwrite the coefficients that must increase with their old value (so do not change these yet).
2. Write LL, LR, RL, RR again, but now change those coefficients that must increase, keeping the other coefficients unchanged.

The consequence of this two-pass coefficient updating is that the application must keep a shadow of the current APU coefficients (the L3 APU coefficients data item is write-only).



(1) Step –0.5 dB per coefficient increment.
(2) Step –1 dB per coefficient increment.

Fig.6 Relation between APU coefficient index and gain.

Decoding control signals

The decoding is performed by 3 signals as shown in Table 6.

Table 6 Signals for decoding control.

SIGNAL	DIRECTION	FUNCTION
RESET	input	reset SAA2500 to default state
STOP	input	stop decoding
URDA	input	unreliable input data; interrupt decoding

The master reset signal RESET forces the SAA2500 into its default state when HIGH. RESET must stay HIGH during at least 24 MCLKIN periods if MCLKIN has frequency 24 MHz (i.e. MCLK24 = 1) or 12 MCLKIN periods if MCLKIN has frequency 12 MHz (MCLK24 = 0). At a reset, the SAA2500 synchronization to the input bitstream is lost, the subband filter and baseband audio output signals are muted, and the SAA2500 settings are initialised.

The decoding can be stopped by making input signal STOP HIGH. Stopping the decoding forces the SAA2500 to end decoding of input data, yet feeding zeroed subband samples to the synthesis subband filter bank to create a soft muting. When using the master input, input requesting is also stopped. CDMWS stays in its current state while STOP is asserted. The SAA2500 assumes the input synchronisation to be lost when the decoding is stopped, thus causing re-synchronization when STOP is de-activated again. Then the SAA2500 mutes, meanwhile searching for a frame sync pattern or frame sync pulse (the synchronisation mode is selected via the L3 control bus) at the input.

If synchronisation is found, the SAA2500 starts producing output data. The maximum response time to the activation of signal STOP is half a sample period; the re-synchronisation time after STOP going LOW again differs in various situations.

An 'unreliable data' indication can be given to the SAA2500 by making signal URDA HIGH. URDA, like STOP, mutes the subband signals and forces the SAA2500 out of synchronisation. However, in contrast to STOP, master input data requesting continues at the bit rate that was decoded before URDA became active. The maximum response time to URDA is half a sample period.

Coded data interfaces

The SAA2500 contains:

- A coded data master input interface
- A coded data slave input interface.

THE CODED DATA MASTER INPUT INTERFACE

When using the master input, the SAA2500 requests for input data. With the master input, the coded input data may not use the ISO/MPEG free format bit rate. The coded data master input interface consists of 4 signals (see Fig.7).

Table 7 Signals of coded data master input interface.

SIGNAL	DIRECTION	FUNCTION
CDM	input	ISO/MPEG coded input data (master input)
CDMEF	input	coded data (master input) error flag
CDMCL	output	coded data (master input) clock
CDMWS	output	coded data (master input) word select

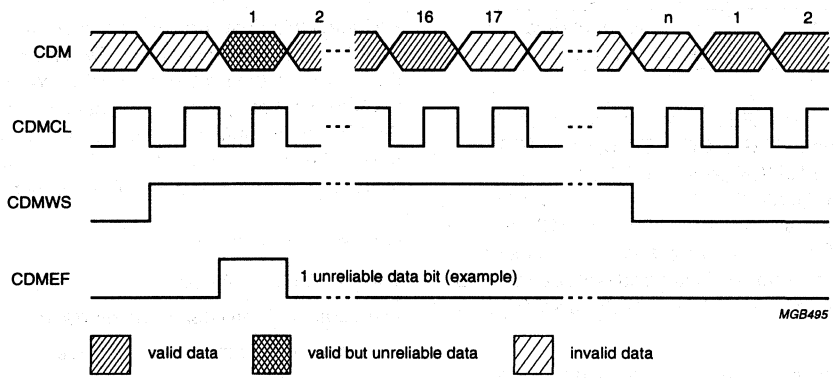


Fig.7 Input data serial transfer format (master input).

Data clock CDMCL is being output, having a fixed frequency of 768 kHz. Signal CDM carries the coded data in bursts of 16 valid bits. Coded data input frames may only start either at the first or at the ninth bit of a 16 bit valid data burst (i.e. only at a byte boundary). The value of word select signal CDMWS is changed every time new input data is needed: one CDMCL period after each transition in CDMWS, 16 bits of valid data are read serially. Assume N is the number of CDMCL periods between two transitions of CDMWS, and R is the number of CDMCL periods to obtain the effective bit rate E (in kbits/s) at a transferring data rate of 768 kbits/s, i.e. R = 16*768/E. The SAA2500 keeps N close to R, but N can vary plus or minus two: $N \in \{round(R)-2,...,round(R)+2\}$.

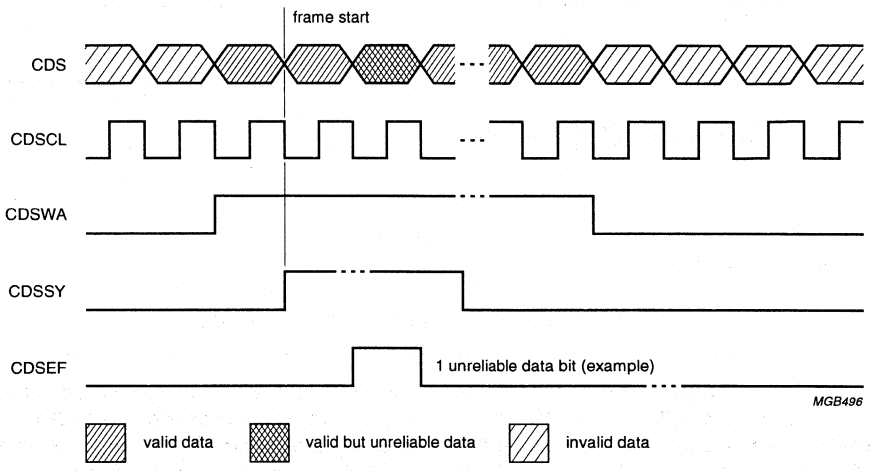
Error flag CDMEF is used to indicate input data insecurities (e.g. due to erratic channel behaviour). In Fig.7, an example with one unreliable bit is shown. The value of CDMEF may vary for each valid data bit, but is combined by the SAA2500 for every group of 8 input bits.

THE CODED DATA SLAVE INPUT INTERFACE

The coded data slave input interface signals are shown in Fig.8. The coded data master input interface consists of 5 signals (see Table 8).

Table 8 Signals of coded data slave input interface.

SIGNAL	DIRECTION	FUNCTION
CDS	input	ISO/MPEG coded input data (slave input)
CDSEF	input	coded data (slave input) error flag
CDSCL	input	coded data (slave input) clock
CDSWA	input	coded data (slave input) burst windowing signal
CDSSY	input	coded data (slave input) frame sync

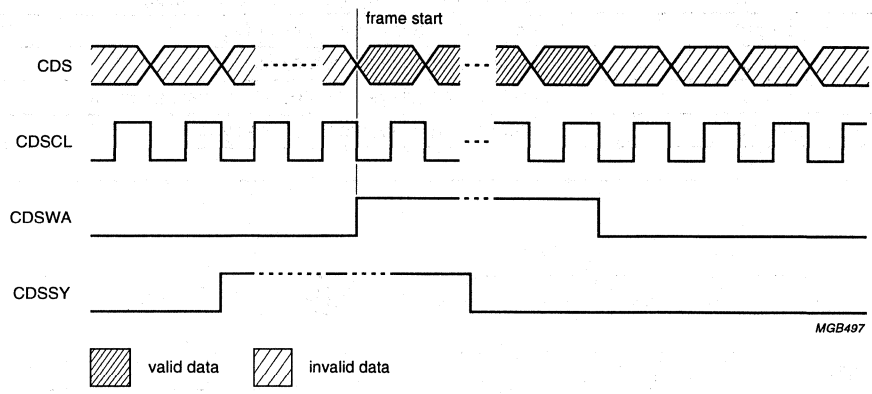


CDSSY indicates frame start during valid data.

Fig.8 Input data serial transfer format (slave input).

CDS is the SAA2500 input data bitstream. Data clock CDSCL must have a frequency equal to or higher than the bit rate. The maximum CDSCL frequency is 768 kHz. Error flag CDSEF is handled in the same way as CDMEF is handled for the master input (in Fig.8, one unreliable data bit is shown as an example). The value of CDSEF is neglected for those bits where CDSWA is LOW. Window signal CDSWA being HIGH indicates valid data; in this way, burst input data is allowed. The constraints for the ability to use 'burst signals' are explained below. Frame sync signal CDSSY indicates the start of each input data frame. CDSSY is synchronous with CDSCL. CDSSY may be present or not: as described below. The first valid CDS bit after a leading edge of CDSSY is interpreted to be the first frame bit.

The minimum time for CDSSY to stay HIGH is one CDSCL period; the maximum HIGH period is constrained by the requirement that CDSSY must be LOW at least during one CDSCL period per frame (a leading edge, i.e. a frame start indication, must be present every frame). Leading edges of CDSSY can occur while CDSWA is HIGH, as in Fig.8. Alternatively, a situation as shown in Fig.9 is also allowed, where CDSSY has a leading edge while CDSWA is LOW, i.e. during invalid data. The first CDS bit after CDSWA going HIGH is now interpreted to be the first frame bit.



CDSSY indicates frame start at next valid data.

Fig.9 Input data serial transfer format (slave input).

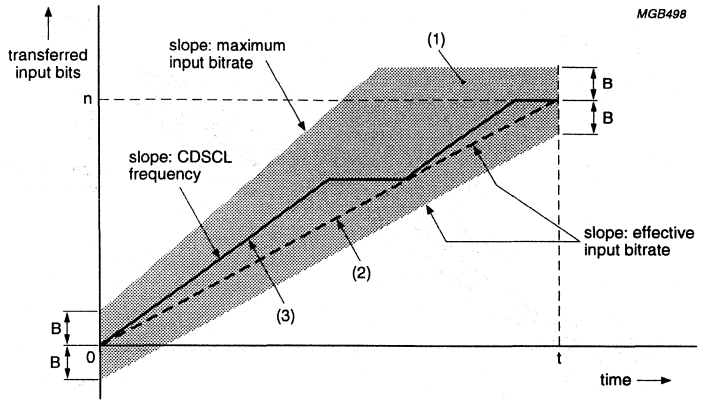
Whether frame sync signal CDSSY is present or not must be selected with L3 settings flags MSEL1 and MSEL0 (see Section "SAA2500 settings item"). With respect to the presence of CDSSY, two situations can be distinguished:

1. If CDSSY is supplied, CDSWA may change each CDSCL period.
2. If CDSSY is not supplied, CDSCL must have a frequency higher than the bit rate (i.e. CDSWA cannot be continuously HIGH), and CDSWA HIGH periods may have only lengths of a multiple of 8 CDSCL periods: data is input in byte bursts. Furthermore, these bursts must be byte aligned with the frame bounds: frames are only allowed to start at the 1st, 9th, 17th etc. bit in a valid data burst. For applications where data is input in bursts of exactly one frame, and where CDSCL has a higher frequency than the bit rate, CDSWA and CDSSY may be interconnected.

SLAVE INPUT TRANSFER SPEED OF FIRST FRAME

Both the average and the instantaneous speed at which data is transferred to the slave input interface are limited. The data transferring of the first ISO/MPEG frame after starting to decode is shown in Fig.10.

It shows the transferring of nf bits in one frame between time 0 and t, where t corresponds to 384 sample periods (ISO/MPEG layer I input data) or 1152 sample periods (ISO/MPEG layer II input data). Buffer margin B equals 16 bytes (128 bits). In Fig.10 an effective transferring characteristic is drawn, representing any of the possible ISO/MPEG bit rates. However, input data may be transferred at a higher-than-effective speed (in other words: CDSCL may have a higher frequency than the effective bit rate) in periods during which CDSWA is HIGH, interleaved with invalid data periods where CDSWA is LOW. In the example of Fig.9 this is used to transfer the data of the frame in two bursts, as shown by the actual transferring characteristic. The actual transferring characteristic has a slope equal to the CDSCL frequency while CDSWA is HIGH, and is horizontal during the periods in which CDSWA is LOW (no bits are being transferred).



(1) The actual transferring characteristics of all frames are restricted to this area.
(2) Effective transferring characteristic (example).
(3) Actual transferring characteristic of the first frame (example).

Fig.10 Slave input data transferring for the first frame.

The shaded area in Fig.10 represents the restrictions to the actual transferring characteristic of all frames. The actual transferring characteristic may not undercut the effective transferring characteristic by more than B bits to avoid an input underflow. On the other hand, the actual transferring characteristic may not cross the shown upper limit of the shaded area to prevent an input buffer overflow. The slope of this upper limit is determined by the maximum effective input bit rate (depending on the input data format). Table 9 summarizes the slopes as determined by the bit rates supported by ISO/MPEG.

Table 9 Slopes determined by bit rates supported by ISO/MPEG.

ISO/MPEG LAYER	EFFECTIVE INPUT BIT RATE (kbits/s)	TRANSFERRING UPPER LIMIT SLOPE (kbits/s)
ISO/MPEG layer I	±13.3[1] to 448	448
ISO/MPEG layer II	3.5[1] to 384	384

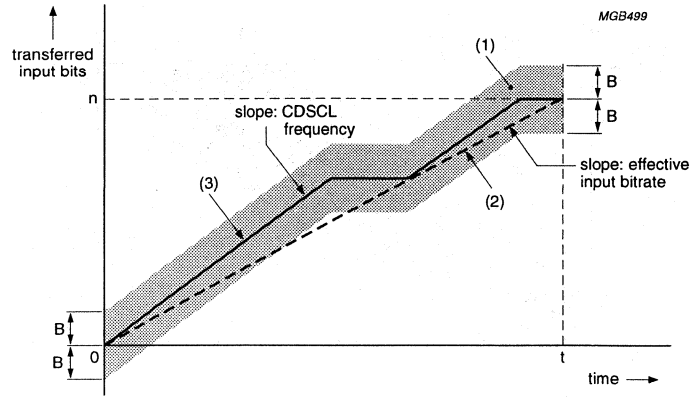
Note

1. Achieved using the free format option and the minimum amount of the side information that must be transmitted (this means using single channel mode, no CRC and 32 kHz sample rate).

SLAVE INPUT TRANSFER SPEED OF SUBSEQUENT FRAMES

The SAA2500 starts decoding as soon as enough data of the first ISO/MPEG input data frame has been received. Thus the start moment of decoding depends on the actual transferring characteristic of the first frame. Decoding start times of subsequent input data frames are also governed by this initial start time.

For this reason the transferring characteristic of all subsequent frames must approximate the characteristic of the first frame within the buffer margin ±B. For the example shown in Fig.10, subsequent frames must be transferred within the shaded area shown in Fig.11.



(1) The actual transferring characteristics of all subsequent frames are restricted to this area.
(2) Effective transferring characteristic (example).
(3) Actual transferring characteristic of the first frame (example).

Fig.11 Slave input data transferring for subsequent frames, referenced to the first frame.

Note that the actual transferring characteristics of all frames must also remain inside the shaded area of Fig.11.

The subband filter interface

As mentioned earlier, decoded signals in the subband domain (before synthesis filtering) are available externally for processing. The associated interface has an I^2S-like format (see Fig.12).

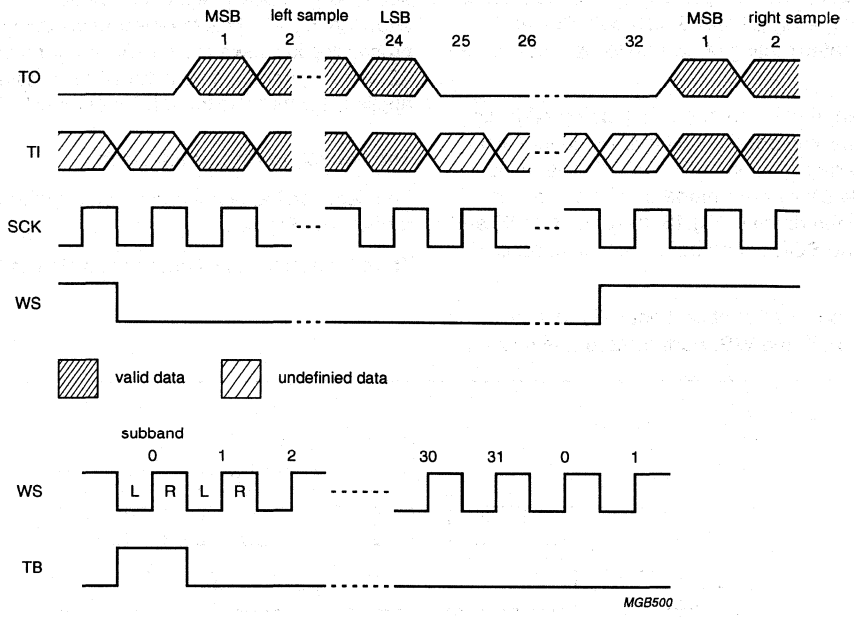


Fig.12 Filter data serial transfer format.

The filter data interface uses 6 signals as shown in Table 10.

Table 10 Signals of filter data interface.

SIGNAL	DIRECTION	FUNCTION
TO	output	filter data output
TA	output	filter data error flag
TI	input	filter data input (optionally processed)
SCK	output	filter data (output/input common) bit clock
WS	output	filter data (output/input common) word select
TB	output	filter data output frame synchronization

Two subband samples (one per channel) are transmitted per sample period with output TO. The transmission pattern of the samples S [sb, ch] (sb: subband index; ch: channel) is: S [0, L], S [0, R], S [1, L], S [1, R],..., S [31, R], S [0, L], S [0, R], etc. Word select signal WS indicates the channel of each sample. (WS is also used for the baseband audio output interfacing).

The subband sample bit clock SCK has a frequency of 64 times the sample frequency. The subband samples are transmitted in 24 bit two's complement PCM form, MSB first. Thus, of the available 32 TO bits per sample per channel, only 24 are used. The MSB of a sample follows one SCK period after each transition in WS. The 8 unused bits between individual samples in TO are zero. (SCK is used for the baseband audio output interface as well.) The optionally processed subband data signal is fed back as input TI in a similar format as TO, but now the 8 unused bits between individual samples are undefined; they are neglected by the SAA2500.

A leading edge in signal TB indicates the start of each TO frame. The length of each TB pulse is one sample period; TB is HIGH during a S[0,L] and S[0,R] pair. Signal TA being HIGH indicates muting of TO due to input data errors (see Fig.13).

TA can only change value at each TB leading edge, i.e. after each 384 sample periods (ISO/MPEG layer I input data) or 1152 sample periods (ISO/MPEG layer II input data): only whole frames are marked to be correct or muted. As shown in detail in Fig.13, transitions of TB and TA take place one SCK period before a trailing edge of WS.

The optionally processed subband data TI must be synchronous to SCK and WS. Furthermore, the subband index of the TI samples must be synchronised to TB: a subband 0 sample pair must be input when TB is HIGH (as shown in Fig.12). This means that the delay of the external processing is allowed to be any integer multiple of 32 sample periods. If no external processing is to be applied, TO must be input back directly to TI.

The baseband output interface

The decoded baseband audio data is output in an I²S-like format (see Fig.14).

The output interfacing consists of 3 signals (see Table 11).

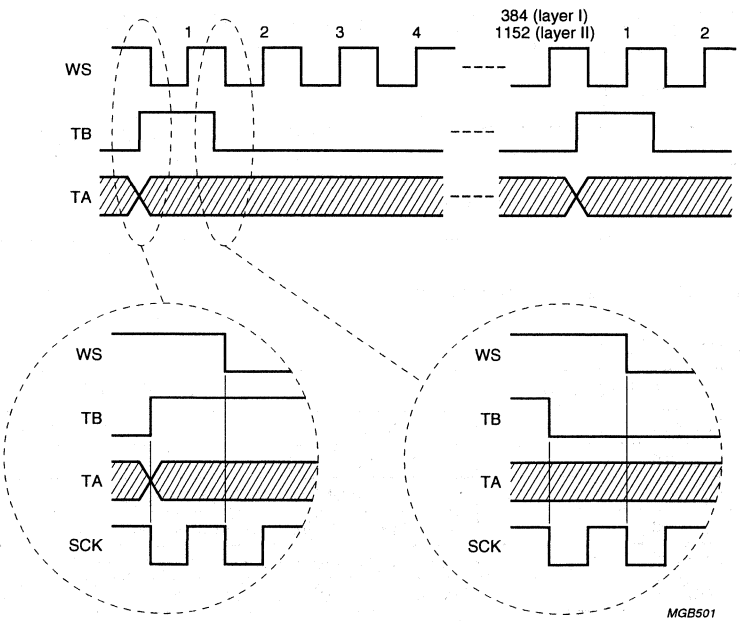


Fig.13 Filter data error flag (TA) timing.

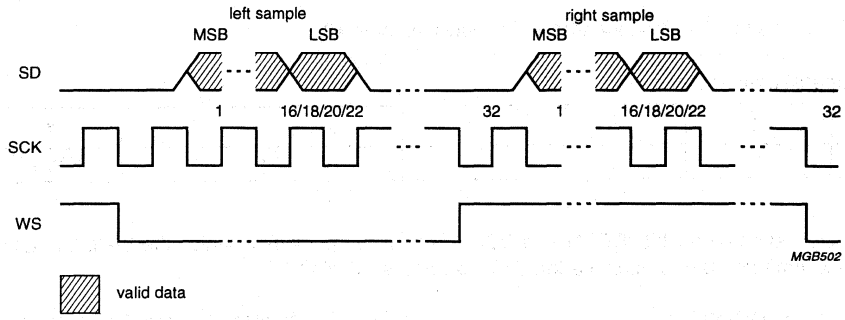


Fig.14 Baseband output data serial transfer format.

Table 11 Signals of output interfacing.

SIGNAL	DIRECTION	FUNCTION
SD	output	baseband audio data
SCK	output	data clock
WS	output	word select

The frequency of clock SCK is 64 times the sample frequency. (SCK is also used for the subband filter interface).

The signal SD is the serial baseband audio data, sample by sample (left/right interleaved. The left sample and the right immediately following it form one stereo pair). 32 bits are transferred per sample per channel. The samples are transmitted in two's complement, MSB first. The output samples are rounded to either 16, 18, 20 or 22 bit precision, selectable by the host with L3 control interface flags RND1 and RND0. The remainder of the 32 transferred bits per sample per channel are zero.

The word select signal WS indicates the channel of the output samples (LOW if left, HIGH if right). (WS is used for the subband filter interface as well.) If indicated in the coded input data, de-emphasis filtering is performed digitally on the output data, thus avoiding the need of analog de-emphasis filter circuitry.

The L3 control interface

The SAA2500 uses the L3 protocol with the associated bus as the control interface with an optional host microcontroller (see Chapter "Appendix" for more information). In the programming sections a general transfer protocol outline is presented. In Section "SAA2500 L3 protocol enhancement options" several optional protocol enhancements are given, which on the one hand are less transparent from the applicant's point of view, but on the other hand increase the efficiency of the L3 interfacing.

L3 SIGNALS

The L3 protocol uses 3 signals (see Table 12).

Table 12 Signals of L3 protocol.

SIGNAL	DIRECTION	FUNCTION
L3DATA	input/output	L3 interface serial data
L3CLK	input	L3 interface bit clock
L3MODE	input	L3 interface address/data select

The signals operate according to the L3 protocol description. After each device reset, the L3 interface of the SAA2500 must be initialised and as a consequence, the L3 interface cannot be used while the device reset signal is activated.

L3 TRANSFER TYPES

The L3 protocol enables the reading and writing of control, status and data. In the L3 protocol, the host first issues an 8 bit wide 'operational address' on L3DATA while keeping L3MODE LOW. All devices connected to the L3 bus read the operational address. Next, data transfers from or to the

host are done while keeping L3MODE HIGH. The devices with an L3 operational address differing from the issued one must ignore these data transfers until the next operational address is issued. Only the device with an address equal to the issued operational address performs the transfer.

The SAA2500 has the L3 operational address as shown in Table 13.

Table 13 L3 operational address.

7	6	5	4	3	2	1	0
0	1	1	0	0	0	DOM1[1]	DOM0[1]

Note

1. The 'Data Operation Mode' bits DOM1 and DOM0 determine the mode in which the SAA2500 L3 interface will stay until the next time an L3 operational address is issued (see Table 14).

Table 14 DOM1 and DOM0 bits.

DOM1	DOM0	TRANSFER TYPE
0	0	write item data
0	1	read item data
1	0	write control to SAA2500
1	1	read SAA2500 status

Control bytes can be written to the SAA2500.

Data is transferred to or from the SAA2500 in so-called data items. The items can be a readable or writeable type. A data item transfer is initiated by writing the corresponding control byte to the SAA2500 first. Next, the item data itself is transferred, always as an integer number of bytes.

The status of the SAA2500 can be read via L3. The SAA2500 status flag L3RDY must be monitored before transferring data item bytes to avoid transferring bytes faster than the L3 interface of the SAA2500 can handle.

L3 INTERFACE INITIALISATION AT AN SAA2500 DEVICE RESET

Figure 15 shows the mandatory actions that must be taken for correct L3 interface start-up at a device reset.

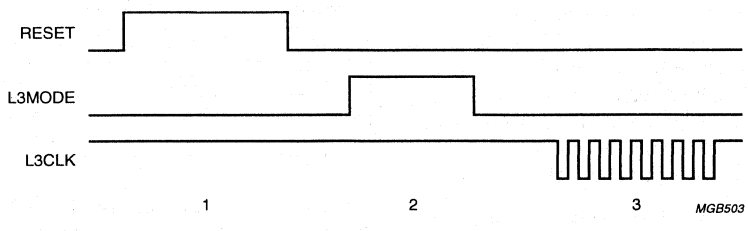


Fig.15 L3 interface initialisation procedure.

The actions shown in Fig.15 are:

1. In order for the SAA2500 to keep L3DATA in 3-state, L3MODE must be kept LOW during the whole period that reset signal RESET is asserted; meanwhile, no transfers can be performed (L3CLK stays HIGH).
2. For a proper initialisation of the L3 interface logic of the SAA2500, it is mandatory to make L3MODE HIGH and LOW again after the device reset has been de-activated. This must be done before any L3 transfer, even to or from other devices than the SAA2500, is performed. Figure 14 shows that L3CLK stays HIGH during this step.
3. Now the first transfer can be performed on the L3 bus. This transfer must be a operational address (indicated in Fig.14 by L3MODE = 0), addressing any of the devices connected to the L3 bus. The first transfer to the SAA2500 itself must always be either the writing of a control word or the reading of the SAA2500 status; the first transfer may never be a data item byte transfer.

Remark: any deviation from these steps may result in illegal L3 protocol behaviour of the SAA2500, even with the possibility of disturbing transfers to other devices connected to the L3 bus.

L3 INTERFACE CONTROL

The control of the SAA2500 L3 interface is performed with one-byte control words. Status polling is not necessary before writing control bytes. After writing the SAA2500 'write control' operational address, one or more control bytes may be written. Each written control byte overrules the previously sent control byte.

Table 15 L3 control.

7	6	5	4	3	2	1	0
CTRL7	CTRL6	CTRL5	CTRL4	CTRL3	CTRL2	CTRL1	CTRL0

The definitions of the control bytes (CTRL7 to CTRL0) are given in Table 16.

Table 16 Explanation of control bytes

CTRL7 TO CTRL0	DEFINITION	TYPE[1]
00000000	read/write SAA2500 settings item	I
00000001	read decoded frame header item	I
00000010	read used frame header item	I
00000011	read error report item	I
00000100	reserved	I
00000101	read ancillary Data item	I
00000110	write APU coefficients item	I
00000111	continue previous transfer	C
00001000 to 11111111	reserved	–

Note

1. Control bytes of type I initiate the transfer of a data item. The control byte of type C may be used after interrupting a transfer, in order to write APU coefficients, to return to the interrupted transfer.

SAA2500 STATUS

The host can check the status of the SAA2500 by reading the one-byte status word. After writing the SAA2500 'read status' operational address, the status byte may be read an arbitrary number of times. If status is read more than once, it is updated by the SAA2500 between the individual readings. The status flags of the SAA2500 have the definition as shown in Table 17.

Table 17 Status flag definitions.

7	6	5	4	3	2	1	0
DST2[1]	DST1[1]	DST0[1]	undefined	undefined	undefined	INSYNC[2][3]	L3RDY[4]

Notes

1. By interpreting DST2 to DST0, the host can synchronize to the input frame frequency, and also determine at which moment which L3 data item is available to be read. The value of DST2 to DST0 is only valid if flag INSYNC is set.
   a) DST2 is a modulo 2 frame counter, i.e. DST2 inverts at the moment the decoding of a new frame is started. DST2 enables to host to sample the decoding subprocess DST1 to DST0 less frequently, meanwhile enabling the host to see if it missed a state.
   b) DST1 and DST0 values are explained in Table 18.
2. INSYNC is synchronization indication:
   a) INSYNC = 0; the SAA2500 is not synchronized to the input data.
   b) INSYNC = 1; the SAA2500 is synchronized to the input data.
3. As indicated in Section "Input data frame header items", some of the readable data item bits only have significance if INSYNC = 1.
4. L3RDY is L3 interface ready indication:
   a) L3RDY = 0; the L3 interface cannot perform a new item data transfer yet.
   b) L3RDY = 1; the L3 interface is ready for the next item data transfer.

   After a device reset, L3RDY is cleared and will only become set after writing the first L3 control byte to the SAA2500. The value of L3RDY can be tested by polling signal L3DATA instead of transferring the whole status byte.

Table 18 Status bytes DST1 and DST0.

DST1	DST0	FUNCTION
0	0	subprocess 0; reading Ancillary Data or decoding header
0	1	subprocess 1; decoding bit allocation or scale factor select information
1	0	subprocess 2; decoding scale factors
1	1	subprocess 3; decoding samples

The DST1 and DST0 values in general do not have a determined duration. However, subprocess 3 takes at least a $\frac{1}{2}$frame period when ISO/MPEG layer I data is decoded, and $\frac{5}{6}$frame period when ISO/MPEG layer II data is decoded. Table 19 indicates the validity of the SAA2500 readable data items with respect to the decoding subprocess. Reading of a data item in a period when it is not valid renders undefined data.

Table 19 Validity of SAA2500 readable data items with respect to the decoding subprocess (notes 1 and 2).

SAA2500 IS DECODING FRAME n				SAA2500 IS DECODING FRAME n + 1			
DST2 = 0				DST2 = 1			
DST1 AND DST0 = 0	DST1 AND DST0 = 1	DST1 AND DST0 = 2	DST1 AND DST0 = 3	DST1 AND DST0 = 0	DST1 AND DST0 = 1	DST1 AND DST0 = 2	DST1 AND DST0 = 3
not valid	Ancillary Data item (frame n – 1)			not valid	–	–	–
	frame header items (frame n)				–	–	–
–	not valid	error report: BALOK (frame n)			not valid	–	–
–		not valid	error report: DECFM (frame n)			not valid	–

Notes

1. The Table shows following:
   a) The received Ancillary Data that was multiplexed in frame n–1 becomes valid after subprocess 0 of frame n, and may be read during subprocesses 1, 2 and 3 of frame n.
   b) The decoded and used frame headers for frame n become valid after subprocess 0 of frame n, and may be read during subprocesses 1, 2 and 3 of frame n.
   c) Flag BALOK for frame n in the error report item becomes valid after subprocess 1 of frame n, and may be read during subprocesses 2 and 3 of frame n and subprocess 0 of frame n+1.
   d) Flag DECFM for frame n in the error report item becomes valid after subprocess 2 of frame n, and may be read during subprocesses 3 of frame n and 0 of frame n+1.
2. Note that during subprocess 3 all data items can be read.

DATA ITEMS

Data can be transferred to or from the SAA2500 in data items. This section describes the general protocol to accomplish item data transfer, followed by the individual SAA2500 data items. Optional enhancements on the general protocol are described in Chapter "Appendix" Section "SAA2500 L3 protocol enhancement options".

General data items

The data items of the SAA2500 are transferred (i.e. read or written, depending on whether the data item is of readable or writeable type) in bytes. A data item transfer is initiated by writing the corresponding type I control byte (see Section "L3 interface control") to the SAA2500. The transfer of every subsequent item data byte must be preceded by reading the status until status flag L3RDY (see Section "SAA2500 status") is HIGH.

L3RDY may be tested alternatively by polling L3DATA, avoiding the need to transfer the whole status byte. Status polling is not required while transferring the APU coefficients item. Table 20 shows an example of how bytes 'DDDDDDDD' of a 2 byte data item, with the corresponding control byte 'CCCCCCCC', can be read. The writing of item data bytes occurs in a similar way.

Table 20 Example of a 2 byte data item.

L3DATA	TRANSFER SOURCE	L3MODE	EXPLANATION
01100010	host	0	1; indicates 'write control' transfer
CCCCCCCC	host	1	2; write transfer initiating (type I) control byte
01100011	host	0	3; indicates 'read status' transfer
SSSSSSSS	SAA2500	1	4; read status (repeat step 4 until L3RDY = 1)
01100001	host	0	5; indicates 'read item data' transfer
DDDDDDDD	SAA2500	1	6; read first item data byte
01100011	host	0	7; indicates 'read status' transfer
SSSSSSSS	SAA2500	1	8; read status (repeat step 8 until L3RDY = 1)
01100001	host	0	9; indicates 'read item data' transfer
DDDDDDDD	SAA2500	1	10; read second item data byte

Each data item has its own length in bytes. It is allowed to transfer less bytes than the data item length, skipping the last one or more bytes (it is even allowed to transfer no bytes at all). It is not allowed to transfer more bytes than the item length. This restriction does not hold for the APU coefficient item. After writing all APU coefficients (i.e. after writing all APU coefficient item bytes), they may be rewritten by continuing writing bytes to the APU coefficient item. Writing more than the specified number of bytes to a writeable data item or writing bytes to a read-only data item may cause the SAA2500 to malfunction. The reading of a write-only data item yields irrelevant data.

SAA2500 SETTINGS ITEM

The SAA2500 is configured with the SAA2500 settings. The initial value of the SAA2500 settings after reset is all zeros.

Table 21 SAA2500 settings item; 1 byte (read/write).

7	6	5	4	3	2	1	0
MSEL1[1]	MSEL0[1]	CRCACT[2]	MCKDIS[3]	FCKENA[4]	SELCH2[5]	RND1[6]	RND0[6]

Notes

1. MSEL1 and MSEL0; these bits select the used input interface, the input data format and the input synchronization type (see Table 22).
2. CRCACT; automatic/forced CRC activity:
   a) CRCACT = 0; the SAA2500 uses the protection bit in the ISO/MPEG frame header to determine the presence of the CRC.
   b) CRCACT = 1; the SAA2500 assumes the CRC always to be present. The protection bit in the used ISO/MPEG frame header is forced to 0.
3. MCKDIS; buffered master clock MCLK disabling:
   a) MCKDIS = 0; enable MCLK.
   b) MCKDIS = 1; disable (3-state) MCLK.
4. FCKENA; buffered $256f_s$ or $384f_s$ output signal FSCLK enabling:
   a) FCKENA = 0; disable (3-sate) FSCLK.
   b) FCKENA = 1; enable FSCLK.
5. SELCH2; with dual channel mode input data (with other modes of input data 'don't care':
   a) SELCH2 = 0; select channel I.
   b) SELCH2 = 1; select channel II.
6. RND1 and RND0; these bits select the rounding of the baseband audio output samples (see Table 23).

Table 22 MSEL1 and MSEL0.

MSEL1	MSEL0	USED INPUT INTERFACE	INPUT SYNCHRONIZATION
0	0	master	to ISO/MPEG synchronization pattern
0	1	reserved	reserved
1	0	slave	to ISO/MPEG synchronization pattern
1	1	slave	to synchronization signal CDSSY

Table 23 RND1 and RND0.

RND1	RND0	OUTPUT SAMPLE ROUNDING LENGTH
0	0	16 bits
0	1	18 bits
1	0	20 bits
1	1	22 bits

INPUT DATA FRAME HEADER ITEMS

Information about the input data, derived by the SAA2500 from the input data frame headers, may be read from the frame header items. Both the frame header bytes decoded from the input bitstream and the header bytes used for the actual decoding may be read.

The decoded frame header item is valid independent of the value of status flag INSYNC, it e.g. shows the decoded headers while the SAA2500 is in the process of synchronising.

The used frame header item is only valid if status flag INSYNC is set. The used header bytes are derived by the SAA2500 from the decoded header bytes by overruling NOPROT to 0 if settings bit CRCACT = 1, and overruling detected errors.

Table 24 Decoded input data frame header item; 3 bytes (read-only).

SUBSEQUENT BYTES	7	6	5	4	3	2	1	0
Decoded header byte 1	SY3[1]	SY2[1]	SY1[1]	SY0[1]	ID[2]	LAY1[3]	LAY0[4]	NOPR[5]
Decoded header byte 2	BR3[6]	BR2[6]	BR1[6]	BR0[6]	FS1[7]	FS0[7]	undefined	undefined
Decoded header byte 3	MOD1[8]	MOD0[8]	MODX1[9]	MODX0[9]	COPR[10]	ORIG[11]	EMPH1[12]	EMPH0[12]

Notes to Tables 24 and 25

1. SY3 to SY0; last 4 bits of the synchronization word.
2. ID; algorithm identification.
3. LAY1; layer Most Significant Bit (MSB).
4. LAY0; layer Least Significant Bit (LSB).
5. NOPR; CRC on header, bit allocation and scale factor select information activity flag.
6. BR3 to BR0; bit rate index.
7. FS1 and FS0; sample rate index.
8. MOD1 and MOD0; mode.
9. MODX1 and MODX0; mode extension.
10. COPR; copyright flag.
11. ORIG; original or home copy flag.
12. EMPH1 and EMPH0; audio de-emphasis, these bits are only meant to monitor the current de-emphasis mode; the corresponding de-emphasis is performed by the SAA2500 automatically before the baseband audio signal is output.

Table 25 Used input data frame header item; 3 bytes (read-only).

SUBSEQUENT BYTES	7	6	5	4	3	2	1	0
Used header byte 1	1	1	1	1	1	1	LAY0	NOPR
Used header byte 2	BR3	BR2	BR1	BR0	FS1	FS0	undefined	undefined
Used header byte 3	MOD1	MOD0	MODX1	MODX0	COPR	ORIG	EMPH1	EMPH0

ERROR REPORT ITEM

The validity of bit allocation plus scale factor select information may be read from the error report item. The error report item is only valid if status flag INSYNC is set.

Table 26 Error report item; 1 byte (read-only).

SUBSEQUENT BYTES	7	6	5	4	3	2	1	0
Error report	BALOK(1)	DECFM(2)	undefined	undefined	undefined	undefined	undefined	undefined

Notes

1. BALOK; bit allocation and scale factor select information validity indication:
   a) BALOK = 0; bit allocation or scale factor select information are incorrect, or the CRC (if active) over header, bit allocation and scale factor select information fail.
   b) BALOK = 1; bit allocation or scale factor select information are correct, and the CRC (if active) over header, bit allocation and scale factor select information passes.
2. DECFM; frame skipping/decoding indication:
   a) DECFM = 0; the current input data frame is skipped, and the corresponding baseband audio output frame is muted due to input data errors or inconsistencies. However, synchronization to the input data is maintained.
   b) DECFM = 1; the current frame is decoded normally.

ANCILLARY DATA ITEM

The last 54 bytes of each ISO/MPEG frame, which may carry Ancillary Data (AD), are buffered by the SAA2500 to be read by the host. The subsequent Ancillary Data bytes are read in reversed order with respect to their order in the input data bitstream. The first item data byte is the last frame byte in the input bitstream. The Ancillary Data item is refilled at every frame. The host must either know or determine itself how many of the Ancillary Data bytes are valid per frame. The Ancillary Data item only has significance if status flag INSYNC is set.

Table 27 Ancillary data item; 54 bytes (read-only).

SUBSEQUENT BYTES	7	6	5	4	3	2	1	0
AD byte 1 to AD byte 54	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

APU COEFFICIENTS ITEM

The APU coefficients are set by writing their 8 bit indices to the 4-byte APU coefficient item. Only the 7 LSBs are valid. The MSB must be zero. At a device reset, indices LL and RR are set to 00000000 ('no attenuation') and indices LR and RL to 01111111 (infinite attenuation; no crosstalk).

Table 28 APU coefficients item; 4 bytes (write-only); see note 1.

SUBSEQUENT BYTES	7	6	5	4	3	2	1	0
APU coefficient LL	0	LL.6	LL.5	LL.4	LL.3	LL.2	LL.1	LL.0
APU coefficient LR	0	LR.6	LR.5	LR.4	LR.3	LR.2	LR.1	LR.0
APU coefficient RL	0	RL.6	RL.5	RL.4	RL.3	RL.2	RL.1	RL.0
APU coefficient RR	0	RR.6	RR.5	RR.4	RR.3	RR.2	RR.1	RR.0

Note

1. Multiple options are supplied by the SAA2500 to increase the timing accuracy of the APU coefficient writing (see Section "SAA2500 L3 protocol enhancement options").

SPEED LIMITATIONS OF THE L3 INTERFACE

When reading the status of, or writing control bytes to the SAA2500, no status polling is necessary, so the speed of these transfers is only limited by the maximum frequency of signal L3CLK and the timing constraints of the L3 protocol.

When reading or writing data item bytes, status polling is necessary. In addition to the speed limitation this poses, the application must take precautions that individual data item bytes are transferred at an interval of at least 200 µs. Neither the status polling nor a minimum interval between transfers is required when transferring the APU coefficient item.

DEFAULT ITEM DATA VALUES AFTER RESET

At a device reset, the L3 interface initialisation procedure must be followed. All writeable data items are pre-loaded with a defined default value after the device reset signal has been de-activated. These default values are summarised in Table 29.

Table 29 SAA2500 settings item; default value after device reset (notes 1 to 6.)

SUBSEQUENT BYTES	7	6	5	4	3	2	1	0
SAA2500 settings	MSEL1	MSEL0	CRCACT	MCKDIS	FCKENA	SELCH2	RND1	RND0
Value	0	0	0	0	0	0	0	0

Notes

1. MSEL1 = 0 and MSEL0 = 0; the master input is selected. The SAA2500 synchronizes to the ISO/MPEG synchronization pattern.
2. CRCACT = 0; the SAA2500 uses the protection bit in the ISO/MPEG frame header to determine if the CRC is active.
3. MCKDIS = 0; the buffered master clock output MCLK is enabled.
4. FCKENA = 0; the buffered $256f_s$ or $384f_s$ clock output is disabled.
5. SELCH2 = 0; when decoding input data with dual channel mode, channel I is output on both baseband audio output channels.
6. RND1 = 0 and RND0 = 0; the baseband audio output signals are rounded to 16 bit.

Table 30 APU coefficients item; default values after device reset.

SUBSEQUENT BYTES	7	6	5	4	3	2	1	0
APU coefficient LL[1]	0	LL.6 = 0	LL.5 = 0	LL.4 = 0	LL.3 = 0	LL.2 = 0	LL.1 = 0	LL.0 = 0
APU coefficient LR[2]	0	LR.6 = 1	LR.5 = 1	LR.4 = 1	LR.3 = 1	LR.2 = 1	LR.1 = 1	LR.0 = 1
APU coefficient RL[3]	0	RL.6 = 1	RL.5 = 1	RL.4 = 1	RL.3 = 1	RL.2 = 1	RL.1 = 1	RL.0 = 1
APU coefficient RR[4]	0	RR.6 = 0	RR.5 = 0	RR.4 = 0	RR.3 = 0	RR.2 = 0	RR.1 = 0	RR.0 = 0

Notes

1. LL = 00000000; no attenuation in the left-to-left APU path.
2. LR = 01111111; infinite attenuation in the left-to-right APU path.
3. RL = 01111111; infinite attenuation in the right-to-left APU path.
4. RR = 00000000; no attenuation in the right-to-right APU path.

APPENDIX

Preliminary specification 3-line 'L3' interface

INTRODUCTION

The main purpose of the new interface definition is to define a protocol that allows for the transfer of control information and operational details between a microcontroller (μC) and a number of slave devices, at a rate that exceeds other common interfaces, but with a sufficient low complexity for application in consumer products. It should be clearly noted that the current interface definition is intended for use in a single apparatus, preferably restricted to a single printed circuit board.

The new interface requires 3 signal lines (apart from a return 'ground') between the microcontroller and the slave devices (from this the name 'L3' is derived). These 3-lines are common to all ICs connected to the bus: L3MODE, L3DATA and L3CLK. L3MODE and L3CLK are always driven by the microcontroller, L3DATA is bidirectional:

Table 31 The 3-lines common to all ICs; L3MODE, L3CLK and L3DATA.

SIGNAL	MICROCONTROLLER	SLAVE DEVICE
L3MODE(1)	output	input
L3CLK(2)	output	input
L3DATA(3)	output/input	input/output

Notes

1. L3MODE is used for the identification of the operation mode.
2. L3CLK is the bitclock to which the information transfer will be synchronized.
3. L3DATA will carry the information to be transferred.

All slave devices in the system can be addressed using a 6 bit address. This allows for up to 63 different slave devices, as the all '0' address is reserved for special purposes. In addition it is possible to extend the number of addressable devices using 'extended addressing'.

In operation 2 modes can be identified:

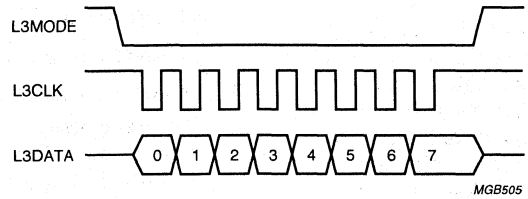
1. Addressing mode (AM).

   During addressing mode a single byte is sent by the microcontroller. This byte consists of 2 data operation mode (DOM) bits and 6 operational address (OA) bits. Each of the slave devices evaluates the operational address. Only the device that has been issued the same operational address will become active during the following data mode. The operation to be executed during the data mode is indicated by the two data operation mode bits.
2. Data mode (DM).

   During data mode information is transferred between microcontroller and slave device. The transfer direction may be from microcontroller to slave ('write') or from slave to microcontroller ('read'). However, during one data mode the transfer direction can not change.

Addressing mode

In order to start an addressing mode the microcontroller will make the L3MODE line LOW. The L3CLK line is lowered 8 times and the DATA line will carry 8 bits. The addressing mode is ended by making the L3MODE line HIGH.



The meaning of the bits on L3DATA.

Bit 0 and bit 1; these are the data operation mode (DOM) bits that indicate the nature of the following data transfer. Each slave device may have its own allocation of operation modes to the 4 possible codes of these bits. For correct information about the operation the device will perform, refer to the descriptions of the individual IC's. For new designs the preferred allocations are given in Table 32.

Bit 2 to bit 7; these bits act as 6 bit (special function) operational IC address, with bit 7 as MSB and bit 2 as LSB. Bit 7 to bit 5 act as system identification and bit 4 to bit 2 as identification of the device within the system.

Fig.16 Addressing mode.

Table 32 Preferred allocations.

DOM1	DOM0	FUNCTION	REMARKS
0	0	data from microcontroller to SAA2500	general purpose data transfer
0	1	data from SAA2500 to microcontroller	general purpose data transfer
1	0	control from microcontroller to SAA2500	e.g. register selection for data transfer
1	1	status from SAA2500 to microcontroller	short device status message

Special function operational address

Operational address 000000 (bit 2 to bit 7) is the special function address, and is used for the L3 device reset, as well as for the declaration and invalidation of the extended addressing. Both will be explained in Sections "Device interface reset" and "Extended addressing".

Data mode

In the data mode the microcontroller sends or receives information to or from the selected device. During data transfer the L3MODE line is HIGH. The L3CLK line is lowered 8 times during which the L3DATA line carries 8 bits. The information is presented LSB first and remains stable during the LOW phase of the L3CLK signal.

The preferred basic data transfer unit is an 8 bit byte. Some implementations that are modifications of older circuits with 16 bit registers may use a basic unit of 16 bits, transferred as 2 bytes, with the most significant byte presented first. No other basic data transfer unit is allowed.

Halt mode

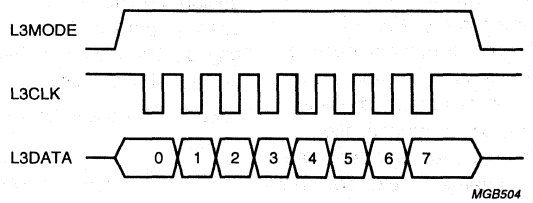


Fig.17 Data transfer mode.

In between units the L3MODE line will be driven LOW by the microcontroller to indicate the completion of a basic unit transfer. This is called 'halt mode' (HM). During halt mode the L3CLK line remains HIGH (to distinguish it from an addressing mode). The halt mode allows an implementation of an interface module without a bit counter. However, an implementation using a bit counter in the interface module may allow for the L3MODE line to be kept HIGH in between units (not using the halt mode).

This implementation must also operate correctly if the halt mode is used. The documentation of the device will have to indicate clearly whether or not the 'halt mode' is necessary for correct operation of the interface.

Device interface reset

If the microcontroller sends an operational address '000000' with DOM1 and DOM0 also equal to '0' this indicates that none of the L3 interface devices is allowed to communicate with the microcontroller during the following data mode. This enables a different application of the L3CLK and L3DATA lines as the L3 devices will not interfere with any communication on these lines as long as L3MODE remains HIGH (e.g. the L3CLK and L3DATA lines are normally connected to USART circuits in the microcontrollers which allow for convenient communication between microcontrollers).

Any addressing mode with a valid L3 operational address will re-enable the communication with the corresponding device.

Devices with a fixed operational address ('Primary L3 devices') will react with a device reset condition regardless of the state of DOM1 and DOM0.

Devices with a programmable operational address ('Secondary L3 devices') can only be put in the interface reset condition if the DOM1 and DOM0 bits are '0'. Other combinations of DOM1 and DOM0 initiate data transfers for 'extended addressing'.

Extended addressing

L3 Devices with a programmable address can be informed of their operational address using a special data transfer.

Operational address declaration

For the declaration (programming) of the operational address of an L3 device with a 'secondary L3 identification code' the following action is required:

1. First the microcontroller must issue an L3 operational address '000000' (special function address) with DOM1 = 0 and DOM0 = 1. This combination defines the operational address declaration operation. Next the microcontroller will start a data transfer mode in which it first sends the secondary L3 identification code for the device that is to be issued an operational address, followed by a byte containing the operational address (the DOM bits in this byte are don't cares).
2. Next the microcontroller will start a data transfer mode in which it first sends the secondary L3 identification code for the device that is to be issued an operational address, followed by a byte containing the operational address (the DOM bits in this byte are don't cares).

A secondary L3 identification code is unique for any design. Devices of the same design have the same identification code of one or more bytes. However, special designs may have a range of identification codes, one of which can be selected by a hardware solution, to enable the connection of more than one device of the same design to the L3 interface. It is also possible to use separate L3MODE lines for multiple devices of the same design, but the same L3 identification code (this also enables 'parallel programming' of these devices). Bit 0 of any identification code byte will indicate whether or not an additional byte follows:

Bit 0 = 0; no additional byte as part of the identification code.

Bit 0 = 1; additional byte follows.

With this the number of secondary L3 identification codes is (theoretically) unlimited.

The operational address for the programmable device is preferable in the range 111000 to 111111. However, it is possible in a given application to issue any operational address that is not used to address primary L3 devices or other secondary L3 devices. An example is given in Table 33.

Table 33 Example of L3 devices; notes 1 to 4.

ADDRESSING MODE	DATA MODE			
SPECIAL ADDRESS	SECONDARY L3 IDENTIFICATION CODE			OPERATIONAL ADDRESS (ONE BYTE)
	BYTE 1	BYTE 2	BYTE 3	
10000000	1XXXXXXX	1XXXXXXX	0XXXXXXXX	MMYYYYYY

Notes

1. Bits are shown in the order they appear on L3DATA (bit 0 first, bit 7 last).
2. X = bit of the identification code.
3. M = DOM bit of operational address (don't care).
4. Y = bit of the operational address.

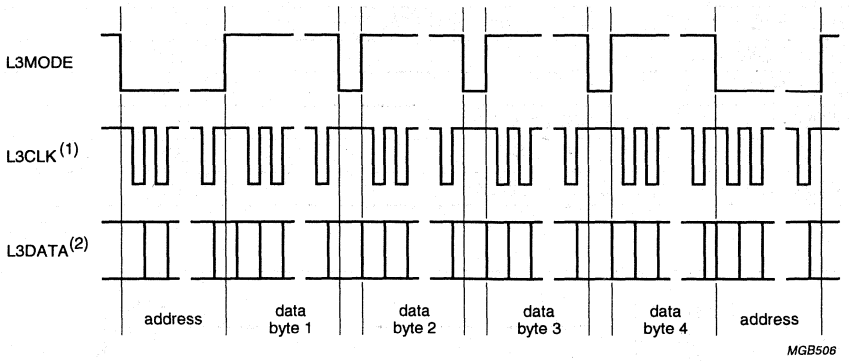
Operational address invalidation

In order to re-allocate an operational address that has been allocated to a secondary L3 device it is possible to invalidate an operational address:

- First the microcontroller must issue an L3 operational address '000000' (special function address) with DOM1 = 1 and DOM0 = 0. This combination defines the operational address invalidation operation.
- Next the microcontroller will start a data transfer mode in which it only sends the secondary L3 identification code for the device that will no longer be addressed. From this moment on the device will not be able to communicate with the microcontroller until it is issued a new operational address by an OA declaration (it will enter a 'device interface reset' condition).

Remark: the combination of a special function address (000000) and DOM1 and DOM0 equal to '1' is reserved for future applications. Designs based on this specification will react with a 'device interface reset'.

EXAMPLE OF A DATA TRANSFER



(1) L3CLK is triggered by L3MODE.
(2) For more details see Fig.20.

Fig.18 Example of transfer of 4 bytes.

A data transfer starts when the microcontroller sends an address on the bus. All ICs will evaluate this address, but only the IC addressed will be an active partner for the microcontroller in the following data transfer mode.

During the data transfer mode bytes will be sent from or to the microcontroller. In this example the L3MODE line is made LOW ('halt mode') in between byte transfers. This is the default operation, although some ICs may allow the L3MODE line to be kept HIGH. This exception must be specified clearly in the IC documentation, and such ICs must be able to communicate with microcontrollers that make L3MODE LOW in between transfers. It is suggested that new designs only use bytes as basic data transfer units. After the data transfer the microcontroller does not need to send a new address until a new data transfer is necessary. Alternatively it may also send the 'special address' 000000 to indicate the end of the data transfer operation.

TIMING REQUIREMENTS

These are requirements for the slave devices designed according to the 'L3' interface definitions.

Addressing mode

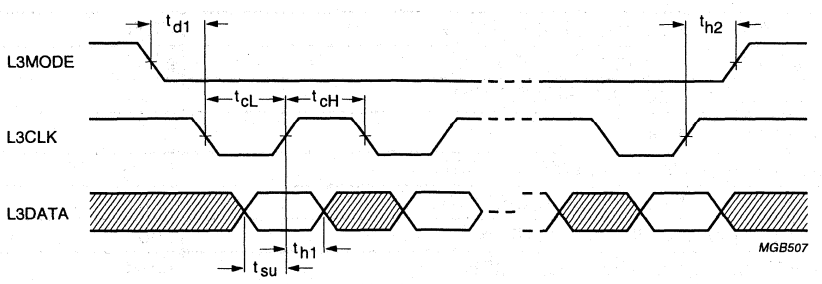


Fig.19 Timing (addressing mode).

Table 34 Requirements for timing (addressing mode); see Fig.19.

SYMBOL	PARAMETER	REQUIREMENT	UNIT
t_{d1}	L3CLK HIGH to L3CLK LOW delay time after L3MODE LOW	≥190	ns
t_{cL}	L3CLK LOW time	≥250	ns
t_{cH}	L3CLK HIGH time	≥250	ns
t_{su1}	L3DATA set-up time before L3CLK HIGH	≥190	ns
t_{h1}	L3DATA hold time after L3CLK HIGH	≥30	ns
t_{h2}	L3CLK hold time before L3MODE HIGH	≥190	ns

Data mode

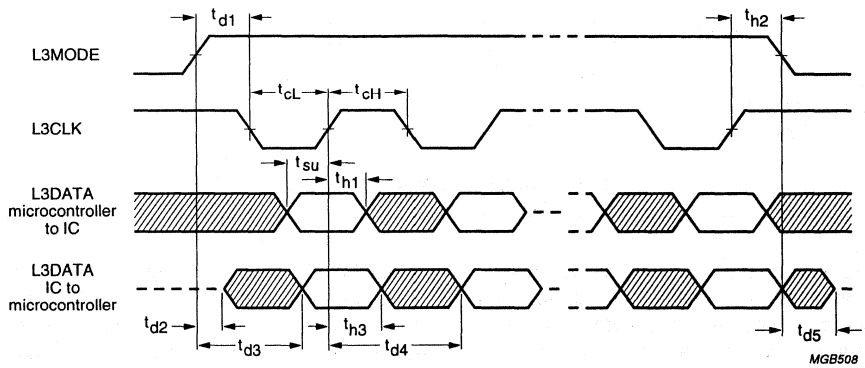


Fig.20 Timing (data mode).

Table 35 Requirements for timing (data mode); see Fig.20.

SYMBOL	PARAMETER	REQUIREMENT	UNIT
t_{d1}	L3CLK HIGH to L3CLK LOW delay time after L3MODE HIGH	≥190	ns
t_{cL}	L3CLK LOW time	≥250	ns
t_{cH}	L3CLK HIGH time	≥250	ns
Microcontroller to slave device			
t_{su1}	L3DATA set-up time before L3CLK HIGH	≥190	ns
t_{h1}	L3DATA hold time after L3CLK HIGH	≥30	ns
t_{h2}	L3CLK hold time before L3MODE HIGH	≥190	ns
Slave device to microcontroller			
t_{d2}	L3DATA enable time after L3MODE HIGH	$0 < t_{d2} \leq 50$	ns
t_{d3}	L3DATA stable time after L3MODE HIGH	≤380	ns
t_{h3}	L3DATA hold time after L3CLK HIGH	≥50	ns
t_{d4}	L3DATA stable time after L3CLK HIGH	≤360	ns
t_{d4}	L3DATA stable time after L3CLK HIGH between bit 7 of a byte and bit 0 of next byte if no halt mode is used	≤530	ns
t_{d5}	L3DATA disable time after L3MODE LOW	$0 < t_{d5} \leq 50$	ns

Halt mode

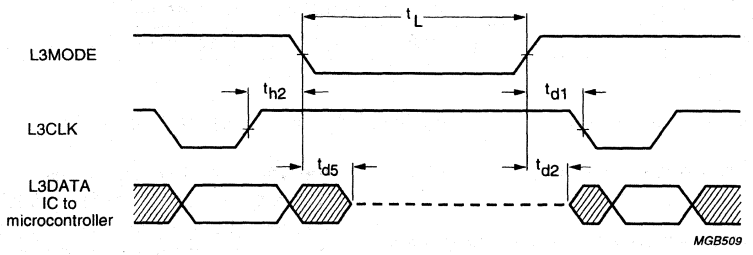


Fig.21 Timing (halt mode).

Table 36 Requirements for timing (halt mode); see Fig.21.

SYMBOL	PARAMETER	REQUIREMENT	UNIT
t_{d1}	L3CLK HIGH to L3CLK LOW delay time after L3MODE HIGH	≥190	ns
t_L	L3MODE LOW time	≥190	ns
t_{h2}	L3CLK hold time before L3MODE LOW	≥190	ns
Slave device to microcontroller			
t_{d2}	L3DATA enable time after L3MODE HIGH	$0 < t_{d2} \leq 50$	ns
t_{d5}	L3DATA disable time after L3MODE LOW	$0 < t_{d5} \leq 50$	ns

SAA2500 L3 protocol enhancement options

The L3 interface on the SAA2500 is limited in speed, dictated both by the maximum SAA2500 handling speed and the upper frequencies of the L3 interfacing standard. On the other hand, the SAA2500 offers several enhancements, described in this section, to make a better use of the SAA2500 L3 interface capacity. The enhancements are optional. The applicant chooses whether to use them or not.

TESTING L3RDY BY POLLING L3DATA

The host must test status flag L3RDY to make sure whether the SAA2500 L3 interface is ready to transfer data item bytes. According to the general protocol, described in Section "Data items", the status is read by first writing the SAA2500 'read status' operational address, after which the status byte can be transferred. To avoid these status byte transfers (thus reducing the host's load), after writing the SAA2500 'read status' operational address, L3RDY is continuously copied to signal L3DATA during the period in which no L3 transfers (i.e. status byte readings) are performed. Meanwhile, L3MODE must be kept HIGH (no L3 operational addresses may be written). As a result, L3RDY can be tested as shown in Table 37.

Table 37 Status bytes DST1 and DST0; note 1.

L3DATA	TRANSFER SOURCE	L3MODE	EXPLANATION
01100011	host	0	write 'read status' operational address
polled	SAA2500	1	test L3DATA; repeat this step until L3DATA = 1

Note

1. No status byte transfers are needed; the load of the host (microcontroller) can thus be reduced.

OPTIONS TO INCREASE THE TIMING ACCURACY OF THE APU COEFFICIENT WRITING

The SAA2500 offers three enhancements to increase the timing accuracy with which APU coefficients can be updated by the application:

1. Status polling is not required when APU coefficients are written. L3 status flag L3RDY, when read anyhow, will always be HIGH, indicating that the next APU coefficient transfer may be done. The transfer speed is only limited by the maximum allowed frequency of L3CLK. As a result, also no 'write item data' operational address is needed any more before writing each APU coefficient index.
2. Normally, no more bytes may be written to a writeable data item than the length of that specific item. An exception is formed by the APU coefficients. They may be written continuously with a coefficient wrap. After the writing of all 4 coefficients, the writing can be continued at the first APU coefficient without having to write a new control byte.
3. The data item transfer protocol, described in Section "Data items", although transparent, allows only for the reading or writing of data items from their first data byte onwards. This approach can lead to situations where e.g. 54 Ancillary Data item bytes must all be read (which takes at least $54 \times 200\ \mu s = 10.8$ ms, due to the interface speed limitations: see Section "Data items") before the next data item can be transferred. The SAA2500 enables the writing of APU coefficients without having to wait for the current item transfer to finish. In order to do so, a running transfer can be interrupted by an APU coefficient write transfer, and then be resumed with the 'continue current transfer' control byte.

   An item transfer may be interrupted at any time to write APU coefficients. After the 'continue previous transfer' control byte, a operational address must always follow, indicating the type of L3 transfer that will follow. An APU coefficient write transfer itself cannot be interrupted.

The 3 mentioned options are all illustrated in Table 38, where a data item transfer is interrupted between the reading of the n^{th} and $(n + 1)^{th}$ data item byte.

Table 38 Example of 3 options to increase the timing accuracy of the APU coefficient writing.

L3DATA	TRANSFER SOURCE	L3MODE	EXPLANATION
DDDDDDDD	SAA2500	1	read n^{th} item data byte
01100010	host	0	indicate 'write control' transfer
00000110	host	1	write 'write APU coefficients' control byte
01100000	host	0	indicate 'write item data' transfer
DDDDDDDD	host	1	write APU coefficient LL
DDDDDDDD	host	1	write APU coefficient LR
DDDDDDDD	host	1	write APU coefficient RL
DDDDDDDD	host	1	write APU coefficient RR
DDDDDDDD	host	1	write APU coefficient LL
DDDDDDDD	host	1	write APU coefficient LR
DDDDDDDD	host	1	write APU coefficient RL
DDDDDDDD	host	1	write APU coefficient RR
01100010	host	0	indicate 'write control' transfer
00000111	host	1	write 'continue previous transfer' control byte
01100011	host	0	indicate 'read status' transfer
SSSSSSSS	SAA2500	1	read status; repeat this step until L3RDY = 1
01100001	host	0	indicate 'read item data' transfer
DDDDDDDD	SAA2500	1	read $(n + 1)^{th}$ item data byte
etc.	etc.	etc.	etc.

APPLICATION INFORMATION

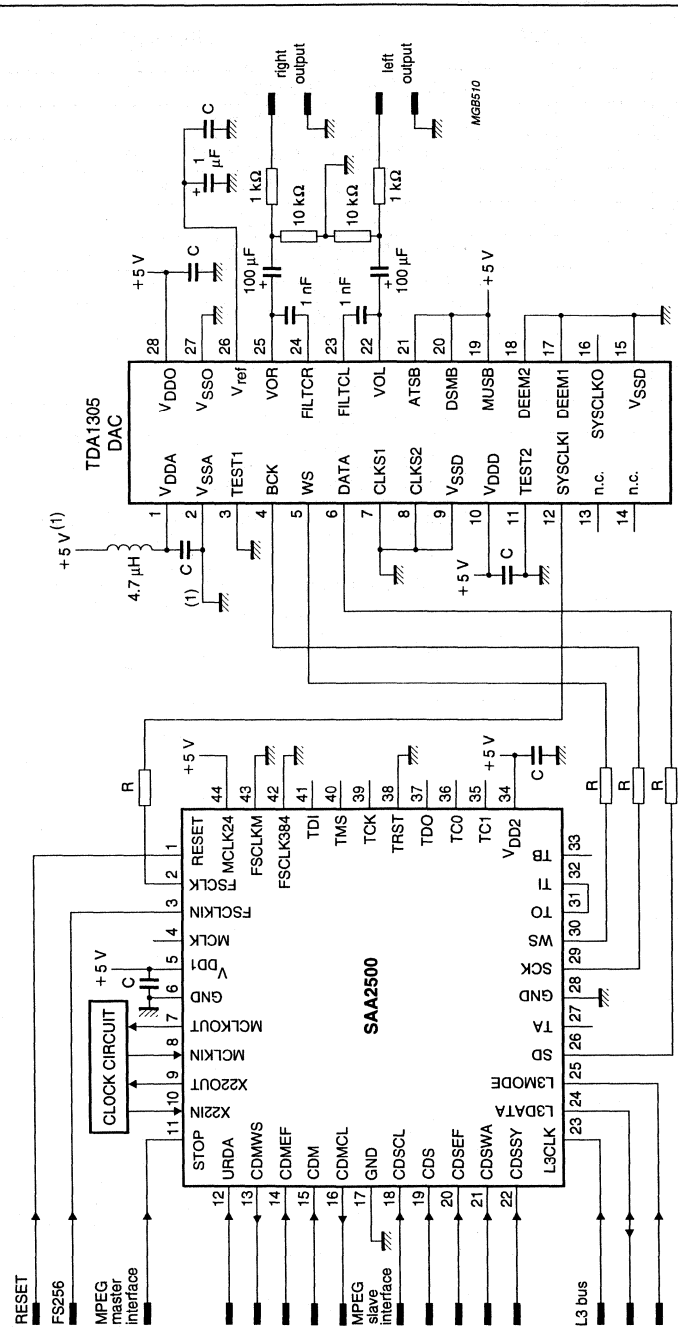


Fig.22 Typical application diagram.

C = 100 nF; R = 47 Ω.

(1) The supply voltage (+5 V) and GND links should be located close to the supply connector.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+6.5	V
V_i	input voltage	note 1	−0.5	V_{DD} + 0.5	V
I_{DD}	supply current		–	100	mA
I_I	input current		–	10	mA
I_O	output current	2 mA outputs	–	10	mA
		4 mA outputs	–	20	mA
P_{tot}	total power dissipation	VDD = 5 V±5%	–	165	mW
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{es1}	electrostatic handling	note 2	−2000	+2000	V
V_{es2}	electrostatic handling	note 3	−200	+200	V

Notes

1. Input voltage should not exceed 6.5 V unless otherwise specified.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

DC CHARACTERISTICS

V_{DD} = 5 V ±10%; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{DD}	quiescent supply current	note 1	100	–	–	µA
Inputs; notes 2 and 3						
V_{IH}	HIGH level input voltage (CMOS)		$0.7V_{DD}$	–	V_{DD}	V
V_{IL}	LOW level input voltage (CMOS)		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage (TTL)		2	–	V_{DD}	V
V_{IL}	LOW level input voltage (TTL)		0	–	0.8	V
V_{tLH}	positive going threshold voltage (CMOS Schmitt trigger)		–	–	$0.8V_{DD}$	V
V_{tHL}	negative going threshold voltage (CMOS Schmitt trigger)		$0.2V_{DD}$	–	–	V
V_{hys}	hysteresis voltage (CMOS Schmitt trigger)		–	$0.3V_{DD}$	–	V
$\|I_I\|$	input current		–	–	1	µA
R_{pull}	pull-up resistor		14	–	140	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
V_{OH}	HIGH level output voltage	I_O = 4 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = 4 mA	–	–	0.5	V
$\|I_{OZ}\|$	3-state off leakage current		–	–	5	μA

Notes

1. TDI, TMS, TRST and L3DATA not driven; TC0 and TC1 driven HIGH; all other inputs driven LOW.
2. Inputs TRST, TCK, TMS and TDI are TTL level compatible; all other inputs are CMOS level compatible.
3. Input TRST (pin 38) should be connected to ground for normal operation and connected to V_{DD} for boundary scan testing.

AC CHARACTERISTICS

V_{DD} = 5 V ±10%; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clocks						
C_I	input capacitance		–	–	10	pF
MCLKIN						
f_{clk}	clock frequency	MCLK24 = 1	–	24.576	–	MHz
		MCLK24 = 0	–	12.288	–	MHz
t_r	rise time		–	12	–	ns
t_f	fall time		–	12	–	ns
t_H	HIGH time		12	–	–	ns
t_L	LOW time		12	–	–	ns
X22IN						
f_{clk}	clock frequency		–	22.579	–	MHz
t_r	rise time		–	12	–	ns
t_f	fall time		–	12	–	ns
t_H	HIGH time		12	–	–	ns
t_L	LOW time		12	–	–	ns
FSCLKIN						
f_{clk}	clock frequency	FSCLK384 = 1	–	$384f_s$	–	Hz
		FSCLK384 = 0	–	$256f_s$	–	Hz
t_r	rise time	note 1	–	5	–	ns
t_f	fall time	note 1	–	5	–	ns
t_H	HIGH time		12	–	–	ns
t_L	LOW time		12	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CDSCL						
f_{clk}	clock frequency		–	–	768	kHz
t_r	rise time	note 1	–	12	–	ns
t_f	fall time	note 1	–	12	–	ns
t_H	HIGH time	note 2	$T_m + 20$	–	–	ns
t_L	LOW time	note 2	$T_m + 20$	–	–	ns
CDMCL						
f_{clk}	clock frequency	note 2	–	$\frac{1}{8T_m}$	–	Hz
L3CLK						
t_H	HIGH time		$T_m + 10$	–	–	ns
t_L	LOW time		$T_m + 10$	–	–	ns
FSCLK						
f_{clk}	clock frequency	MSEL = 00; FSCLKM = 0; f_s = 44.1 kHz	–	$\frac{f_{X22IN}}{2}$	–	MHz
		MSEL = 00; FSCLKM = 0; f_s = 48 kHz	–	$\frac{f_{MCLKIN}}{2}$	–	MHz
		MSEL = 00; FSCLKM = 0; f_s = 32 kHz	–	$\frac{f_{MCLKIN}}{3}$	–	MHz
MCLK						
f_{clk}	clock frequency		–	f_{MCLKIN}	–	MHz
SCK						
f_{clk}	clock frequency	FSCLK384 = 0; $f_{SCK} = 64f_s$	–	$\frac{f_{FSCLK}}{4}$	–	MHz
		FSCLK384 = 1; $f_{SCK} = 64f_s$	–	$\frac{f_{FSCLK}}{6}$	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
C_I	input capacitance		–	–	10	pF
t_{su1}	set-up time TI to SCK HIGH	$C_L < 25$ pF	33	–	–	ns
t_{su2}	set-up time CDM and CDMEF to CDMCL, CDS, CDSEF and CDSWA HIGH	$C_L < 25$ pF	42	–	–	ns
t_{su3}	set-up time CDSSY to CDSCL HIGH		$T_m + 10$	–	–	ns
t_{d1}	delay time L3MODE to L3LCK LOW		0	–	–	ns
t_{h1}	hold time TI to SCK HIGH		0	–	–	ns
t_{h2}	hold time CDM, CDMEF to CDMCL, CDS, CDSEF and CDSWA HIGH		0	–	–	ns
t_{h3}	hold time CDSSY to CDSCL HIGH		10	–	–	ns
t_{h4}	input hold time		0	–	–	ns
t_L	L3MODE LOW time		$T_m + 10$	–	–	ns
Outputs						
C_O	output capacitance		–	–	50	pF
t_h	hold time SD, WS, TO, TB and TA to SCK LOW	notes 3 and 4	–22	–	–	ns
t_h	hold time CDMWS to CDMCL LOW	notes 3 and 4	–15	–	–	ns
t_d	delay time SD, WS, TO, TB and TA to CDMCL LOW	note 3	–	–	10	ns
t_d	delay time CDMWS to CDMCL LOW	note 3	–	–	0	ns
Inputs/outputs						
C_O	output capacitance		–	–	50	pF
t_{su}	input set-up time	note 5	$T_m + 10$	–	–	ns
t_h	input hold time	note 5	10	–	–	ns
t_h	output hold time	notes 3 and 5	T_m	–	–	ns
t_d	output delay time	notes 3 and 5	–	–	$2T_m + 30$	ns
t_{d2}	3-state enable time	notes 3 and 6	–	–	20	ns
t_{d3}	3-state stable time	notes 3 and 6	–	–	20	ns
t_{d5}	3-state disable time L3DATA to L3MODE LOW	note 3	–	–	20	ns

Notes

1. Short rise and fall times improve the tolerance of clocks to signal and supply noise.
2. If MCLK24 = 1 then $T_m = \frac{4}{f_{MCLKIN}}$ else $T_m = \frac{2}{f_{MCLKIN}}$.
3. To allow for the effects of load capacitance the timing values should be de-rated by 0.5 ns/pF.
4. For maximum clock signal load of 25 pF.
5. L3DATA to L3CLK HIGH.
6. L3DATA to L3MODE HIGH.

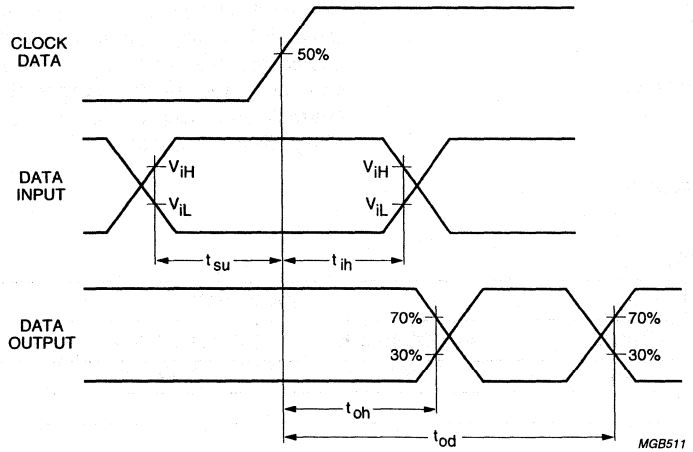


Fig.23 Timing diagram.

Stereo filter and codec for MPEG layer 1 audio applications

SAA2520

FEATURES

- Stereo filtering and codec functions in a single chip
- MPEG coded interface
- Filtered data interface
- Baseband audio data interface
- LT interface to microcontroller
- Clock generator
- Low operating voltage capability.

GENERAL DESCRIPTION

The SAA2520 performs the sub-band filtering and audio frame codec functions to provide efficient audio compression/decompression for MPEG (11172-3) Layer1 applications. It is capable of functioning as a stand-alone decoder but requires the addition of an adaptive masking threshold processor (SAA2521) in order to function as a highly efficient encoder.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2520GP	44	QFP	plastic	SOT205AG

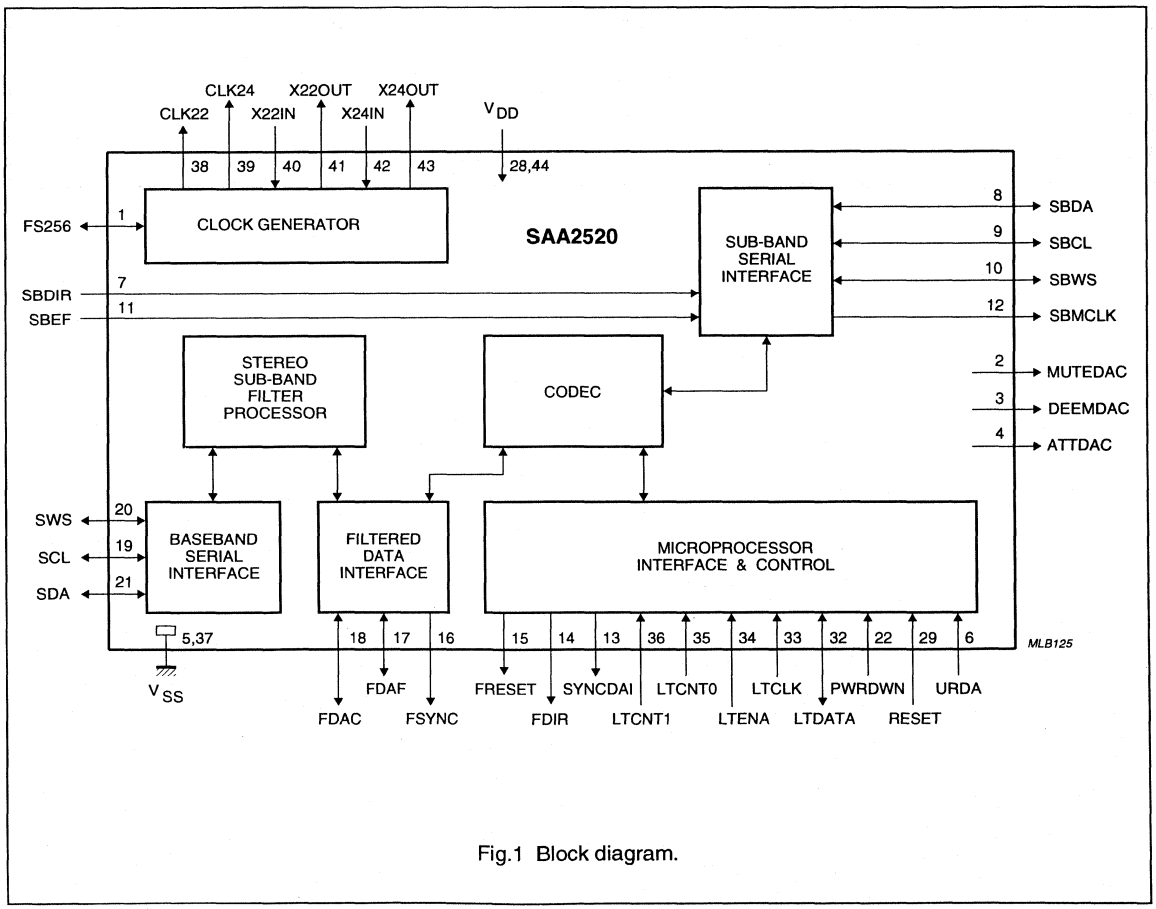


Fig.1 Block diagram.

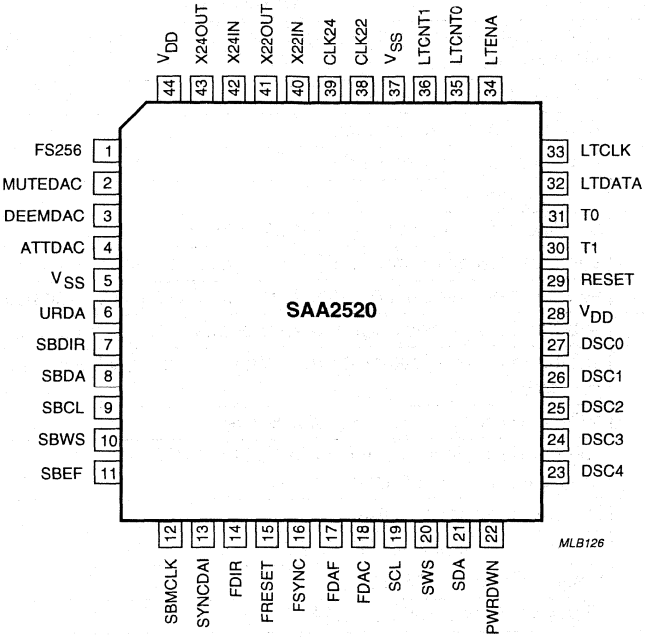


Fig.2 Pin configuration.

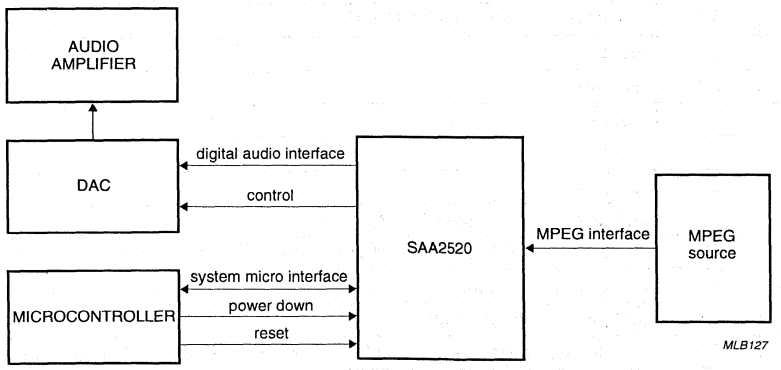


Fig.3 MPEG decoder system data flow diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
FS256	1	(Filtered)-I²S clock; 256 x sample frequency. 12 mA 3-state output + CMOS input with pull-down	I/O
MUTEDAC	2	DAC control/output expander	O
DEEMDAC	3	DAC control/output expander	O
ATTDAC	4	DAC control/output expander	O
V_{SS}	5	supply ground (0 V)	
URDA	6	unreliable drive processing data; CMOS level	I
SBDIR	7	sub-band I²S direction: (SWBS, SBCL, SBDA); CMOS level	I
SBDA	8	sub-band I²S data; 4 mA, 3-state output + CMOS input with pull-down	I/O
SBCL	9	sub-band I²S bit clock; 4 mA, 3-state output + CMOS input with pull-down	I/O
SBWS	10	sub-band I²S word select; 4 mA, 3-state output + CMOS input with pull-down	I/O
SBEF	11	sub-band I²S byte error flag; CMOS level	I
SBMCLK	12	sub-band I²S clock, 6.144 MHz locked to FS256; 8 mA, 3-state output + CMOS input with pull-down	O
SYNCDAI	13	DAI synchronization pulse	O
FDIR	14	(Filtered)-I²S direction: (FDAC, FDAF, SDA);	O
FRESET	15	reset signal for SAA2521	O
FSYNC	16	Filtered-I²S sync signal for SAA2521	O
FDAF	17	Filtered-I²S sub-band filter data; 4 mA, 3-state output + CMOS input with pull-down	I/O
FDAC	18	Filtered-I²S sub-band codec data; 4 mA, 3-state output + CMOS input with pull-down	I/O
SCL	19	I²S bit clock; 4 mA, 3-state output + CMOS input with pull-down	I/O
SWS	20	I²S-word select; 4 mA, 3-state output + CMOS input with pull-down	I/O
SDA	21	I²S baseband data filter; 4 mA, 3-state output + CMOS input with pull-down	I/O
PWRDWN	22	power-down mode; CMOS level	I
DSC4	23	test pin	
DSC3	24	test pin	
DSC2	25	test pin	
DSC1	26	test pin	
DSC0	27	test pin	
V_{DD}	28	positive supply voltage (+5 V)	
RESET	29	system reset; CMOS level with pull-down and hysteresis	I
T1	30	test pin; do not connect	
T0	31	test pin; do not connect	
LTDATA	32	LT interface data; 4 mA, 3-state output + CMOS input with pull-down	I/O
LTCLK	33	LT interface bit clock; CMOS level	I

SYMBOL	PIN	DESCRIPTION	TYPE
LTENA	34	LT interface enable; CMOS level	I
LTCNT0	35	LT interface control; CMOS level	I
LTCNT1	36	LT interface control; CMOS level	I
V_{SS}	37	supply ground (0 V)	
CLK22	38	22.5792 MHz buffered output	O
CLK24	39	24.576 MHz buffered output	O
X22IN	40	22.5792 MHz crystal input	I
X22OUT	41	22.5792 MHz crystal output	O
X24IN	42	24.576 MHZ crystal input	I
X24OUT	43	24.576 MHz crystal output	O
V_{DD}	44	positive supply voltage (+5 V)	

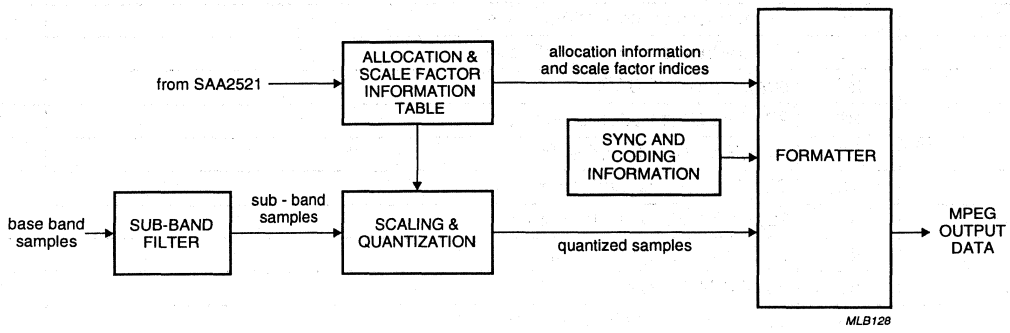


Fig.4 Encoding mode.

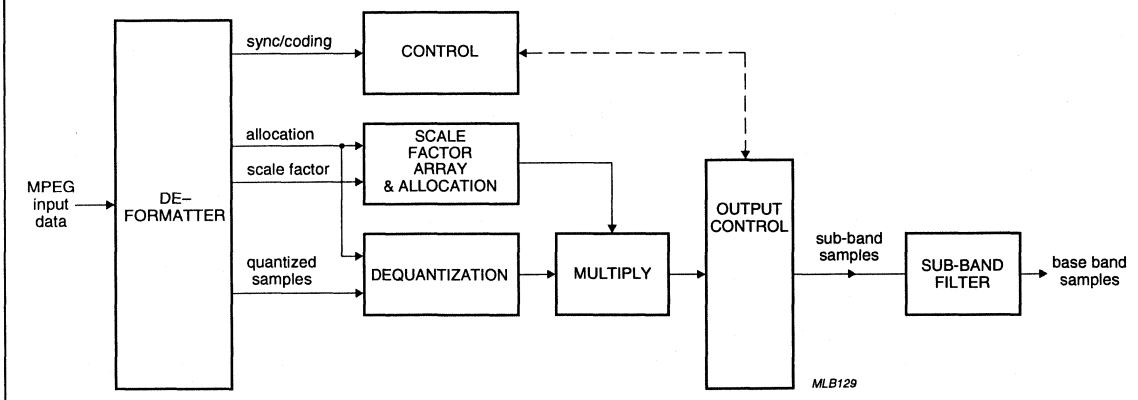


Fig.5 Decoding mode.

FUNCTIONAL DESCRIPTION

Coding System

MPEG coding achieves highly efficient digital encoding of audio signals by using an algorithm based on the characteristics of the human auditory system.

The broad-band audio signal is split into 32 sub-band signals during encoding. For each of the sub-band signals the masking threshold is calculated. The samples of the sub-bands are incorporated in the signal with an accuracy that is determined by the signal to masking threshold ratio for that sub-band.

During decoding, the sub-band signals are reconstructed and combined into a broadband audio signal. The integrated filter processor performs the splitting (encoding) and joining (decoding) including the corresponding formatting functions.

For encoding, a SAA2521 is necessary to calculate the masking threshold and required accuracy of the sub-band samples.

Encoding (See Fig.4)

An encoding algorithm table is used during the coding process but, due to the Adaptive Allocation functions of the SAA2521, this may change with every frame. The table is therefore calculated for each frame by the SAA2521 and then transferred to the SAA2520.

A frame contains 2 x 384 samples of Left and Right audio data. This results in 12 samples per sub-band (32 sub-bands). The samples of the greatest amplitude are used to determine the scale factor for a given sub-band. All samples are then scaled to represent a fraction of the greatest amplitude.

Once scaled, the samples are quantized to reduce the number of bits to correspond with the allocation table as calculated by the SAA2521. Synchronization and coding information data is then added to result in a fully encoded MPEG signal.

Decoding (See Fig.5)

All essential information (synchronization, system information, scale factors and encoded sub-band samples) are conveyed by incoming data. Decoding is repeated for every frame.

After sync and coding information, allocation data and the scale factors are used to correctly fill the scale factor array.

This is followed by a process of multiplication to provide de-quantization and de-scaling of the samples. The decoded sub-band samples, which are represented in 24-bit two's complement notation, are processed by the sub-band filters and reconstituted into a single digital audio signal.

RESET

Reset must be active under the following conditions:

1. From system power-up until CLK24 has executed more than 24 clock cycles.
2. From the falling edge of PWRDWN for a period equivalent to 24 cycles of CLK24 + oscillator start-up time. This is typically >1 ms, however, this value is crystal dependent.

PWRDWN

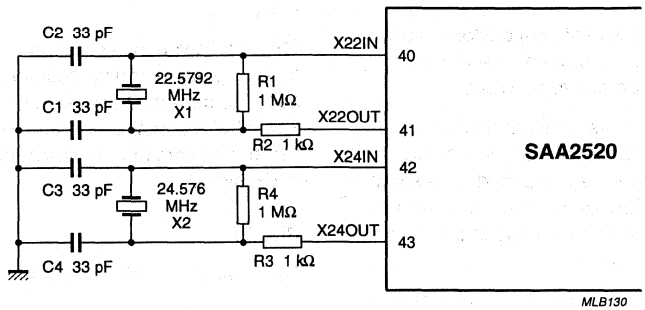
A HIGH input applied to this pin will halt all internally generated clock signals. As a result, chip activity will halt completely with outputs frozen in the state which was current at the time of PWRDWN activation.

The bi-directional outputs: LTDATA, FDAC, FDAF, SDA, SBWS, SBCL and SBDA will be 3-stated.

Crystal Oscillators

A 24.576 MHz crystal together with some external components form the 24.576 MHz oscillator (pins 42 and 43). Similarly a 22.5792 MHz oscillator (pins 40 and 41) is formed by similar peripheral components together with an appropriate crystal (see Fig.6).

The component values shown apply only to crystals from the Philips 4322 156 series which exhibit an equivalent series resistance of $\leq 40\ \Omega$.



Component values apply only to crystals from the Philips 4322 156 series.

Fig.6 Crystal oscillator components.

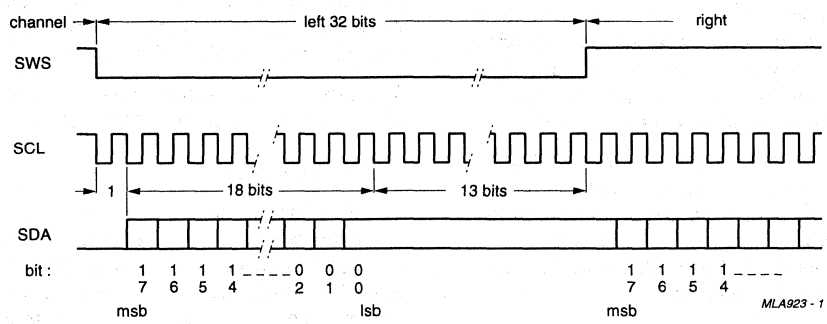


Fig.7 Transfer of SDA data (Standard I²S default format).

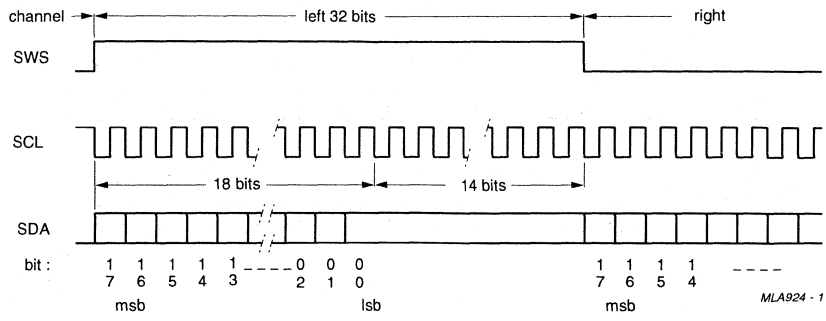


Fig.8 Transfer of SDA data (alternative format).

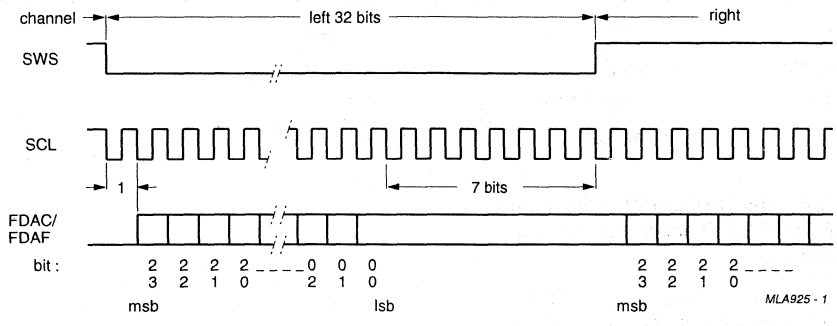


Fig.9 Transfer of FDAF and FDAC (filtered) data.

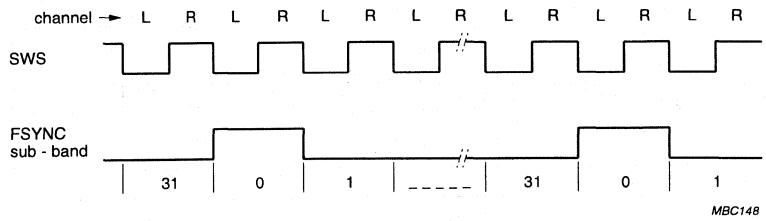


Fig.10 SWS related to phase of FSYNC.

Baseband Interface Signals

The interface between the SAA2520 and the baseband input/output circuitry consists of the following signals:

SWS	bi-directional	word (channel) select	FS
SCL	bi-directional	bit clock	64FS
SDA	bi-directional	baseband data	
FDIR	output	decoding mode (direction control)	

The SWS signal indicates the channel of the sample signal (either LEFT or RIGHT) and is equal to the sampling frequency FS.

Operating at a frequency of 64 times that used for sampling, the bit clock dictates that each SWS period contains 64 SDA data bits. Of these, a maximum of 36 are used to transfer data (samples may have a length up to 18-bits). Samples are transferred most significant bit first. Both SWS and SDA change state at the negative edge of SCL.

This baseband data is transferred between the SAA2520 and the input/output using either Standard I²S (default) or the alternative format shown in Fig.8.

Interface between SAA2520 and SAA2521 consists of the following signals:

FILTERED-I²S INTERFACE

SWS	bi-directional	word select (common to I²S)	FS
SCL	bi-directional	bit clock (common to I²S)	64FS
FDAC	bi-directional	codec data	
FDAF	bi-directional	filter data	
FSYNC	output	synchronization	FS/32

Filtered data is transferred between SAA2520 filter/codec functions and the SAA2521 using the format shown in Fig.9.

The frequency of the SWS signal is equal to the sample frequency FS and the bit clock SCL is 64 times the sample frequency. Each period of SWS contains 64 data-bits, 48 of which are used to transfer data. The half period in which SWS is LOW is used to transfer the information of the LEFT channel while the following half period during which SWS is HIGH carries the data of the RIGHT channel. The 24-bit samples are transferred most significant bit first. This bit is transferred in the bit clock period with a 1-bit delay following the change in SWS. Both SWS and FDAF/FDAC change state at the negative edge of SCL.

The SAA2521 may be synchronized to the sub-band codec using the FSYNC signal, which defines the SWS period in which the samples of sub-band 0 (containing the lowest frequency components) are transferred (see Fig. 10).

SAA2521 AND INPUT/OUTPUT MODE CONTROL

The operation of SAA2521 and the input/output circuitry is controlled by three signals shown in Table 1.

FRESET and SYNCDAI are given whenever:

- FS256, SCL and SWS outputs switch between high and low impedance
- FS256 frequency is changed (12.288/11.2896/8.192 MHz)
- FDIR is switching
- bit rate is changing
- system reset is active

MPEG CODED INTERFACE

The interface that carries the MPEG coded signal uses the following signals:

The MPEG I²S interface

SBWS	bi-directional	word selection
SBCL	bi-directional	bit clock
SBDA	bi-directional	sub-band coded data
SBEF	input	error signal

Operation is further controlled by:

SBDIR	input	direction of data flow
URDA	input	unreliable encoded data signal

The SBMCLK signal is the main frequency from which other clock signals are derived. In encode mode this division is performed internally. In decode mode the external source should provide SBWS and SBCL. The frequency of the signal is equal to 1/32nd of the bit rate. The frequency of the bit clock SBCL is twice that of the bit rate. Some examples of the frequencies are given in Table 2.

Table 1 SAA2521 input/output control.

FRESET	output	request a general reset of SAA2521
FDIR	output	'1' for decoding and '0' for encoding mode (common to I²S)
SYNCDAI	output	pulse for synchronization of digital input/output (TDA1315)

Table 2 Frequency examples.

BIT RATE (k BITS/s)	SBWS FREQUENCY (kHz)	SBCL FREQUENCY (kHz)
384	12	768
256	8	512
192	6	384
128	4	256

ENCODE MODE

The following modes are supported:

Stereo or 2-channel mono with allowable bit rates of 384, 256, 192 and 128 kbits/s; audio sampling frequencies of 48, 44.1 and 32 kHz.

DECODE MODE

The following modes are supported:

Stereo and joint stereo, 2-channel mono and 1-channel mono with allowable bit rates in the range 448 to 32 k bits/s; audio sampling frequencies of 48, 44.1 and 32 kHz.

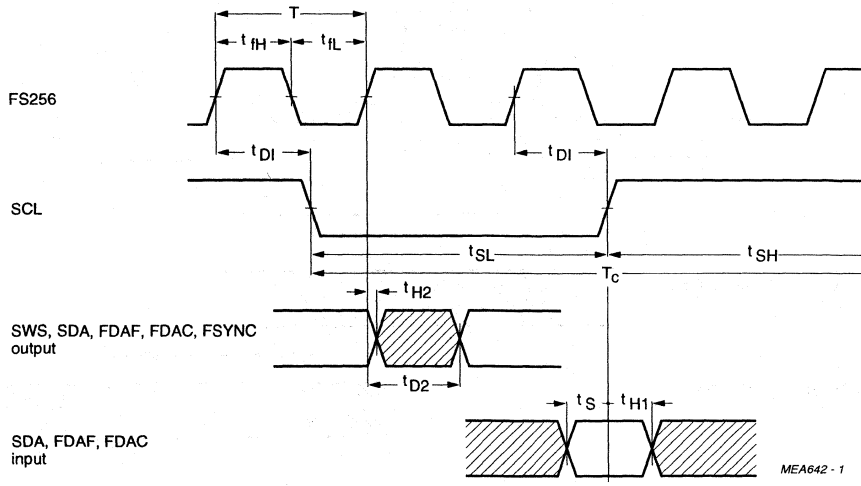


Fig.11 (Filtered)-I²S interface timing (master mode - FS256, SCL and SWS are output).

Notes to Fig.11

T	FS256 cycle time (f_s = 48 kHz)	81.4 ns nominal
	FS256 cycle time (f_s = 44.1 kHz)	88.6 ns nominal
	FS256 cycle time (f_s = 32 kHz)	122.1 ns nominal
T_c	SCL cycle time	4T ns nominal
t_{fH}	FS256 HIGH time (f_s = 48 kHz)	≥ 35 ns
	FS256 HIGH time (f_s = 44.1 kHz)	≥ 38 ns
	FS256 HIGH time (f_s = 32 kHz)	≥ 35 ns
t_{fL}	FS256 LOW time (f_s = 48 kHz)	≥ 35 ns
	FS256 LOW time (f_s = 44.1 kHz)	≥ 38 ns
	FS256 LOW time (f_s = 32 kHz)	≥ 75 ns
t_{SH}	SCL HIGH time	≥ 2T - 20 ns
t_{SL}	SCL LOW time	≥ 2T - 20 ns
t_S	SDA, FDAF, FDAC input set-up before FS256 HIGH	≥ 20 ns
t_{H1}	SDA, FDAF, FDAC input hold after FS256 HIGH	≥ 30 ns
t_{H2}	SDA, FDAF, FDAC output hold after FS256 HIGH	≥ 0 ns
$t_{D1, 2}$	FS256 HIGH to SCL, SWS, SDA, FDAF, FDAC output valid	≤ 50 ns

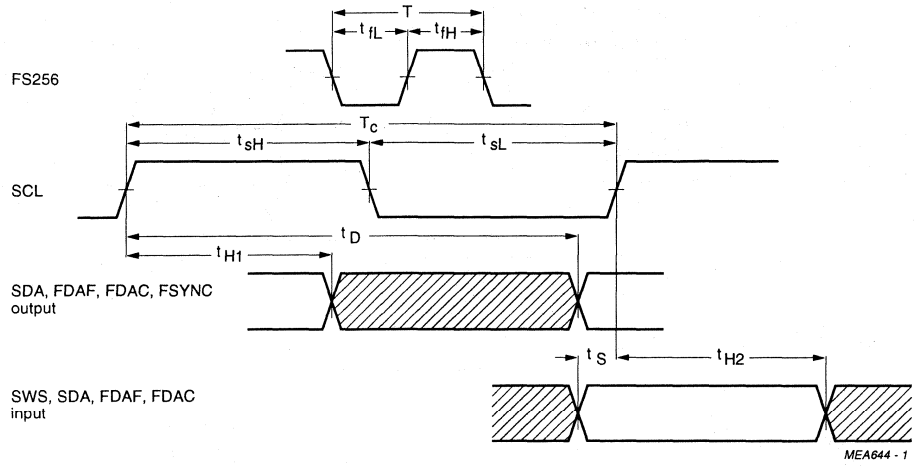


Fig.12 Filtered I²S interface timing (slave mode - FS256, SCL and SWS are input).

Notes to Fig.12

t_{fH}	FS256 HIGH time	≥ 35 ns
t_{fL}	FS256 LOW time	≥ 35 ns
t_{sH}	SCL HIGH time	≥ T + 35 ns
t_{sL}	SCL LOW time	≥ T + 35 ns
t_{H1}	SDA, FDAF, FDAC output hold after SCL HIGH	≥ 2T - 15 ns
t_D	SCL HIGH to SDA, FDAF FDAC output valid	≤ 3T + 60 ns
t_s	SDA, FDAF, FDAC input valid after SCL HIGH	≥ 20 ns
t_{H2}	SDA, FDAF, FDAC input hold after SCL HIGH	≥ T + 20 ns

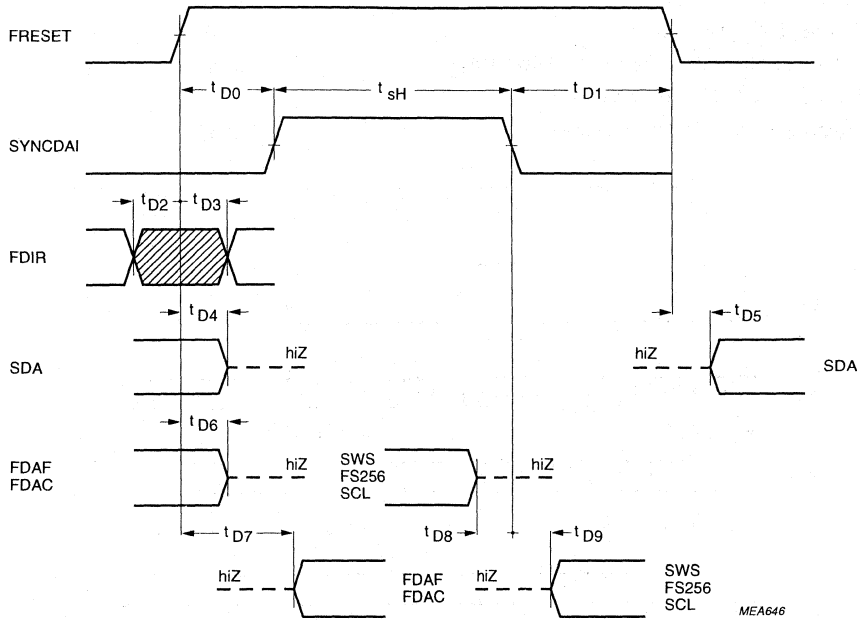


Fig.13 Mode switch timing.

Notes to Fig.13

t_{DO}	FRESET HIGH to SYNCDAI HIGH	≥ 300 ns
t_{SH}	SYNCDAI HIGH time	≥ 1280 ns
t_{D1}	SYNCDAI LOW to FRESET LOW	≥ 790 ns
t_{D2}	FDIR hold to FRESET HIGH	≤ 20 ns
t_{D3}	FRESET HIGH to FDIR valid	≤ 20 ns
t_{D4}	SDA change to high impedance	
	after FRESET HIGH	≥ 0 ns
		≤ 170 ns
t_{D5}	SDA remains high impedance	
	after FRESET LOW	≥ 0 ns
		≤ 170 ns
t_{D6}	FDAF, FDAC change to high impedance	
	after FRESET HIGH	≤ 20 ns
t_{D7}	FDAF, FDAC remain high impedance	

Notes to Fig.13

	after FRESET HIGH	≥ 460 ns
t_{D8}	FS256, SWS, SCL change to high impedance before SYNCDAI HIGH	≥ 140 ns
t_{D9}	FS256, SWS, SCL remain HIGH impedance after SYNCDAI HIGH	≥ 140 ns

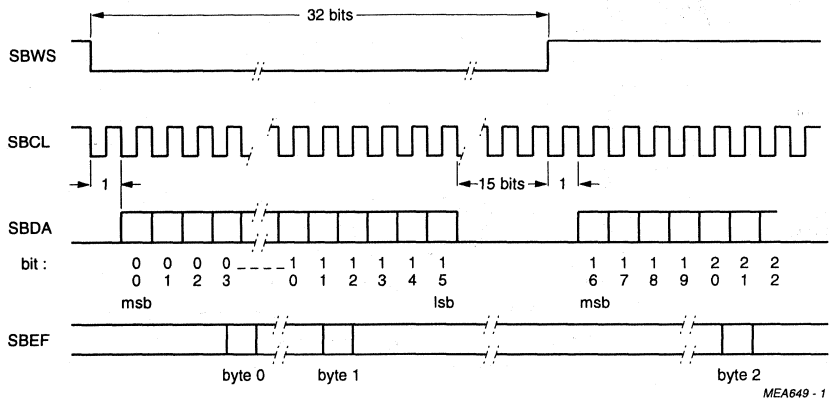


Fig.14 Transferring MPEG data to and from the SAA2520.

MPEG Coded Interface (Sub-band I²S)

The MPEG coded data is transferred to and from the SAA2520 using the format shown in Fig.14.

Each period of SBWS contains 64 data bits, 32 of which are used to convey data. The half-period during which SBWS is logic 0 is used to transfer the first 16-bits (0 to 15) of a sub-band slot. The remaining half-period during which SBWS is logic 1 carries the remaining 16-bits (16 to 31). Thus one period of SBWS corresponds with one slot of the sub-band signal.

Bits 0 and 16 are transferred in the bit clock period, one bit-time after the change in SBWS. Both SBWS and SBDA change state during the negative edge of SBCL.

In decode mode a byte error flag SBEF is also transferred. This occurs approximately in the middle of the corresponding byte (byte 0 = bits 0 to 7, byte 1 = bits 8 to 15 etc).

Encoding mode

SBCL, SBWS and SBDA are generated by the SAA2520. However, if the SBDIR signal is logic 1, the output buffers are not enabled and these signals do not appear on the pins. This mode is available to permit a change of operating mode whilst the bus signals are driven from an external source.

Decoding mode

SBCL, SBWS and SBDA are generated by an external source.
Table 3 contains a summary of the source signals in the various modes.

Table 3 Modes and source signals.

			source of:					
Mode	**FDIR**	**SBDIR**	**SBWS**	**SBCL**	**SBDA**	**SBEF**	**SBMCLK**	
Encode	0	0	INT	INT	INT	----	INT	note 1
Encode	0	1	EXT	EXT	EXT	----	INT	note 2
Decode	1	0	INT	INT	INT	EXT	INT	note 3
Decode	1	1	EXT	EXT	EXT	EXT	INT	

Notes

1. During encoding the SBEF signal is 'don't care'
2. Incoming data is not decoded. The SAA2520 operates in the encoding mode and the data does not enter the interface.
3. Operation is undefined. The SAA2520 is in decoding mode whilst the SBWS, SBCL and SBDA output drivers are enabled.

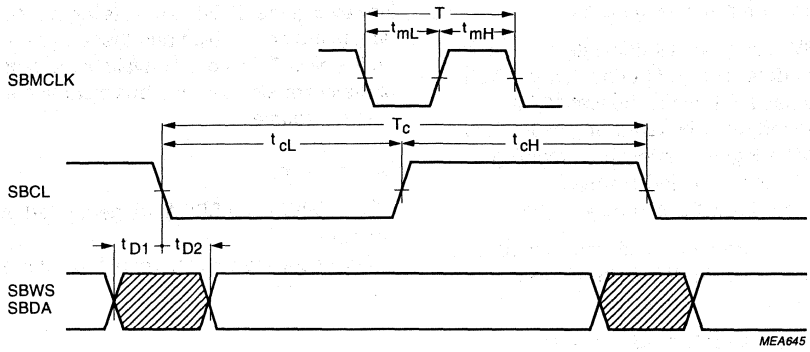


Fig.15 Sub-band I²S interface timing (master mode - SBCL, SBWS and SBDA are output).

Notes to Fig.15

T	SBMCLK cycle time	120 to 205 ns (163 ns nominal)
t_{mH}	SBMCLK HIGH time	≥ 35 ns
t_{mL}	SBMCLK LOW time	≥ 75 ns
T_c	SBCL cycle time (384 kB/s)	8T ns nominal
	SBCL cycle time (256 kB/s)	12T ns nominal
	SBCL cycle time (192 kB/s)	16T ns nominal
	SBCL cycle time (128 kB/s)	24T ns nominal
t_{CH}	SBCL HIGH time (384 kB/s)	≥ 4T - 20 ns
	SBCL HIGH time (256 kB/s)	6T - 20 ns
	SBCL HIGH time (192 kB/s)	≥ 8T - 20 ns
	SBCL HIGH time (128 kB/s)	≥ 12T - 20 ns
t_{CL}	SBCL LOW time (384 kB/s)	≥ 4T - 20 ns
	SBCL LOW time (256 k/Bs)	≥ 6T - 20 ns
	SBCL LOW time (192 kB/s)	≥ 8T - 20 ns
	SBCL LOW time (128 kB/s)	≥ 12T - 20 ns
t_{D1}	SBWS, SBDA hold to SBCL LOW	≤ 20 ns
t_{D2}	SBCL LOW to SBWS, SBDA valid	≤ 20 ns

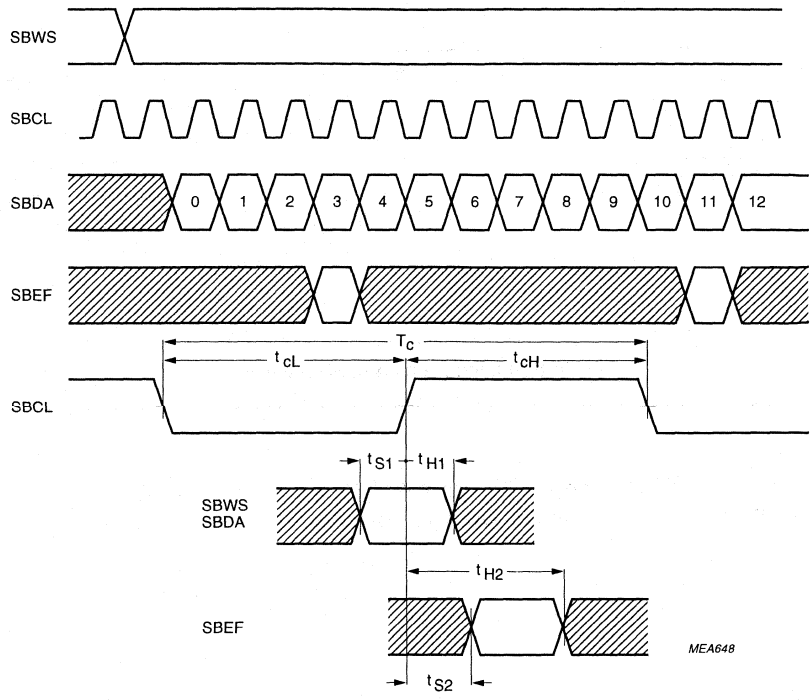


Fig.16 Sub-band I²S interface timing (slave mode - SBCL, SBWS and SBDA are input).

Notes to Fig.16

T_C	SBCL cycle time (see note 1)	6.86T to 96T ns (8T ns nominal)
t_{CH}	SBCL HIGH time	≥ T + 30 ns
t_{CL}	SBCL LOW time	≥ T + 30 ns
t_{S1}	SBWS, SBDA input set-up before SBCL HIGH	≥ T + 30 ns
t_{H1}	SBWS, SBDA input hold after SBCL HIGH	≥ 30 ns
t_{S2}	SBCL HIGH to SBEF valid	≤ T - 30 ns
t_{H2}	SBEF hold after SBCL HIGH	≥ 2T - 30 ns

Note 1:
Minimum at bit rate = 448 kB/s
Nominal at bit rate = 384 kB/s
Maximum at bit rate = 32 kB/s

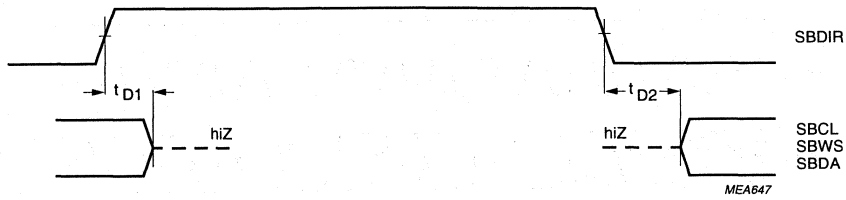


Fig.17 Sub-band I²S mode switch timing.

Notes to Fig.17

t_{D1}	SBDIR HIGH to SBCL, SBWS, SBDA high impedance	≤ 50 ns
t_{D2}	SBCL, SBWS, SBDA after SBDIR LOW high impedance	≥ 240 ns

Microcontroller interface

The SAA2520 has an interface connection to the serial interface of a microcontroller. The following signals are used:

LTCLK	input	bit clock
LTDATA	bi-directional	serial data
LTCNT0	input	control line 0
LTCNT1	input	control line 1
LTENA	input	enable

The SAA2520 microcontroller interface is enabled only if LTENA (pin 34) is logic 1. Information to or from the SAA2520 is conveyed in serial 8 or 16-bit units, whilst the type of information is controlled by LTCNT0 (pin 35) and LTCNT1 (pin 36).

A transfer commences when the microcontroller sets the control lines to the correct combination for the required action. LTENA is set to logic 1. The SAA2520 determines its required action and prepares to transfer data. When the microcontroller supplies the LTCLK, data is transferred to or from the SAA2520 in units of 8-bits. 16-bit transfers are conveyed as two 8-bit units during which LTENA remains high.

During the transfer of 8-bit units, the least significant bit is first to be transferred. When 16-bit units are transferred the most significant byte is sent first.

EXTENDED SETTINGS (LTCNT1 = 0, LTCNT0 = 0)

Four information bits together with four address bits are transferred in this mode. The order in which the bits appear on the interface is:

D0..D1..D2..D3..A0..A1..A2..A3

Table 4 Extended Settings.

BIT A3	BIT A2	BIT A1	BIT A0	DESCRIPTION
0	0	0	0	CODEC external settings (see Table 5)
0	0	0	1	FILTER settings (see note 1)
0	0	1	0	not used
..	..	..	..	..
1	1	1	1	not used

Table 5 Extended Settings.

BIT	DESIGNATION	DEFAULT	FUNCTION
D0	MUTEDAC	1	connected to DAC mute input
D1	ATTDAC	0	connected to DAC attenuation input
D2	DEEMDAC	0	emphasis control for DAC circuit
D3	HOLDCLKOK	0	selects CLKOK hold mode

Note

If not used for DAC control, the MUTEDAC, ATTDAC and DEEMDAC can be used as general purpose output expanders.

Bits D0 to D3 are copied directly to the corresponding output pins/mode flip-flop.

For HOLDCLKOK = logic 1. When CLKOK drops it will remain LOW until set by an encode/decode mode, sample frequency, external 256FS or bit rate index change.

Note 1.

When D0 = logic 1 (default) I²S mode is selected. For D0 = logic 0 the alternative mode is selected. The setting of D0 remains dormant until activated by the occurrence of FRESET.

ALLOCATION/SCALE FACTOR INFORMATION (LTCNT1 = LOGIC 0, LTCNT0 = LOGIC 1)

For encoding, the allocation and scale factor arrays can be filled using this mode. To completely fill the allocation array 16 complete transfers of 16-bits are required. After the first transfer of allocation information a check must be made to determine when the SAA2520 is ready to receive the remaining information. This will ensure synchronization with the internal program of the SAA2520. Transfer of the allocation information is completed by sending the internal settings.

This is then followed by the scale factor information.

In the event that only internal settings information is sent, then a default allocation of logic 0 will be assigned to all sub-bands. If in addition no internal settings are sent then the previous settings remain valid.

The allocation information is transferred in 4-bit units. Each of these units contains the number of bits allocated to the sub-band, MINUS 1, except in the case of a logic 0 value, which indicates that no bits are allocated to that sub-band.

Scale factor information is transferred in units of 8-bits, containing the 6-bit scale factor which is extended to 8-bits by adding two logic 0's at the most significant end.

In the case of stereo encoding the channels are indicated by L (left) and R (right). This changes to I and II in the case of 2 channel mono encoding.

Table 6 Allocation information format.

msb						lsb	channel	sub-band
B15	-	B14	-	B13	-	B12	L or I	0 .. 30 (even)
B11	-	B10	-	B9	-	B8	R or II	0 .. 30 (even)
B7	-	B6	-	B5	-	B4	L or I	1 .. 31 (odd)
B3	-	B2	-	B1	-	B0	R or II	1 .. 31 (odd)

Table 7 Scalefactor information format.

msb	bits	lsb	channel	sub-band
B15	.....	B8	L or I	0 .. 31
B7	.....	B0	R or II	0 .. 31

INTERNAL SETTINGS (LTCNT1 = LOGIC 1, LTNCT 0 = LOGIC 0)

The operation of the codec is controlled by the bits transferred in this mode.

Table 8 Internal Settings (LTCNT1 = logic 1, LTNCT 0 = logic 0).

msb		lsb	name	function	valid in
S15	...	S12	bit rate index	bit rate indication	encode
S11	...	S10	sample frequency	44.1, 48 or 32 kHz indication	encode
S9			decode	1 = decode; 0 = encode	encode/decode
S8			EXT 256FS	1 = external; 0 = internal 256FS	encode/decode
S7			2-channel mono	1 = 2-CH mono; 0 = stereo	encode
S6			MUTE	1 = mute; 0 = no mute	encode/decode
S5				not used	
S4			CH1	1 = CH1; 0 = CH2	decode
S3	...	S2	Tr0 to Tr1	transparent bits	encode
S1	...	S0	EMPHASIS	emphasis indication	encode

Table 9 Internal Settings (LTCNT1 = logic 1, LTCNT0 = logic 0).

msb			lsb	bit rate	
1	1	0	0	384 kbits/s	default value
1	0	0	0	256 kbits/s	
0	1	1	0	192 kbits/s	
0	1	0	0	128 kbits/s	

The bit rate index indicates the bit rate of the encoded signal and is only effective in the encode mode.

The decode bit determines the operation mode of the SAA2520. The default value is logic 1 (decoding mode).

EXT 256FS in the encoding mode determines whether or not the SAA2520 is master or slave of the Filtered-I²S interface (default is logic 0, master mode).

2CH MONO is used in the encoding mode to determine whether the sub-band signal is generated as a stereo or 2-channel mono signal. Default value is logic 0.

MUTE is used in both the encoding and decoding modes to mute the information to or from the Filtered-I²S interface (the default value is logic 0).

CH1 is utilized in the decoding mode to select one of the 2-channel mono signals to be decoded (default is I - channel 1). A value of 0 results in channel 2 being decoded).

The transparent bits are copied in the sub-band signal, default is 00.

The information from S15 to S10, S7 and S3 to S0 will be copied into the sub-band signal.

Table 10 Sample frequency indication.

msb	lsb	sample frequency	
0	0	44.1 kHz	default value
0	1	48 kHz	
1	0	32 kHz	
1	1	not used	

Table 11 EMPHASIS indication.

msb	lsb	emphasis	
0	0	no emphasis	default value
0	1	50/15 μs	
1	0	reserved	
1	1	CCITT J.17	

Before sending internal settings the microcontroller should check whether or not the SAA2520 is ready-to-receive. However, this does not apply for the transfer of internal settings to end a transfer of allocation information.

STATUS (LTCNT = LOGIC 1, LTNCT0 = LOGIC 1)

Table 12 Status information 16-bit units.

msb		lsb	name	function	valid in
T15	...	T12	bit rate index	bit rate indication	encode/decode
T11	...	T10	sample frequency	44.1, 48 or 32 kHz indication	encode/decode
T9			ready-to-receive	1 = ready; 0 = not ready	encode/decode
T8			not used		
T7		T6	MODE	sub-band signal mode indication	encode/decode
T5			SYNC	synchronization indication	decode
T4			CLKOK	1 = o.k.; 0 = not o.k.	encode/decode
T3		T2	Tr0 to Tr1	transparent bits	encode/decode
T1	...	T0	EMPHASIS	emphasis indication	encode/decode

The bit rate index indicates the bit rate of the sub-band signal in units of 32 kbits/s. bit rate index 0000 indicates the 'free format' condition. bit rate 1111 is illegal and should not be found.

The coding of the sample frequency indication is equal to the one in the internal settings.

Table 13 MODE identification.

msb	lsb	mode	output
0	0	stereo	L and R
0	1	joint stereo	L and R
1	0	2 channel mono	I or II as selected
1	1	1 channel mono	mono; no selection

Ready-to-receive indicates whether the SAA2520 is ready to receive allocation, scale factor or internal setting transfers. This should be checked in order to synchronize the transfer of such information.

In 2 channel mono decode mode the selected samples are transferred to both output channels. The same occurs with all samples in 1-channel mono decode mode. In both of these instances the L and R filter output channels are identical.

In decode mode the SYNC bit is logic 0 when the SAA2520 is unable to decode the sub-band frames. This will occur in the following situations:

- with the loss of synchronization
- when incorrect allocation information is received for two or more subsequent frames (SBEF was HIGH).
- when the URDA input pin is HIGH

In these situations the SAA2520 data output will be muted. The SYNC bit will return to logic 1 as soon as the decoder is resynchronized to the incoming sub-band data.

CLKOK indicates whether the 256FS clock corresponds to specified sample frequency. The CLKOK bit is set to logic 1 after a change in sample frequency, operation mode or EXT256FS setting. It drops to logic 0 as soon as the 256FS clock deviates from the nominal frequency by more than approximately 0.2%. Return to logic 1 will only occur automatically when the extended setting CLKOK-hold-mode is logic 0.

The transparent bits are copied from the MPEG coded signal.

The EMPHASIS indication is as defined in the internal settings. It can be used to apply the correct de-emphasis.

Note: the two bytes of the status are 'sampled' at different moments so the information may not result from the same sub-band frame.

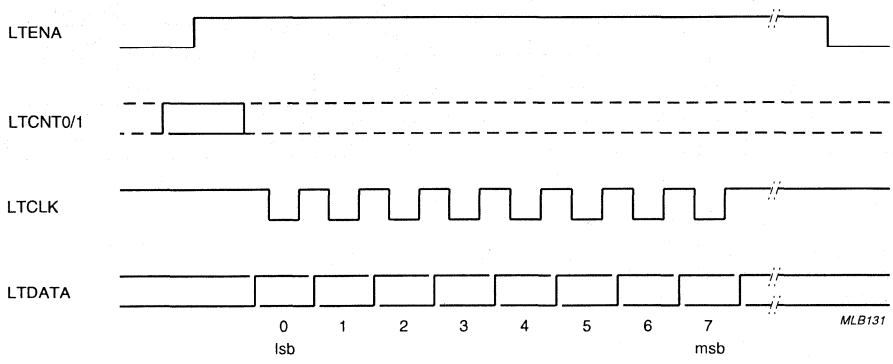


Fig.18 Transfer of data on SAA2520 microcontroller interface.

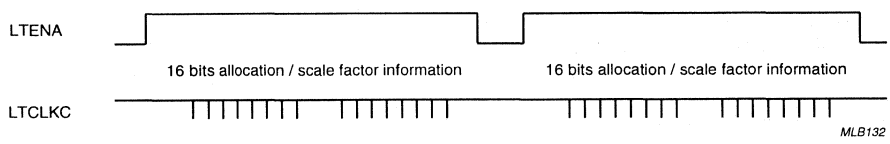


Fig.19 The LTENA line must return to logic 0 between information transfers.

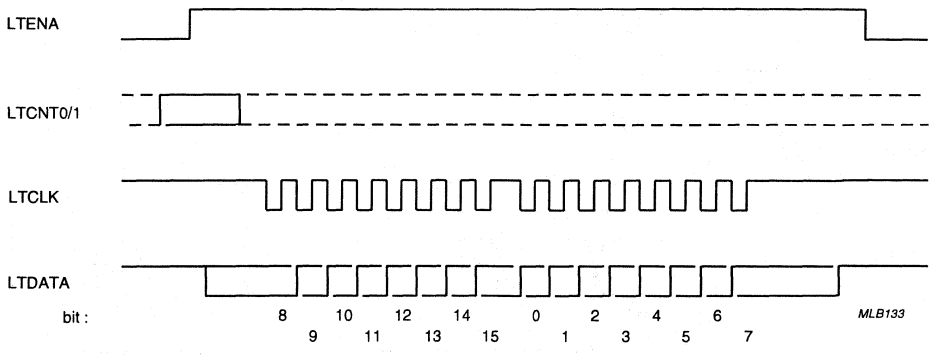
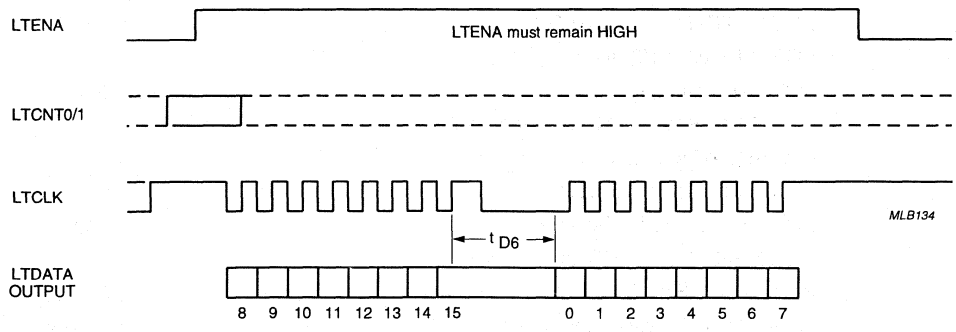


Fig.20 Order of settings and status bits on the SAA2520 microcontroller interface.



t_{D6} delay LTCLK HIGH to LTDATA valid output for bit 0 in 16-bit transfers

Fig.21 16-bit transfers.

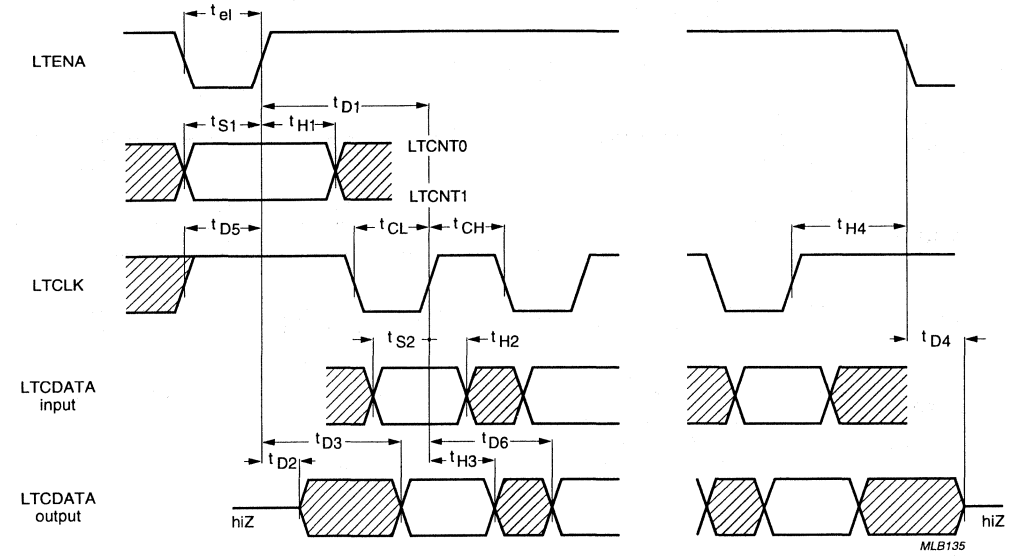


Fig.22 Microcontroller interface timing.

Notes to Fig.22

t_{eL}	LTENA LOW time	≥ 190 ns
t_{CH}	LTCLK HIGH time	≥ 190 ns
t_{CL}	LTCLK LOW time	≥ 190 ns
t_{D1}	LTENA HIGH to LTCLK HIGH	≥ 190 ns
t_{D2}	LTENA HIGH to LTDATA output low impedance	≥ 0 ns
t_{D3}	LTENA HIGH to LTDATA output valid	≤ 380 ns
t_{D4}	LTENA LOW to LTDATA high impedance	≤ 50 ns
t_{H4}	LTENA hold after LTCLK HIGH	≥ 355 ns
t_{D5}	LTCLK HIGH to LTENA HIGH	≥ 190 ns
t_{D6}	LTCLK HIGH to LTDATA output valid for bit 0 (see Fig.21)	≤ 355 ns
	for first bit in the second 8-bit unit	≤ 520 ns
t_{S1}	LTCNT0/1 set-up before LTENA HIGH	≥ 190 ns
t_{H1}	LTCNT0/1 hold after LTENA HIGH	≥ 190 ns
t_{S2}	LTDATA set-up before LTCLK HIGH	≥ 190 ns
t_{H2}	LTDATA input hold after LTCLK HIGH	≥ 30 ns
t_{H3}	LTDATA output hold after LTCLK HIGH	≥ 145 ns
t_{H4}	LTENA hold after LTCLK HIGH	≥ 355 ns

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	6.5	V
V_I	input voltage	note 1	−0.5	V_{DD} + 0.5	V
I_{SS}	supply current from V_{SS}		–	160	mA
I_{DD}	supply current in V_{DD}		–	160	mA
I_I	input current		−10	10	mA
I_O	output current		−20	20	mA
P_{tot}	total power dissipation		–	880	mW
T_{stg}	storage temperature range		−55	150	°C
T_{amb}	operating ambient temperature range		- 40	85	°C
V_{es1}	electrostatic handling	note 2	−1500	1500	V
V_{es2}	electrostatic handling	note 3	−70	70	V

Notes

1. Input voltage should not exceed 6.5 V unless otherwise specified
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor
3. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

DC CHARACTERISTICS

T_{amb} = −40 to 85 °C; V_{DD} = 3.8 to 5.5 V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		3.8	5.0	5.5	V
I_{DD}	operating current	V_{DD} = 5 V (note 1)	–	82	110	mA
I_{DD}	operating current	V_{DD} = 3.8 V (note 1)	–	58	80	mA
Inputs URDA, SBDIR, SBEF, LTCLK, LTCNT0, LTNCT1, X22IN, X24IN						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
$-I_I$	input current	V_i = 0 V; T_{amb} = 25 °C	–	–	10	µA
$+I_I$	input current	V_i = 5.5 V; T_{amb} = 25 °C	–	–	10	µA
Inputs PWRDWN, LTENA						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
$+I_I$	input current	$V_i = V_{DD}$; T_{amb} = 25°C	40	–	250	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input RESET						
V_{tlh}	positive-going threshold		–	–	$0.8V_{DD}$	V
V_{thl}	negative-going threshold		$0.2V_{DD}$	–	–	V
V_{hys}	hystersis	$(V_{tlh} - V_{thl})$	–	1.5	–	V
$+I_I$	input current	$V_i = V_{DD}$; $T_{amb} = 25°C$	40	–	250	µA
Outputs MUTEDAC, DEEMDAC, ATTDAC, SYNCDAI, FDIR, FRESET, FSYNC, CLK22						
V_{OH}	HIGH level output voltage	$+I_o = 2$ mA	V_{DD}-0.5	–	–	V
V_{OL}	LOW level output voltage	$-I_o = 2$ mA	–	–	0.4	V
Outputs CLK24						
V_{OH}	HIGH level output voltage	$+I_o = 8$ mA	V_{DD}-0.5	–	–	V
V_{OL}	LOW level output voltage	$-I_o = 8$ mA	–	–	0.4	V
Inputs/outputs SBDA, SBCL, SBWS, FDAF, FDAC, SCL, SWS, SDA, LTDATA						
V_{OH}	HIGH level output voltage	$+I_o = 2$ mA	V_{DD}-0.5	–	–	V
V_{OL}	LOW level output voltage	$-I_o = 2$ mA	–	–	0.4	V
Outputs SBDA, SBCL, SBWS, FDAF, FDAC, SCL, SWS, SDA, LTDATA in 3-state						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
I_I	input current	$V_i = V_{DD}$; $T_{amb} = 25°C$	40	–	250	µA
Input/output SBMCLK						
V_{OH}	HIGH level output voltage	$+I_o = 8$ mA	V_{DD}-0.5	–	–	V
V_{OL}	LOW level output voltage	$-I_o = 8$ mA	–	–	0.4	V
Output SBMCLK in 3-state						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
I_I	input current	$V_i = V_{DD}$; T_{amb} 25°C	40	–	250	µA
Input/output FS256						
V_{OH}	HIGH level output voltage	$+I_o = 12$ mA	V_{DD}-0.5	–	–	V
V_{OL}	LOW level output voltage	$-I_o = 12$ mA	–	–	0.4	V
Output FS256 in 3-state						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
I_I	input current	$V_i = V_{DD}$; $T_{amb} = 25$ °C	40	–	250	µA

Note

1. For load impedances representative of the application.

AC CHARACTERISTICS

T_{amb} = −40 to 85 °C; V_{DD} = 3.8 to 5.5 V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
C_I	input capacitance		–	–	10	pF
X24IN and X22IN						
f	crystal frequency at X22OUT, CLK22	note 1	21	22.5792	24	MHz
f	crystal frequency at X24OUT, CLK24	note 1	23	24.576	26	MHz
gm	mutual conductance	100 kHz	1.5	–	–	mA/V
A_v	small signal gain	$A_v = gm.R_o$	3.5	–	–	V/V
C_{fb}	feedback capacitance		–	–	5	pF
C_O	output capacitance		–	–	10	pF
Outputs						
C_O	output capacitance		–	–	10	pF
Inputs URDA, RESET, LTDATA, LTCLK, LTENA, LTCNT0, LTCNT1						
t_{SU}	setup time to X24IN		15	–	–	ns
t_{HD}	hold time to X24IN		60	–	–	ns
Outputs LTDATA, MUTEDAC, DEEMDAC, ATTDAC, SYNCDAI, FDIR, FRESET						
t_d	propagation delay from X24IN		–	–	80	ns
Inputs FDAF, FDAC, SDA, SCL, SWS						
t_{SU}	setup time to FS256		15	–	–	ns
t_{HD}	hold time to FS256		25	–	–	ns
Outputs FDAF, FDAC, SDA, SCL, SWS, FSYNC						
t_d	propagation delay from FS256		–	–	50	ns
Inputs SBDA, SBCL, SBWS, URDA, SBDIR, SBEF						
t_{SU}	setup time to SBMCLK		15	–	–	ns
t_{HD}	hold time to SBMCLK		25	–	–	ns
Outputs SBDA, SBCL, SBWS						
t_d	propagation delay from SBMCLK		–	–	50	ns
FS256						
T	FS256 cycle time	f_s = 48 kHz	–	81.4	–	ns
T	FS256 cycle time	f_s = 44.1 kHz	–	88.6	–	ns
T	FS256 cycle time	f_s = 32 kHz	–	122.1	–	ns
T_C	SCL cycle time		–	4T	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FS256 master mode (FS256,SCL and SWS are output)						
t_{fH}	FS256 HIGH time	f_s = 48 kHz	35	–	–	ns
t_{fH}	FS256 HIGH time	f_s = 44.1 kHz	38	–	–	ns
t_{fH}	FS256 HIGH time	f_s = 32 kHz	75	–	–	ns
t_{fL}	FS256 LOW time	f_s = 48 kHz	35	–	–	ns
t_{fL}	FS256 LOW time	f_s = 44.1 kHz	38	–	–	ns
t_{fL}	FS256 LOW time	f_s = 32 kHz	75	–	–	ns
t_{sH}	SCL HIGH time		2T-20	–	–	ns
t_{sL}	SCL LOW time		2T-20	–	–	ns
t_s	SDA, FDAF, FDAC input setup time before FS256 HIGH		20	–	–	ns
t_{H1}	SDA, FDAF, FDAC input hold time after FS256 HIGH		30	–	–	ns
t_{H2}	SDA, FDAF, FDAC output hold time after FS256 HIGH		0	–	–	ns
$t_{D1,2}$	FS256 HIGH-to SCL, SWS, SDA, FDAF, FDAC output valid		–	–	50	ns
FS256 slave mode (FS256, SCL and SWS are input)						
t_{fH}	FS256 HIGH time		35	–	–	ns
t_{fL}	FS256 LOW time		35	–	–	ns
t_{sH}	SCL HIGH time		T+35	–	–	ns
t_{sL}	SCL LOW time		T+35	–	–	ns
t_{H1}	SDA, FDAF, FDAC output hold time after SCL HIGH		2T-15	–	–	ns
t_D	SCL HIGH-to SDA, FDAF, FDAC output valid		–	–	3T+60	ns
t_S	SDA, FDAF, FDAC input valid after SCL HIGH		20	–	–	ns
t_{H2}	SDA, FDAF, FDAC input hold time after SCL HIGH		T+20	–	–	ns
SBMCLK						
T	SBMCLK cycle time		120	163	205	ns
t_{mH}	SBMCLK HIGH time		35	–	–	ns
t_{mL}	SBMCLK LOW time		75	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SBMCLK master mode (SBCL, SBWS and SBDA are output)						
T_C	SBCL cycle time	384 kB/s	–	8T	–	ns
T_C	SBCL cycle time	256 kB/s	–	12T	–	ns
T_C	SBCL cycle time	192 kB/s	–	16T	–	ns
T_C	SBCL cycle time	128 kB/s	–	24T	–	ns
t_{cH}	SBCL HIGH time	384 kB/s	4T - 20	–	–	ns
t_{cH}	SBCL HIGH time	256 kB/s	6T - 20	–	–	ns
t_{cH}	SBCL HIGH time	192 kB/s	8T - 20	–	–	ns
t_{cH}	SBCL HIGH time	128 kB/s	12T - 20	–	–	ns
t_{cL}	SBCL LOW time	384 kB/s	4T - 20	–	–	ns
t_{cL}	SBCL LOW time	256 kB/s	6T - 20	–	–	ns
t_{cL}	SBCL LOW time	192 kB/s	8T - 20	–	–	ns
t_{cL}	SBCL LOW time	128 kB/s	12T - 20	–	–	ns
t_{D1}	SBWS, SBDA hold	to SBCL LOW	20	–	–	ns
t_{D2}	SBWS, SBDA valid	after SBCL 0	–	–	20	ns
SBMCLK slave mode (SBCL, SBWS and SBDA are input)						
T_C	SBCL cycle time	note 2	6.86T	8T	96T	ns
t_{cH}	SBCL HIGH time		T+30	–	–	ns
t_{cL}	SBCL LOW time		T+30	–	–	ns
t_{S1}	SBWS, SBDA setup time	before SBCL HIGH	T+30	–	–	ns
t_{H1}	SBWS, SBDA hold time	after SBCL HIGH	30	–	–	ns
t_{S2}	delay before SBEF valid	after SBCL HIGH	–	–	T-30	ns
t_{H2}	SBEF hold time	after SBCL HIGH	2T-30	–	–	ns

Notes

1. % deviation from nominal frequency must be the same for X24, X22 and FS256 inputs to within 0.2%
2. Minimum value for bit rate = 448 kB/s
Typical value for bit rate = 384 kB/s
Maximum value for bit rate = 32 kB/s

Masking threshold processor for MPEG layer 1 audio compression applications

SAA2521

FEATURES

- Stereo or 2-channel mono encoding
- Status may be read continuously
- Microcontroller interface
- I²S-interfaces
- Allocation algorithm including optional emphasis correction (for 44.1 kHz)
- Reduced power consumption
- 4 V nominal operating voltage capability.

GENERAL DESCRIPTION

The SAA2521 performs the adaptive allocation and scaling function for calculating the masking thresholds and sub-band sample accuracy in MPEG layer 1 applications. The SAA2521 is intended for use in conjunction with the stereo filter codec SAA2520.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2521GP	44	QFP	plastic	SOT205AG

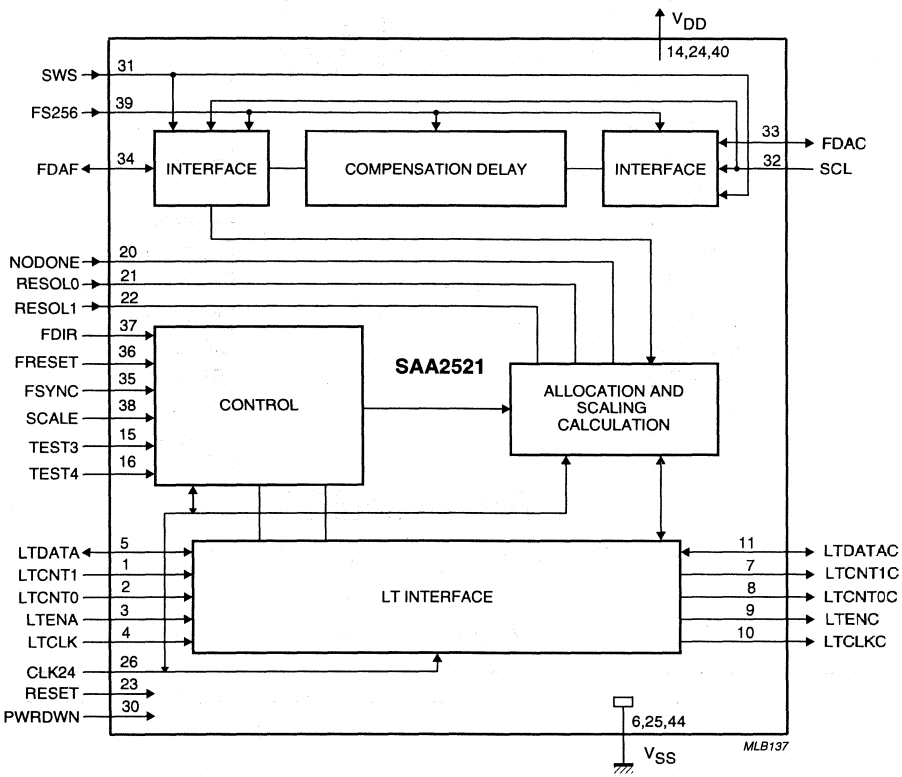


Fig.1 Block diagram.

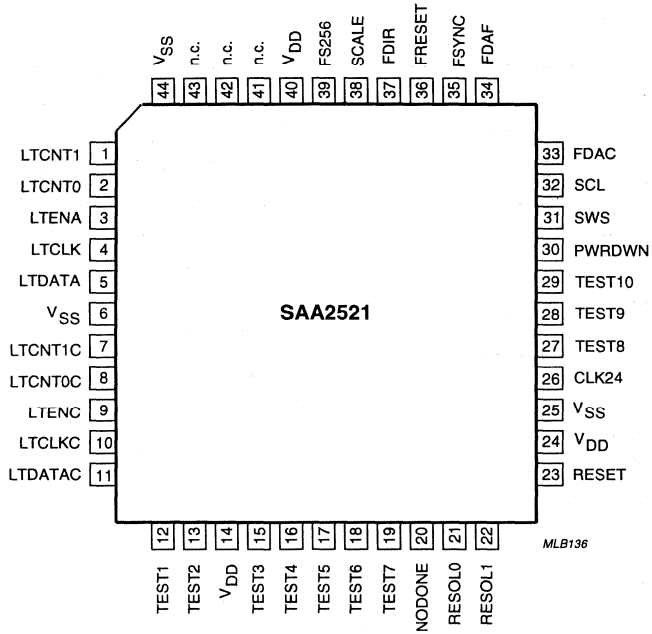


Fig.2 Pin configuration.

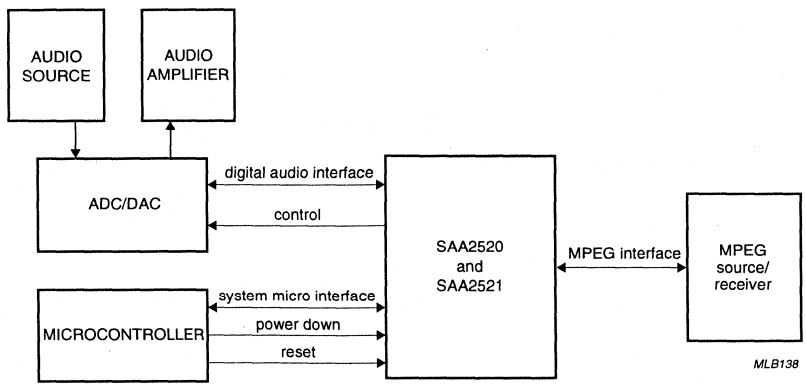


Fig.3 MPEG codec system data flow diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
LTCNT1	1	mode control 1, microcontroller interface input	I
LTCNT0	2	mode control 0, microcontroller interface input	I
LTENA	3	enable microcontroller interface input	I
LTCLK	4	bit clock microcontroller interface input	I
LTDATA	5	data, microcontroller interface (3-state inputs/outputs)	I/O
V_{SS}	6	supply ground (0 V)	
LTCNT1C	7	control 1; microcomputer interface	O
LTCNT0C	8	control 0; microcomputer interface	O
LTENC	9	enable microcontroller interface	O
LTCLKC	10	bit clock; microcontroller interface	O
LTDATAC	11	data; microcontroller interface, (3-state inputs/outputs)	I/O
TEST1	12	test output; do not connect	
TEST2	13	test output; do not connect	
V_{DD}	14	positive supply voltage (+ 5 V)	
TEST3	15	test mode input; to be connected to V_{DD}	
TEST4	16	test mode input; to be connected to V_{DD}	
TEST5	17	test input; to be connected to V_{SS}	
TEST6	18	test input; to be connected to V_{SS}	
TEST7	19	test input; to be connected to V_{SS}	
NODONE	20	no done state selection input	I
RESOL0	21	resolution selection 0 input	I
RESOL1	22	resolution selection 1 input	I
RESET	23	active HIGH reset input	I
V_{DD}	24	positive supply voltage (+ 5 V)	
V_{SS}	25	supply ground (0 V)	
CLK24	26	24.576 MHz processing clock input	I
TEST8	27	test input; to be connected to V_{SS}	
TEST9	28	test input; to be connected to V_{SS}	
TEST10	29	test input; to be connected to V_{SS}	
PWRDWN	30	power-down input	I
SWS	31	word selection input; (Filtered) - I²S-interface	I
SCL	32	bit clock input; (Filtered) - I²S-interface	I
FDAC	33	filtered data (Filtered) - I²S-interface (3-state inputs/outputs)	I/O
FDAF	34	filtered data (Filtered) - I²S-interface (3-state inputs/outputs)	I/O
FSYNC	35	sub-band synchronization on (Filtered) - I²S-interface, input	I
FRESET	36	reset signal input from SAA2520	I
FDIR	37	direction of the I²S-interface; input	I
SCALE	38	scale factor index select (note 1)	I

SYMBOL	PIN	DESCRIPTION	TYPE
FS256	39	system clock input; sample frequency x 256	I
V_{DD}	40	positive supply voltage (+ 5 V)	
n.c.	41	not connected	
n.c.	42	not connected	
n.c.	43	not connected	
V_{SS}	44	supply ground (0 V)	

Note to the Pinning Description

The scale input must be set LOW for use with the SAA2521.

FUNCTIONAL DESCRIPTION

Coding System

This efficient MPEG audio encoder is used in conjunction with the SAA2520 filter codec (bit rates of 384, 256, 192 and 128 k bits/s). The encoder utilizes a system producing sub-band samples from an incoming digital audio signal. This relies upon the audibility of signals above a given level and upon high amplitude signals masking those of lower amplitude. Although each sub-band signal is of approximately 750 Hz bandwidth, it possesses considerable overlap with those adjacent to it.

During the process of encoding, the masking threshold processor analyses the broadband audio signal at sampling frequency f_s by splitting it into 32 sub-band signals at a sampling frequency (f_s/32).

The coded signal consists of frames conveying the information corresponding to the sub-band samples. These also include a synchronization pattern identifying the start of each new frame. The allocation information for the 32 sub-bands is transferred as 4-bit values. If the amplitude of a sub-band signal is below the masking threshold it will be omitted from the coded signal.

The duration of a MPEG frame depends upon sampling frequency and is adjusted to 384 divided by f_s.

Adaptive Allocation and Scaling

The coding system calculates the masking power of the sub-band signals and adds the masking threshold. Sub-band signals with power below this threshold denote information to be discarded. Non-masked signals are coded using floating point notation in which a mantissa corresponds in length to the difference between peak power and masking threshold. The process is repeated for every MPEG frame and is known as the Adaptive Allocation of the available capacity.

Encoding Mode

Signal FDIR sets the data flow direction on the Filtered-I²S-interface. In the encoding mode (FDIR LOW) the device will accept samples from FDAF. These will be delayed by a number of sample periods depending upon the setting of the SCALE input. In the instance of operation with the SAA2520 (SCALE = logic 0) this delay will be 480 SWS periods. This will ensure alignment of the data with the computed allocations.

After the delay the samples will be presented on FDAC (pin 33). The circuit also performs all the calculations required to build the allocation table which is used in the codec (SAA2520). When used with the SAA2520 the calculated scale factor indices are sent via the LT interface. These operations are performed for every frame of the sub-band codec.

In order to synchronize with the codec and utilize the correct tables for the calculations the SAA2521 frequently requests the status of the codec. It monitors the bit-rate, sample frequency, operation mode and the emphasis information and uses the 'ready to receive' bit of the codec to determine the moment of the transfer of allocation information.

Decoding Mode

In the decoding mode (FDIR HIGH) the SAA2521 will take samples from FDAC which will be presented on the FDAF after a delay of 160 SWS periods. The LT interface between microcontroller and codec (SAA2520) will only be affected by the 'ready to receive' bit from the codec (SAA2520).

Microcontroller Interface Operation

Information on the interface between microcontroller and codec (SAA2520) will flow in a regular sequence synchronized with the codec (SAA2520):

- with every FSYNC the SAA2521 will read the status of the codec (SAA2520)
- Following the calculation of the allocation and scale factors the SAA2521 will send the first allocation information unit (16-bits). It will then continuously read the codec (SAA2520) status to ascertain when it is able to receive further allocation information units. When the transfer of these units is complete the SAA2521 will send settings and (for SCALE = logic 0) scale factor indices.
- The extended settings will be sent to the codec as soon as possible after reception from the microcontroller.

The microcontroller communicates with the SAA2521 in a similar fashion:

- status can be read continuously. The SAA2521 will output a copy of the codec (SAA2520) status on the LTDATA line except for the 'ready to receive' bits which are generated by the SAA2521. These indicate whether the SAA2521 is ready to receive the next settings or extended settings.
- settings can be sent following every occasion that the 'ready to receive' bit 'S' changes to logic 1.
- extended settings can be sent following each occasion that the 'ready to receive' bit 'E' changes to logic 1.

Mode Control

Operation is controlled by the FRESET and FDIR signals. FRESET causes a general reset. The FDIR signal is sampled at the falling edge of the FRESET signal to determine the operation mode:

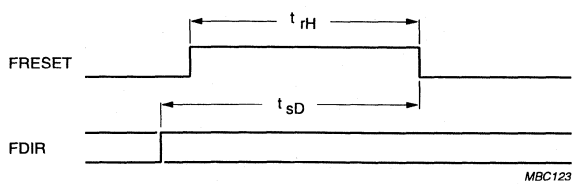
FDIR = logic 1	decoding mode, SAA2521 in feed-through mode
FDIR = 0	encoding mode, SAA2521 in calculation mode

Fig.4 shows the timing diagram for FRESET and FDIR.

Resolution Selection

The (SAA2521) is designed for operation with input devices (ADCs) which may possess a different sample resolution capability, i.e. audio sample inputs into the sub-band filters. Pins RESOL0 and RESOL1 (respectively pins 21 and 22) may be utilized to adjust the allocation information calculation to the resolution of the samples.

With the instance of pin 20 (NODONE) being HIGH, all available bits in the bit-pool will be allocated. If NODONE is LOW, no bits will be allocated to the sub-bands with energy levels below the theoretical threshold for the selected resolution.



$T_rH > 5T_{CLK24} = 210$ ns (for CLK24 = 24.576 MHz) min. time FRESET HIGH

$T_sD < 0$ ns min. set-up time FDIR to FRESET = LOW

Fig.4 Timing: FRESET and FDIR.

Power-down Mode Switching

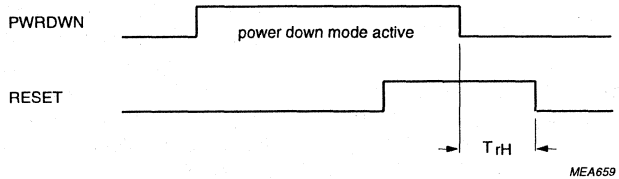
When the potential on the RESET pin (pin 23) is held HIGH for at least $5T_{CLK24}$ clock periods, the device will be reset after which it will operate in its decoding mode.

The power-down mode is activated when the PWRDWN pin (pin 30) is held HIGH. The 3-state buffers will be set to a high impedance while the normal outputs will retain the state attained prior to this mode being entered. This mode can only be used if other associated circuits react accordingly. The power-down mode is de-activated by a reset action.

Fig.5 shows the operation for the power-down mode switching.

Table 1 Resolution selection.

RESOL1	RESOL0	RESOLUTION
0	0	16-bits
0	1	18-bits
1	0	14-bits
1	1	15-bits



$T_{rH} > 5T_{CLK24} = 210$ ns (for CLK24 = 24.576 MHz) minimum time RESET HIGH

Fig.5 Power-down mode switching.

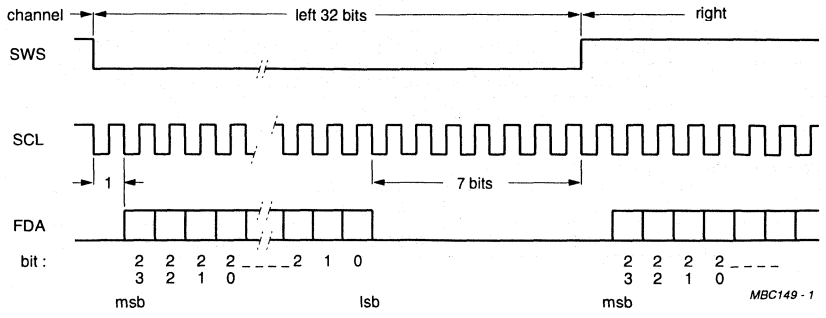


Fig.6 Format for transferring filtered data.

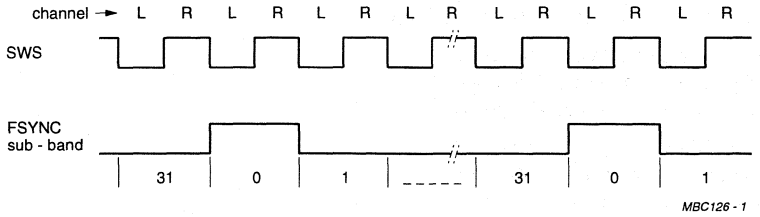


Fig.7 FSYNC related to SWS 0 data transfer period.

Table 2 The (Filtered) - I²S-interface.

SWS	input	word selection	F_s
SCL	input	bit clock	64 F_s
FDAF	bi-directional	filtered data to/from the filter section of SAA2520	
FDAC	bi-directional	filtered data to/from the codec section of SAA2520	
FSYNC	input	filter synchronization	$F_s/32$

Table 3 The (Filtered) - I²S-interface.

FRESET	input	reset
FDIR	input	Filtered - I²S-interface direction of data flow

(Filtered) - I²S-interfaces

Interfaces with the sub-band filter and codec (SAA2520) consist of the following signals.

Fig.6 shows the format for transferring filtered data.

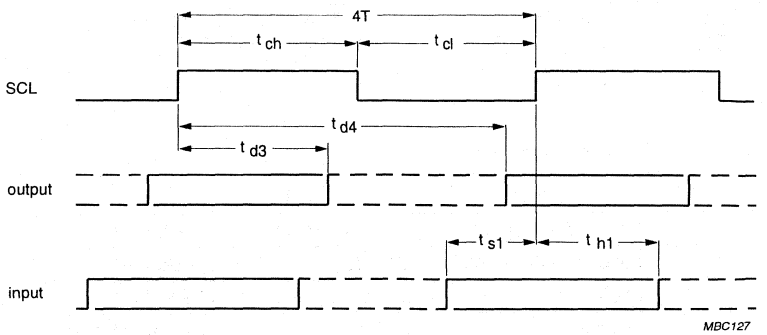
F_s 256 must be provided as system clock. This frequency is used by the interfaces with the SAA2520.

The frequency of the SWS signal (pin 31) is equal to the sample frequency F_s. Bit clock SCL (pin 32) is 64 times the sample frequency; thus each SWS period contains 64 data bits, 48 of which are actually used in data transfer. The half period during which SWS is logic 0 is used to transfer Left-channel information while that during which it is 1 permits transfer of Right-channel data.

The 24-bit samples are transferred with the most significant bit first. This bit is transferred during the bit clock period, one bit time after the change in SWS.

FSYNC signal is provided for the purposes of synchronization and indicates the portion of the SWS period during which the samples of sub-band 0 are transferred.

Fig. 7 shows the relationship between FSYNC and the SWS 0 data transfer period.



OUTPUT applies to FDAF and FDAC in the output mode.

INPUT applies to FDAF and FDAC in the input mode, SWS and FSYNC.

T = one F_s256 cycle time

$t_{cH} \geq T + 35$ ns minimum HIGH time SCL

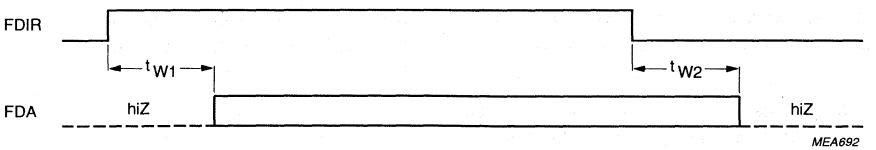
$T_{cL} \geq T + 35$ ns minimum LOW time SCL

$t_{d3} \geq 2T - 10$ ns hold time output after SCL HIGH

$t_{d4} \leq 3T + 60$ ns delay time output after SCL HIGH

$t_{s1} \geq 20$ ns set-up time input before SCL HIGH

$t_{h1} \geq T + 35$ ns hold time input after SCL HIGH



$t_{w1} \geq 3T$ minimum time high impedance to FDA enabled

$t_{w2} \geq 2T + 35$ ns maximum time FDA enabled to high impedance

Fig.8 (Filtered) - I²S-interface timing.

Table 4 SAA2521 interface with microcontroller.

LTCLK	input	bitclock
LTDATA	bi-directional	data
LTCNT0	input	control line 0
LTCNT1	input	control line 1
LTENA	input	enable

Table 5 SAA2521 interface with SAA2520.

LTCLKC	output	bit clock
LTDATAC	bi-directional	data
LTCNT0C	output	control line 0
LTCNT1C	output	control line 1
LTENC	output	enable

Table 6 SAA2521 interface control lines functions.

LTCNT1(C)	LTCNT0(C)	MODE	FROM	TO	TRANSFER OF
0	0	extended settings	microcontroller	SAA2520	8-bits
0	1	allocation (see note)	SAA2521	SAA2520	16/48 x 16-bits
1	0	settings	microcontroller	SAA2520	16-bits
1	1	status	codec	microcontroller	8 or 16-bits

Microcontroller Interface

Two microcontroller interfaces are provided; one for connection to the microcontroller interface of the SAA2520, the other to connect to the system controller. Information is conveyed via the SAA2521 which executes monitoring and extracts signals (e.g. settings and synchronization) essential to its operation. Additionally it also sends allocation information to the SAA2520. However, the SAA2521 does not monitor the external settings bits from the microcontroller (see Extended Settings).

The SAA2521 is a slave on the interface with the microcontroller which is active only when the enable signal LTENA (pin 3) is logic 1. This permits connection of this interface to other devices. Only the enable signal is not common to all devices.

SAA2521 is master on the interface with the SAA2520 and provides all signals with the exception of the data in the instance of status transfer from SAA2520 to SAA2521.

Information conveyed via these interfaces is transferred in 8 or 16-bit serial units with the type of information designated by the control lines (LTCNT1(C) and LTCNT0(C)).

A transfer of information begins when the master sets the control lines for the required action. It then sets the LTENA/C line to logic 1. Once this signal is established the slave determines the kind of action required and prepares for the transfer of data.

When the master supplies the LTCLK/C signal, data is transferred either to or from the slave in units of 8-bits; the least significant bit is always transferred first. A transfer of 16-bits is made in two, 8-bit units with the most significant 8-bit unit first. In between the two 8-bit units the LTENA/C signal remains logic 1.

Fig.9 shows an example of information transfer via SAA2521 interfaces.

Note to Table 6

This mode only on the interface between SAA2521 and SAA2520.
If SCALE = logic 1 then 16 x 16-bits
If SCALE = logic 0 then 48 x 16-bits

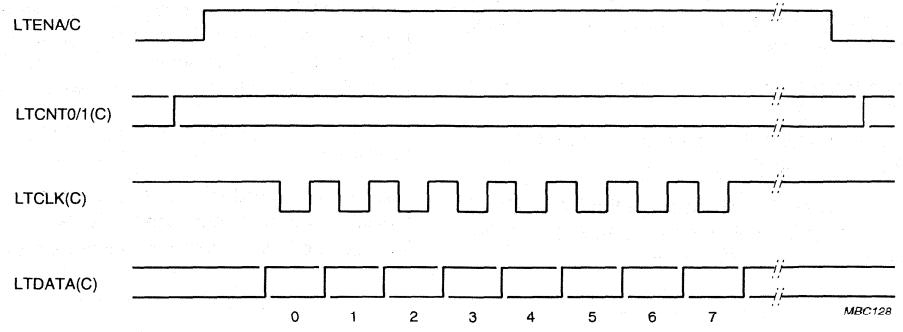
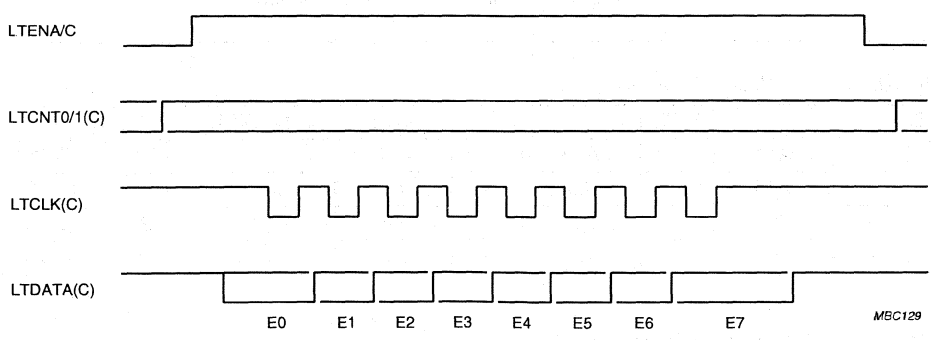


Fig.9 Example of information transfer via SAA2521 interfaces.



Refer to the SAA2520 description for the meaning of these bits as they pass SAA2521 unchanged.

Fig.10 Extended settings (LTCNT1 and LTCNT0)

Extended settings (LTCNT1(C) = logic 0, LTCNT0(C) = logic 0)

Eight information bits, generated by the microcontroller, are transferred in this mode. The SAA2521 will transfer these bits to the SAA2520 as soon as possible but does not monitor this information.

Fig.10 shows the relationship of the extended settings.

Allocation and SCALING information (LTCNT1C = logic 0, LTCNT0C = logic 1)

In the encoding mode (FDIR = logic 0) the SAA2521 will transfer allocation information to the SAA2520. This will occur once for every SAA2520 frame.

The information will consist of 16 transfers each of 16-bits. To synchronize the SAA2521 operation with that of the SAA2520, following the first 16-bit transfer of allocation data the SAA2521 checks the SAA2520 status to ensure it is ready to receive the remainder of the allocation information. Transfer of allocation data is completed by sending settings. Between 16-bit transfers the LTENC line returns to 0 as shown in Fig.11.

Fig.12 shows the order in which the bits occur on the interface during allocation information transfer.

The 4-bit sub-band allocation unit contains the number of bits allocated to the sub-band MINUS 1. A value of 0000 indicates no bits allocated to that sub-band.

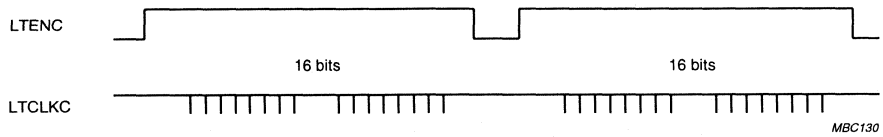


Fig.11 LTENC behaviour for 16-bit transfers.

Table 7 Allocation and SCALING information.

MSB			BITS			LSB	CHANNEL	SUB-BAND	
A15	-	A14	-	A13	-	A12	L	2 *	COUNT
A11	-	A10	-	A9	-	A8	R	2 *	COUNT
A7	-	A6	-	A5	-	A4	L	(2 *	COUNT) + 1
A3	-	A2	-	A1	-	A0	R	(2 *	COUNT) + 1

Table 8 Allocation and SCALING information.

MSB		BITS		LSB	CHANNEL	CONTENTS
SL15	-	SL14	-		---	00
SL13	-	SL12 - SL11 - SL10 - SL9	-	SL8	L	SCALE FACTOR (COUNT)
SL7	-	SL6			---	00
SL5	-	SL4 - SL3 - SL2 - SL1	-	SL0	R	SCALE FACTOR (COUNT)

With stereo encoding, Left and Right channels are designated **L** and **R.** This changes to channels I or II for 2-channel mono mode. If SCALE = logic 0 the transfer of allocation information will be followed by the transfer of scale factors. Each 16-bit transfer contains two scale factor indices.

Algorithm showing the process of information transfer:

COUNT : = logic 0

SEND ALLOCATION (COUNT)

REPEAT

READ STATUS

UNTIL

READY-TO-RECEIVE

FOR COUNT : = 1 to 15

DO

SEND ALLOCATION (COUNT)

SEND SETTINGS

IF SCALE = logic 0

THEN

FOR COUNT; = logic 0 TO 31

DO

SEND SCALE FACTORS (COUNT)

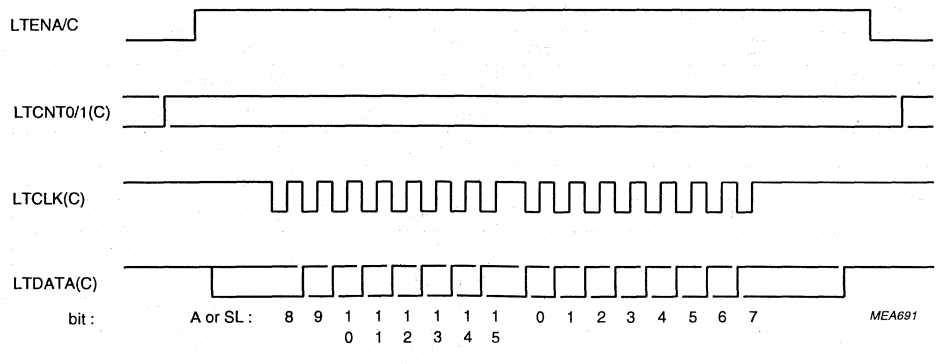


Fig.12 Order of interface bits during allocation information transfer.

SETTINGS (LTCNT1(C) = logic 1, LTCNT0(C) = logic 0)

Without using the information, the SAA2521 transfers microcontroller settings to the SAA2520.

Prior to sending settings, the microcontroller would utilize the SAA2521 status readings to ensure its readiness to accept and convey the data.

Following reception of the settings the SAA2521 will cause the ready-to-receive bit to be logic 0 until the settings have been sent to the SAA2520. The microcontroller can only send this data when this bit is logic 1.

Fig.13 shows the order of the bits on the interface.

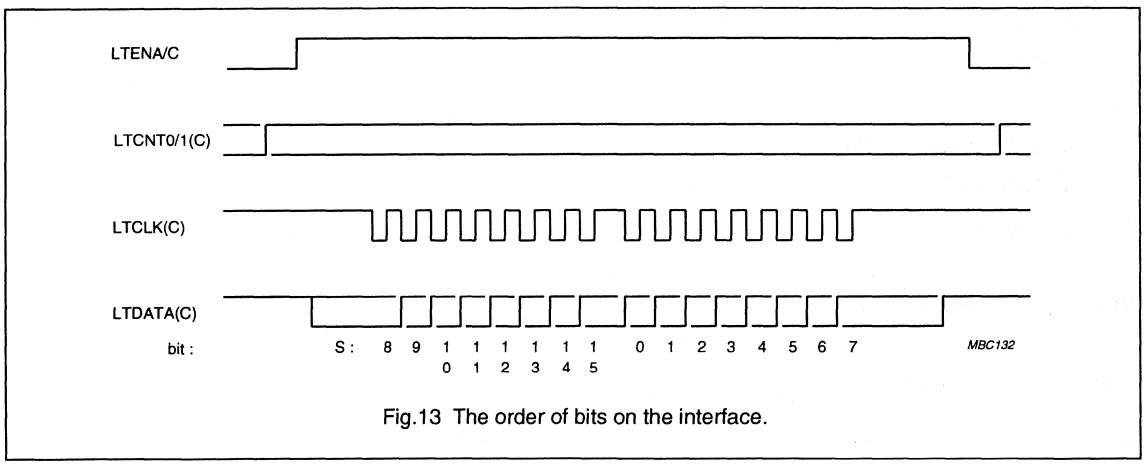


Fig.13 The order of bits on the interface.

Table 9 Microprocessor settings applied to the SAA2520 via the SAA2521.

MSB							BITS							LSB	NAME	FUNCTION	VALID IN
S15	-	S14	-	S13	-	S12									bitrate index	bitrate indication	encode
S11	-	S10													sample frequency	44.1, 48 or 32 kHz indic.	encode
S9															DECODE	1 - decode; 0 - encode	enc/dec
S8															ext 256f_s	1 - ext; 0 - int	enc/dec
S7															2-ch mono	1 - 2 ch mono; 0 - stereo	encode
S6															MUTE	1 - mute; 0 - no mute	enc/dec
S5															not used	–	enc/dec
S4															CH I	1 - CH I; 0 - CH II	decode
S3	-	S2													Tr0 - Tr1	transparent bits	encode
S1	-	S0													EMPHASIS	emphasis indication	encode

Status (LTCNT1(C) = logic 1, LTCNT0(C) = logic 1)

The SAA2520 and SAA2521 operation may be checked by reading these bits. All, except the ready-to-receive bits, are generated by the SAA2520.

The bit rate index indicates the bit rate of the sub-band signal in units of 32 kbits/s. The SAA2521 is designed for bit rates of 384, 256, 192 and 128 kbits/s only.

With EMPHASIS activated (S1 = T1 = 0 and S0 = T0 = 1) only bit rates 384 and 256 kbits/s can be used.

A ready-to-receive **S** or **E** indicates whether or not the SAA2521 can receive new settings or extended settings respectively from the microcontroller and should be checked prior to sending new information.

The SAA2521 can only be used to encode stereo (mode 00) signals and 2-channel mono (mode 10) signals.

During the decoding mode this bit indicates if the operation of the SAA2520 is in synchronization with the MPEG coded signal. Should this not be the case the SAA2520 cannot perform the decoding.

CLKOK indicates whether or not the F_s256 clock corresponds with the specified sample frequency.

EMPHASIS indication may be used to apply correct de-emphasis. During the encoding 50 / 15 μs mode the SAA2521 will correct the calculated allocation if emphasis is applied for a 44.1 kHz sampling frequency.

Table 10 Order of SAA2520 bits as they appear on the interface (see also Fig. 14).

MSB	BITS	LSB	NAME	FUNCTION	VALID IN
T15 - T14 - T13 -	T12		bitrate index	bitrate indication	enc/dec
T11 - T10			sample frequency	44.1, 48 or 32 kHz indic.	enc/dec
T9			ready-to-rec S	1 - ready; 0 - not ready	enc/dec
T8			ready-to-rec E	1 - ready; 0 - not ready	enc/dec
T7 - T6			MODE	sub-band signal mode ID	enc/dec
T5			SYNC	synchronization indic.	dec
T4			CLKOK	1 - OK; 0 - not OK	enc/dec
T3 - T2			Tr0 - Tr1	transparent bits	enc/dec
T1 - T0			EMPHASIS	emphasis indication	enc/dec

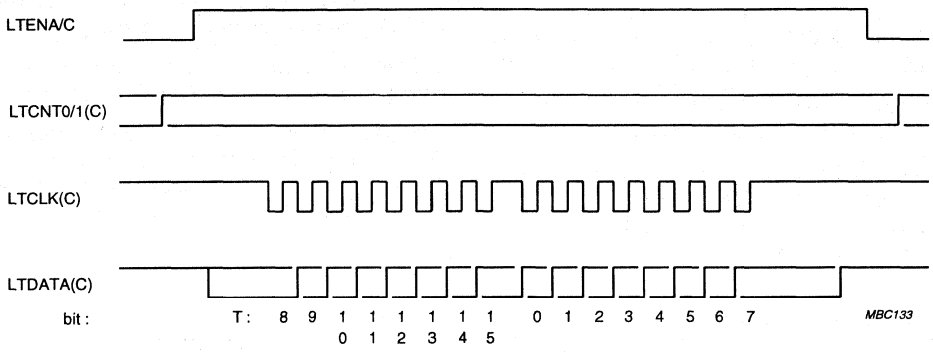


Fig.14 Order of appearance of bits on the interface.

Table 11 Sample frequency indication.

MSB	LSB	
00	44.1 kHz	default value
01	48 kHz	
10	32 kHz	
11	--	do not use

Table 12 MODE identification.

MSB LSB	MODE	OUTPUT
00	stereo	**L** and **R**
01	joint stereo	**L** and **R**
10	2 - channel mono	**I** or **II** as selected
11	1 - channel mono	mono, no selection

Frequency Range Limitation

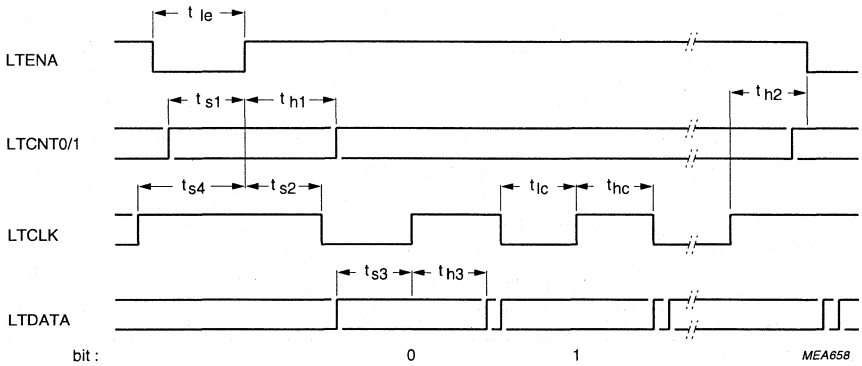
In encode mode the frequency range will be limited at lower rates. This is implemented by making the samples of higher frequency sub-bands equal to logic 0 before the allocation calculation. This automatically ensures that these sub-bands do not get any bits allocated.

The following table shows the sub-bands affected and the resulting frequency range.

The transfer of either 8-bits or 16-bits is permitted for the transfer of status information. When only 8-bits are transferred, these will always form the first byte and may be used in checking the ready-to-receive bit.

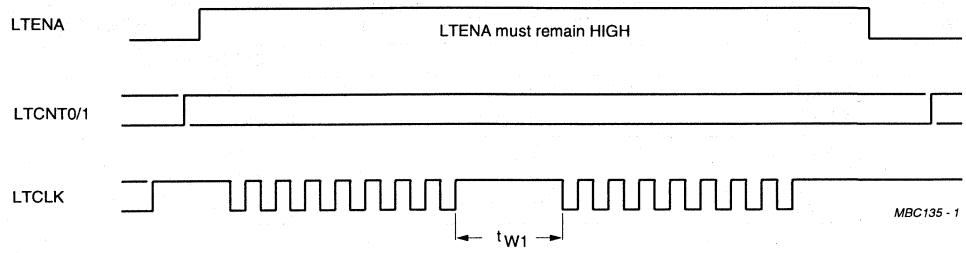
Table 13 Frequency examples.

BIT RATE	F_s	SUB-BANDS SET TO 0	@ FREQUENCY
256 kbit/s	48 kHz	29, 30, 31	> 21750 Hz
192 kbit/s	48 kHz 44.1 kHz	20, 21, ... , 30, 31 22, 23, ... , 30, 31	> 15000 > 15159
128 kbit/s	48 kHz 44.1 kHz 32 kHz	12, 13, ... , 30, 31 13, 14, ... , 30, 31 20, 21, ... , 30, 31	> 9000 > 8957 >10000



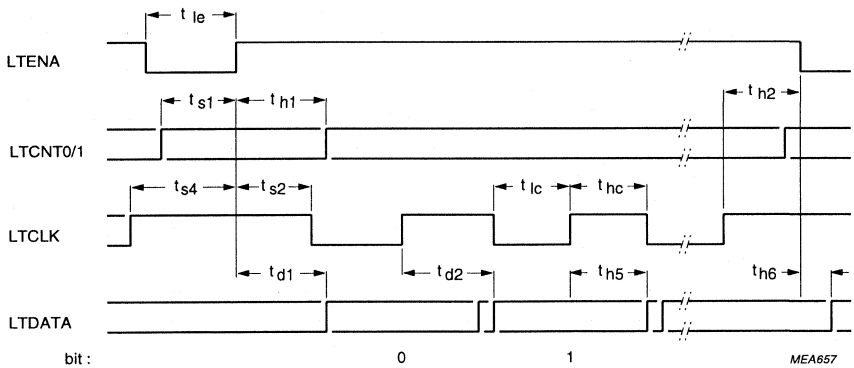
t_{le} > 210 ns minimum LOW time LTENA prior to transfer
t_{s1} > 50 ns set-up time LTCNT0, 1 before LTENA HIGH
t_{h1} > 210 ns hold time LTCNT0, 1 after LTENA HIGH
t_{s2} > 210 ns set-up time LTENA before LTCLK LOW
t_{h2} > 210 ns hold time LTENA after LTCLK HIGH
t_{lc} > 210 ns minimum LOW time LTCLK
t_{hc} > 210 ns minimum HIGH time LTCLK
t_{s3} > 210 ns set-up time LTDATA before LTCLK HIGH
t_{h3} > 50 ns hold time LTDATA after LTCLK HIGH
t_{s4} > 210 ns set-up time LTCLK before LTENA HIGH

Fig.15 Microcontroller to SAA2521 timing.



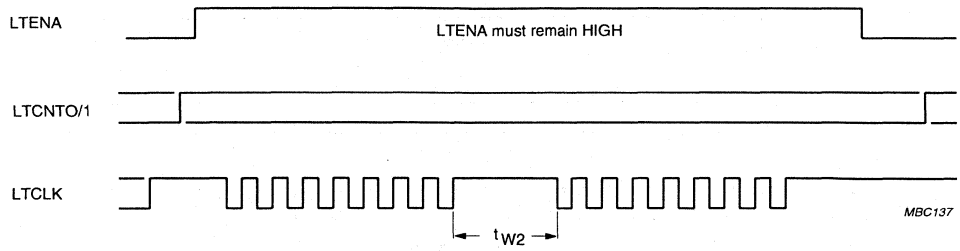
t_{w1} > 550 ns minimum time between two 8-bit transfers

Fig.16 16-bit transfers.



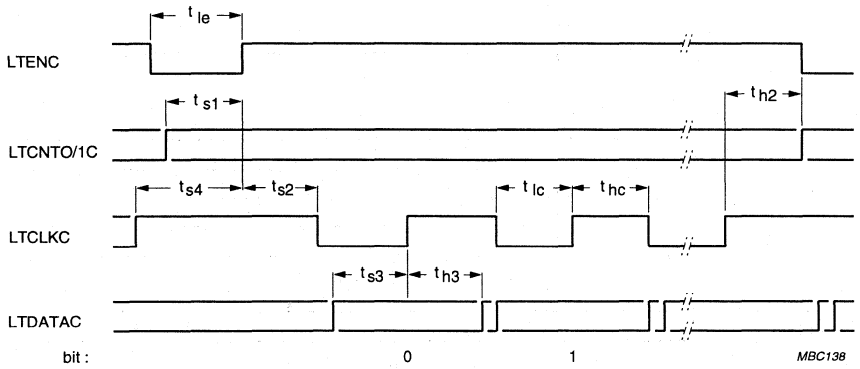
t_{le} > 210 ns minimum LOW time LTENA prior to transfer
t_{s1} > 50 ns set-up time LTCNT0, 1 before LTENA HIGH
t_{h1} > 210 ns hold time LTCNT0, 1 after LTENA HIGH
t_{s2} > 210 ns set-up time LTENA before LTCLK LOW
t_{h2} > 210 ns hold time LTENA after LTCLK HIGH
t_{lc} > 210 ns minimum LOW time LTCLK
t_{hc} > 210 ns minimum HIGH time LTCLK
t_{d1} < 385 ns maximum delay LTDATA after LTENA HIGH
t_{d2} < 385 ns maximum delay LTDATA after LTCLK HIGH
t_{h5} > 145 ns hold time LTDATA after LTCLK HIGH
t_{S4} > 210 ns set-up time LTCLK before LTENA HIGH
t_{h6} > 0 ns hold time LTDATA after LTENA LOW

Fig.17 SAA2521 to Microcontroller timing.



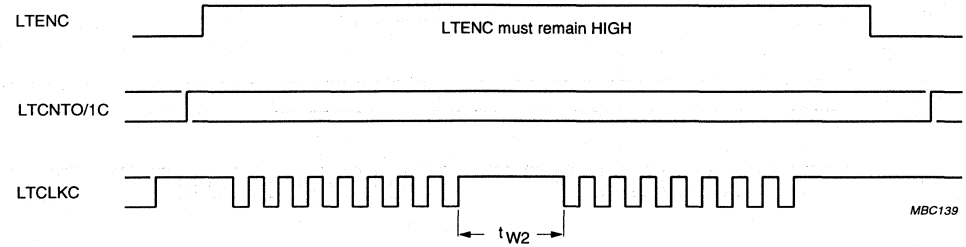
t_{w2} > 550 ns minimum time between two 8-bit transfers

Fig.18 16-bit transfers.



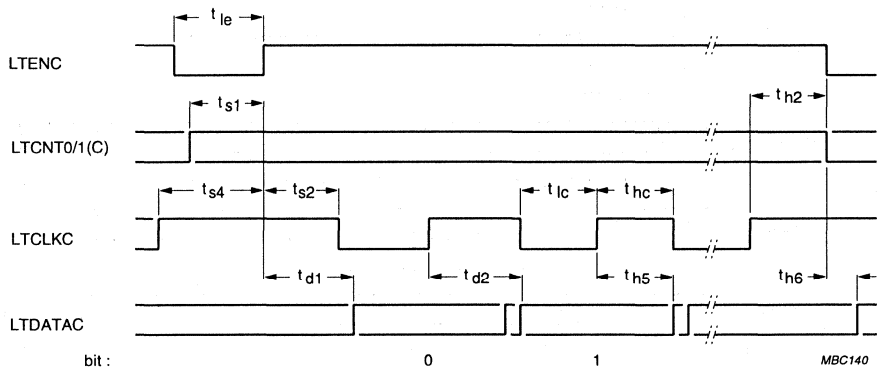
t_{le} > 400 ns minimum LOW time LTENA prior to transfer
t_{s1} > 400 ns set-up time LTCNT0, 1C before LTENC HIGH
t_{s2} > 200 ns set-up time LTENC before LTCLKC LOW
t_{h2} > 400 ns hold time LTENC after LTCLK HIGH
t_{lc} > 210 ns minimum LOW time LTCLKC
t_{hc} > 210 ns minimum HIGH time LTCLKC
t_{s3} > 210 ns set-up time LTDATAC before LTCLKC HIGH
t_{h3} > 160 ns hold time LTDATAC after LTCLKC HIGH
t_{s4} > 900 ns set-up time LTCLKC before LTENC HIGH

Fig.19 SAA2521 to SAA2520 timing.



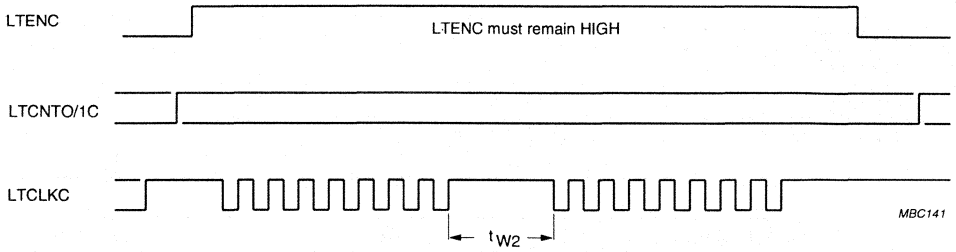
t_{w2} > 600 ns minimum time between two 8-bit transfers

Fig.20 16-bit transfers.



t_{le} > 400 ns minimum LOW time LTENC prior to transfer
t_{s1} > 400 ns set-up time LTCNT0, 1C before LTENC HIGH
t_{s2} > 200 ns set-up time LTENC before LTCLKC LOW
t_{h2} > 400 ns hold time LTENC after LTCLKC HIGH
t_{lc} > 210 ns minimum LOW time LTCLKC
t_{hc} > 210 ns minimum HIGH time LTCLKC
t_{d1} < 300 ns maximum delay LTDATAC after LTENC HIGH
t_{d2} < 300 ns maximum delay LTDATAC after LTCLKC HIGH
t_{s4} > 900 ns set-up time LTCLKC before LTENC HIGH
t_{h5} > 160 ns hold time after LTCLKCC HIGH
t_{h6} > 0 ns hold time LTDATAC after LTENC LOW

Fig.21 SAA2520 to SAA2521 timing.



t_{w1} > 600 ns minimum time between two 8-bit transfers

Fig.22 16-bit transfers.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	6.5	V
V_I	input voltage (note 1)	−0.5	V_{DD} + 0.5	V
I_{DD}	supply current	−	100	mA
I_I	input current	−	± 10	mA
I_o	output current	−	± 40	mA
P_{tot}	total power dissipation	−	550	mW
T_{stg}	storage temperature	−55	+ 150	°C
T_{amb}	operating ambient temperature	−40	+ 85	°C
V_{es1}	electrostatic handling (note 2)	−1500	1500	V
V_{es2}	electrostatic handling (note 3)	−70	70	V

Notes

1. Input voltage should not exceed 6.5 V unless otherwise specified.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

DC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 VT_{amb} = −40 to 85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		3.8	5	5.5	V
I_{DD}	operating current	V_{DD} = 3.8 V	–	15	30	mA
I_{DD}	operating current	V_{DD} = 5 V	–	25	50	mA
I_{PWRDWN}	stand-by current	in power-down mode	–	100	–	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	0.3 V_{DD}	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}	–	V_{DD}	V
I_I	input current		–	–	10	µA
Outputs						
V_{OL}	LOW level output voltage	note 1	–	–	0.4	V
V_{OH}	HIGH level output voltage	note 1	V_{DD}-0.5	–	–	V
3-state outputs						
I_{oz}	OFF state current	V_i = 0 to 5.5 V	–	–	10	µA

Note

1. Maximum load current for LTDATA, LTCNT1C, LTCNT0C, LTENC, LTCLKC, TEST1, TEST2, FDAC, FDAF = 2 mA; for LTDATAC = 3 mA.

AC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V T_{amb} = −40 to 85 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CLOCK CLK24						
f_s	frequency		23	24.576	26	MHz
CLOCK F_s256						
f_s	frequency	f_s = 48 kHz	–	–	13	MHz
Inputs FSYNC, SWS, LTCNT1, LTCNT0, LTENA, LTCLK, LTDATA, LTDATAC, FDAF, FDAC, SCL, SWS						
C_I	input capacitance		–	–	10	pF
INPUT SET-UP TIME						
t_{SU}	set-up time of inputs related to CLK24 rising edge	note 1	15	–	–	ns
t_{SU}	set-up time of inputs related to $256f_s$ rising edge	note 2	15	–	–	ns
INPUT HOLD TIME						
t_{HD}	hold time of inputs related to CLK24 rising edge	note 1	20	–	–	ns
t_{HD}	hold time of inputs related to $256f_s$ rising edge	note 2	10	–	–	ns
Outputs LTDATA, LTDATAC, LTCNT1C, LTCNT0C, LTENC, LTCLKC, FDAF, FDAC						
C_o	output capacitance		–	–	10	pF
t_d	output delay time related to CLK24 rising edge	C_L = 25 pF; note 3	–	–	45	ns
t_d	output delay time related to $256f_s$ rising edge	C_L = 25 pF; note 4	–	–	30	ns
3-state outputs						
t_{PHZ}	disable time HIGH-to-Z	C_L = 25 pF	–	–	65	ns
t_{PLZ}	disable time LOW-to-Z	C_L = 25 pF	–	–	65	ns
t_{PZH}	enable time Z-to-HIGH	C_L = 25 pF	–	–	65	ns
t_{PZL}	enable time Z-to-LOW	C_L = 25 pF	–	–	65	ns

Notes

1. Inputs FSYNC, SWS, LTCNT1, LTCNT0, LTENA, LTCLK, LTDATA, LTDATAC
2. Inputs FDAF, FDAC, SCL, SWS
3. Outputs LTDATA, LTDATAC, LTCNT1C, LTCNT0C, LTENC, LTCLK
4. Outputs FDAF, FDAC

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATASHEET

INFRARED REMOTE CONTROL TRANSMITTER RC-5

GENERAL DESCRIPTION

The SAA3010 is intended as a general purpose (RC-5) infrared remote control system for use where a low voltage supply and a large debounce time are expected. The device can generate 2048 different commands and utilizes a keyboard with a single pole switch for each key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands. The keyboard interconnection is illustrated by Fig.3.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified in the section **"KEYBOARD OPERATION"**.

Features

- Low voltage requirement
- Biphase transmission technique
- Single pin oscillator
- Test mode facility

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{DD}	2	–	7	V
Input voltage range*	V_I	−0.5	–	V_{DD}+0.5	V
Input current	I_I	–	–	±10	mA
Output voltage range*	V_O	−0.5	–	V_{DD}+0.5	V
Output current	I_O	–	–	±10	mA
Operating ambient temperature range	T_{amb}	−25	–	85	°C

* V_{DD}+0.5 V must not exceed 9 V.

The use of this device must conform with the Philips Standard number URT-0421.

PACKAGE OUTLINES

28-lead DIL plastic; (SOT117).
28-lead mini-pack; plastic (SO28; SOT136A).

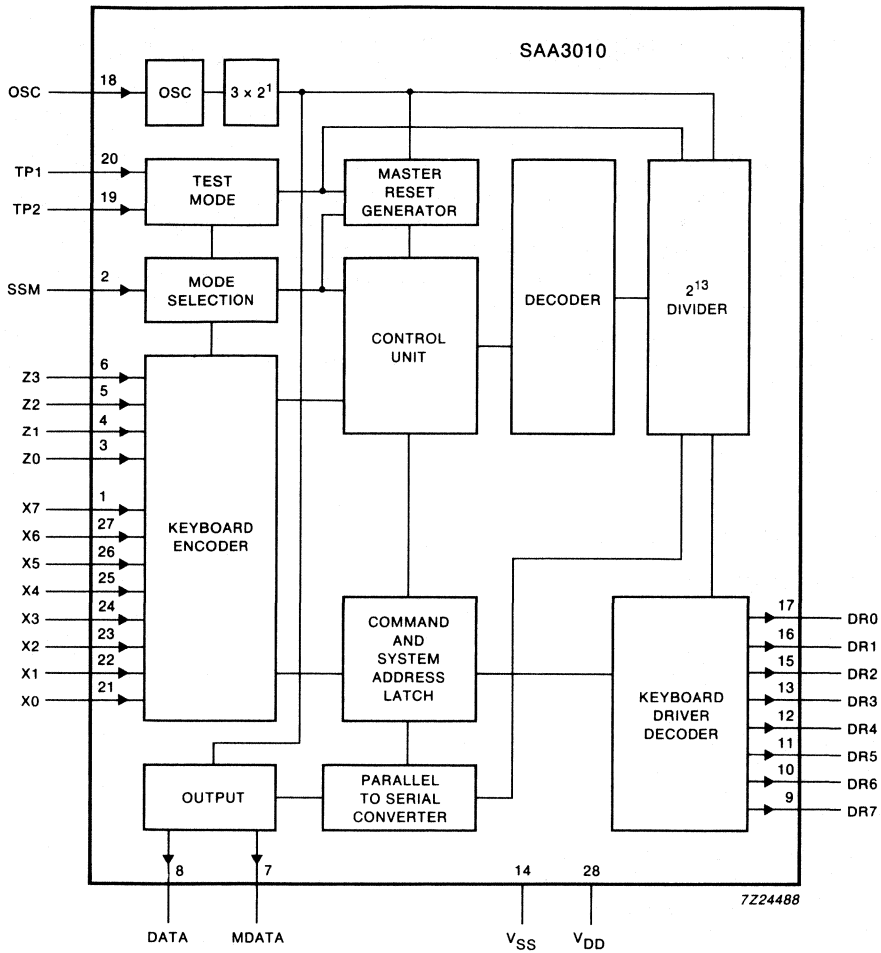


Fig.1 Block diagram.

Drive processor for DCC systems SAA3323

FEATURES

- Operating supply voltage: 2.7 to 3.6 V
- Low power dissipation: 84 mW (typ)
- Single chip digital equalizer, tape formatting and error correction
- 8-bit flash analog-to-digital converter (ADC) for low symbol error rate
- Two switchable Infinite Impulse-Response (IIR) filter sections
- 10-tap Finite Impulse-Response (FIR) filter per main data channel, with 8 bit coefficients, identical for all main channels
- 10-tap FIR filter for the AUX channel
- Analog and digital eye outputs
- Interrupt line triggered by internal auxiliary envelope processing e.g. label, counter, and others
- Robust programmable digital PLL clock extraction unit
- Low power SLEEP mode
- Slew rate limited Electromagnetic Compatibility (EMC) friendly output
- Digital Compact Cassette (DCC) optimized error correction
- Programmable symbol synchronization strategy for tape input data
- Microcontroller control of capstan servo possible during playback and recording

- Frequency and phase regulation of capstan servo during playback
- Choice of Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM) types for system Random Access Memory (RAM)
- Scratch pad RAM for microcontroller in system RAM
- Integrated interface for Precision Adaptive Sub-band Coding (PASC) data bus
- Three wire microcontroller 'L3' interface
- Protection against invalid auxiliary data
- Seamless joins between recordings.

GENERAL DESCRIPTION

The SAA3323 performs the drive processor function in the DCC system. This function is built up of digital equalizer, error correction and tape formatting functions. The digital equalizer is intended for use with DCC read amplifiers TDA1318 or TDA1380. The tape formatting and error correction circuit is intended for use with PASC ICs SAA2003 and SAA2013, and write amplifiers TDA1319 or TDA1381.

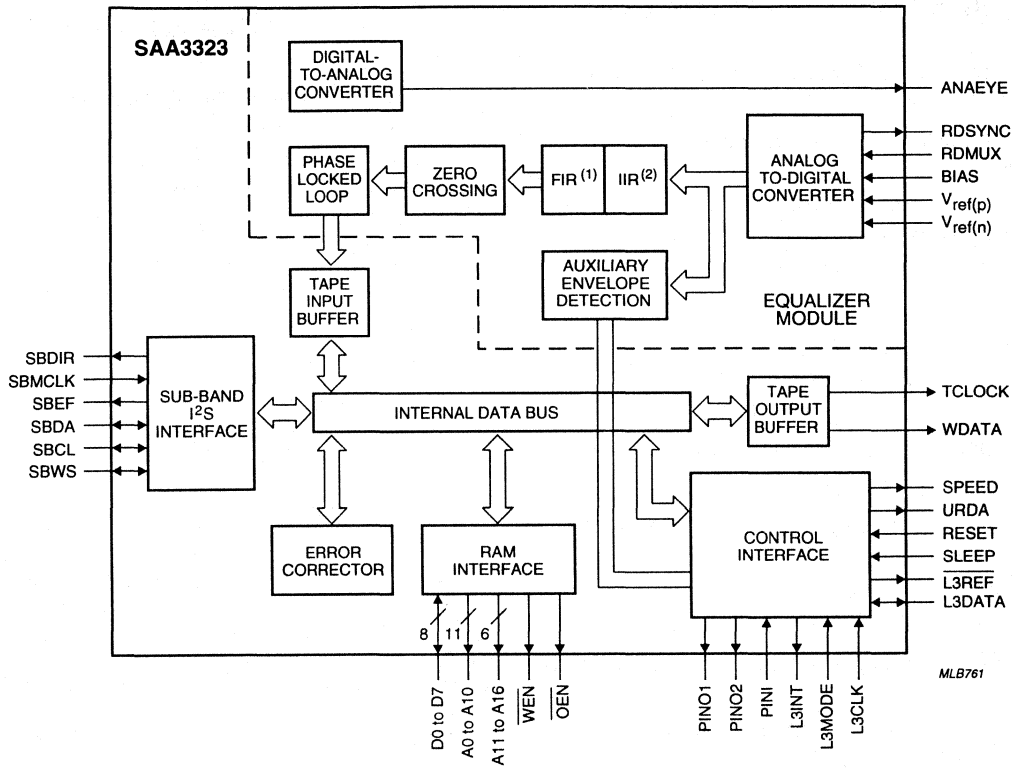
ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA3323H	80	TQFP80[1]	plastic	SOT315-1
SAA3323GP	80	QFP80[1]	plastic	SOT318-2

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* are followed. The pocketbook can be ordered using the code 9398 510 34011.

BLOCK DIAGRAM



(1) FIR = Finite Impulse-Response.
(2) IIR = Infinite Impulse-Response.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION	TYPE[1]
	QFP80	TQFP80		
SBWS	1	79	word select for sub-band PASC interface	I/O (1 mA)
SBCL	2	80	bit clock for sub-band PASC interface	I/O (1 mA)
SBDA	3	1	data line for sub-band PASC interface	I/O (1 mA)
SBDIR	4	2	direction line for sub-band PASC interface	O (1 mA)
SBMCLK	5	3	master clock for sub-band PASC interface	I
URDA	6	4	unreliable data	O (1 mA)
L3MODE	7	5	mode line for L3 interface	I
L3CLK	8	6	bit clock line for L3 interface	I
L3DATA	9	7	serial data line for L3 interface	I/O (2 mA)
L3INT	10	8	L3 interrupt output	O (1 mA)
V_{DD1}	11	9	digital supply voltage	S
V_{SS1}	12	10	digital ground	S
$\overline{L3REF}$	13	11	L3 bus timing reference	O (1 mA)
RESET	14	12	reset SAA3323	I
SLEEP	15	13	sleep mode selection of SAA3323	I
CLK24	16	14	24.576 MHz clock input	I
AZCHK	17	15	channel 0 and channel 7 azimuth monitor	O (1 mA)
MCLK	18	16	6.144 MHz clock output	O (1 mA)
TEST3	19	17	TEST3 output; do not connect	O (1 mA)
ERCOSTAT	20	18	ERCO status, for symbol error rate measurements	O (1 mA)
$\overline{OEN}$	21	19	output enable for RAM	O (2 mA)
A10/$\overline{RAS}$	22	20	address SRAM; $\overline{RAS}$ DRAM	O (2 mA)
V_{DD2}	23	21	digital supply voltage	S
V_{SS2}	24	22	digital ground	S
D7	25	23	data SRAM	I/O (4 mA)
D6	26	24	data SRAM	I/O (4 mA)
D5	27	25	data SRAM	I/O (4 mA)
D4	28	26	data SRAM	I/O (4 mA)
D3	29	27	data SRAM; data DRAM	I/O (4 mA)
D2	30	28	data SRAM; data DRAM	I/O (4 mA)
D1	31	29	data SRAM; data DRAM	I/O (4 mA)
V_{DD7}	32	30	digital supply voltage for RAM	S
V_{SS7}	33	31	digital ground for RAM	S
D0	34	32	data SRAM; data DRAM	I/O (4 mA)
A0	35	33	address SRAM; address DRAM	O (2 mA)
A1	36	34	address SRAM; address DRAM	O (2 mA)
A2	37	35	address SRAM; address DRAM	O (2 mA)
A3	38	36	address SRAM; address DRAM	O (2 mA)

SYMBOL	PIN		DESCRIPTION	TYPE[1]
	QFP80	TQFP80		
A4	39	37	address SRAM; address DRAM	O (2 mA)
V_{SS3}	40	38	digital ground	S
V_{DD3}	41	39	digital supply voltage	S
A5	42	40	address SRAM; address DRAM	O (2 mA)
A6	43	41	address SRAM; address DRAM	O (2 mA)
A7	44	42	address SRAM; address DRAM	O (2 mA)
A12/PINO5	45	43	address SRAM; Port expander output 5	O (2 mA)
A14/PINO1	46	44	address SRAM; Port expander output 1	O (2 mA)
A16/PINO3	47	45	address SRAM; Port expander output 3	O (2 mA)
A15/PINO4	48	46	address SRAM; Port expander output 4	O (2 mA)
$\overline{WEN}$	49	47	write enable for RAM	O (2 mA)
A13/PINO2	50	48	address SRAM; Port expander output 2	O (2 mA)
A8	51	49	address SRAM; address DRAM	O (2 mA)
V_{DD4}	52	50	digital supply voltage	S
V_{SS4}	53	51	digital ground	S
A9/$\overline{CAS}$	54	52	address SRAM; $\overline{CAS}$ for DRAM	O (2 mA)
A11	55	53	address SRAM	O (2 mA)
SPEED	56	54	Pulse Width Modulation (PWM) capstan control output for deck	O_t (1 mA)
PINO2	57	55	Port expander output 2	O_t (1 mA)
WDATA	58	56	serial output to write amplifier	O (1 mA)
TCLOCK	59	57	3.072 MHz clock output for tape I/O	O (1 mA)
V_{SS5}	60	58	digital ground	S
V_{DD5}	61	59	digital supply voltage	S
TEST2	62	60	TEST mode select; do not connect	I_{pd}
RDMUX	63	61	analog multiplexed input from read amplifier	I_A
$V_{ref(p)}$	64	62	ADC positive reference voltage	I_A
$V_{ref(n)}$	65	63	ADC negative reference voltage	I_A
SUBSTR	66	64	substrate connection	I_A
BIAS	67	65	bias current for ADC	I_A
V_{SSA}	68	66	analog ground	S
V_{DDA}	69	67	analog supply voltage	S
ANAEYE	70	68	analog eye pattern output	O_A
RDSYNC	71	69	synchronization output for read amplifier	O (1 mA)
V_{DD6}	72	70	digital supply voltage	S
V_{SS6}	73	71	digital ground	S
CHTST1	74	72	channel test pin 1	O (1 mA)
CHTST2	75	73	channel test pin 2	O (1 mA)
TEST0	76	74	TEST mode select; do not connect	I_{pd}
TEST1	77	75	TEST mode select; do not connect	I_{pd}

SYMBOL	PIN		DESCRIPTION	TYPE[1]
	QFP80	TQFP80		
PINI	78	76	Port expander input	I
PINO1	79	77	Port expander output 1	O (1 mA)
SBEF	80	78	sub-band PASC error flag line	O (1 mA)

Note

1. I = input; I_A = analog input; I_{pd} = input with pull-down resistance; I/O = bidirectional; O = output; O_A = analog output; O_t = 3-state output; S = supply.

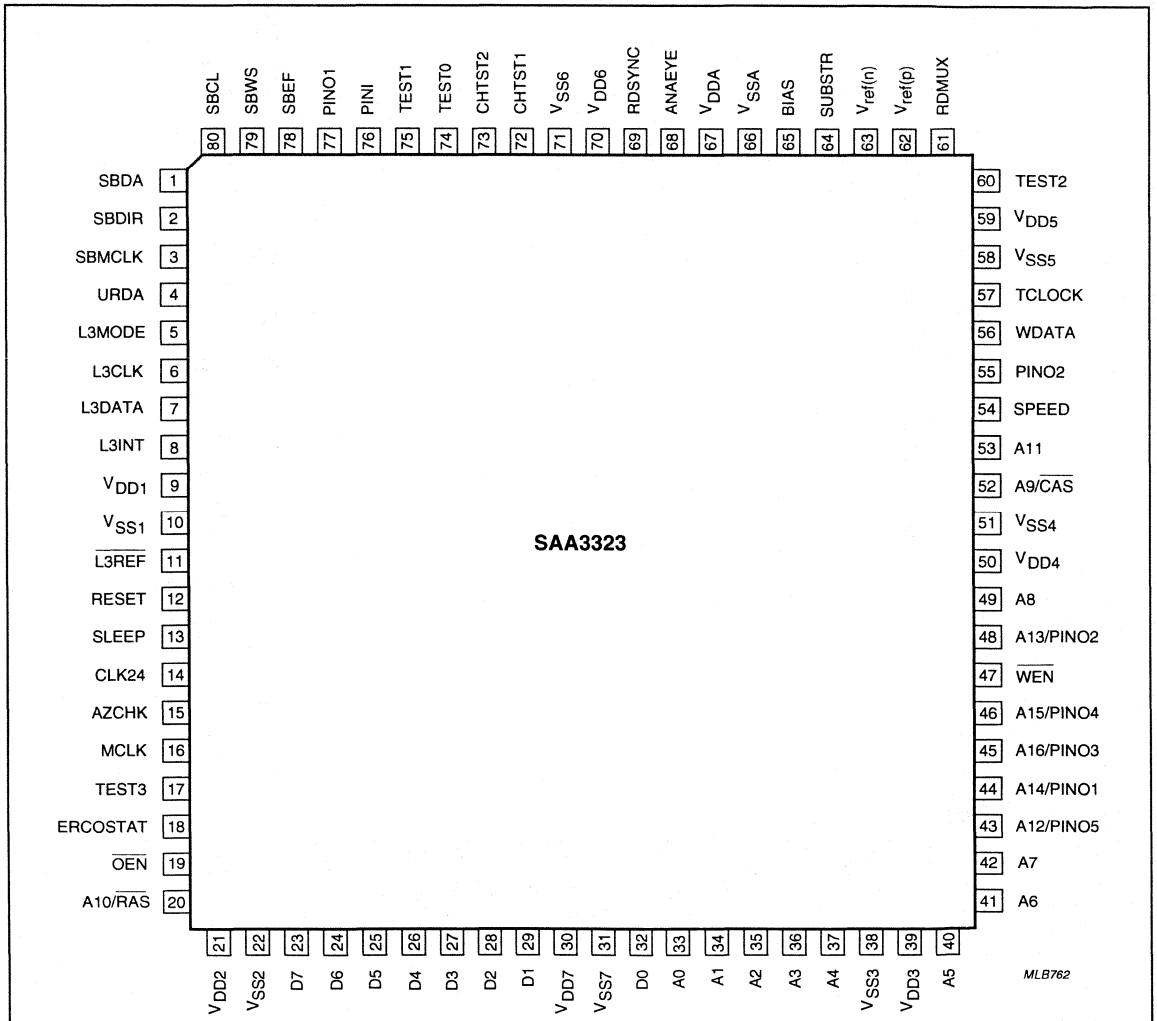


Fig.2 Pin configuration (SOT315-1; TQFP80).

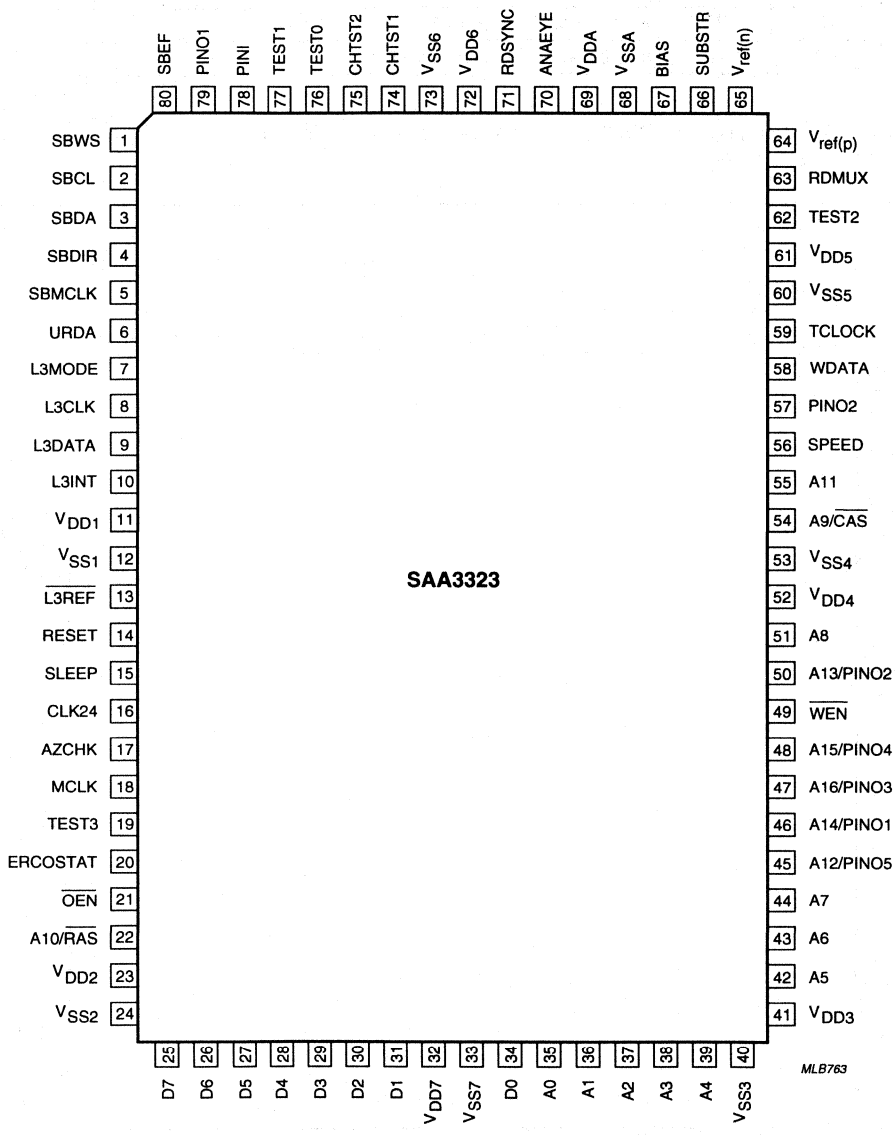


Fig.3 Pin configuration (SOT318-2; QFP80).

FUNCTIONAL DESCRIPTION

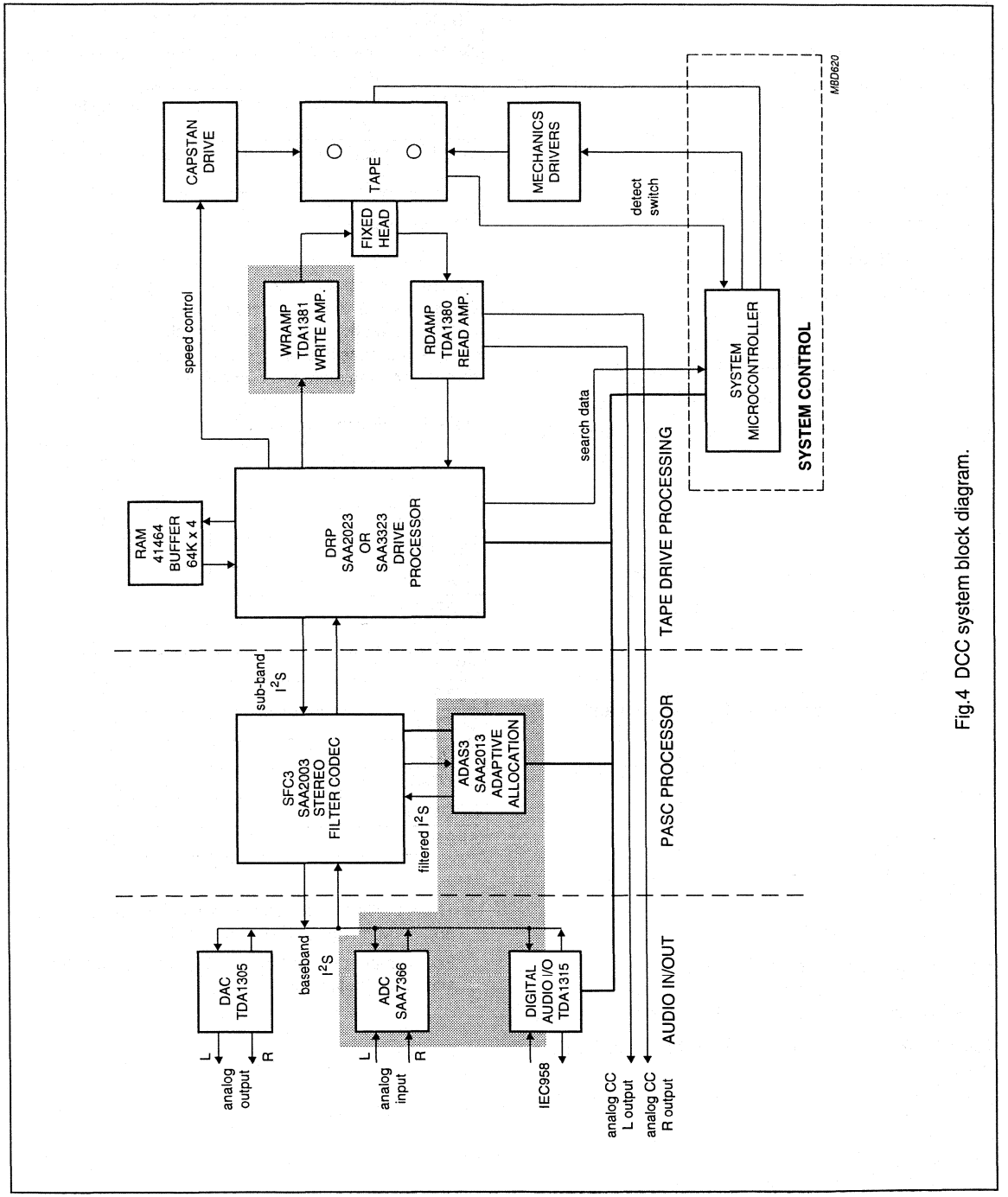


Fig.4 DCC system block diagram.

A simplified block diagram of the SAA3323 is shown in Fig.1.

DCC drive processing

The SAA3323 provides the following functions for the DCC drive processing.

PLAYBACK MODES

- Analog-to-digital conversion
- Tape channel equalization
- Tape channel data and clock recovery
- 10-to-8 demodulation
- Data placement in system RAM
- C1 and C2 error correction decoding
- Interfacing to sub-band serial PASC interface
- Interfacing to microcontroller for SYSINFO and AUX data
- Capstan control for tape deck.

RECORD MODES

- Interfacing to sub-band serial PASC interface
- C1 and C2 error correction encoding
- Formatting for tape transfer
- 8-to-10 modulation
- Interfacing to microcontroller for SYSINFO and AUX data
- Capstan control for tape deck, programmable by microcontroller.

SEARCH MODE

- Detection and interpretation of AUX envelope information
- AUX envelope counting
- Search speed estimation.

Tape Formatting and Error (TFE) correction module

The TFE module has 3 basic modes of operation as shown in Table 1.

Table 1 Basic modes of TFE module.

MODE	EXPLANATION
DPAP	audio and SYSINFO (main data) play; AUX play
DPAR	audio and SYSINFO (main data) play; AUX record
DRAR	audio and SYSINFO (main data) record; AUX record

TFE REGISTERS

The TFE module has 8 writable and 5 readable registers that are accessible via the L3 interface, one write register (CMD) and four read registers (STATUS0 to STATUS3) which are directly addressable, the other registers are indirectly addressable via commands sent to the CMD register. The registers are named as shown in Table 2.

Table 2 TFE register names.

REGISTER NAME	READ/WRITE
CMD	W
STATUS0	R
STATUS1	R
STATUS2	R
STATUS3	R
SET0	W
SET1	W
SET2	W
SET3[1]	W
SPDDTY	W
BYTCNT	W
RACCNT	W
SPEED	R

Note

1. The 4 LSBs of register 'SET3' set RAM type (RType) and RAM timing (RTim). See Table 3.

   For normal operation the 4 MSBs of register 'SET3' should be logic 0.

Table 3 RAM settings by register SET3.

RAM	REGISTER SET3
RTYPE 0	bit 0
RTYPE 1	bit 1
RTim 0	bit 2
RTim 1	bit 3

TFE DATA STREAMS

The TFE module has three read/write data streams that are accessible via the L3 interface and they are shown in Table 4.

Table 4 TFE data streams.

DATA STREAM NAME	READ/WRITE
SYSINFO	R/W
AUXINFO	R/W
Scratch pad RAM	R/W

TFE 'COMMANDS'

These are the commands that need to be sent to the TFE in order to access the indirectly accessible registers and the data streams, see Table 5.

Table 5 TFE commands.

NAME	COMMAND BYTE								EXPLANATION
	7	6	5	4	3	2	1	0	
RDSPEED	0	0	0	0	0	0	0	0	read SPEED register
LDSET0	0	0	0	1	0	0	0	0	load new TFE settings register 0
LDSET1	0	0	0	1	0	0	0	1	load new TFE settings register 1
LDSET2	0	0	0	1	0	0	1	0	load new TFE settings register 2
LDSET3	0	0	0	1	0	0	1	1	load new TFE settings register 3
LDSPDDTY	0	0	0	1	0	1	0	1	load SPDDTY register
LDBYTCNT	0	0	0	1	0	1	1	1	load BYTCNT register
LDRACCNT	0	0	0	1	1	0	0	0	load RACCNT register
RDAUX	0	0	1	0	0	0	0	0	read AUXILIARY information
RDSYS	0	0	1	0	0	0	0	1	read SYSINFO
RDDRAC	Y	Z	1	0	0	0	1	0	read RAM data bytes (8 bits) from quarter YZ
RDWDRAC	Y	Z	1	0	0	0	1	1	read RAM data words (12 bits) from quarter YZ
WRAUX	0	0	1	1	0	0	0	0	write AUXILIARY information
WRSYS	0	0	1	1	0	0	0	1	write SYSINFO
WRDRAC	Y	Z	1	1	0	0	1	0	write RAM data bytes (8 bits) to quarter YZ
WRWDRAC	Y	Z	1	1	0	0	1	1	write RAM data words (12 bits) to quarter YZ

Digital equalizer module

The digital equalizer module has 2 basic modes of operation as shown in Table 6.

Table 6 Basic modes of equalizer module.

MODE	EXPLANATION
Play	main data and AUX channels are equalized
Search	only AUX channel is processed; AUX envelope information is processed

DIGITAL EQUALIZER REGISTERS

The digital equalizer module has 9 write only, 3 read only and 1 read/write register(s) that are accessible via the L3 interface, one write register (CMD) and 2 read registers (STATUS0 and STATUS1) which are directly addressable, the other registers are indirectly addressable via commands sent to the CMD register. The registers are named as shown in Table 7.

Table 7 Digital equalizer register names.

REGISTER NAME	READ/WRITE
CMD	W
STATUS0	R
STATUS1	R
COEFCNT	W
FCTRL	W
CHT1SEL	W
CHT2SEL	W
ANAEYE	W
AEC	R/W
SSPD	R
INTMASK	W
DEQ2SET	W
CLKSET	W

DATA STREAMS

The digital equalizer module has one write only and one read only data stream that are accessible via the L3 interface and they are shown in Table 8.

Table 8 Digital equalizer data streams.

DATA STREAM NAME	READ/WRITE
FIR coefficients to buffer bank	W
FIR coefficients from active bank	W

DIGITAL EQUALIZER "COMMANDS"

These are the commands that need to be sent to the digital equalizer in order to access the indirectly accessible registers and the data streams.

Table 9 Digital equalizer commands.

NAME	COMMAND BYTE								EXPLANATION
	7	6	5	4	3	2	1	0	
WRCOEF	0	0	1	1	0	0	0	0	write FIR coefficients to the digital equalizer buffer bank
RDCOEF	0	0	1	0	0	0	0	0	read FIR coefficients from the digital equalizer active bank
LDCOEFCNT	0	0	0	1	0	0	1	1	load FIR coefficient counter
LDFCTRL	0	0	0	1	0	1	0	0	load filter control register
LDT1SEL	0	0	0	1	0	1	1	0	load CHTST1 pin selection register
LDT2SEL	0	0	0	1	0	1	1	1	load CHTST2 pin selection register
LDTAEYE	0	0	0	1	1	0	0	0	load ANAEYE channel selection register
LDAEC	0	0	0	1	1	0	0	1	load AEC counter
RDAEC	0	0	1	0	0	0	1	0	read AEC counter
RDSSPD	0	0	1	0	0	1	0	0	read SEARCH speed register
LDINTMSK	0	0	0	1	0	0	1	0	load interrupt mask register
LDDEQ3SET	0	0	0	1	0	0	0	0	load digital equalizer settings register
LDCLKSET	0	0	0	1	0	0	0	1	load PLL clock extraction settings register

Table 10 Filter control register.

BIT	7	6	5	4	3	2	1	0
Meaning	–	–	–	µCS[1]	SH1	SH0	Reserved	
Default	0	0	0	0	1	0	1	1

Note

1. µCS is a microcontroller controlled coefficient bank switch. This causes the filter coefficients to be activated at a time that is safe for the digital equalizer, i.e. at the end of the FIR program and that the complete value of coefficient number 9 has been received.

Table 11 SH1 and SH2 (FIR output scaling).

SH		EFFECT ON FIR OUTPUT
1	0	
0	0	FIR mod 256
0	1	$\frac{FIR}{2}$ mod 256
1	0	$\frac{FIR}{4}$ mod 256
1	1	$\frac{FIR}{8}$ mod 256

Transfer of FIR coefficients

For the main data channels (tracks 0 to 7) there are 10 coefficients (taps) each of 8 bits, where all of the data channels make use of the same coefficients. The addresses for the main data coefficients 0 to 9 are 0 to 9_{dec} respectively.

There are ten coefficients (taps) each of 8 bits for the aux channel (CHAUX). The addresses for the auxiliary coefficients 0 to 9 are 16 to 25_{dec} respectively.

There are 2 banks of coefficients for both the aux and the main data channels, namely the 'buffer', and the 'active' banks. The microcontroller writes only to the 'buffer' banks, and reads only from the 'active' banks.

The microcontroller can poll the digital equalizer status bit BKSW to see when the switch occurs. BKSW starts life LOW, goes HIGH as a result of the bank switching and goes LOW as result of the complete value of a main data coefficient being received by the digital equalizer.

The microcontroller sets µCS HIGH before sending the new set of aux or main data coefficients, the digital equalizer resets it once the bank switch occurs.

The actual FIR coefficients that are used are a function of the tape head, read amplifier and type of tape (i.e. pre-recorded or own recorded) used, such information is outside of the scope of this data sheet.

Coefficient address counter (COEFCNT)

This 5 bit counter is used to point to the FIR coefficient to be transferred to or from the digital equalizer.

Table 12 Coefficient address counter.

BIT	7	6	5	4	3	2	1	0
Meaning	–	–	–	CC4	CC3	CC2	CC1	CC0
Default	0	0	0	0	0	0	0	0

Pin explanations and interfacing to other hardware

RESET

This is an active HIGH input which resets the SAA3323 and brings it into its default mode, DPAP. This reset does not affect the contents of the FIR filter coefficients in the digital equalizer. This should be connected to the system reset, which can be driven by the microcontroller. The duration of the reset pulse should be at least 15 µs.

SLEEP

This pin is an active HIGH input which puts the SAA3323 in a low power consumption SLEEP mode. This pin should be connected to the DCC SLEEP signal, which can be driven by the microcontroller. The CLK24 clock may be stopped and the VREFP and VREFN inputs brought to ground while the SAA3323 is in 'sleep' mode to further reduce power consumption. When recovering from sleep mode, the SLEEP pin should be taken LOW and the SAA3323 reset.

CLK24

This is the 24.576 MHz clock input and should be connected directly to the SAA2003 (pin CLK24).

Sub-band serial PASC interface connections

The timing for the sub-band serial PASC interface is given in Figs 5 to 7.

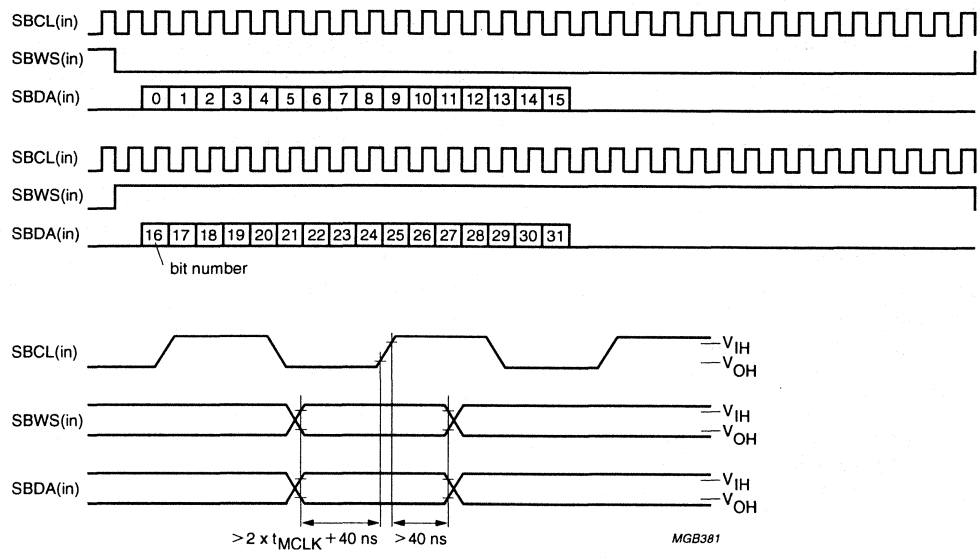


Fig.5 Sub-band serial PASC interface timing; DRAR mode.

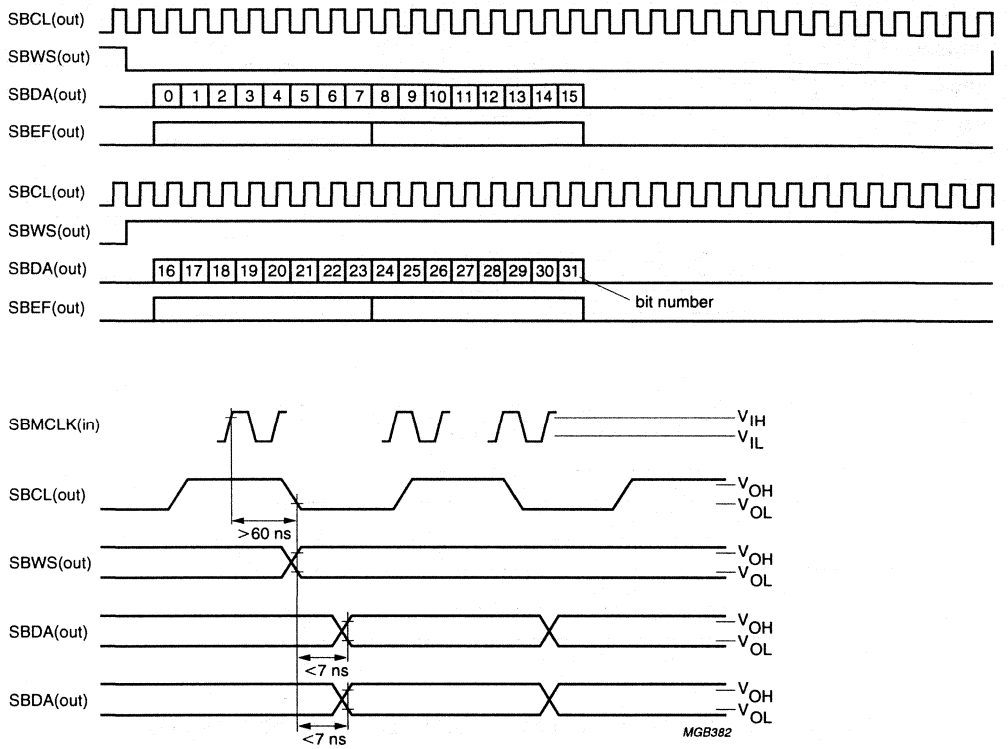


Fig.6 Sub-band serial PASC interface timing in play modes; DRPMAS = logic 1.

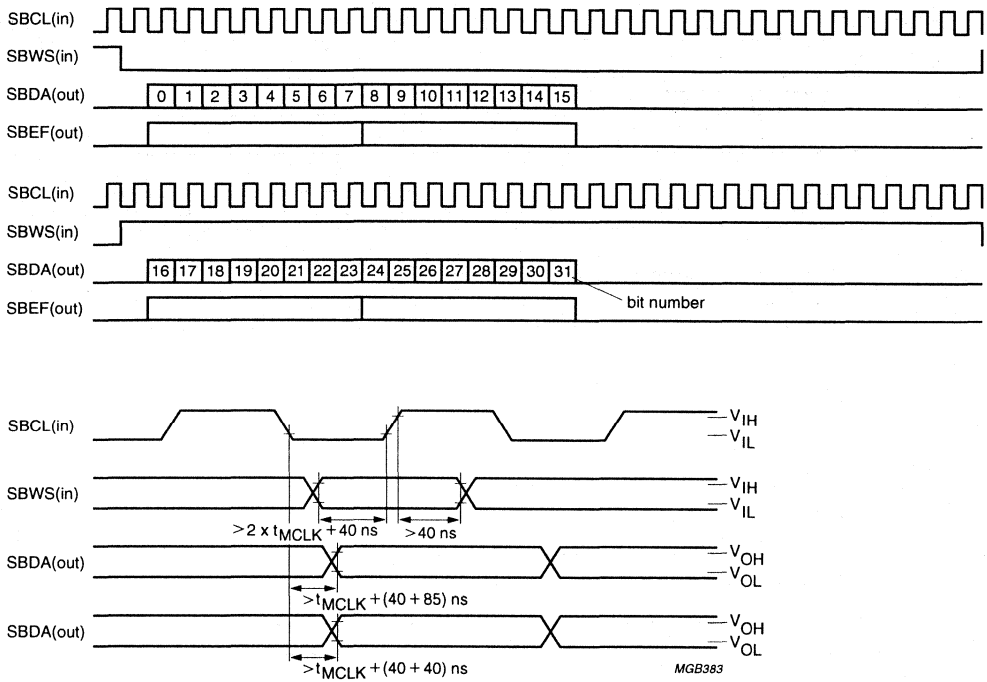


Fig.7 Sub-band serial PASC interface timing in play modes; DRPMAS = logic 0.

SBMCLK

This is the sub-band master clock input for the sub-band serial PASC interface. The frequency of this signal is nominally 6.144 MHz. When the SAA3323 is used with SAA2003 this pin is tied to ground, and the TFE settings bit 'DRPMAS' set to logic 1.

SBDIR

This output pin is the sub-band serial PASC bus direction signal, it indicates the direction of transfer on the sub-band serial PASC bus. This pin connects directly to the SBDIR pin on the SAA2003. The transfer directions are shown in Table 13.

Table 13 PASC bus transfer directions.

SBDIR	DIRECTION
1	SAA3323 to SAA2003 transfer (audio play)
0	SAA2003 to SAA3323 transfer (audio record)

SBCL

This input/output pin is the bit clock line for the sub-band serial PASC interface to the SAA2003. When used with SAA2003 this pin is input only. It has a nominal frequency of 768 kHz.

SBWS

This input/output pin is the word select line for the sub-band serial PASC interface to the SAA2003. When used with SAA2003 this pin is input only. It has a nominal frequency of 12 kHz.

SBDA

This input/output pin is the serial data line for the sub-band serial PASC interface to the SAA2003.

SBEF

This active HIGH output pin is the error-per-byte line for the sub-band serial PASC interface to the SAA2003.

URDA

This active HIGH output pin indicates that the main data (audio), the SYSINFO and the AUXILIARY data are NOT usable, regardless of the state of the corresponding reliability flags. The state of this pin is reflected in the URDA bit of STATUS byte 0, which can be read by the microcontroller. This pin should be connected directly to the URDA pin of the SAA2003. URDA goes active as a result of a reset, a mode change from mode DRAR to DPAP, or if the SAA3323 has had to re-synchronize with the incoming data from tape.

The position of the first sub-band serial PASC bytes in a tape frame is shown in Figs 8 and 9.

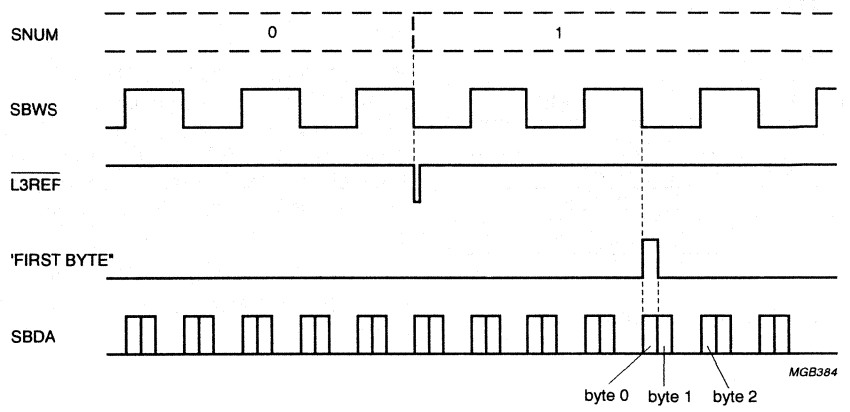


Fig.8 Position of first sub-band serial PASC bytes in a tape frame in DPAP/DPAR mode.

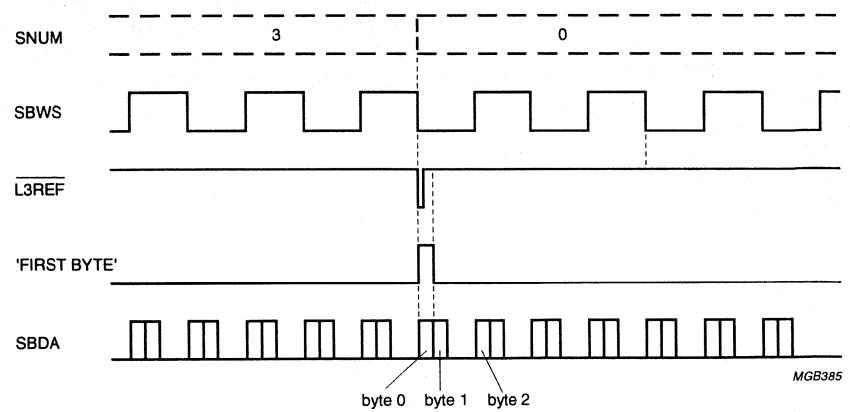


Fig.9 Position of first sub-band serial PASC bytes in a tape frame in DRAR mode.

RAM connections

The SAA3323 has been designed to operate with DRAMs and SRAMs. Suitable DRAMs are 64K × 4-bit or 256K × 4-bit configurations operating in page mode, with an access time of 80 to 100 ns. The timing for read, write and refresh cycles for DRAMs is shown in Figs 10 to 12. The timing for SRAMs is shown in Figs 13 to 19.

For fast SRAMs: (these values are subject to verification during characterization in). The conditions (most critical at the required V_{DD}) are shown in Table 14.

Table 14 Fast SRAM conditions.

CONDITION[1]	TIME
Write pulse duration	$t_W \leq 140$ ns
Data set-up to rising $\overline{WEN}$	$t_{su} \leq 72$ ns
Write cycle time	$T_{cy} \leq 200$ ns
Read access time	$t_{ACC} \leq 240$ ns

Note

1. The SAA3323 should work in: RType = '01'; RTim = '00' mode.

A9/$\overline{CAS}$

When SAA3323 is used with SRAM this output pin is Address line 9, and should be connected directly to the corresponding address pin on the SRAM. When SAA3323 is used with DRAM this output pin is the column address strobe (active LOW), it connects directly to the column address strobe pin of the DRAM.

A10/$\overline{RAS}$

When SAA3323 is used with SRAM this output pin is Address line 10, and should be connected to the corresponding address pin of the SRAM. When SAA3323 is used with DRAM this output pin is the row address strobe (active LOW), it connects directly to the row address strobe pin of the DRAM.

$\overline{OEN}$

This output pin is the output enable (active LOW) for the RAM, it connects directly to the output enable pin of the RAM.

$\overline{WEN}$

This output pin is the write enable (active LOW) for the RAM, it connects directly to the write enable pin of the RAM.

A0 TO A8

When SAA3323 is used with DRAM these output pins are the multiplexed column and row address lines. When the 64K × 4-bit DRAM is used, pins A0 to A7 should be connected to the DRAM address input pins, and pin A8 should be left unconnected. When using the 256K × 4-bit DRAM the address pins A0 to A8 should be connected to the address input pins of the DRAM.

When SAA3323 is used with SRAM these are the lower address pins and should be connected directly to the SRAM address pins.

A11

This output pin is the an address pin for the SRAM and when SRAM is used they should be connected directly to the address pins of the SRAM. When DRAM is used this pin should not be connected.

A10 AND A12 TO A16

These output pins are the upper address pins for the SRAM and when SRAM is used they should be connected directly to the address pins of the SRAM. When DRAM is used or when the small SRAM is used all or some of these pins become available as Port expander outputs.

Table 15 Port expander outputs.

PIN NAME	PIN		PORT EXPANDER OUTPUT	CONDITIONS
	QFP80	TQFP80		
A14/PINO1	46	44	PINO1	RType = 00
A13/PINO2	50	48	PINO2	RType = 00
A16/PINO3	47	45	PINO3	RType = 00 or RType = 01
A15/PINO4	48	46	PINO4	RType = 00 or RType = 01
A12/PINO5	45	43	PINO5	RType = 00

D0 TO D3

When SAA3323 is used with SRAM these I/O pins form the lower nibble of the data bus connection to the RAM, and should be connected to the corresponding data I/O pins of the SRAM. When SAA3323 is used with DRAM these input/output pins are the data lines for the RAM, they should be connected directly to the DRAM data I/O pins.

D4 TO D7

These input/output pins are the upper nibble of the data bus for use with SRAM, and when SRAM is being used they should be connected directly to the corresponding SRAM I/O pins.

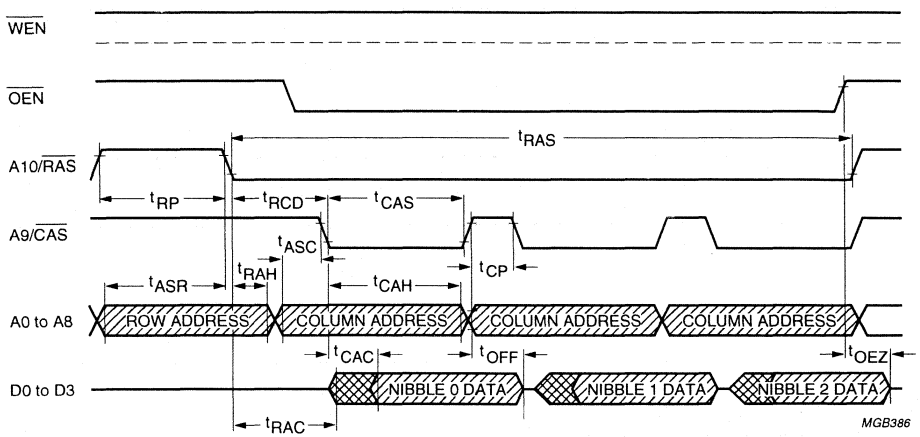


Fig.10 DRAM read cycle timing.

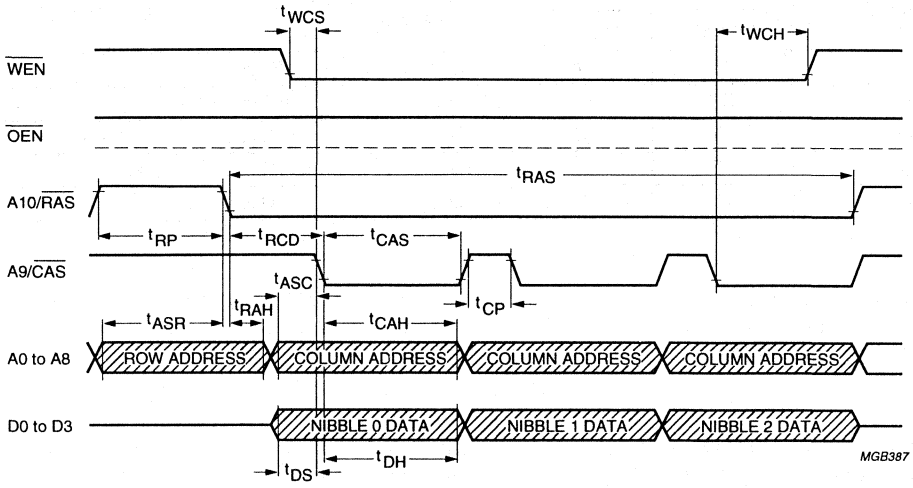


Fig.11 DRAM write cycle timing.

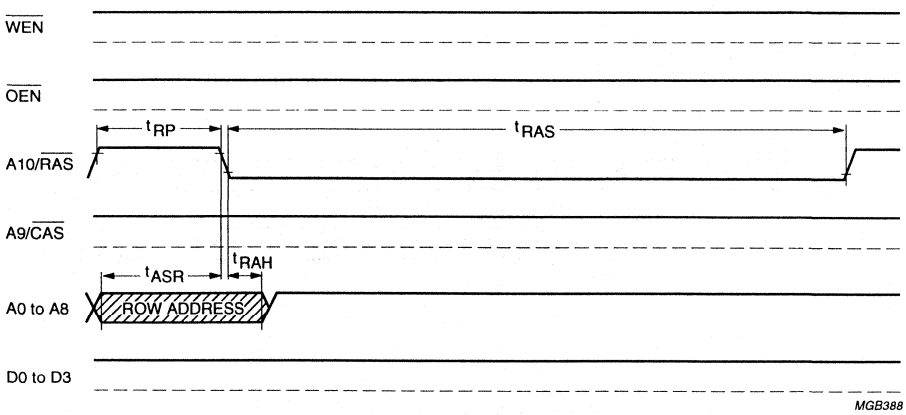


Fig.12 DRAM refresh cycle timing.

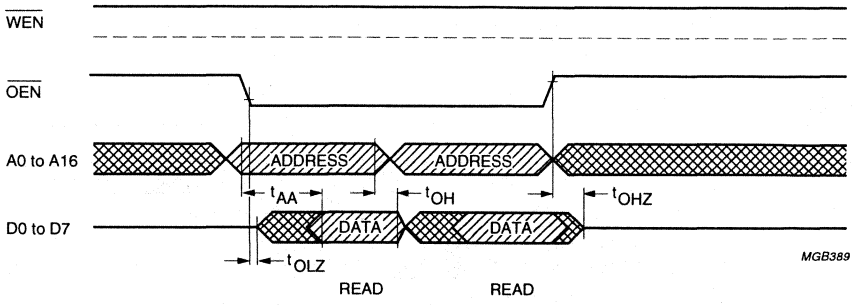


Fig.13 Fast SRAM read cycle timing.

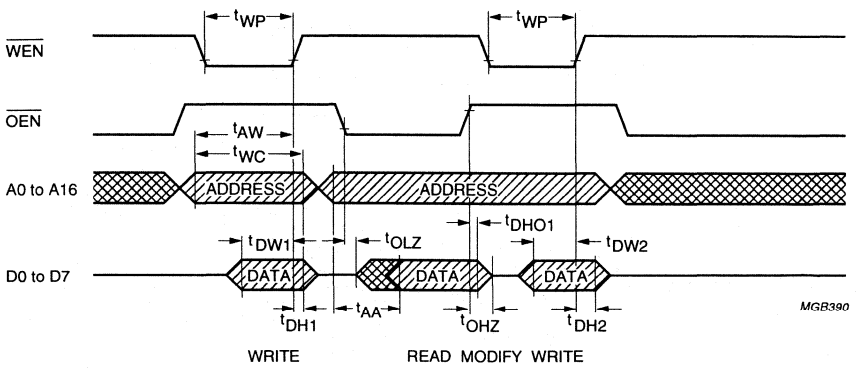


Fig.14 Fast SRAM write cycle timing; RTim = "00".

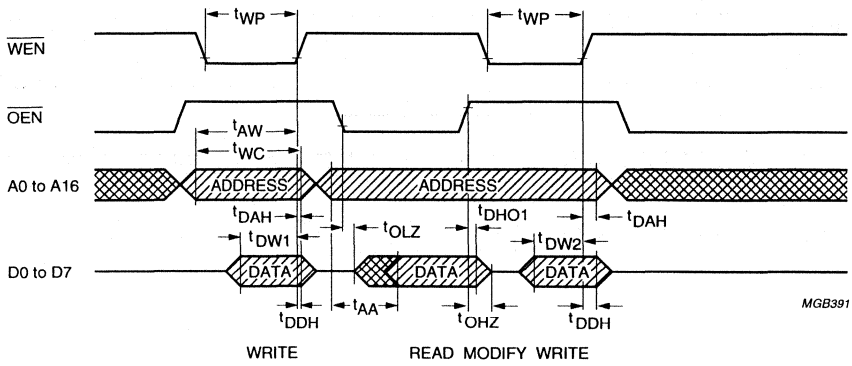


Fig.15 Fast SRAM write cycle timing; RTim = "01".

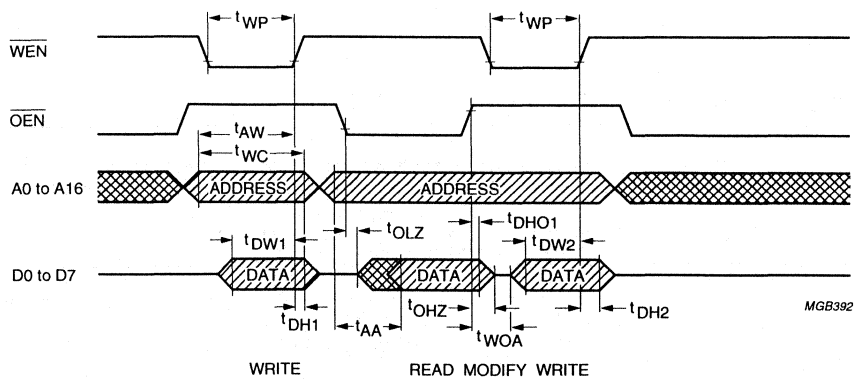


Fig.16 Fast SRAM write cycle timing; RTim = "10".

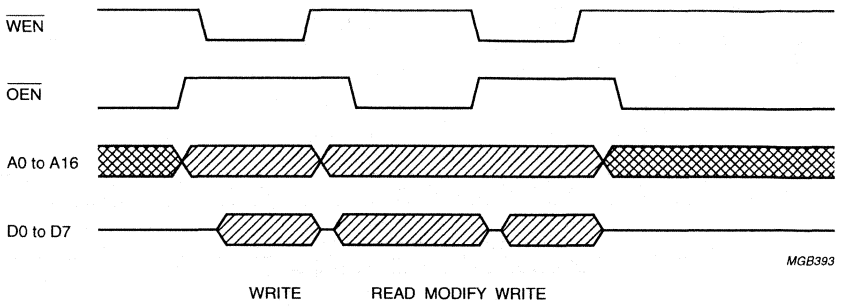


Fig.17 Fast SRAM write cycle timing; RTim = "11".

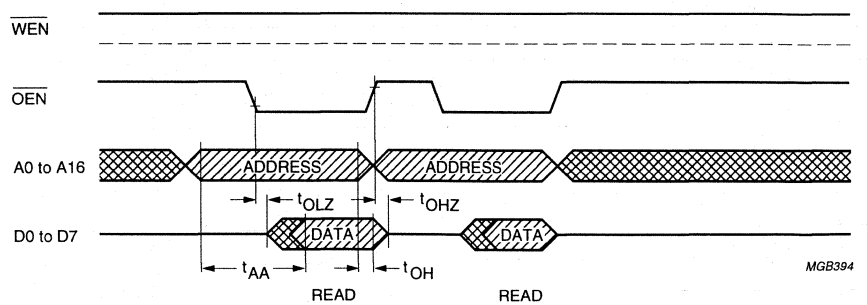


Fig.18 Slow SRAM read cycle timing.

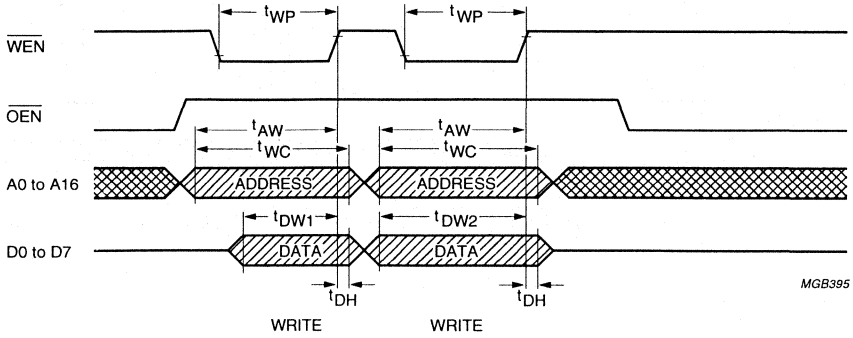


Fig.19 Slow SRAM write cycle timing.

Table 16 Timing values for Figs 10 to 12.

SYMBOL	VALUE (ns)
t_{RP}	≥110
t_{RAS}	≥510
t_{RCD}	≥70
t_{CP}	≥30
t_{CAS}	≥100
t_{ASR}	≥100
t_{RAH}	≥25
t_{ASC}	≥30
t_{CAM}	≥100
t_{DS}	≥25
t_{DH}	≥100
t_{WCS}	≥30
t_{WCH}	≥100
t_{RAC}	≤160
t_{CAC}	≤80

Table 17 Timing values for Figs 13 to 17.

SYMBOL	VALUE (ns)
t_{WP}	≥140
t_{AW}	≥180
t_{WC}	≥200
t_{DW}	≥72
t_{DM}	≥25
t_{AA}	≤240
t_{HC}	≥250

Table 18 Timing values for Figs 18 and 19.

SYMBOL	VALUE (ns)
t_{WP}	≥225
t_{AW}	≥260
t_{WC}	≥300
t_{DW}	≥140
t_{DM}	≥25
t_{AA}	≤280

Read/write connections

TCLOCK

This output pin is the 3.072 MHz clock output for the read and write amplifiers, it should be connected directly to the WCLOCK pin of the write amplifier and to the RDCLK pin of the read amplifier.

RDMUX

This input pin carries the time multiplexed analog tape channel signals from the read amplifier.

$V_{ref(n)}$ AND $V_{ref(p)}$

These are the lower and upper voltage reference inputs for the ADC in the digital equalizer part of SAA3323.

BIAS

This pin defines a bias current for the ADC. It should be connected to the analog supply voltage V_{DDA} via a 47 kΩ resistor.

RDSYNC

This output line provides synchronization information for the read Amplifier data transfers. The relationship between TCLOCK, RDSYNC and the channel information carried by the RDMUX line is given in Fig.20. This pin should be connected directly to the RDSYNC pin of the read amplifier. When the digital equalizer in SAA3323 is in search mode this pin will be HIGH ensuring that only the AUX channel is processed by the SAA3323.

WDATA

This output pin is the multiplexed data and control line for the write amplifier. Figure 21 shows the manner in which this information is multiplexed onto WDATA. The WDATA pin should be connected directly to the WDATA pin of the write amplifier.

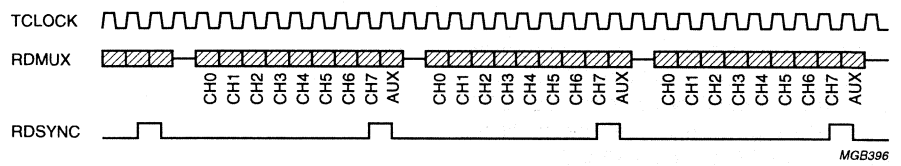


Fig.20 RDMUX, RDSYNC and TCLOCK timing.

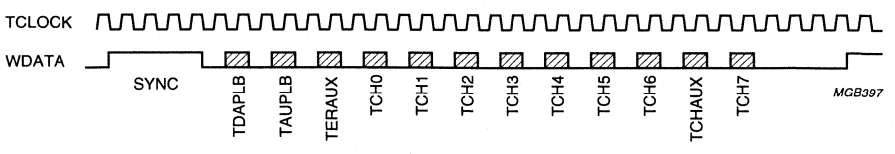


Fig.21 WDATA and TCLOCK timing.

Tape deck capstan control connections

SPEED

This pin outputs a pulse width modulated signal that may be used for controlling the tape capstan of the deck.

Operation of the SPEED control signal

Table 19 gives the sources that determine the duty factor of the SPEED signal. Note that the 3-state SPEED output may be put into high-impedance state by programming the TFE setting by bit HiZSpd.

Table 19 SPEED signal duty factor.

MODE	µCSPD	SOURCE FOR SPEED DUTY FACTOR
DPAP	0	tape(1)
DPAP	1	µC(2)
DPAR	0	tape(1)
DPAR	1	µC(2)
DRAR	0	50%(3)
DRAR	1	µC(2)

Notes

1. "Tape" means that the duty factor has been calculated from the played back main data tape signal. When tape is the source for the duty factor of the SPEED signal, the type of regulation can be chosen with the TFE settings bits EnFReg and SelNBand.
2. "µC" means that the microcontroller programs the duty factor via the SPDDTY register.
3. "50%" means that the duty factor is fixed at 50%.

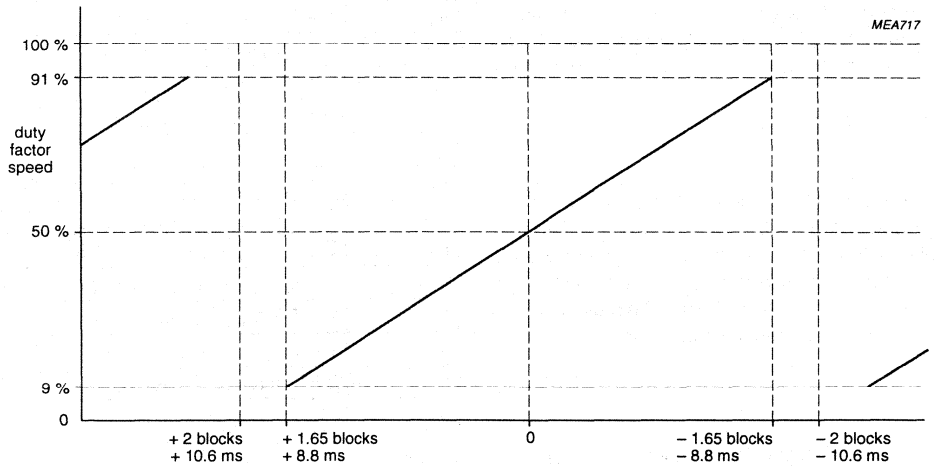


Fig.22 SPEED regulation duty factor as a function of phase characteristic.

If EnFReg is programmed 'LOW' then there is phase regulation of the capstan speed. The period of the pulse width modulated SPEED signal is 41.66 µs. The SAA3323 performs a new calculation to determine the duty factor of SPEED once every 21.33 ms, giving a sampling rate of approximately 46.9 Hz. This calculation is basically a phase comparison between the incoming Main Data tape frame and an internally generated reference. The SPEED duty factor as a function of phase characteristic is shown in Fig.22. As shown the duty factor increases monotonously from approximately 9% when the incoming Main Data tape frame is 1.65 tape blocks (8.8 ms) too early up to 91% when it is 1.65 tape blocks (8.8 ms) too late. Outside of a ±2 tape blocks range the pulse width characteristic overflows and repeats itself forming a sawtooth pattern. The SAA3323 has an internal buffer of ±8.8 ms outside of which the phase information is invalid.

If EnFReg is programmed 'HIGH' then the above description is over-ridden with frequency information. If the incoming main data bit rate deviation from the nominal 96000 bits/s rate is less than the Phase Only Threshold (POT) then the control is as described above in the phase control description. If the deviation is more than the Frequency Only Threshold (FOT) then the SPEED information is gated with the phase information resulting in the SPEED signal being continuously HIGH or LOW while the condition continues. If the deviation is between the POT and the FOT then the frequency information is gated with the Phase information for 50% of the time.

The deviation thresholds POT and FOT are programmable via the TFE settings bit SelNBand.

Table 20 POT and FOT deviation thresholds.

SelNBand	POT (DEVIATION FROM NOMINAL)	FOT (DEVIATION FROM NOMINAL)
0	±6%	±9%
1	±3%	±4.5%

If SLEEP is 'HIGH' then the state of the SPEED signal will be the state that it was in just before the SAA3323 went into sleep. Thus if SPEED was HIGH just before sleep it will stay HIGH during sleep. The same applies if it was LOW or if it was in 'high-Z' state. Note that a reset of the SAA3323 will take the SPEED signals out of 'high-Z' state.

Microcontroller connections

$\overline{\text{L3REF}}$

This active LOW output pin indicates the start of a time segment, it goes LOW for 5.2 µs once every 42.66 ms approximately and can be used for generating interrups for the microcontroller. If a re-synchronization occurs then the time between the occurrences van vary. This pin can be connected directly to the interrupt input of the microcontroller.

L3CLK

This input pin is the clock line for the microcontroller interface.

L3DATA

This input/output pin is the serial data line for the microcontroller interface.

L3MODE

This input determines the type of transfer that is occurring between the microcontroller and the SAA3323. If L3MODE is LOW then a device address can be sent by the microcontroller. If L3MODE is HIGH then a data transfer may be occurring.

L3INT

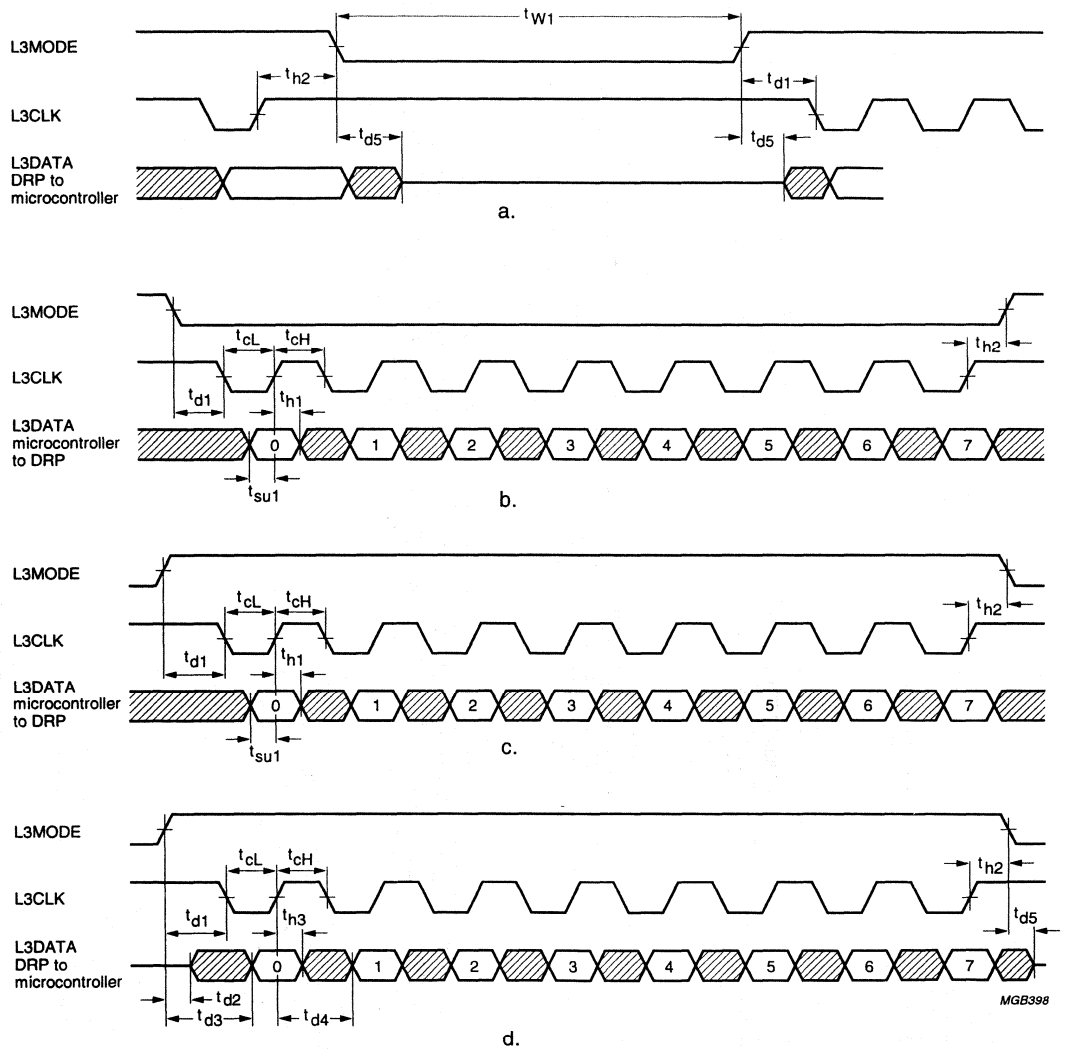
This pin carries interrupts from the digital equalizer module. It can also be programmed to reflect the state of the AENV, LABEL and VIRGIN signals.

Table 21 Timing values for Fig.23.

SYMBOL	TIME[1]
t_{W1}	$T + t_{su\ (L3MODE)} + t_{h\ (L3MODE)}$; $t_{w1} \geq 200$ ns
t_{d1}	$T + t_{su\ (L3MODE)} + t_{h\ (L3CLK)}$; $t_{d1} \geq 200$ ns
t_{h2}	$T + t_{su\ (L3CLK)} + t_{h\ (L3MODE)}$; $t_{h2} \geq 200$ ns
t_{d2}	$T + t_{su\ (L3CLK)} + t_{d\ (L3DATA)}$; $t_{d2} \leq 250$ ns
t_{d5}	$0 \leq t_{d5} \leq 50$ ns
t_{cL}	$T + t_{su\ (L3CLK)} + t_{h\ (L3CLK)}$; $t_{cL} \geq 200$ ns
t_{cH}	$T + t_{su\ (L3CLK)} + t_{h\ (L3CLK)}$; $t_{cH} \geq 200$ ns
t_{su1}	$T + t_{su\ (L3DATA)} + t_{h\ (L3CLK)}$; $t_{su1} \leq 200$ ns
t_{h1}	$T + t_{su\ (L3CLK)} + t_{h\ (L3DATA)}$; $t_{h1} \leq 35$ ns
t_{d3}	$2 \times T + t_{su\ (L3MODE)} + t_{d\ (L3DATA)}$; $t_{d3} \leq 250$ ns
t_{h3}	$T + t_{h\ (L3CLK)} + t_{d\ (L3DATA)}$; $t_{h3} \geq 50$ ns
t_{d4}	$2 \times T + t_{su\ (L3CLK)} + t_{d\ (L3DATA)}$; $t_{d4} \leq 410$ ns
t_{d4}[2]	$3 \times T + t_{su\ (L3CLK)} + t_{d\ (L3DATA)}$; $t_{d4} \leq 575$ ns

Notes

1. T is the period of the master clock on the chip.
2. t_{d4} is the delay time between the last bit of a byte and first bit of the next byte, if no 'halt' is used.



a. Halt mode.
b. Addressing mode.
c. Data mode (transfer from microcontroller to SAA3323).
d. Data mode (transfer from SAA3323 to microcontroller).

Fig.23 L3 interface timing and typical transfers (1).

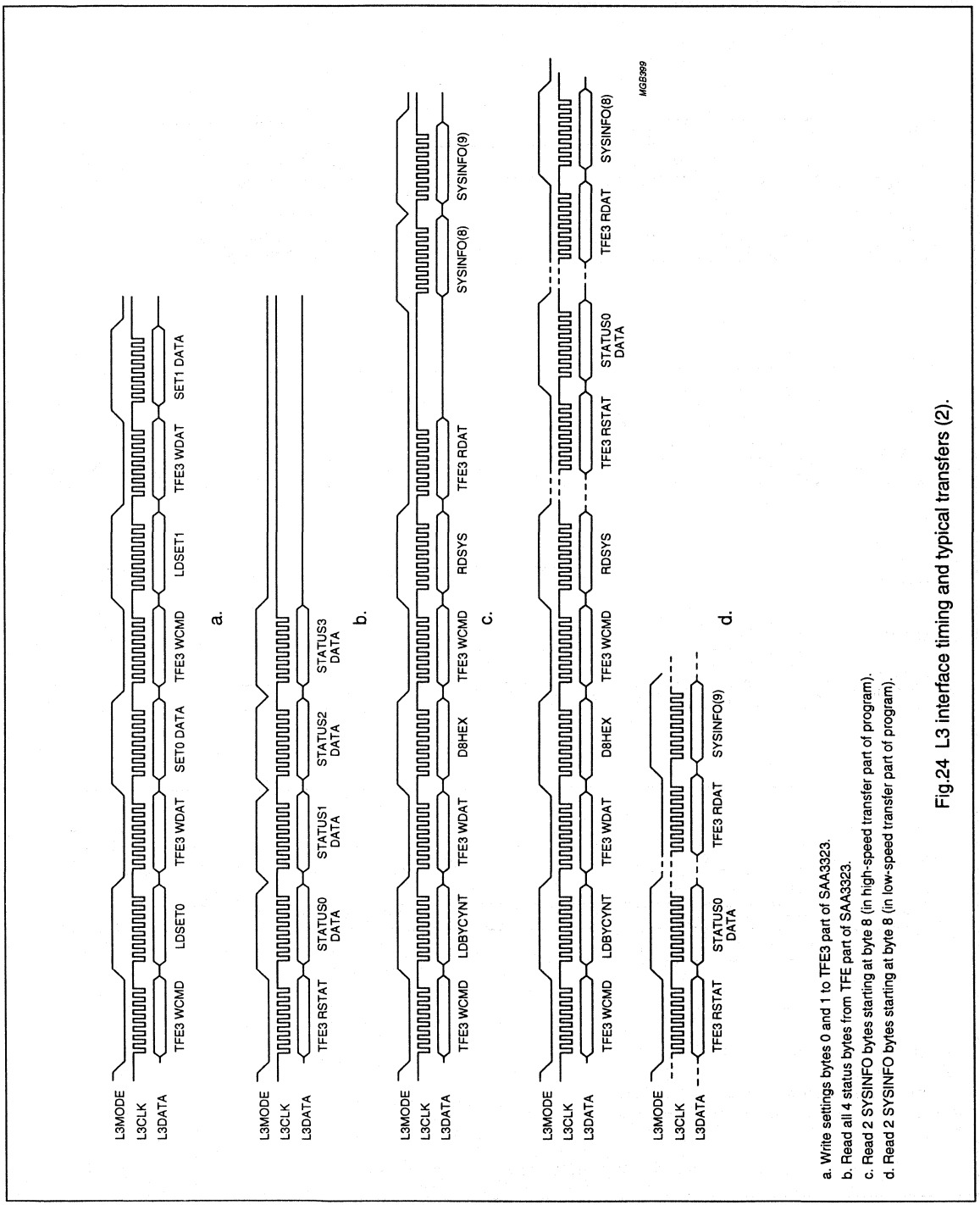


Fig.24 L3 interface timing and typical transfers (2).

a. Write settings bytes 0 and 1 to TFE3 part of SAA3323.
b. Read all 4 status bytes from TFE part of SAA3323.
c. Read 2 SYSINFO bytes starting at byte 8 (in high-speed transfer part of program).
d. Read 2 SYSINFO bytes starting at byte 8 (in low-speed transfer part of program).

SAA3323 test pins

TEST0 TO TEST3

These input pins are for test only, **do not connect**.

AZCHK

This output pin indicates the occurrence of a tape channel sync symbol on tape channels TCH0 and TCH7, the distance between the pulses for the TCH0 and TCH7 channels gives a measure of the azimuth error between the tape and head alignment. Figure 25 shows the typical timing for this signal.

ERCOSTAT

This output pin can be connected to a symbol error rate measurement system.

Port expansion pins

PINI

This input pin is connected directly to the PINI bit in the status byte 1, it can be read by the microcontroller, and may be used for any CMOS level compatible input signals.

PINO1

This output pin is connected directly to the PINO1 bit of the TFE settings 0 register. The microcontroller can set or reset this pin.

PINO2 TO PINO5

Depending upon the type and the size of system RAM used, some or all of these Port expander output pins may be available, (please see Section "RAM connections" "A10 and A12 to A16" on interfacing to the RAM pins).

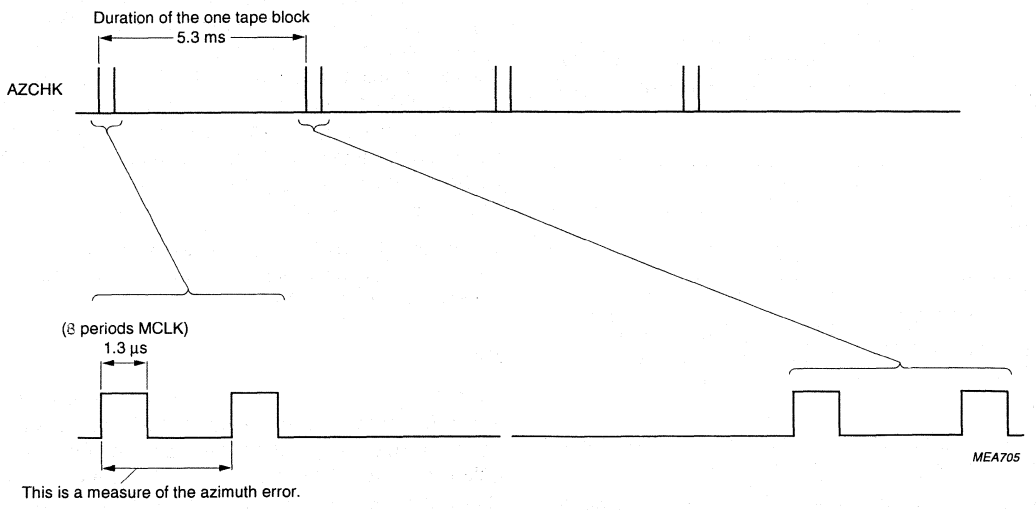
Supply pins

V_{DD1} TO V_{DD6}

These are the supply pins, all of these pins must be connected. We recommend that each power supply pin pair (i.e. V_{DD1} to V_{SS1}, V_{DD2} to V_{SS2}, etc.) be decoupled using a 22 nF capacitor as close as is physically possible to the pins of the SAA3323.

V_{SS1} TO V_{SS6}

These are the supply ground pins, all of which must be connected.



Nominal Inter Frame Gap (IFG) lasts 660 µs.

Fig.25 AZCHK timing.

V_{DD7}

This is the supply pin for the output buffers to the data lines of the system RAM. It should always be connected externally. Decouple this pin with a 22 nF capacitor to the V_{SS7} pin.

V_{SS7}

This is the ground supply pin for the output buffers of the data lines of the system RAM. This pin is connected internally to all the supply ground pins (V_{SS1} to V_{SS6}), however it should always be connected externally.

Auxiliary envelope detection

INTMASK

INTMASK is a interrupt mask register. This register sets the mode of operation for the interrupt interface, and is writable only.

Table 22 Interrupt mask register.

BIT	7	6	5	4	3	2	1	0
Meaning	BP1	BP0	Vup(1)	AEup(2)	AEdn(3)	Lup(4)	Ldn(5)	ECZ(6)
Default	0	0	0	0	0	0	0	0

Notes

1. Vup ≡ rising edge of VIRGIN interrupt.
2. AEup ≡ rising edge of AUX envelope interrupt.
3. AEdn ≡ falling edge of AUX envelope interrupt.
4. Lup ≡ rising edge of LABEL interrupt.
5. Ldn ≡ falling edge of LABEL interrupt.
6. ECZ ≡ AUX envelope counter has just reached zero interrupt.

BP1 AND BP0 (BYPASS)

If any of the bypass bits are HIGH then the interrupts are not passed on to the microcontroller, instead the level of the corresponding signal is available an the interrupt pin.

Table 23 BP1 and BP0.

BP		EFFECT OF BYPASS
1	0	
0	0	no bypass
0	1	LAB on L3INT pin; note 1
1	0	AENV on L3INT pin; note 2
1	1	VIR on L3INT pin; note 3

Notes

1. LAB = LABEL (HIGH if a LABEL condition is detected in the envelope of the AUX channel).
2. AENV = envelope of the AUX channel (1 bit binary).
3. VIR = VIRGIN (indicated by the total [continuous] absence of signal on the AUX channel).

The AUX envelope information is only valid when the digital equalizer is in search mode and when the tape speed is between the values of 3 to 48 × nominal tape speed. The timing relationships between the AUX channel input signal, AENV, LAB and VIR are shown in Figs 26 to 28. The delays t_{d1} and t_{d2} are between 0.25 and $0.5t_{AUX}$ (AUX envelope periods). The delays t_{d3}, t_{d4}, t_{d5} and t_{d6} are between 2 and $6t_{AUX}$ (AUX envelope periods).

When using the digital equalizer in search mode first program the digital equalizer to search mode, then program the INTMASK register.

MASK

If the BP1 and BP0 bits are LOW then the mask bits take effect. Any combination of the mask bits may be HIGH, enabling the corresponding interrupts. The interrupt pin L3INT is active LOW when used for interrupts and active HIGH when used for bypassing. So if it is not in bypass mode and at least one of the interrupts has occurred it will go LOW and stays LOW until DEQ status byte 0 has been read. Extra interrupts that occur after the first interrupt and before the DEQ status byte 0 is read are seen in the status register. Extra interrupts that occur after the status byte

has been read will generate a new interrupt. Interrupts that are already noted in the digital equalizer Status 0 are cleared by reading it.

Table 24 Digital equalizer STATUS0.

BIT	7	6	5	4	3	2	1	0
Meaning	BKSW(1)	TEST	Vup(2)	AEup(3)	AEdn(4)	Lup(5)	Ldn(6)	ECZ(7)

Notes

1. BKSW (filter bank switched) indicates that the last main data coefficients sent to the digital equalizer have been activated.
2. Vup indicates whether an interrupt caused by the rising edge of VIRGIN has occurred.
3. AEup indicates whether an interrupt caused by the rising edge of AUX envelope has occurred.
4. AEdn indicates whether an interrupt caused by the falling edge of AUX envelope has occurred
5. Lup indicates whether an interrupt caused by the rising edge of LABEL has occurred.
6. Ldn indicates whether an interrupt caused by the falling edge of LABEL has occurred.
7. ECZ indicates that the AUX envelope counter has reached zero.

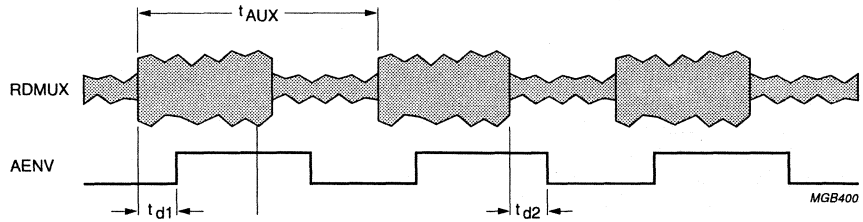


Fig.26 AUX channel envelope to AENV delays.

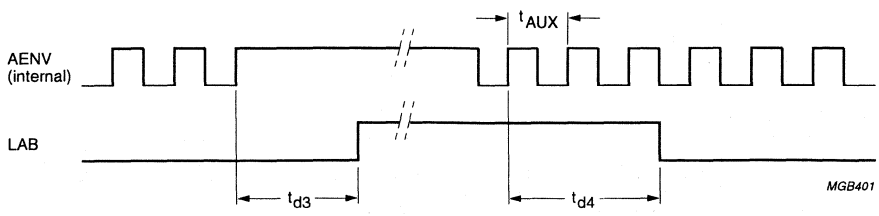


Fig.27 AENV to LAB delays.

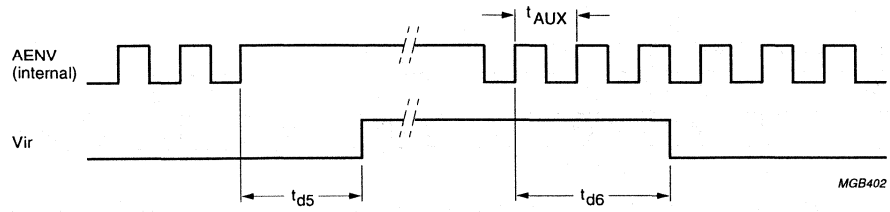


Fig.28 AENV to VIR delays.

Table 25 Digital equalizer STATUS1.

BIT	7	6	5	4	3	2	1	0
Meaning	–	–	–	–	–	VIR(1)	AENV(2)	LAB(3)

Notes

1. VIR gives the state of the VIRGIN signal.
2. AENV represents the state of the AENV signal.
3. LAB gives the state of the LAB signal.

AUX envelope count (AECNT) register

This 16 bit register is used for loading the AUX envelope counter and for reading the state of that counter, it is therefore readable and writable as 2 bytes. Least Significant Byte first.

Table 26 AECNT register.

AECNT	LEAST SIGNIFICANT BYTE								MOST SIGNIFICANT BYTE							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Meaning	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8

Search speed (SSPD) register

$$\text{Search speed} = \left(2^{SR}\right) \times \left(\frac{51.2}{SV}\right) \times \text{normal speed}$$

Table 27 Search speed register.

BIT	7	6	5	4	3	2	1	0
Meaning	SVF(1)	SV4(2)	SV3(2)	SV2(2)	SV1(2)	SV0(2)	SR1(3)	SR0(3)

Notes

1. SVF speed validation flag, if HIGH then the search speed measurement is invalid.
2. SV4 to SV0 search speed value.
3. SR1 and SR0 search speed range.

ANAEYE register

Table 28 ANAEYE register analog eye pattern selection register.

BIT	7	6	5	4	3	2	1	0
Meaning	–	–	–	AEN[1]	ACHN3[2]	ACHN2[2]	ACHN1[2]	ACHN0[2]
Default	0	0	0	0	0	0	0	0

Notes

1. AEN analog eye pattern output enable. If this bit is LOW the Digital-to-Analog Converter (DAC) is switched off and the output is HIGH.
2. ACHN3 to ACHN0 select channel for analog eye output.

Table 29 ACHN3 to ACHN0 channel selections for analog eye output.

ACHN				CHANNEL ON ANAEYE
3	2	1	0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	AUX

T1sel register

Table 30 T1SEL register CHTST1 pin selection register.

BIT	7	6	5	4	3	2	1	0
Meaning	–	T1F2	T1F1	T1F0	T1C3	T1C2	T1C1	T1C0
Default	0	0	0	0	0	0	0	0

Table 31 T1C3 to T1C0 CHTST1 pin channel selections.

T1C				CHANNEL ON CHTST1
3	2	1	0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	AUX

Table 32 T1F2 to T1F0 CHTST1 pin function selections.

T1F			FUNCTION OF CHTST1 PIN
2	1	0	
0	0	0	off; logic 0
0	0	1	digital eye pattern
0	1	0	sliced data
0	1	1	bit clock
1	0	0	clock extraction frequency

The digital eye pattern is in 8 bits two's complement notation, the sliced data and the bit clock give the current binary state of the corresponding signals, and the clock extraction frequency output is in 8 bits offset binary format. The timing diagrams for the digital eye pattern output and the clock extraction frequency output are shown in Fig.29.

T2sel register

Table 33 T2SEL register CHTST2 pin selection register.

BIT	7	6	5	4	3	2	1	0
Meaning	–	T2F2	T2F1	T2F0	T2C3	T2C2	T2C1	T2C0
Default	0	0	0	0	0	0	0	0

Table 34 T2C3 to T2C0 CHTST2 pin channel selections.

T2C				CHANNEL ON CHTST2
3	2	1	0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	AUX

Table 35 T2F2 to T2F0 CHTST2 pin function selections.

T2F			FUNCTION OF CHTST2 PIN
2	1	0	
0	0	0	off; logic 0
0	0	1	digital eye pattern
0	1	0	sliced data
0	1	1	bit clock
1	0	0	clock extraction frequency

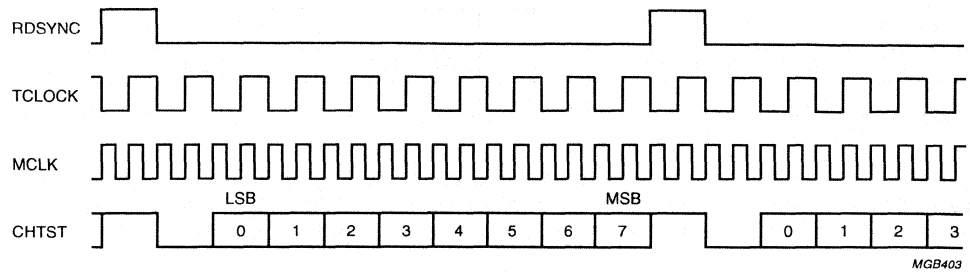


Fig.29 CHTST1 and CHTST2 output timing.

Table 36 DEQSET digital equalizer settings.

BIT	7	6	5	4	3	2	1	0
Meaning	–	–	–	–	–	ACup[1]	DM1	DM0
Default	0	0	0	0	0	0	0	0

Note

1. ACup is the AUX envelope counter direction is up. This setting caused the AUX envelope counter increment or to decrement by 1 every rising edge of the AUX envelope signal AENV.

DM1 and DM0

Table 37 DM1 and DM0 digital equalizer mode of operation.

DM		MODE OF OPERATION OF DIGITAL EQUALIZER
1	0	
0	0	normal[1]
0	1	search[2]
1	0	off[3]
1	1	off[3]

Notes

1. In normal mode the main data channels and the AUX channel are processed (equalized), the AUX channel envelope information is not processed.
2. In search mode only the AUX channel is processed by the digital equalizer.
3. Off means that the digital equalizer is put to sleep (low power), this can be used for example in portable recording equipment. RDSYNC is HIGH if off mode. Also note that the other digital equalizer registers are not addressable while the digital equalizer is in off mode.

CLKSET

Table 38 CLKSET clock extraction settings.

BIT	7	6	5	4	3	2	1	0
Meaning	LEAE[1]	FR1	FR0	GNOR	GE1	GE0	RD1	RD0
Default	1	0	0	1	1	0	1	0

Note

1. LEAE (leakage enable): this setting enables a leakage function in the PLL clock extraction loop filter. This gives a slightly improved performance with high SER tapes at the cost of a slight decrease in dynamic performance. For home (static) applications program this bit to logic 1 and for portable applications to logic 0.

Table 39 FR1 and FR0 clock extraction frequency range control.

FR		EFFECT ON PLL FREQUENCY LOOP
1	0	
0	0	range ±8%
0	1	range ±16%
1	0	range ±22%
1	1	range ±28%

Note that in the (FR = 0) range the clock extraction stays in its normal range only, hence it does not enter the extended range.

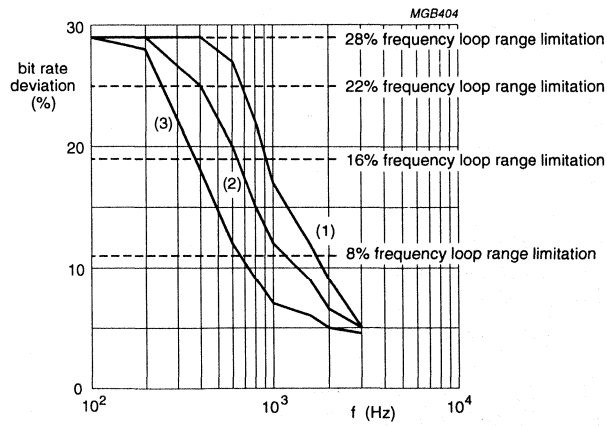
Figure 30 shows the lock characteristic of the clock extraction PLL.

Table 40 GNOR gain in normal frequency range mode of clock extraction.

GNOR	EFFECT ON GAIN IN NORMAL RANGE
0	gain 2; for portable (mobile) applications
1	gain 1; for home (static) applications

Table 41 GE1 and GE0 gain in extended frequency range mode of clock extraction.

GE		EFFECT ON PLL GAIN IN EXTENDED RANGE
1	0	
0	0	gain 2
0	1	gain 3
1	0	gain 4
1	1	gain 5; do not use



(1) Gain 4.
(2) Gain 3.
(3) Gain 2.

Fig.30 Clock extraction PLL lock characteristic.

RD1 and RD0 return delay

This is the delay before returning to normal mode after being in 'extended range mode' (i.e. the number of consecutive channel clock bit periods where the bit clock frequency falls within the normal range before the clock extraction returns to normal frequency mode).

Table 42 RD1 and RD0 return delay.

RD		DELAY IN BITS TO RETURN TO NORMAL MODE
1	0	
0	0	64
0	1	128
1	0	256
1	1	512

SYSINFO and AUX data offsets in the SAA3323

AUX data consists of 4 blocks of 36 bytes, one block being transferred in each (n) time segment.

The 128 bytes in each tape frame contain SYSINFO. The SYSINFO bytes can for convenience, be considered as being grouped into 4 SYSINFO blocks with:
SYSBLK0 → SI0 to SI31, SYSBLK1 → SI31 to SI63, etc.

In modes DPAP and DRAR SYSINFO transfers may occur in two ways:

1. 4 blocks of 36 bytes, one block being transferred to the SAA3323 in each time segment.
2. 1 block of 128 bytes being transferred in time segment 1.

In mode DRAR SYSINFO must be transferred as 4 blocks of 32 bytes, one block in each segment.

Figures 31 to 34 show the offsets between the SYSINFO and AUX and the time segment counter, for the various modes of operation of the SAA3323.

Table 43 Block offsets with respect to time segment.

MODE	DESCRIPTION
DPAP	SYSBLK = (SNUM + 3) MOD4; or read all 4 SYSINFO blocks when SNUM = logic 0; if AUX and main were recorded simultaneously then AUXBLK = (SNUM + 1) MOD4; else read and interpret 1 AUX block in each time segment.
DRAR	SYSBLK = SNUM; AUXBLK = (SNUM + 1) MOD4
DPAR	SYSBLK = (SNUM + 3) MOD4; or read all 4 SYSINFO blocks when SNUM = logic 0

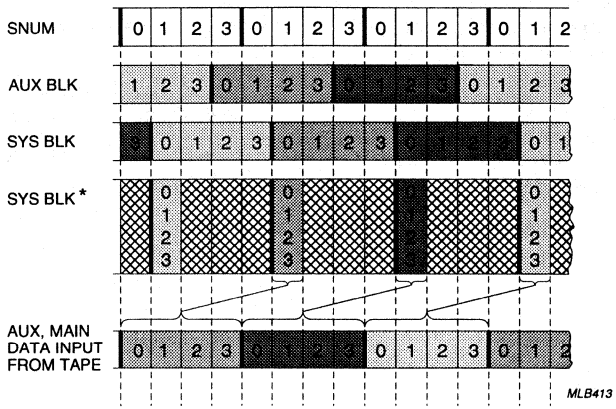


Fig.31 SYSINFO and AUX block delays in DPAP mode; audio and AUX simultaneously recorded.

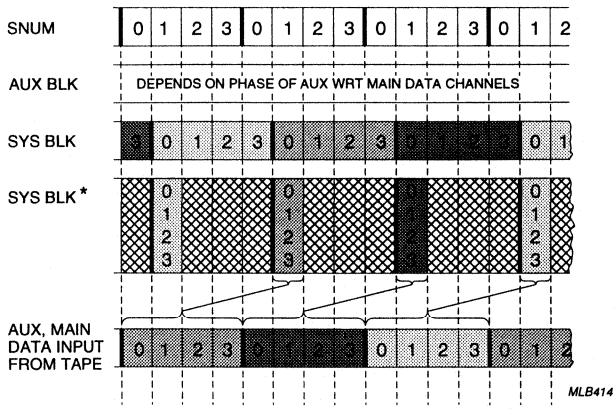


Fig.32 SYSINFO and AUX block delays in DPAP mode; audio and AUX separately recorded.

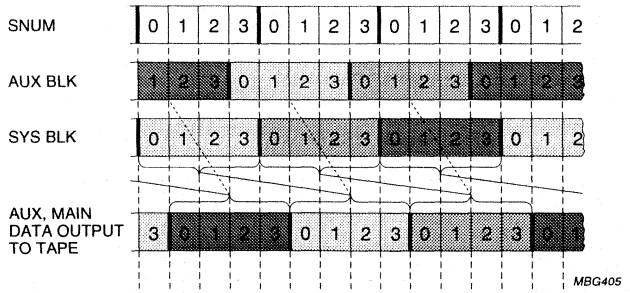


Fig.33 SYSINFO and AUX block delays in DRAR mode.

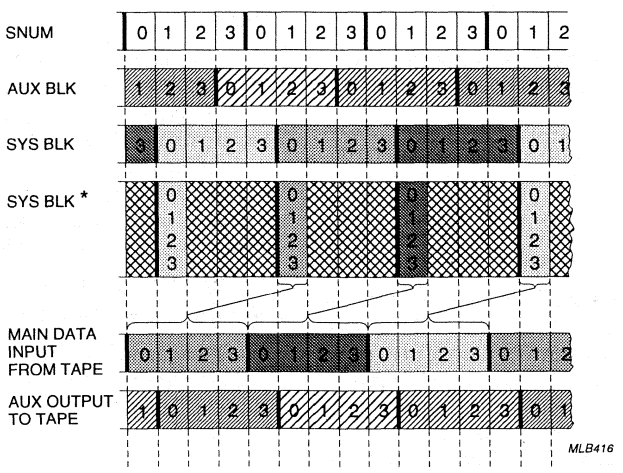


Fig.34 SYSINFO and AUX block delays in DPAR mode.

Scratch pad RAM

The SAA3323 provides the microcontroller with a scratch pad RAM that the microcontroller can use for whatever it likes. The size of the scratch pad depends upon the size and type of RAM used with the SAA3323. The locations in the scratch pad RAM may be written and read in 8 bit or 12 bit units.

The RAM may be viewed as having up to 4 quarters, the availability of these quarters for the scratch pad RAM is given in Table 44.

Table 44 Availability of RAM quarters for the scratch pad RAM.

RTYPE		TYPE OF RAM USED	AVAILABLE RAM QUARTERS YZ[1]
1	0		
0	0	DRAM 64K × 4	00
0	0	DRAM 256K × 4	00, 01, 10 and 11
0	1	SRAM 32K × 8 fast	00
1	0	SRAM 128K × 8 fast	00, 01, 10 and 11
1	1	SRAM (2×) 32K × 8 slow	00
1	1	SRAM 128K × 8 slow	00 and 10

Note

1. In RAM quarter YZ = 00, the scratch pad is arranged as 6 pages, where each page consists of 7 columns × 64 rows. The pages are numbered **0 to 5**, the columns **1 to 7** and the rows **0 to 63**. This gives a total of (6 × 7 × 64) 2688 locations.

   In each of the RAM quarters YZ = 01, 10 and 11 the scratch pad is arranged as 6 pages where each page consists of 8 columns × 448 rows. The pages are numbered **0 to 5**, the columns **0 to 7** and the rows **0 to 447**. This gives then a total of (6 × 8 × 448) 21504 locations per RAM quarter YZ.

During communication with the scratch pad RAM, the RAM quarter YZ is chosen when sending the RDDRAC, RDWDRAC, WRDRAC or WRWDRAC commands to the TFE module.

Use of the scratch pad RAM outside the specified ranges is not allowed and it may upset the operation of the SAA3323.

As with SYSINFO and AUX transfers can occur at high speed at all times except the second half of time segment 0, that is when the status bit SLOWTFR is HIGH. When SLOWTFR is HIGH the microcontroller must poll the status bit RFBT to investigate when a transfer can occur.

Two addressing modes are available for the scratch pad, namely random access and auto-increment. For random access mode the address of each location is sent by the microcontroller to the SAA3323 before each location transfer. For auto-increment mode the address of the first location is sent by the microcontroller before the first location transfer, auto-incrementing of the row occurs then for all transfers until the end of the column.

The 8 bit transfers are initiated by the WRDRAC and RDDRAC commands, these transfers are each 1 byte per memory location, therefore the byte counter will increment after each byte transfer.

The 12 bit transfers are initiated by the WRDRAC and RDDRAC commands, these transfers are each 2 bytes per memory location. The first byte contains the 4 Most Significant Bits (MSBs) of the memory location in its 4 Least Significant Bits (LSBs) positions. The other bit positions being 'don't care'. The second byte contains the 8 LSBs of the memory location. The byte counter is incremented after the transfer of the second byte.

The RACCNT and BYTCNT registers are used for addressing the scratch pad.

For RAM quarter YZ = 00 the mapping of the scratch pad RAM address onto the RACCNT and BYTCNT registers is shown in Table 45.

Table 45 Mapping of scratch pad RAM address for RAM quarter YZ = 00.

REGISTER	RACCNT							BYTCNT							
BIT	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Value	P2	P1	P0	C2	C1	C0	1	1	R6	R5	R4	R3	R2	R1	R0

For The other three quarters of the RAM the mapping of the scratch pad RAM address onto the RACCNT and BYTCNT registers is shown in Table 46.

Table 46 Mapping of scratch pad RAM address for RAM quarter YZ = 01, 10 and 11.

REGISTER	RACCNT							BYTCNT							
BIT	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Value	P2	P1	P0	C2	C1	C0	R8	R7	R6	R5	R4	R3	R2	R1	R0

Mode changes

The possible mode changes for the TFE are shown in Table 47.

Table 47 Mode changes.

CURRENT MODE	NEW MODE		
	DPAP	DRAR	DPAR
DPAP	–	yes	yes
DRAR	yes	–	no
DPAR	yes	no	–

TIMING FOR SAA3323 MODE CHANGES

Mode change DPAP to DRAR

This mode change occurs at the end of the time segment in which the TFE module receives the new settings. Writing of the first Main and AUX data to tape starts at the start of the time segment 1 which occurs 2 'end of time segment 3' s after the mode change. The delay to writing to tape is approximately 222 ms, as shown in Fig.35.

If 'seamless appending' is required the new settings should be sent to the TFE module during time segment 2.

Mode change DPAP to DPAR

This mode change occurs at the first end of time segment 2 after the TFE module receives the new settings. Output of AUX to tape begins at the start of the following time segment 1, (i.e. approximately 85.3 ms after the mode change), as shown in Fig.36.

Mode change DRAR to DPAP

This mode change occurs at the first end of time segment 0 after the TFE module receives the new setting. Writing of Main and AUX data stops immediately after the mode change.The time segment jumps back to logic 0, URDA goes HIGH and stays HIGH for 5 time segments (i.e. approximately 213.3 ms) after which it goes LOW, as shown in Fig.37.

Mode change DPAR to DPAP

This mode change occurs at the first end of time segment 0 after the TFE module receives the new setting. The writing of AUX data to tape stops immediately after the mode change. The first AUX read from tape can be expected during the following time segment 0 or 1 (i.e. approximately 128 to 170.67 ms after the mode change), as shown in Fig.38.

Mode change DPAP to search

This mode change occurs almost instantaneously, program the digital equalizer module in SAA3323 to go to search mode, then program the interrupt mask register to select the required type of interrupt.

Mode change search to DPAP

This mode change occurs almost instantaneously, program the interrupt mask register to disable interrupts program the digital equalizer module of SAA3323 to go to normal mode. A re-synchronization will most likely occur when as result of the data being read from tape, thus causing URDA to go HIGH.

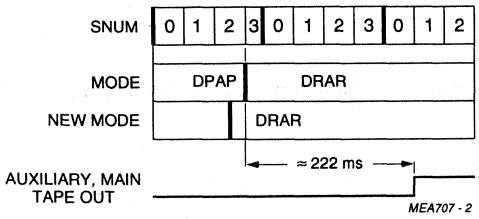


Fig.35 Mode change to DRAR.

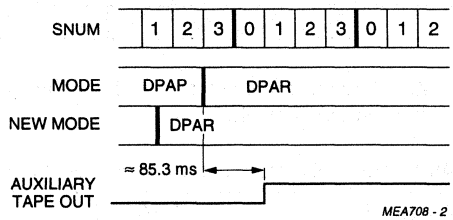


Fig.36 Mode change to DPAR.

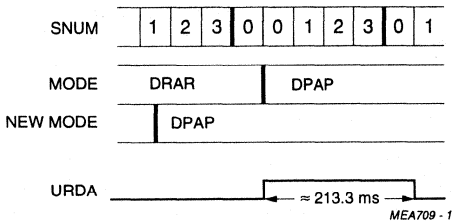


Fig.37 Mode change from DRAR.

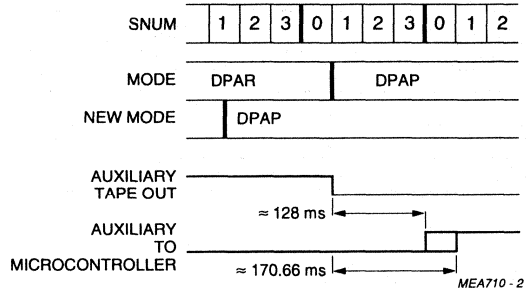


Fig.38 Mode change from DPAR.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.7	3.6	V
V_I	input voltage	note 1	−0.5	V_{DD} + 0.5	V
I_I	input current		−10	+10	mA
V_O	output voltage		tbf	tbf	V
I_O	output current		−20	+20	mA
I_{DD}	supply current		−	100	mA
I_{SS}	supply current		−100	−	mA
P_{tot}	total power dissipation		−	500	mW
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{es1}	electrostatic handling	note 2	−2000	+2000	V
V_{es2}	electrostatic handling	note 3	−200	+200	V

Notes

1. The input voltage must not exceed maximum supply voltage unless otherwise specified.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

DC CHARACTERISTICS

V_{DD} = 2.7 to 3.6 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.7	tbf	3.6	V
I_{DD}	supply current	digital plus analog; see Fig.39	−	28.1	−	mA
		inputs with internal pull-down to V_{SS}; all other inputs to V_{SS} or V_{DD}	−	−	100	µA
Inputs CLK24, L3CLK, L3MODE, PINI, SLEEP and SBMCLK						
V_{IL}	LOW level input voltage		−	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	−	V
I_I	input current	V_I = 0 V to V_{DD}; T_{amb} = 25 °C	−10	−	+10	µA
Inputs TEST0, TEST1 and TEST2						
V_{IL}	LOW level input voltage		−	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	−	V
I_I	input current	$V_I = V_{DD}$; T_{amb} = 25 °C	25	−	400	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input RESET						
V_{tLH}	positive-going threshold		–	–	$0.8V_{DD}$	V
V_{tHL}	negative-going threshold		$0.2V_{DD}$	–	–	V
V_{hys}	hysteresis (V_{tLH} to V_{tHL})		–	$0.3V_{DD}$	–	V
Outputs AZCHK, CHTST1, CHTST2, ERCOSTAT, L3INT, $\overline{\text{L3REF}}$, MCLK, PINO3, RDSYNC, SBDIR, SBEF, URDA, TCLOCK and WDATA						
V_{OH}	HIGH level output voltage	I_O = 1 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = –1 mA	–	–	0.4	V
Outputs A0 to A8, A9/$\overline{\text{CAS}}$, A10/$\overline{\text{RAS}}$, $\overline{\text{OEN}}$ and $\overline{\text{WEN}}$						
V_{OH}	HIGH level output voltage	I_O = 2 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = –2 mA	–	–	0.4	V
Outputs SPEED and PINO2						
V_{OH}	HIGH level output voltage	I_O = 1 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = –1 mA	–	–	0.4	V
I_{OZ}	3-state leakage current	V_I = 0 V to V_{DD}; T_{amb} = 25 °C	–10	–	+10	µA
Inputs/outputs SBCL, SBDA and SBWS						
V_{OH}	HIGH level output voltage	I_O = 1 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = –1 mA	–	–	0.4	V
V_{IL}	LOW level input voltage	outputs in 3-state	–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	outputs in 3-state	$0.7V_{DD}$	–	–	V
I_{OZ}	3-state leakage current	V_I = 0 V to V_{DD}; T_{amb} = 25 °C	–10	–	+10	µA
Inputs/outputs A11 to A16 and L3DATA						
V_{OH}	HIGH level output voltage	I_O = 2 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = –2 mA	–	–	0.4	V
V_{IL}	LOW level input voltage	outputs in 3-state	–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	outputs in 3-state	$0.7V_{DD}$	–	–	V
I_{OZ}	3-state leakage current	V_I = 0 V to V_{DD}; T_{amb} = 25 °C	–10	–	+10	µA
Inputs/outputs D0 to D7						
V_{OH}	HIGH level output voltage	I_O = 4 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = –4 mA	–	–	0.4	V
V_{IL}	LOW level input voltage	outputs in 3-state	–	–	0.8	V
V_{IH}	HIGH level input voltage	outputs in 3-state	2	–	–	V
I_{OZ}	3-state leakage current	V_I = 0 V to V_{DD}; T_{amb} = 25 °C	–10	–	+10	µA

Average current consumption

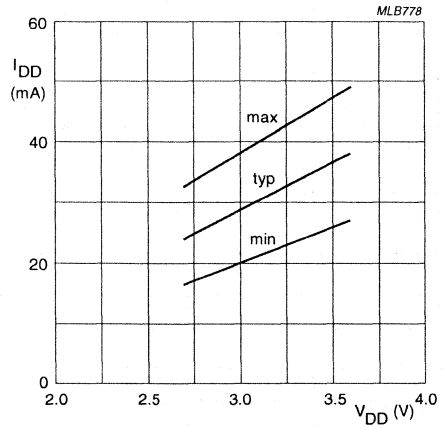


Fig.39 Average current consumption.

AC CHARACTERISTICS

V_{DD} = 2.7 to 3.6 V; T_{amb} = −40 to +85 °C; C_L = 10 pF on all outputs; see Fig.40; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock inputs						
C_I	input capacitance		–	–	10	pF
CLK24						
f_{CLK24}	clock frequency		24	24.576	25	MHz
t_{24L}	pulse width LOW		12	–	–	ns
t_{24H}	pulse width HIGH		12	–	–	ns
SBMCLK						
f_{SBMCLK}	clock frequency			6.144	12.5	MHz
t_{SCL}	pulse width LOW		30	–	–	ns
t_{SCH}	pulse width HIGH		30	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock output MCLK						
C_L	load capacitance		–	–	20	pF
t_d	delay time from SLEEP HIGH to SLEEP active		–	20	–	ns
f_{MCLK}	clock frequency			6.144	6.25	MHz
t_{MCL}	MCLK pulse width LOW		50	–	–	ns
t_{MCH}	MCLK pulse width HIGH		50	–	–	ns
t_{pd}	propagation delay time from rising edge of CLK24		–	–	65	ns
Inputs						
C_I	input capacitance		–	–	10	pF
L3CLK, L3MODE AND RESET						
t_{su}	set-up time to rising edge of MCLK		35	–	–	ns
t_h	hold time from rising edge of MCLK		0	–	–	ns
PINI						
t_{su}	set-up time to rising edge of MCLK		60	–	–	ns
t_h	hold time from rising edge of MCLK		0	–	–	ns
Outputs						
C_L	load capacitance		–	–	20	pF
A0 TO A8						
t_{pd}	propagation delay time from falling edge of CLK24		–	–	50	ns
A9/$\overline{\text{CAS}}$, A10/$\overline{\text{RAS}}$ AND $\overline{\text{OEN}}$						
t_{pd}	propagation delay time from falling edge of CLK24		–	–	50	ns
t_d	delay time from SLEEP HIGH to SLEEP active		–	20	–	ns
$\overline{\text{WEN}}$						
t_{pd}	propagation delay time					
	from falling edge of CLK24		–	–	50	ns
	from falling edge of $\overline{\text{WEN}}$ to rising edge of CLK24	long write pulse mode	–	–	50	ns
t_d	delay time from SLEEP HIGH to SLEEP active		–	20	–	ns
AZCHK, CHTST1, CHTST2, L3INT, PINO3, RDSYNC, SBEF AND WDATA						
t_{pd}	propagation delay time from rising edge of MCLK		–	–	45	ns
ERCOSTAT, $\overline{\text{L3REF}}$, SBDIR, SPEED, PINO2, URDA AND TCLOK						
t_{pd}	propagation delay time from rising edge of MCLK		–	–	55	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs/outputs						
C_I	input capacitance		–	–	10	pF
C_L	load capacitance		–	–	20	pF
A11 TO A16						
t_d	delay time from SLEEP HIGH to SLEEP active		–	25	–	ns
t_{pd}	propagation delay time from falling edge of CLK24		–	–	55	ns
D0 TO D3						
t_d	delay time from SLEEP HIGH to SLEEP active		–	20	–	ns
t_{su}	set-up time to falling edge of CLK24		5	–	–	ns
t_h	hold time from falling edge of CLK24		15	–	–	ns
t_{pd}	propagation delay time					
	from falling edge of CLK24		–	–	50	ns
	from rising edge of CLK24	early write mode	–	–	50	ns
D4 TO D7						
t_d	delay time from SLEEP HIGH to SLEEP active		–	25	–	ns
t_{su}	set-up time to falling edge of CLK24		5	–	–	ns
t_h	hold time from falling edge of CLK24		15	–	–	ns
t_{pd}	propagation delay time					
	from falling edge of CLK24		–	–	50	ns
	from rising edge of CLK24	early write mode	–	–	50	ns
L3DATA						
t_d	delay time from SLEEP HIGH to SLEEP active		–	25	–	ns
t_{su}	set-up time to rising edge of MCLK		35	–	–	ns
t_h	hold time from rising edge of MCLK		0	–	–	ns
t_{pd}	propagation delay time					
	from rising edge of MCLK		–	–	50	ns
	from L3MODE		–	–	45	ns
SBCL AND SBWS						
t_d	delay time from SLEEP HIGH to SLEEP active		–	25	–	ns
t_{su}	set-up time to rising edge of MCLK		40	–	–	ns
t_h	hold time from rising edge of MCLK		0	–	–	ns
t_{pd}	propagation delay time					
	from rising edge of SBMCLK		–	–	60	ns
	from rising edge of MCLK (3-state control)		–	–	55	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SBDA						
t_d	delay time from SLEEP HIGH to SLEEP active		–	25	–	ns
t_{su}	set-up time to rising edge of MCLK		35	–	–	ns
t_h	hold time from rising edge of MCLK		0	–	–	ns
t_{pd}	propagation delay time from rising edge of MCLK		–	–	55	ns

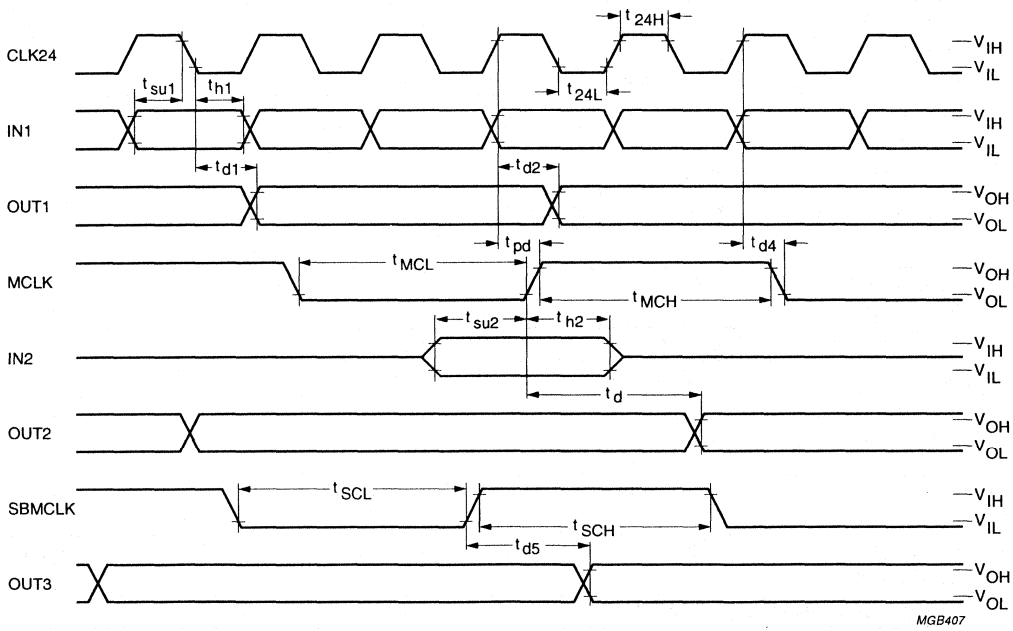


Fig.40 Timing for AC characteristics.

ADC CHARACTERISTICS

V_{DD} = 2.7 to 3.6 V; T_{amb} = −40 to +85 °C; C_L = 10 pF on TCLOCK output; see Fig.41; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	AC RDMUX ADC resolution		–	8	–	bits
$V_{ref(p)}$	positive reference voltage		–	–	V_{DD} − 0.5	V
$V_{ref(n)}$	negative reference voltage		0	–	–	V
ΔV_{ref}	$V_{ref(p)}$ to $V_{ref(n)}$		2.0	–	–	V
Z_i	input impedance	$V_{ref(p)}$ to $V_{ref(n)}$	700	1200	1500	Ω
		$V_{ref(n)}$ to V_{SS}	–	650	–	Ω
C_I	input capacitance (RDMUX)		–	–	15	pF
I_I	input current		–	–	90	μA
DNL	differential non-linearity		–	–	±0.99	LSB
S/(THD+N)	signal-to-total harmonic distortion plus noise ratio	−20 dB (FS); 100 to 500 kHz	24	–	–	dB
Timing						
T_{cy}	cycle time of CLK24		40	–	–	ns
t_{d1}	TCLOCK delay time from rising edge of CLK24	C_L = 10 pF	–	–	80	ns
t_{su}	RDMUX set-up time to falling edge of CLK24	Z_{source} < 150 Ω	60	–	–	ns
t_h	RDMUX hold time from falling edge of CLK24		40	–	–	ns

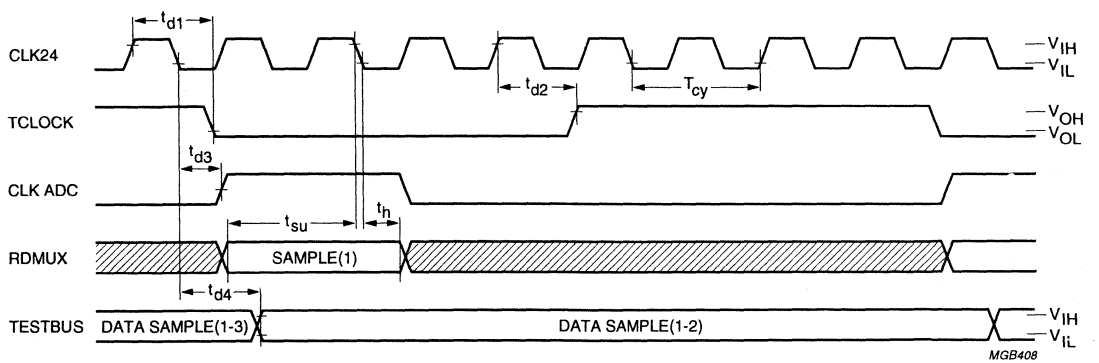


Fig.41 ADC timing.

DAC CHARACTERISTICS

V_{DD} = 2.7 to 3.6 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	DIGEYE/ANAEYE resolution		–	6	–	bits
V_o	ANAEYE output voltage	Z_L > 1 MΩ	–	(V_{DD} − 1.1) to V_{DD}	–	V

Radio data system demodulator (RDS) SAA6579

FEATURES

- Anti-aliasing filter (2nd order)
- Integrated 57 kHz bandpass filter (8th order)
- Reconstruction filter (2nd order)
- Clocked comparator with automatic offset compensation
- 57 kHz carrier regeneration
- Synchronous demodulator for 57 kHz modulated RDS signals
- Selectable 4.332 / 8.664 MHz crystal oscillator with variable dividers
- Clock regeneration with lock on biphase data rate
- Biphase symbol decoder with integrate and dump functions
- Differential decoder
- Signal quality detector
- Subcarrier output.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	3.6	5	5.5	V
V_{DDD}	digital supply voltage (pin 12)	3.6	5	5.5	V
I_{tot}	total supply current	–	6	–	mA
V_i	RDS input amplitude (RMS value, pin 4)	1	–	–	mV
V_{OH}	output level HIGH for signals RDDA, RDCL, QUAL and T57	4.4	–	–	V
V_{OL}	output level LOW for signals RDDA, RDCL, QUAL and T57	–	–	0.4	V
T_{amb}	operating ambient temperature	–40	–	+85	°C

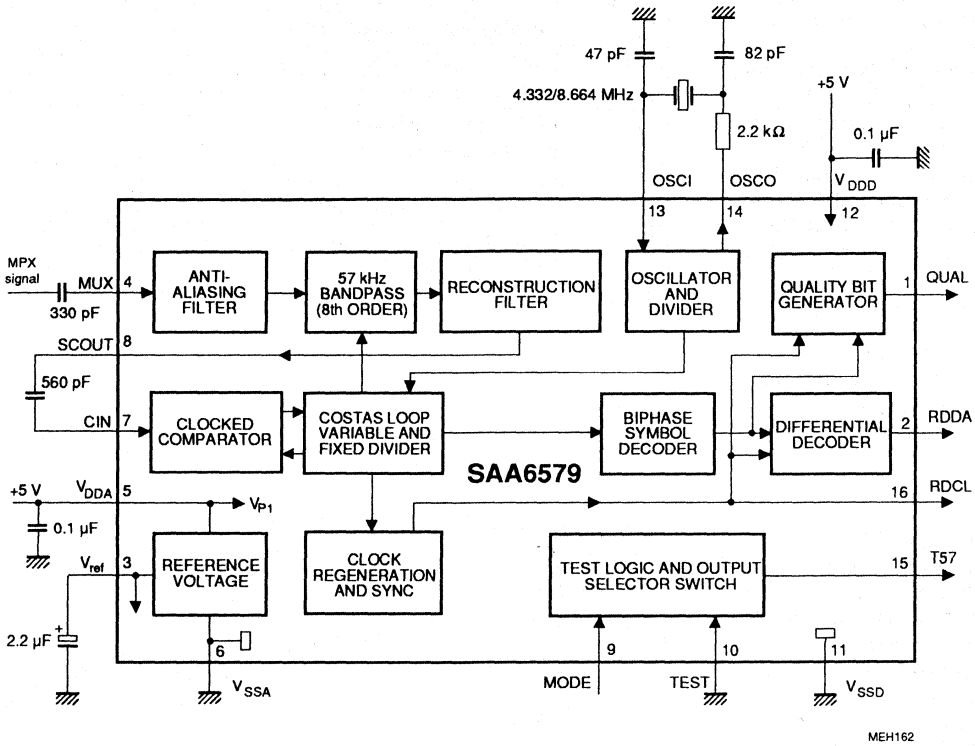
GENERAL DESCRIPTION

The integrated CMOS circuit SAA6579 is an RDS demodulator. It recovers the additional inaudible RDS information which is transmitted by FM radio broadcasting.

The data signal RDDA and the clock signal RDCL are provided as outputs for further processing by a suitable decoder (microcomputer). The operational functions of the device are in accordance with the CENELEC EN 50067.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA6579	16	DIL	plastic	SOT38GG6
SAA6579T	16	mini-pack	plastic	SOT162A



Via the pin MODE two different crystal frequencies can be used

MODE	x-tal clock
LOW	4.332 MHz
HIGH	8.664 MHz

Fig.1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
QUAL	1	quality indication output
RDDA	2	RDS data output
V_{ref}	3	reference voltage output (0.5 V_{DDA})
MUX	4	multiplex signal input
V_{DDA}	5	+5 V supply voltage for analog part
V_{SSA}	6	ground for analog part (0 V)
CIN	7	subcarrier input to comparator
SCOUT	8	subcarrier output of reconstruction filter
MODE	9	oscillator mode / test control input
TEST	10	test enable input
V_{SSD}	11	ground for digital part (0 V)
V_{DDD}	12	+5 V supply voltage for digital part
OSCI	13	oscillator input
OSCO	14	oscillator output
T57	15	57 kHz clock signal output
RDCL	16	RDS clock output

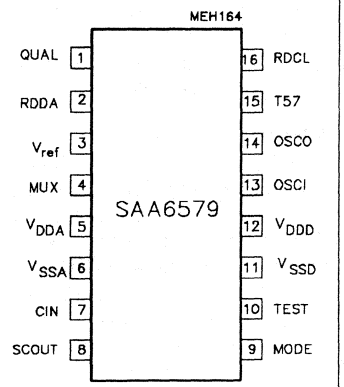


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); ground pins 6 and 11 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	supply voltage (pin 5)	0	6	V
V_{DDD}	supply voltage (pin 12)	0	6	V
V_n	voltage on all pins, grounds excluded	−0.5	V_{DD}+0.5	V
T_{stg}	storage temperature	−40	+150	°C
T_{amb}	operating ambient temperature	−40	+85	°C
V_{ESD}	electrostatic handling for all pins except pins 9 and 10			
	see note 1	±300	−	V
	see note 2	+1500	−3000	V

Notes to the limiting values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 Ω series resistor.

FUNCTIONAL DESCRIPTION

The SAA6579 is a demodulator circuit for RDS applications. It contains a 57 kHz bandpass filter and a digital demodulator to regenerate the RDS data stream out of the multiplex signal (MPX).

Filter part

The MUX signal is band-limited by a second-order anti-aliasing-filter and fed through a 57 kHz bandpass filter (8th order bandpass filter with 3 kHz bandwidth) to separate the RDS signals. This filter is formed in switched capacitor technique and clocked by a clock frequency of 541.5 kHz derived from the 4.332/8.664 MHz crystal oscillator. Then the signal is fed to the reconstruction filter to smooth the sampled and filtered RDS signal before it is output on pin 8.
The signal is AC-coupled to the comparator (pin 7), which is clocked with a frequency of 228 kHz (synchronized by the 57 kHz of the demodulator).

Digital part

The synchronous demodulator (Costas loop block) with carrier regeneration demodulates the internal coupled, digitized signal. The suppressed carrier is recovered from the two sidebands (Costas loop). The demodulated signal is low-pass-filtered in such a way that the overall pulse shape (transmitter and receiver) approaches a cosinusoidal form in conjunction with the following "Integrate and Dump" circuit.
The data-spectrum shaping is split into two equal parts and handled in the transmitter and in the receiver. Ideally, the data filtering should be equal in both of these parts. The overall data-channel-spectrum shaping of the transmitter and the receiver is approximately 100% roll-off.
The "Integrate and Dump" circuit performs an integration over a clock period. This results in a demodulated and valid RDS signal in form of biphase symbols being output from the integrate and dump circuit. The final stages of RDS data processing are the biphase symbol decoding and the differential decoding. After synchronization by data clock RDCL (pin 16) data appears on the RDDA output (pin 2). The output of the biphase symbol decoder is evaluated by a special circuit to provide an indication of "good" data (QUAL = HIGH) or "corrupt" data (QUAL = LOW).

Timing

Fixed and variable dividers are applied to the 4.332/8.664 MHz crystal oscillator to generate the 1.1875 kHz RDS clock RDCL, which is synchronized by the incoming data. Which ever clock edge is considered (positive or negative going edge) the data will remain valid for 399 µs after the clock transition. The timing of data change is 4 µs before a clock change. Which clock transition (positive or negative going clock) the data change occurs in, depends on the lock conditions and is arbitrary (bit slip).
During poor reception it is possible that faults in phase occur, then the clock signal stays uninterrupted, and data is constant for 1.5 clock periods. Normally, faults in phase do not occur on a cyclic basis. If however, faults in phase occur in this way, the minimum spacing between two possible faults in phase depends on the data being transmitted. The minimum spacing cannot be less than 16 clock periods. The quality bit changes only at the time of a data change.

CHARACTERISTICS

$V_{DDA} = V_{DDD} = 5$ V; $T_{amb} = +25$ °C and measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	supply voltage (pin 5)		3.6	5	5.5	V
V_{DDD}	supply voltage (pin 12)		3.6	5	5.5	V
I_{tot}	total supply current	$I_1 + I_2$	–	6	–	mA
V_{ref}	reference voltage (pin 3)	$V_{DDA} = 5$ V	–	2.5	–	V
MPX input (signal before the capacitor on pin 4)						
$V_{i\,MPX}$	RDS amplitude (RMS value)	$\Delta f = \pm 1.2$ kHz RDS; $\Delta f = \pm 3.5$ kHz ARI; see Fig.4	1	–	–	mV
	maximum input signal capability (peak-to-peak value)	$f = 57 \pm 2$ kHz	200	–	–	mV
		$f < 50$ kHz	1.4	–	–	V
		$f < 15$ kHz	2.8	–	–	V
		$f > 70$ kHz	3.5	–	–	V
R_{4-6}	input resistance	f = 0 to 100 kHz	40	–	–	kΩ
G_{8-4}	signal gain	f = 57 kHz	17	20	23	dB
57 kHz bandpass filter						
f_0	centre frequency	$T_{amb} = -40$ to $+85$ °C	56.5	57.0	57.5	kHz
B	–3 dB bandwidth		2.5	3.0	3.5	kHz
G	stopband attenuation	$\Delta f = \pm 7$ kHz	31	–	–	dB
		$f < 45$ kHz	40	–	–	dB
		$f < 20$ kHz	50	–	–	dB
		$f > 70$ kHz	40	–	–	dB
R_8	output resistance (pin 8)	f = 57 kHz	–	26	–	Ω
Comparator input (pin 7)						
V_i	minimum input level (RMS value)	f = 57 kHz	–	1	10	mV
R_{CIN}	input resistance		70	110	150	kΩ
Oscillator input (pin 13)						
$V_{I\,H}$	input voltage HIGH	$V_{DDD} = 5.0$ V	4.0	–	–	V
$V_{I\,L}$	input voltage LOW	$V_{DDD} = 5.0$ V	–	–	1.0	V
I_I	input current	$V_{DDD} = 5.5$ V	–	–	±1	μA
Digital demodulator and outputs QUAL, RDDA, T57, OSCO and RDCL (pins 1, 2, 14, 15 and 16)						
$V_{Q\,H}$	output voltage HIGH	$I_Q = -20$ μA; $V_{DDD} = 4.5$ V	4.4	–	–	V
$V_{Q\,L}$	output voltage LOW	$I_Q = 3.2$ mA; $V_{DDD} = 5.5$ V	–	–	0.4	V
f_{RDCL}	nominal clock frequency RDCL		–	1187.5	–	Hz
Δt_{RDCL}	jitter of RDCL		–	–	18	μs
f_{T57}	nominal subcarrier frequency T57	note 1	–	57.0	–	kHz
I_Q	output current OSCO (pin 14)	$V_{DDD} = 4.5$ V				
		$V_{14} = 0.4$ V	1.5	–	–	mA
		$V_{14} = 4.1$ V	–1.6	–	–	mA
	QUAL, RDDA, T57, RDCL (pins 1, 2, 15 and 16)	$V_{14} = 0.4$ V	5.9	–	–	mA
		$V_{14} = 4.1$ V	–5.3	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
4.332 MHz crystal parameters						
XTAL	frequency f_0		–	4.33200	–	MHz
	maximum permitted tolerance		–	±50	–	10^{-6}
	adjustment tolerance of f_0	T_{amb} = +25 °C	–	–	±20	10^{-6}
	load capacitance	T_{amb} = −40 to +85 °C	–	–	±25	10^{-6}
			–	30	–	pF
	resonance resistance		–	–	60	Ω
8.664 MHz crystal parameters						
XTAL	frequency f_0		–	8.664	–	MHz
	maximum permitted tolerance		–	±50	–	10^{-6}
	adjustment tolerance of f_0	T_{amb} = +25 °C	–	–	±30	10^{-6}
	load capacitance	T_{amb} = −40 to +85 °C	–	–	±30	10^{-6}
			–	30	–	pF
	resonance resistance		–	–	60	Ω

Note to the characteristics

1. The signal T57 has a phase lead of 123° (±180°) relative to the ARI carrier at output SCOUT.

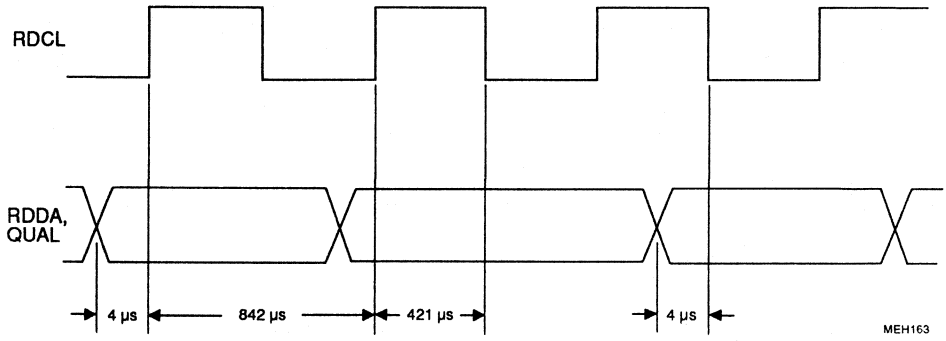


Fig.3 RDS timing diagram including a phase jump.

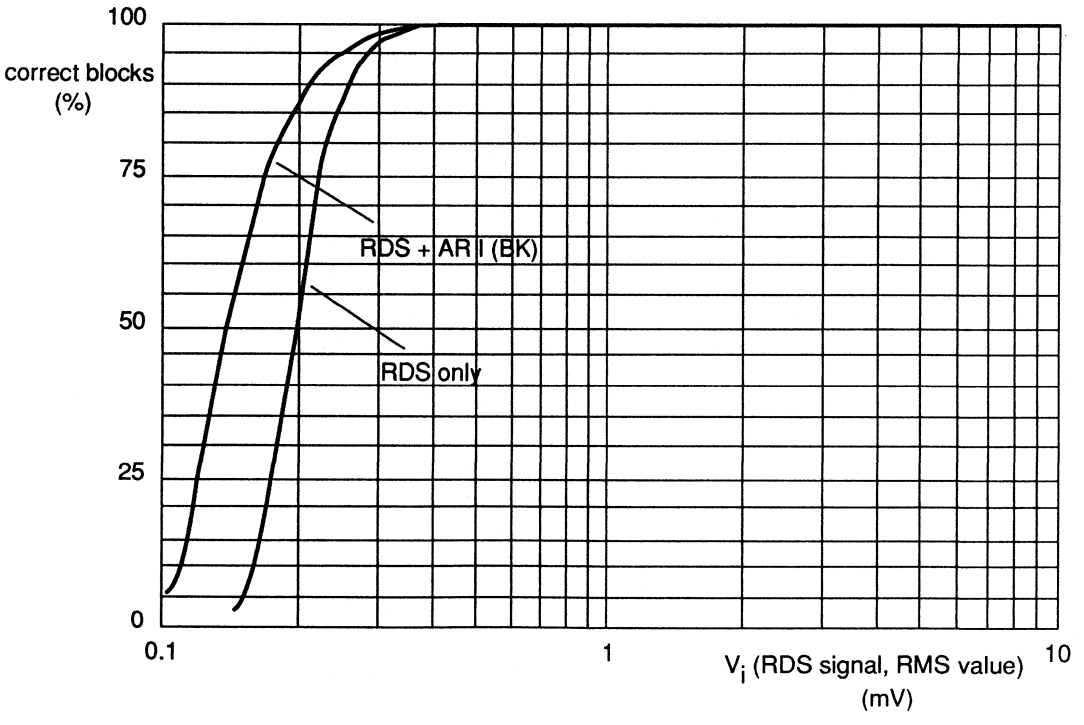


Fig.4 Typical RDS sensitivity.

AUDIO DIGITAL INPUT CIRCUIT (ADIC)

GENERAL DESCRIPTION

The SAA7274 is an Audio Digital Input Circuit (ADIC) which converts digital audio signals in accordance with the IEC/EBU standards, IEC tech. com. No. 84, secr. 50, Jan. 1987 into an equivalent binary value of data and control bits. The output function of this device is to convert the equivalent binary value of the data bits (for each channel) into a serial digital audio signal which conforms to the I²S format.

Features

- I²S bus output
- Biphase audio signal (Satellite radio, compact disc and DAT)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	4.5	–	5.5	V
Inputs	except IBIFA					
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Input voltage LOW		V_{IL}	0	–	0.3 V_{DD}	V
Input current	V_I = 0 V	$-I_I$	–	–	1	μA
	V_I = 5.5 V	I_I	–	–	1	μA
Input capacitance		C_I	–	4	6	pF
Outputs						
Output voltage HIGH		V_{OH}	V_{DD}–0.5	–	–	V
Output voltage LOW		V_{OL}	–	–	0.4	V
Operating ambient temperature range		T_{amb}	–40	–	+70	°C

PACKAGE OUTLINES

SAA7274P: 24-lead DIL; plastic (SOT101A).
SAA7274T: 24-lead mini-pack; plastic (SO24; SOT137A).

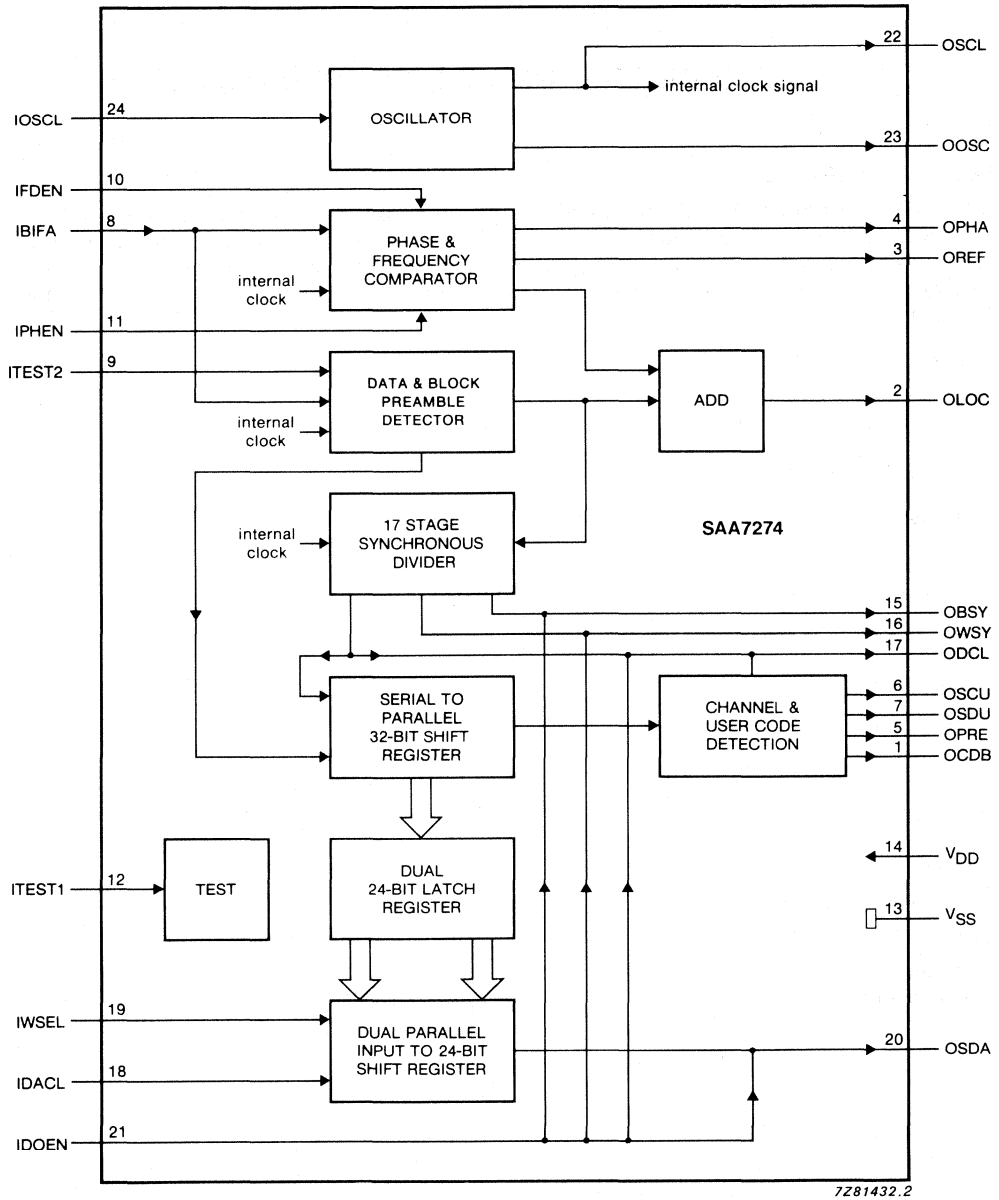


Fig.1 Block diagram.

PINNING

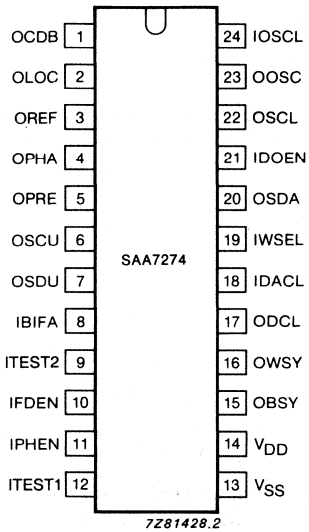


Fig.2 Pinning diagram.

Power supply

V_{DD}	positive supply voltage (5 V)
V_{SS}	ground (0 V)

Inputs (CMOS protection)

IBIFA	biphase input signal (min. 1 MHz; max. 3.1 MHz)
IFDEN	frequency detector enable
IPHEN	phase-locked loop edge selector
ITEST1	test input enable
ITEST2	test input enable
IDACL	data clock input signal (max. 5 MHz)
IWSEL	word select input signal (max. 50 kHz)
IDOEN	output enable
IOSCL	clock oscillator input (min. 8 MHz; max. 12.5 MHz)

Outputs (CMOS push-pull)

OCDB	control data bits (max. 400 kHz)
OLOC	out-of-lock signal
OREF	phase reference signal (max. 6.2 MHz)
OPHA	phase output signal (max. 6.2 MHz)
OPRE	pre-emphasis level
OSCU	user clock/copy-bit signal (max. 3.1 MHz)
OSDU	user data/pre-emphasis (max. 3.1 MHz)
OSCL	system clock output (min. 8 MHz; max. 12.5 MHz)
OOSC	clock oscillator output (min. 8 MHz; max. 12.5 MHz)

Outputs (3-state push-pull)

OBSY	block synchronization output signal (1/49152 system clock)
OWSY	word clock output signal (1/256 system clock)
ODCL	data clock output signal (1/4 system clock)
OSDA	data output signal (max. 2.5 MHz)

FUNCTIONAL DESCRIPTION

Main function

The biphase input signal must conform to the IEC/EBU standards, IEC tech. com. No. 84, secr. 50, Jan. 1987 format, as well as satisfying the following conditions:

- number of channels: 2
- transmission code: biphase mark
- synchronization method: biphase violation
- number of data bits: 24, starting with the LSB
- number of control bits: 4
- preamble values:

preceding cell	0	1
block preamble	11101000	00010111

The main function performs the following tasks:

- Provides the output function with the equivalent binary value of the data bits separately for each of the two channels. These values are available until new information is received.
- Generates an out-of-lock output signal (OLOC) which is HIGH when the frequency of the biphase input signal is equal to 1/4 of the system clock frequency and when the block preambles are detected in the biphase input signal.
- If the biphase input signal is not present after 32 clock pulses and also whenever the biphase input signal and IOSCL/4 drift away from each other by more than 32 clock pulses, then the output OSCU is forced HIGH and output OSDU, OPRE, OLOC, OCDB and OSDA are forced LOW.
- Generates a data clock output signal (ODCL) with a frequency of 1/4 of the system clock. When a block preamble is detected in the biphase input signal ODCL is synchronized to a LOW value.
- Generates a word clock output signal (OWSY) with a frequency of 1/256 of the system clock. When a block preamble is detected in the biphase input signal OWSY is synchronized to a LOW value.
- Generates a block synchronization output signal (OBSY). This signal is HIGH during 4 system clock periods and has a frequency of 1/49152 of the system clock. The signal is synchronized with the block preambles of the biphase input signal.
- Generates a phase output signal (OPHA) and a phase reference signal (OREF). If the frequency of the biphase input signal (IBIFA) equals 1/4 of the system clock frequency ($f_{IOSCL}/4$) then the IC generates OPHA and OREF as shown in Fig.3.
  If the frequency of the biphase input signal (IBIFA) is greater or less than 1/4 of the system clock frequency then the IC generates OPHA and OREF as shown in Fig.4.

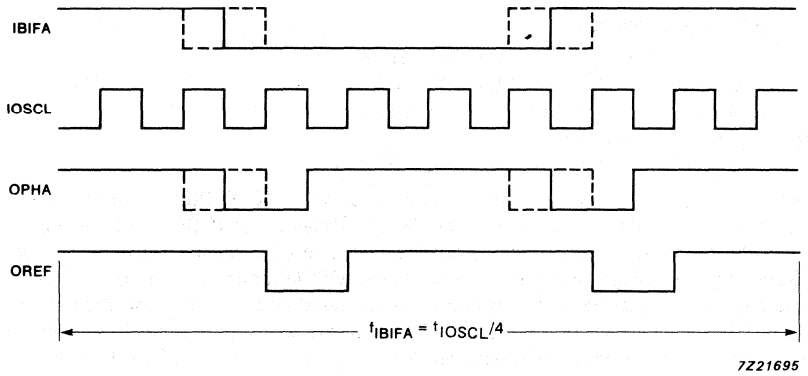


Fig.3 Generation of phase output signal (OPHA) and phase reference signal (OREF); $f_{IBIFA} = f_{IOSCL}/4$.

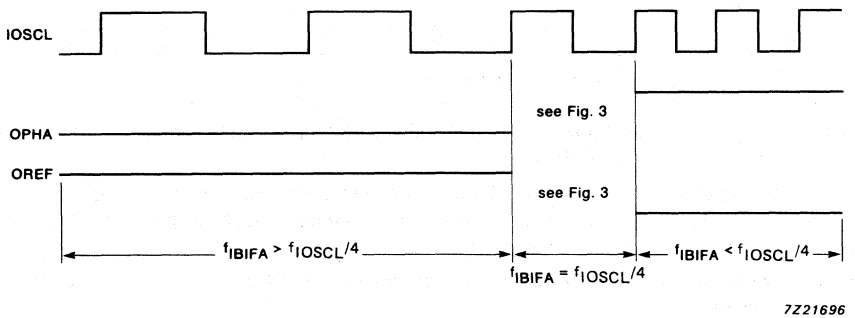


Fig.4 Generation of phase output signal (OPHA) and phase reference signal (OREF); $f_{IBIFA} \neq f_{IOSCL}/4$.

Output function

The output function performs the following tasks:

- Provides the data output (OSDA) with the data bits from each channel in the following order:

MSB . . . . . LSB 0 0 0 0 0 0 0 0

- Outputs the data of the right and left channel. When word select input signal (IWSEL) is HIGH the data of the right channel is output and when LOW the data of the left channel is output.
- Delivers serial data to the OSDA output, if IDOEN = HIGH. This occurs on each negative transition of the data clock input signal (IDACL). Following a status change at the word select input (IWSEL), the data (MSB first) is output on the first negative transition of IDACL. If the number of clock pulses in a word exceeds 24, then the following bits will be internally set to zero.

FUNCTIONAL DESCRIPTION (continued)

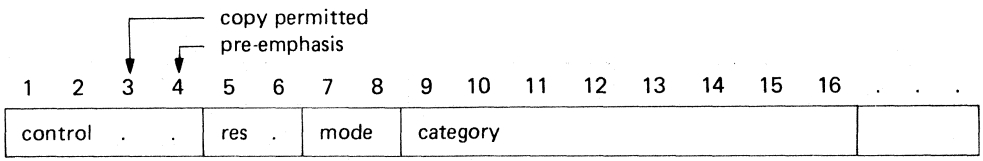
- Generates the following subcodes:

series 1,	0	0	U1	T1	S1	R1	Q1	1	0	0
series 2,	CRC	0	V1	U1	T1	S1	R1	Q1	1	0
series 3,	0	0	W1	V1	U1	T1	S1	R1	Q1	1

and after receiving the next user byte:

series 4,	0	0	W2	V2	U2	T2	S2	R2	Q2	1 etc.

- If the value of the category bits, bits 9 to 16 of the input signal, = 10000000 (compact disc format) and the value of the mode bits, bits 7 and 8, = 00, the user data output (OSDU) will deliver the bits of the subcode following the specified lay-out (above). The subcode starts only after receipt of at least 16 zero bits. Simultaneously a user clock signal (OSCU) consisting of 10 clock pulses is present. The output signal starts when a subcode is completed and is clocked on the negative transition of OSCU. The first data word of each subcode frame is output 3 times in succession with the data pattern shifted each time as outlined for series 1 through series 3 in the layout given above. The CRC performs a check on the 96 Q bits of the preceding subcode. If CRC is correct then the CRC bit = 1.
- Channel status:



If the value of the category bits **does not** equal 10000000 (compact disc format) and the value of the mode bits equals 00 (mode 0), then:

output OSDU indicates the status of bit 4 (pre-emphasis) of the channel status and output OSCU indicates the status of bit 3 (copy permitted) of the channel status provided the control bits conform to the 2-channel audio signal format.

- Uses the output pre-emphasis (OPRE) to indicate the status of bit 4 of the channel status for a 2-channel audio signal.
- Outputs the 4 control bits of the biphase input signal (IBIFA) represented by V, U, C and P at OCDB. The output delivers the bits in the same sequence during the next word, each bit continues for 32 clock pulses.

Additional input and output signals

The following input and output signals are available from this circuit:

- Phase output signal (OPHA) and phase reference signal (OREF) for use in a phase-locked loop (PLL). The OPHA signal is a result of the difference between the frequency and phase of the biphase input signal and the system clock. OREF signal provides the reference signal for the PLL.
- Input signal IFDEN enables the frequency detector. The frequency detection as present in the 2 signals OPHA and OREF can be enabled by making this signal LOW.
- Data clock output signal (ODCL), which has a frequency of 1/4 of the system clock frequency.
- Word clock output signal (OWSY), which has a frequency of 1/256 of the system clock frequency.
- Block synchronization output signal (OBSY), which has a frequency of 1/49152 of the system clock.
- ODCL, OWSY and OBSY will be synchronized to the block preambles in the biphase input signal IBIFA.

- Outputs ODCL, OWSY, OBSY and OSDA are enabled via a 3-state mode with a HIGH level on input IDOEN.
- IPHEN input selects dual or single edge detection of the input signal IBIFA in the phase detector. A low level selects the single-edge detection mode.
- Out-of-lock signal (OLOC). This output is continuously LOW or random HIGH/LOW if the PLL is out-of-lock, or no block preambles and present in the biphase input signal IBIFA. It is continuously HIGH if the PLL is in lock.
- User data/pre-emphasis output signal (OSDU). After receiving a category code of mode 0 from a non-compact disc source this signal outputs the pre-emphasis bit of the channel status bits in the biphase input signal. If the category code of mode 0 is from a compact disc source then the user data bits from the subcode channel including the CRC check on the 96 preceding Q bits are output.
- User clock/copy bit output signal (OSCU). After receiving a category code of mode 0 from a non-compact disc source then the copy bit of the channel status bits in the biphase input signal is output. If the category code of mode 0 is from a compact disc source then 10 clock pulses for the 'user data' are output.
- Pre-emphasis level output signal (OPRE), which indicates the value of the pre-emphasis bit of the channel status bits after receiving the two-channel audio fromat in the biphase input signal (IBIFA).
- Control data bits output signal (OCDB), which contains the 4 control bits of each word of the biphase input signal.
- The inputs ITEST1 and ITEST2 are used for device tests at the factory only, for normal operation they have to be connected to V_{SS}.

Clock oscillator

The clock oscillator of the circuit can be formed by connecting a crystal or a ceramic resonator between the oscillator input and output pins.

The circuit can also be driven by an external signal source applied to the oscillator input. The oscillator output is buffered and available at pin OSCL. The internal circuitry is driven via an inverter, which is connected to the output OSCL. This allows all the output signals (especially ODCL, OWSY and OBSY) to change their state after a pulse from OSCL, independent of the capacitive load of the OSCL pin. All output signals of the circuit are triggered on the positive transition of the OSCL signal.

Application note

If the capacitive load is higher than specified in **AC CHARACTERISTICS**, a buffer circuit can be used. A suitable device is the PC74HC126 (3-state quad buffer/line driver). The input IDOEN to the SAA7274 must be made HIGH and the original 3-state enable signal must be connected to the OE inputs of the PC74HC126 (pins 1, 4, 10 and 13). Because the capacitive load of the SAA7274 is very low, the loss of speed is limited.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0.5	7.0	V
Input voltage	note 1	V_I	−0.5	V_{DD}+0.5	V
Maximum input current		I_{IM}	–	±10	mA
Maximum output current		I_{OM}	–	±10	mA
Maximum supply current		I_{SS}, I_{DD}	–	±50	mA
Total power dissipation		P_{tot}	–	500	mW
Storage temperature range		T_{stg}	−55	+150	°C
Operating ambient temperature range		T_{amb}	−40	+70	°C

Note

1. Input voltage should not exceed 7 V.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = −40 to + 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply current	note 1	I_{DD}	–	–	250	μA
	note 2	I_{DD}	–	10	–	mA
Inputs						
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Input voltage LOW		V_{IL}	0	–	0.3 V_{DD}	V
Input current	$V_{SS} \leqslant V_I \leqslant V_{DD}$	$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	4	6	pF
Outputs						
OSCL						
Output voltage HIGH	$-I_{OH}$ = 8 mA	V_{OH}	V_{DD}−0.5	–	–	V
Output voltage LOW	I_{OL} = 8 mA	V_{OL}	–	–	0.4	V
OCDB, OLOC, OREF, OPHA, OPRE, OSCU, OSDU, OSDA						
Output voltage HIGH	$-I_{OH}$ = 2 mA	V_{OH}	V_{DD}−0.5	–	–	V
Output voltage LOW	I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
OBSY, OWSY, ODCL, OOSC						
Output voltage HIGH	$-I_{OH}$ = 1.5 mA	V_{OH}	V_{DD}−0.5	–	–	V
Output voltage LOW	I_{OL} = 1.5 mA	V_{OL}	–	–	0.4	V
OSDA, ODCL, OWSY, OBSY						
Output leakage current	3-state	$\|I_{LO}\|$	–	–	15	μA

Notes to the DC characteristics

1. All inputs at V_{DD} or V_{SS}, except ITEST2 on V_{SS}, all outputs open circuit.
2. f_{OSCL} = 11.3 MHz.

AC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V.
T_{amb} = −40 to + 70 °C.
Load capacitance (C_L): OSCL = 50 pF; OWSY, ODCL and OSDA = 30 pF (see application note); all other outputs = 20 pF.
Clock frequency $f_{IOSCL} = \leqslant 12.5$ MHz.
IOSCL timing pulse LOW, $t_{LOW} \geqslant 37$ ns; rise and fall times t_r and $t_f = \leqslant 10$ ns.
Delay times are specified from clock input = 50% V_{DD} to output = 50% V_{DD}; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Set-up and hold times						
IWSEL to IDACL	see Fig.5					
Data set-up time		t_{SU}	1	–	–	*
Data hold time		t_{HD}	–	–	1	*
Propagation delays						
IOSCL to OSCL		t_p	–	–	25	ns
IDACL to OSDA		t_p	–	–	60	ns
OSCL to OWSY and ODCL		t_p	5	–	50	ns
Rise and fall times						
OSCL						
Rise and fall time	TTL levels = 0.4 to 2 V	t_r, t_f	–	–	10	ns
Rise and fall time	CMOS levels = 10 to 90% V_{DD}	t_r, t_f	–	–	15	ns
OWSY and ODCL						
Rise and fall time	TTL levels = 0.4 to 2 V	t_r, t_f	–	–	15	ns
Rise and fall time	CMOS levels = 10 to 90% V_{DD}	t_r, t_f	–	–	25	ns

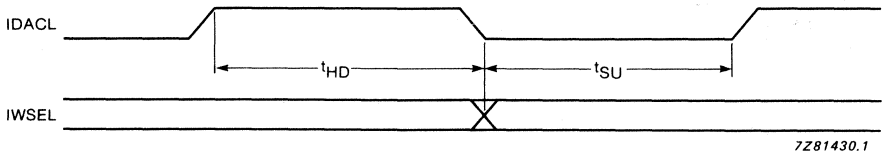
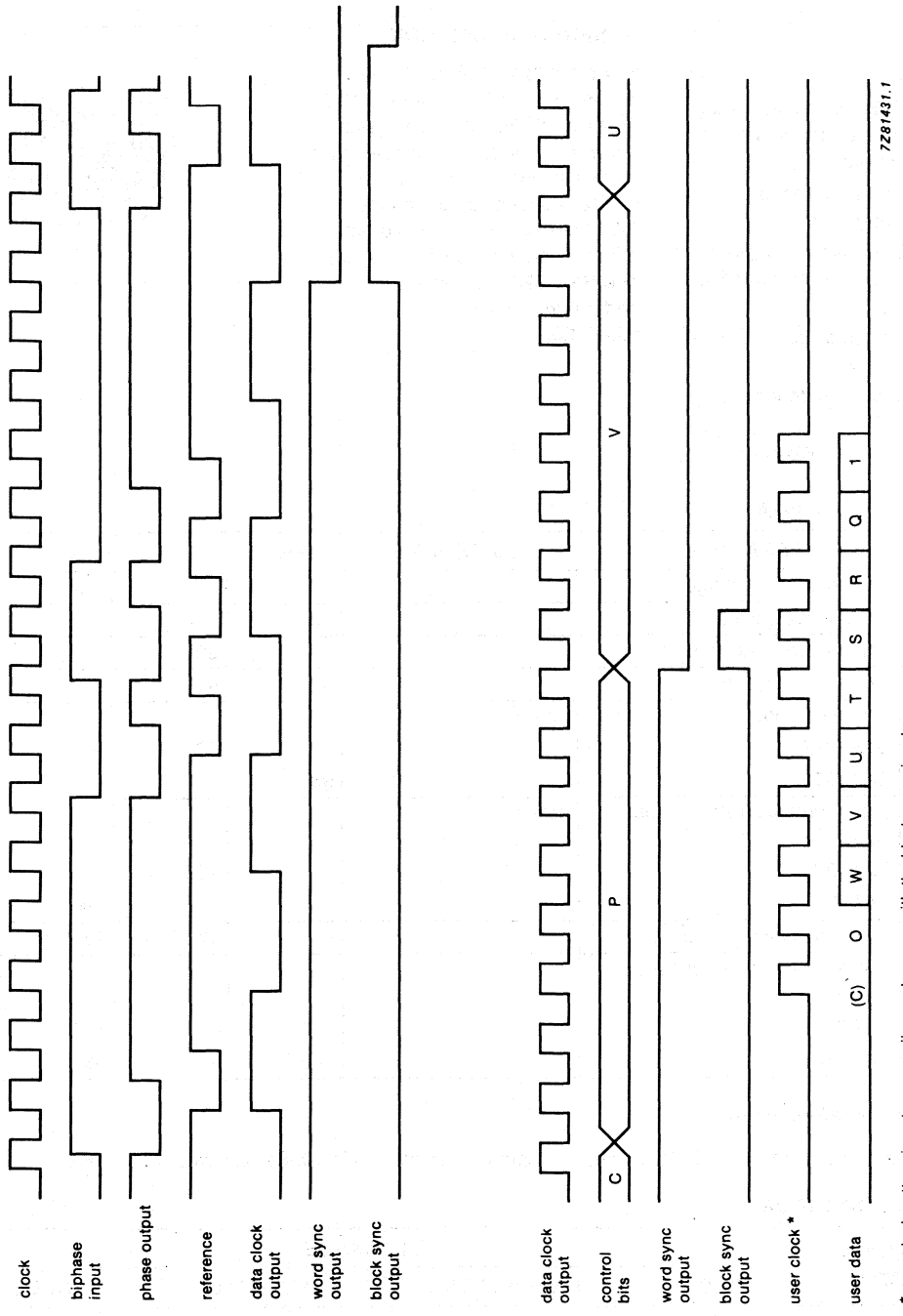


Fig.5 Set-up and hold time diagram.

* Clock periods of OSCL.



* user clock pattern is not necessarily synchronous with the block sync signal.

Fig.6 Timing diagram.

Stereo CMOS bitstream DAC for digital audio systems

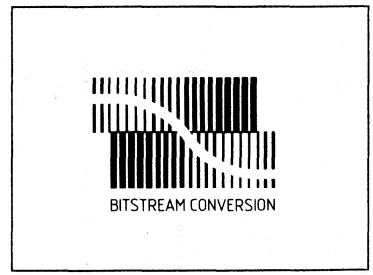
SAA7322/SAA7323

FEATURES

- I²S data input
- 3-stage digital filter incorporating F.I.R. filter, linear interpolator and sample-and-hold
- 2nd order noise shaper to improve analog performance
- 16-bit resolution from a bitstream conversion DAC, using switched capacitor integrator
- 3rd order low-pass filter to reduce out-of-band noise
- −12 dB attenuation, de-emphasis and mute control
- TTL compatible input/outputs

GENERAL DESCRIPTION

The SAA7322/7323 (DAC3) is a complete monolithic stereo CMOS 16-bit input bitstream conversion digital-to-analog converter designed for use in digital audio systems. The device is a replacement for the SAA7320, offering improved "idle pattern" performance at low-levels. The SAA7322 is a lower performance version of the SAA7323.



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current		–	20	35	mA
I_{DDD}	digital supply current		–	40	85	mA
DR	dynamic range	note 1				
	SAA7322		–	93	–	dB
	SAA7323		93	–	–	dB
THD+N	total harmonic distortion plus noise	note 1				
	SAA7322		–	−88	–	dB
	SAA7323		–	–	−90	dB
f_{XTAL}	operating crystal frequency		8	11.2896	12.3	MHz
T_{amb}	operating ambient temperature range					
	SAA7322		−10	–	+70	°C
	SAA7323		−40	–	+85	°C

Note to the quick reference data

1. Output characteristics measured with external components shown in Fig.10. Sample rate = 44.1 kHz.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7322GP	44	QFP	plastic	SOT205AG
SAA7323GP	44	QFP	plastic	SOT205AG

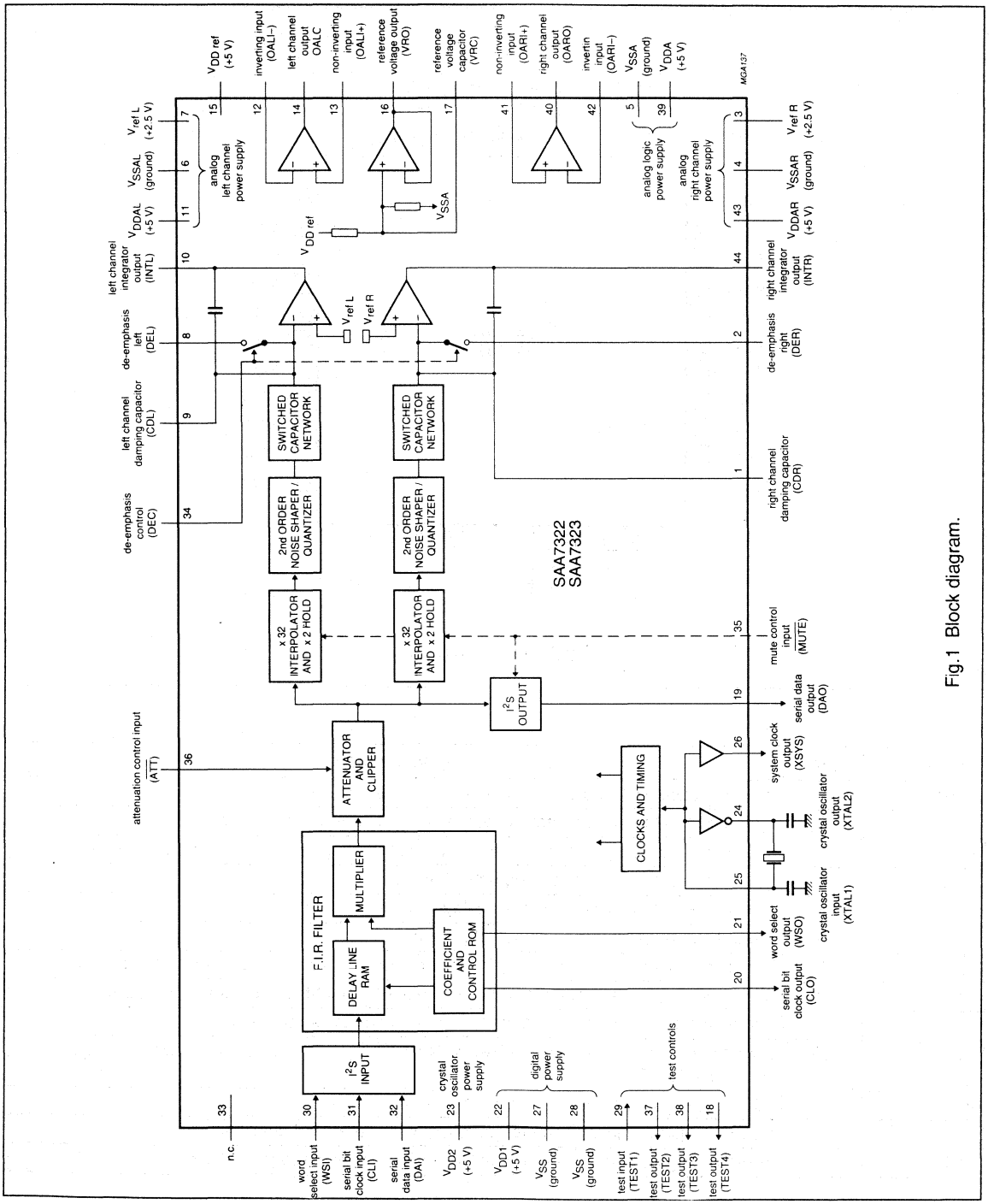


Fig.1 Block diagram.

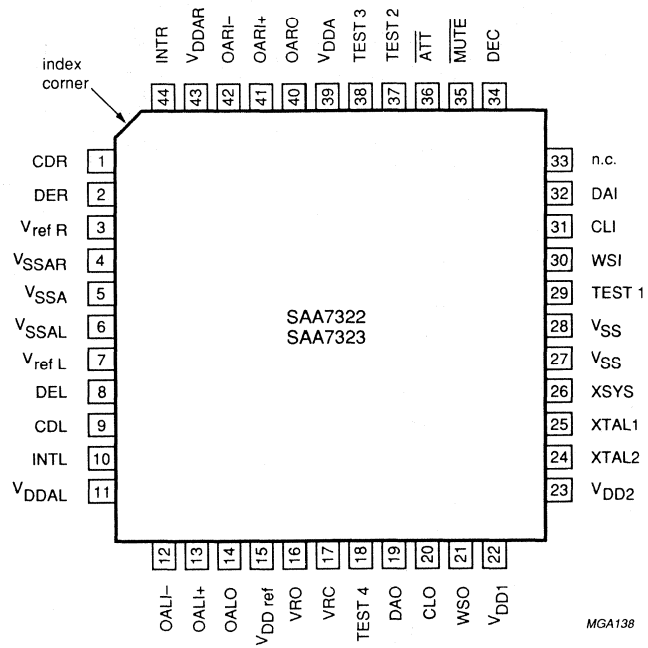


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
CDR	1	damping capacitor for the right channel switched-capacitor integrator
DER	2	connection to the de-emphasis switch in the right channel integrator
V_{refR}	3	reference voltage input for the analog channel ground (normally connected to VRO)
V_{SSAR}	4	ground connection for the analog right channel
V_{SSA}	5	ground connection for logic in the analog section
V_{SSAL}	6	ground connection for the analog left channel
V_{refL}	7	reference voltage input for the analog left channel ground (normally connected to VRO)
DEL	8	connection to the de-emphasis switch in the feedback of the left channel integrator
CDL	9	damping capacitor for the left channel switched-capacitor integrator
INTL	10	output from the left channel switched-capacitor integrator. Internal capacitor (85 pF typ.) connected to CDL
V_{DDL}	11	+5 V supply voltage for the analog left channel
OALI−	12	inverting input to the left channel low-pass filter operational amplifier
OALI+	13	non-inverting input to the left channel low-pass filter operational amplifier

SYMBOL	PIN	DESCRIPTION
OALO	14	output from the left channel operational amplifier
V_{DDref}	15	+5 V supply voltage for the reference voltage generator
VRO	16	internal reference voltage output (+2.5 V typ.)
VRC	17	internal reference voltage high impedance node requiring an external smoothing capacitor
TEST4	18	test output 4: pin should be left open-circuit
DAO	19	I²S serial data output is a 16-bit linear two's-complement PCM signal at a data rate of 176.4 kHz (typ.) formatted in accordance with I²S . After 4 x upsampling by the digital filter this signal is output so that an external DAC could be used; combined with CLO and WSO it can be considered as a master transmitter
CLO	20	I²S serial bit clock output, f_{CLKO} = 5.6448 MHz (typ).
WSO	21	I²S word select output 176.4 kHz (typ).
V_{DD1}	22	+5 V supply voltage for the digital section
V_{DD2}	23	+5 V supply voltage for the crystal oscillator
XTAL2	24	drive output to clock crystal
XTAL1	25	input from crystal oscillator or external clock input 11.2896 MHz (typ.)
XSYS	26	buffered output from crystal oscillator
V_{SS}	27, 28	ground connection for the digital section
TEST1	29	test input 1, pin should be connected to ground
WSI	30	I²S word select input, 44.1 kHz (typ) WSI together with CLI, is used to clock the I²S serial data input (DAI) and synchronize the main timing chain
CLI	31	I²S serial bit clock input, f_{CLKI} = 2.8224 MHz (typ).
DAI	32	I²S serial data input is a 16-bit linear two's-complement PCM signal formatted in accordance with I²S. If more than 16 bits are supplied then the least significant bits (LSBs) will be truncated
n.c.	33	not connected
DEC	34	de-emphasis control input switches an extra external capacitor network into both the analog left and right channel integrator feedback
MUTE	35	when active LOW this Schmitt trigger control input will force the interpolator data input to zero. It will also force the I²S data output (DAO) to zero
ATT	36	when active LOW this control input provides –12 dB attenuation to the analog output amplitude
TEST2	37	test output 2, pin should be left open-circuit
TEST3	38	test output 3, pin should be left open-circuit
V_{DDA}	39	+5 V supply voltage for logic in the analog section
OARO	40	output from the right channel operational amplifier
OARI+	41	non-inverting input to the right channel low-pass filter operational amplifier
OARI–	42	inverting input to the right channel low-pass filter operational amplifier
V_{DDAR}	43	+5 V supply voltage for the analog right channel
INTR	44	output from the right channel switched-capacitor integrator. Internal capacitor (85 pF typ.) connected to CDR

FUNCTIONAL DESCRIPTION

General

The SAA7322/7323 CMOS DAC heavily oversamples to several MHz (256 x the sampling frequency f_s), so that the band-limiting filters required for waveform smoothing and out-of-band noise reduction are mainly digital. In addition to the digital filters, the circuit contains active components for analog post filtering. In most applications very few external components are required. An output after the 4 x upsampling filter allows the circuit to be used as an interface between the decoder and external DAC in high-performance compact disc systems. The device requires only one +5 V supply; the required reference voltage is generated internally.

Separate supply pins for each of the bitstream conversion DACs achieves high performance signal-to-noise ratio and channel separation.

There is no phase delay between the two analog outputs despite the fact that the upsampling filter structure is multiplexed between the two data channels.

Oversampling digital filter

This is a 3-stage digital filter

- The first stage provides 4 x oversampling to 176.4 kHz using a 128-tap F.I.R. low-pass filter. Data is stored in a cyclic RAM, the filter coefficients in a ROM and the convolutions are performed using an array multiplier.
- The second stage is a 32 x oversampling linear interpolator.
- The third stage provides 2 x upsampling using a sample-and-hold, giving a total of 256 x upsampling (11.2896 MHz).

The first stage oversamples to 176.4 kHz with a band-pass ripple of ±0.035 dB and a stop-band attenuation of –60 dB above 24.2 kHz. It also contains frequency response compensation for the interpolator/analog post-filtering roll-off and coefficient scaling to prevent overflow in the noise shaper.

The characteristics of the F.I.R. filter are shown in Fig.9.

Switched-capacitor DAC

The digital-to-analog conversion is achieved with a bitstream conversion DAC oversampled to 256 f_s with second-order noise shaping performed digitally to give a 1-bit Pulse Density Modulated (PDM) code. Integral with the actual bitstream conversion converter is a first-order low-pass filtering action which reduces the total HF noise power.

A switched capacitor technique is used for the bitstream conversion DAC which converts the PDM stream to an analog signal. A fixed charge is either added or subtracted from the virtual earth node of a first-order filter. As this output is a continuous time output a highly symmetrical operational amplifier is used to give a low distortion figure. The output slew rate of this filter is chosen so that the operational amplifiers always remains within its high gain linear region.

An internally generated out-of-band dither signal is used to suppress audible idling patterns in the noise shaper at low signal levels. This signal is injected digitally into the x 32 upsampling interpolator at a frequency of 352.8 kHz and a level of –20 dB.

Attenuation

Attenuation is controlled by the ATT input at pin 36. This input will allow an attenuation of the analog output amplitude by 12 dB during track search.

De-emphasis and low-pass filter

Extra on-chip analog circuitry provides post filtering:

- Input DEC (pin 34) switches an extra external capacitor network into both the left and right channel analog integrator feedback to control roll-off. Output from the right channel switched-capacitor integrator (INTR) is available at pin 44. Output from the left channel switched-capacitor integrator (INTL) is available at pin 10.
- A low-pass filter, for further attenuation of out-of-band noise, can be constructed using the internal CMOS operational amplifiers. The digital filter contains compensation for a third-order Butterworth filter with a –3 dB cut-off at 60 kHz.

I²S serial interface

The SAA7322/7323 has two I²S ports incorporated; DAI (pin 32) and DAO (pin 19).

- DAI receives data from the compact disc decoder IC (or any 16-bit 44.1 kHz I²S source).
- DAO transmits the 4 x oversampled data to an external DAC.

The 'slave' receiver requires a serial bit clock input (CLI; pin 31) and a word select input (WSI; pin 30). To ensure that the filter is 'in-phase' with the input, the main timing chain

is automatically synchronized to the incoming word select signal. The frequency of the data must also be synchronized to the filter by:

- the source supplying the 11.2896 MHz system clock via crystal oscillator input (XTAL1; pin 25).

or

- SAA7322/7323 supplying the system clock to the source via XSYS (pin 26).

The SAA7322/7323 will use only the 16 most significant bits of input data even though the I²S format allows a variable word length (see Fig.4).

The 'master' transmitter supplies bit clock, word select and data signals for the 4 x upsampled output (see Fig.5).

Conversion path

The data conversion path is shown in Fig.3. As both paths are identical only one path is shown. The data flow is in a serial format up to the linear interpolator stage and then separated into two channels.

A recommended system application diagram of the SAA7322/7323 is shown in Fig.10.

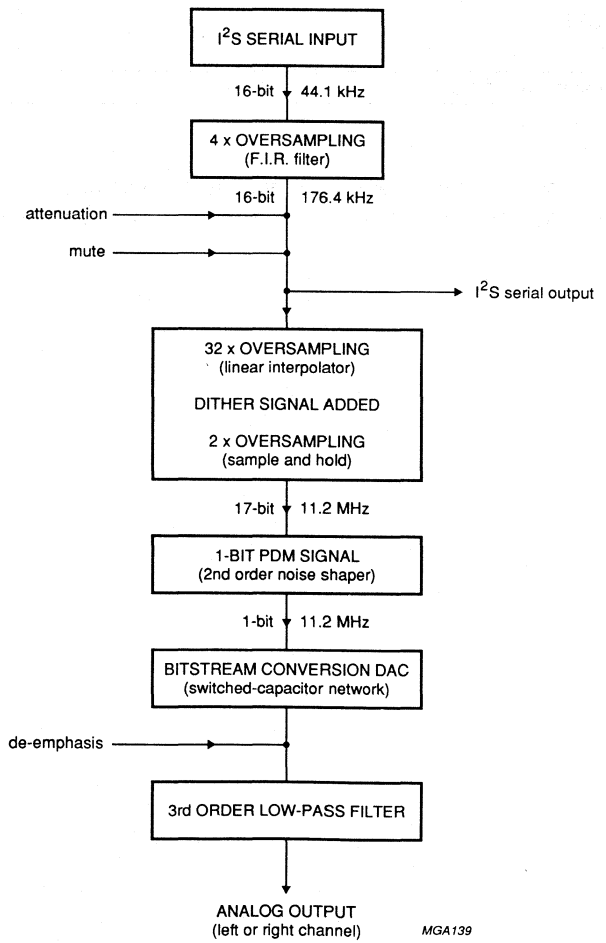


Fig.3 Flow diagram of SAA7322/7323 data conversion path (one channel).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	note 1	−0.5	+6.5	V
V_I	DC input voltage		−0.5	V_{DD}+0.5	V
I_{IK}	DC input diode current		–	±20	mA
V_O	DC output voltage		−0.5	V_{DD}+0.5	V
I_O	DC output sink/source current		–	±25	mA
$I_{DD.\ SS}$	total DC current V_{DD} or V_{SS}		–	±0.5	A
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range				
	SAA7322		−10	+70	°C
	SAA7323		−40	+85	°C
V_{es}	electrostatic handling	note 2	−1000	+1000	V

Notes to the limiting values

1. All V_{DD} and V_{SS} pins must be connected externally to the same power supply unit.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; f_s = 44.1 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Suppy						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current		–	20	35	mA
I_{DDD}	digital supply current		–	40	85	mA
Analog part						
REFERENCE VOLTAGE SOURCE VRC						
V_{refC}	high impedance reference voltage level		–	2.5	–	V
Z_{refO}	reference voltage output impedance		–	2	–	Ω
OUTPUTS OALO AND OARO (NOTES 1 AND 2)						
$V_{O\ RMS}$	output level (RMS value)	note 3; 0 dB	0.8	0.9	1.0	V
CHM	channel matching	note 4	–	–	±0.25	dB
OUTPUT PERFORMANCE (NOTE 1)						
DR	dynamic range					
	SAA7322		–	93	–	dB
	SAA7323		93	–	–	dB
THD+N	total harmonic distortion plus noise	at 0 dB/1 kHz				
	SAA7322		–	–88	–	dB
	SAA7323		–	–	–90	dB
	digital silence		–	–96	–	dB
α	channel separation	at 1 kHz	–	90	–	dB
SVRR	supply voltage rejection ratio to V_{DD}		–	60	–	dB
L	linearity	–60 to –100 dB	–	±2	–	dB
Digital part						
INPUTS WSI, CLI, DAI, DEC AND ATT						
V_{IL}	LOW level input voltage	note 5	–0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 5	2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	note 6	–10	0	+10	μA
C_I	input capacitance		–	–	10	pF
MUTE (Schmitt trigger)						
V_{IL}	LOW level input voltage	note 5	–0.5	–	1.8	V
V_{IH}	HIGH level input voltage	note 5	3.3	–	V_{DD}+0.5	V
I_{LI}	input leakage current	note 6	–10	0	+10	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_I	input capacitance		–	–	10	pF
XTAL1 (external clock only)						
V_{IL}	LOW level input voltage	note 5	−0.5	–	1.5	V
V_{IH}	HIGH level input voltage	note 5	3.5	–	V_{DD} to 5 V	V
I_{LI}	input leakage current	note 6	−10	0	+10	µA
C_I	input capacitance		–	–	10	pF
OUTPUTS DAO, CLO, WSO AND XSYS						
V_{OL}	LOW level output voltage	note 5; I_{OL} = 400 µA	−0.5	–	+0.4	V
V_{OH}	HIGH level output voltage	note 5; I_{OH} = 20 µA	2.4	–	V_{DD}+0.5	V
C_L	load capacitance		–	–	35	pF
Crystal oscillator (input XTAL1, output XTAL2) (see Fig.8)						
f_{XTAL}	crystal operating frequency		8	11.2896	12.3	MHz
gm	mutual conductance	at 100 kHz	1.5	–	–	mA/V
G_v	small signal voltage gain	G_v = gm x R_O	3.5	–	–	V/V
C_I	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	–	5	pF
C_O	output capacitance		–	–	10	pF
I_{LI}	input leakage current	note 6	−10	–	+10	µA
Timing						
EXTERNAL CLOCK INPUT						
XTAL1						
f_{CLK}	input frequency	f_s x 256	8	11.2896	12.3	MHz
t_r, t_f	input rise and fall time	note 7	–	–	20	ns
t_{HIGH}	input HIGH time	relative at 1.5 V to clock period	45	–	55	%
SYSTEM CLOCK OUTPUT XSYS (NOTE 8)						
t_r, t_f	input rise and fall time	note 7	–	–	20	ns
t_{HIGH}	input HIGH time	note 9; relative at 1.5 V to clock period	45	–	55	%
I²S TIMING; RECEIVER CLOCK INPUT CLK_I (SEE FIG.6)						
t_{CLK}	input clock period		320	354	1000	ns
t_{CLKH}	input clock time HIGH		112	–	–	ns
t_{CLKL}	input clock time LOW		112	–	–	ns
Data input WSI and DAI						
$t_{SU;DAT}$	data set-up time		40	–	–	ns
$t_{HD;DAT}$	data hold time		40	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TRANSMITTER (SEE FIG.7)						
clock output CLO						
t_{CLK}	output clock period		–	$2/f_{CLK}$	–	ns
t_{CLKH}	output clock time HIGH		60	–	–	ns
t_{CLKL}	output clock time LOW		60	–	–	ns
Word select WSO						
$t_{SU;DAT}$	data set-up time		40	–	–	ns
$t_{HD;DAT}$	data hold time		40	–	–	ns
t_r, t_f	input rise and fall time	note 7	–	–	20	ns
Data output DAO						
$t_{SU;DAT}$	data set-up time		40	–	–	ns
$t_{HD;DAT}$	data hold time		40	–	–	ns
t_r, t_f	input rise and fall time	note 7	–	–	20	ns

Notes to the characteristics

1. Output characteristics measured with external components shown in Fig.10. Sample rate = 44.1 kHz.
2. Maximum load on INTL, INTR (excluding feedback) is 10 kΩ, 20 pF to V_{ref}. Dynamic output impedance is typ. 150 Ω (open loop).

   Maximum load on OALO, OARO (excluding feedback) is 3 kΩ, 200 pF. Dynamic output impedance is typ. 100 Ω (open loop).
3. Output level changes linearly with clock frequency.
4. With matched external components.
5. Minimum V_{IL}, V_{OL} and maximum V_{IH}, V_{OH} are peak values to allow for transients.
6. $I_{LI\ min}$ and $I_{LO\ min}$ measured at V_I = 0 V; $I_{LI\ max}$ and $I_{LO\ max}$ measured at $V_I = V_{DD}$.
7. Reference levels = 0.8 V and 2 V.
8. Output times are measured with a capacitive load of 35 pF.
9. t_{HIGH} valid only when used with XTAL.

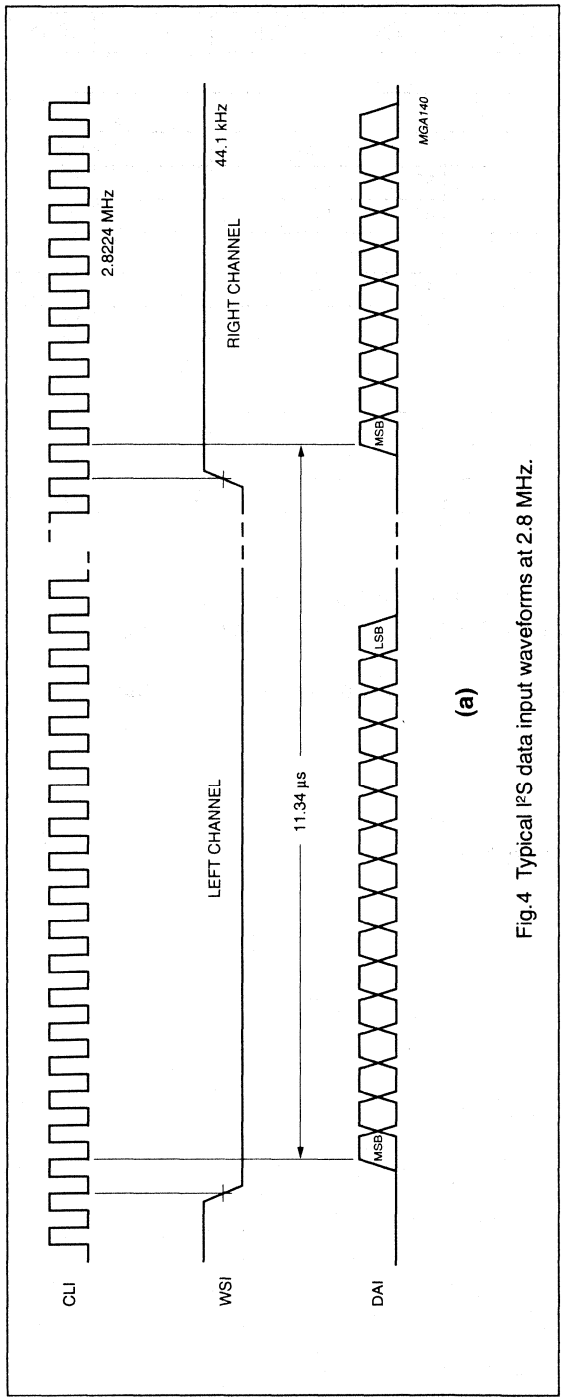


Fig.4 Typical I²S data input waveforms at 2.8 MHz.

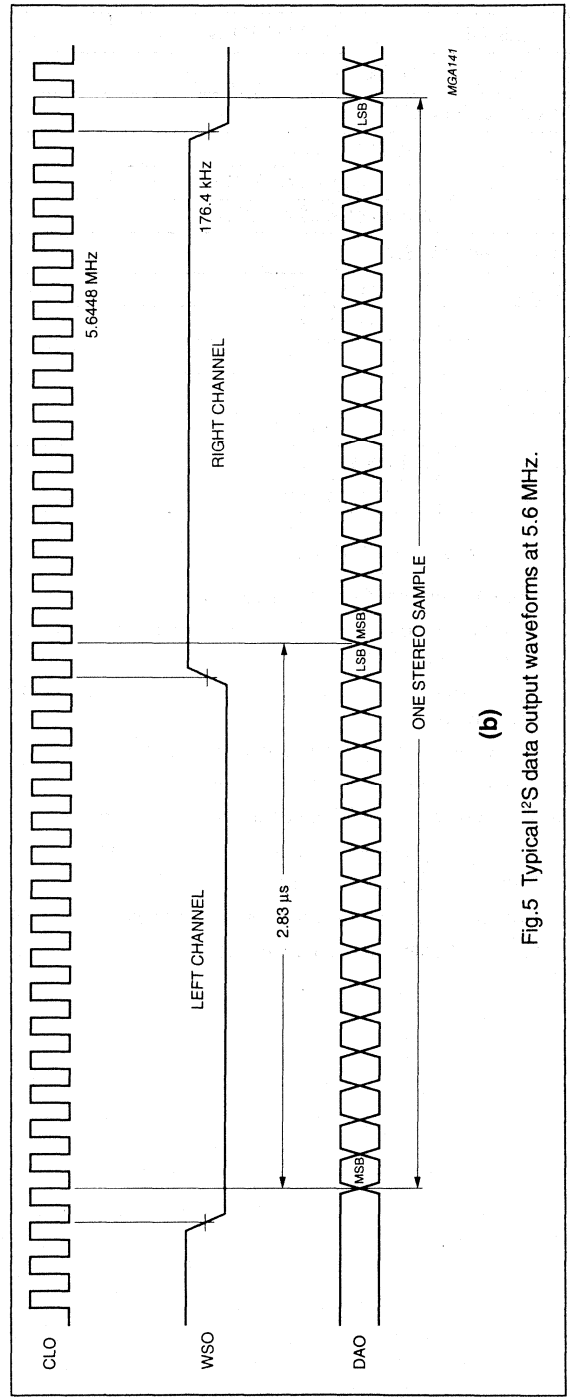
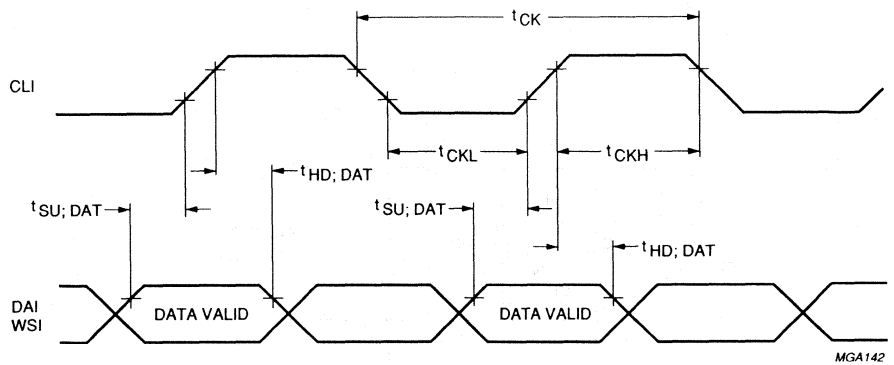
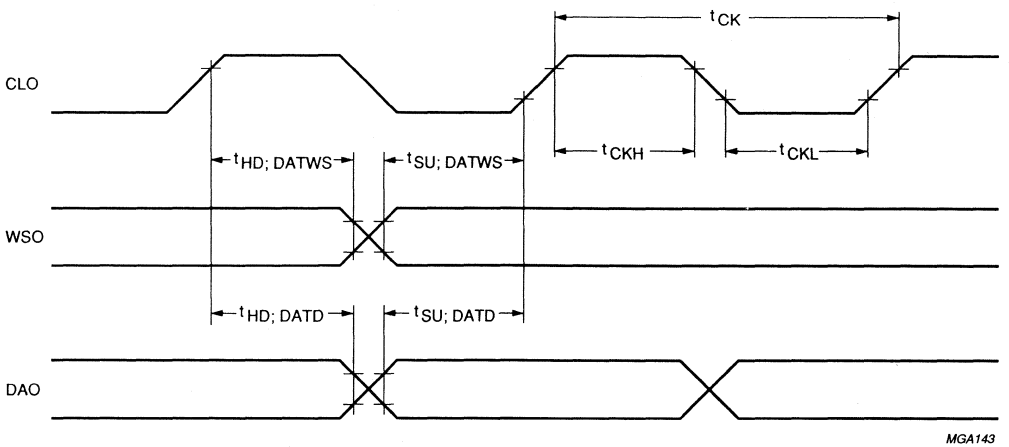


Fig.5 Typical I²S data output waveforms at 5.6 MHz.



Reference levels = 0.8 V and 2 V.

Fig.6 Data input timing with respect to I²S serial bit clock input (CLI).



Reference levels = 0.8 V and 2 V.

Fig.7 Data output timing with respect to clock output (CLO).

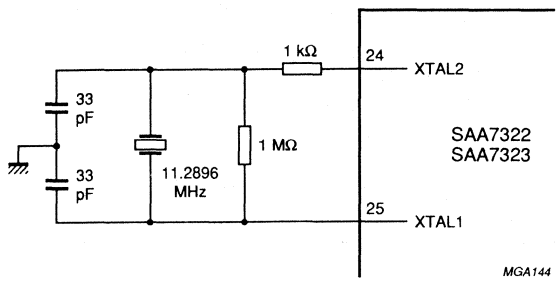


Fig.8 Crystal oscillator circuit using crystal type: 4322 143 05031.

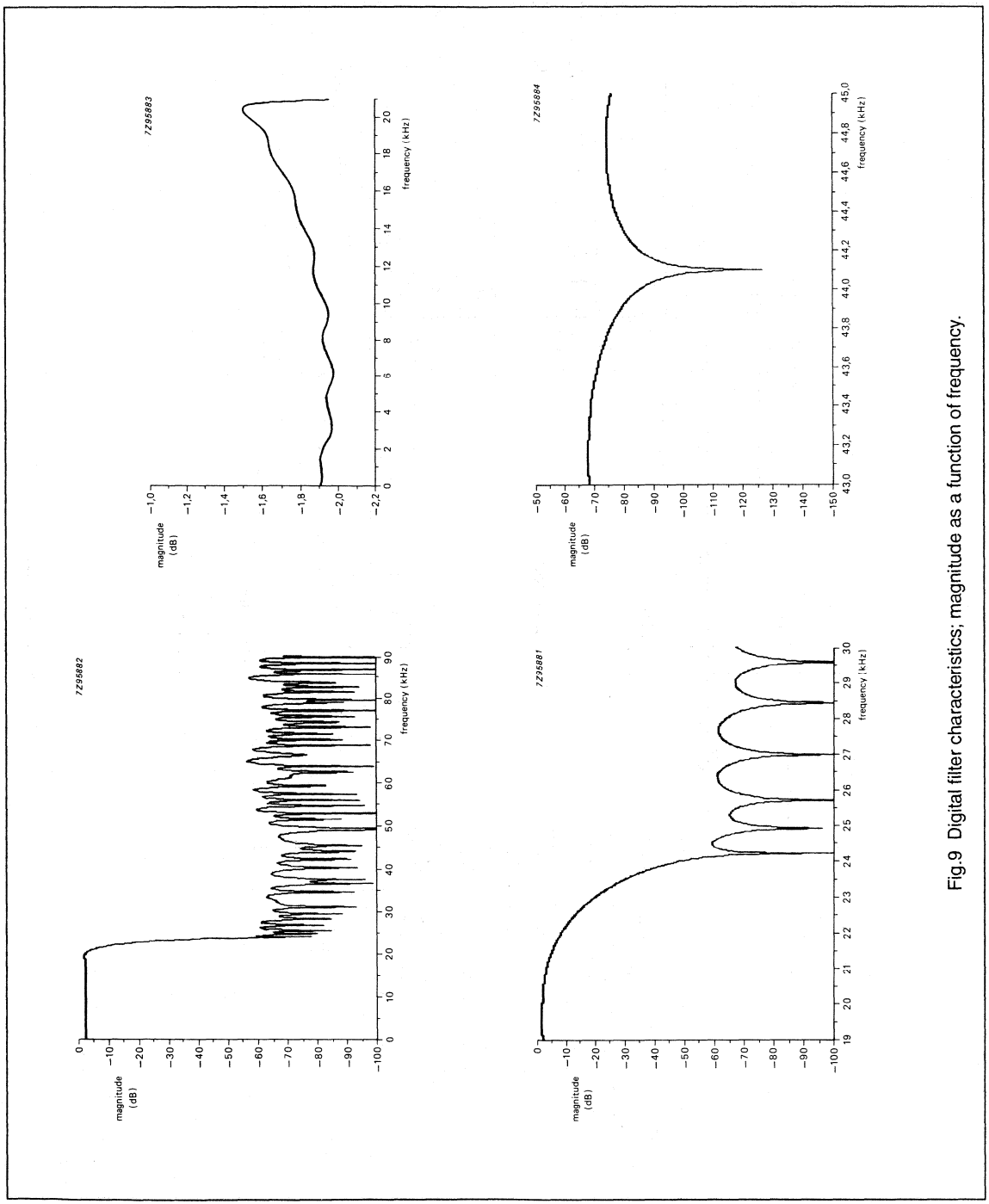


Fig.9 Digital filter characteristics; magnitude as a function of frequency.

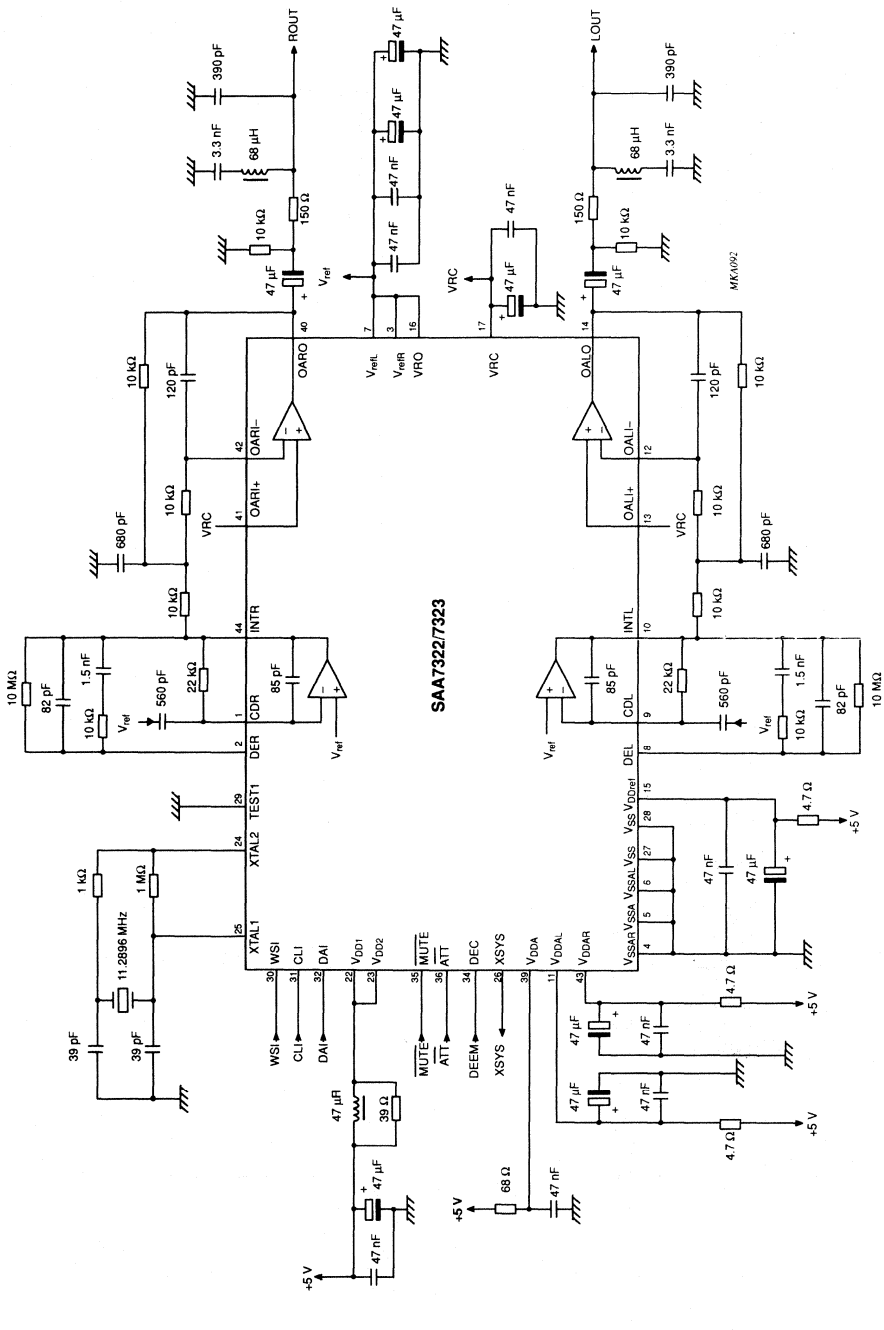


Fig.10 System application diagram.

Pins 18 to 21, 37 and 38 are open circuit.

CMOS Digital decoding IC with RAM for Compact Disc

SAA7345

FEATURES

- Integrated data slicer and clock regenerator
- Digital Phase-Locked Loop (PLL)
- Demodulator and Eight-to-Fourteen Modulation (EFM) decoding
- Subcoding microcontroller serial interface
- Integrated programmable motor speed control
- Error correction and concealment functions
- Embedded Static Random Access Memory (SRAM) for de-interleave and First-In First-Out (FIFO)
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface [European Broadcasting Union (EBU)]
- 2 to 4 times oversampling integrated digital filter
- Audio data peak level detection
- Versatile audio data serial interface
- Digital de-emphasis filter
- Kill interface for Digital-to-Analog Converter (DAC) deactivation during digital silence
- Double speed mode
- Compact Disc Read Only Memory (CD-ROM) modes
- A single speed only version is available (SAA7345GP/SS).

GENERAL DESCRIPTION

The SAA7345 incorporates the CD signal processing functions of decoding and digital filtering. The device is equipped with on-board SRAM and includes additional features to reduce the processing required in the analog domain.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	3.4	5.0	5.5	V
I_{DD}	supply current	–	22	50	mA
f_{xtal}	crystal frequency	8	16.9344 or 33.8688	35	MHz
T_{amb}	operating ambient temperature	−40	–	+85	°C
T_{stg}	storage temperature	−55	–	+125	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7345GP	44	QFP[1]	plastic	SOT205A

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the "*Quality Reference Pocketbook*" are followed. The pocketbook can be ordered using the code 9398 510 34011.

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

BLOCK DIAGRAM

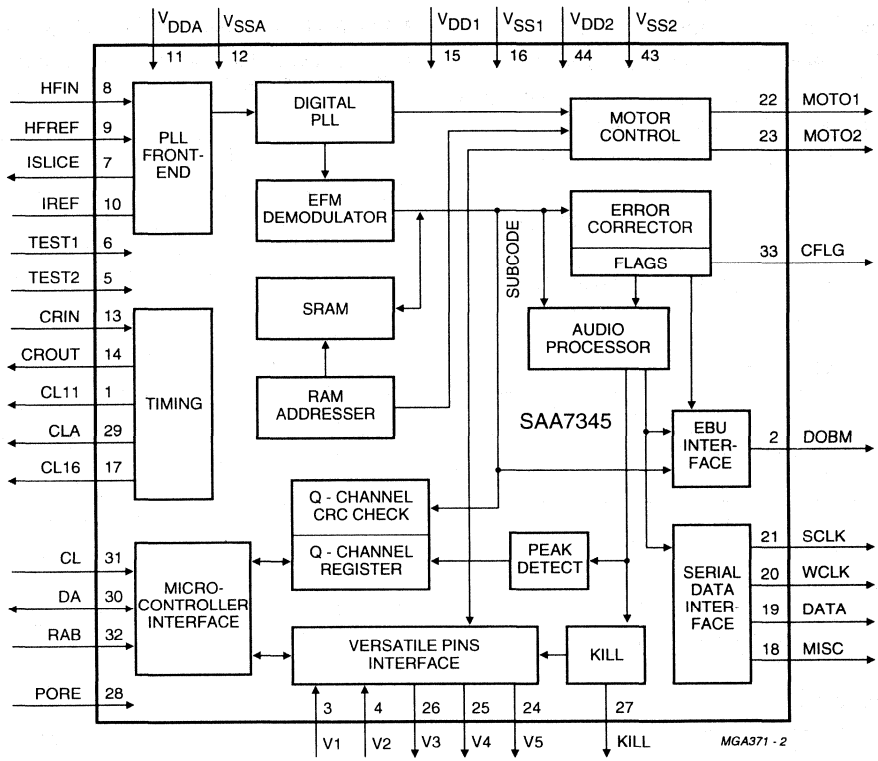


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CL11	1	11.2896 or 5.6448 MHz clock output (3-state); (divide-by-3)
DOBM	2	bi-phase mark output (externally buffered; 3-state)
V1	3	versatile input pin
V2	4	versatile input pin
TEST2	5	test input; this pin should be tied LOW
TEST1	6	test input; this pin should be tied LOW
ISLICE	7	current feedback output from data slicer
HFIN	8	comparator signal input
HFREF	9	comparator common-mode input
IREF	10	reference current pin (nominally $\frac{1}{2}V_{DD}$)
V_{DDA}	11	analog supply voltage; note 1
V_{SSA}	12	analog ground; note 1
CRIN	13	crystal/resonator input
CROUT	14	crystal/resonator output
V_{DD1}	15	digital supply to input and output buffers; note 1
V_{SS1}	16	digital ground to input and output buffers; note 1
CL16	17	16.9344 MHz system clock output
MISC	18	general purpose DAC output (3-state)
DATA	19	serial data output (3-state)
WCLK	20	word clock output (3-state)
SCLK	21	serial bit clock output (3-state)
MOTO1	22	motor output 1; versatile (3-state)
MOTO2	23	motor output 2; versatile (3-state)
V5	24	versatile output pin
V4	25	versatile output pin
V3	26	versatile output pin (open-drain)
KILL	27	kill output; programmable (open-drain)
$\overline{PORE}$	28	power-on reset enable input (active LOW)
CLA	29	4.2336 MHz microcontroller clock output
DA	30	interface data I/O line
CL	31	interface clock input line
RAB	32	interface R/$\overline{W}$ and acknowledge input
CFLG	33	correction flag output (open-drain)
n.c.	34 to 42	no internal connection
V_{SS2}	43	digital ground to internal logic; note 1
V_{DD2}	44	digital supply voltage to internal logic; note 1

Note

1. All supply pins must be connected to the same external power supply.

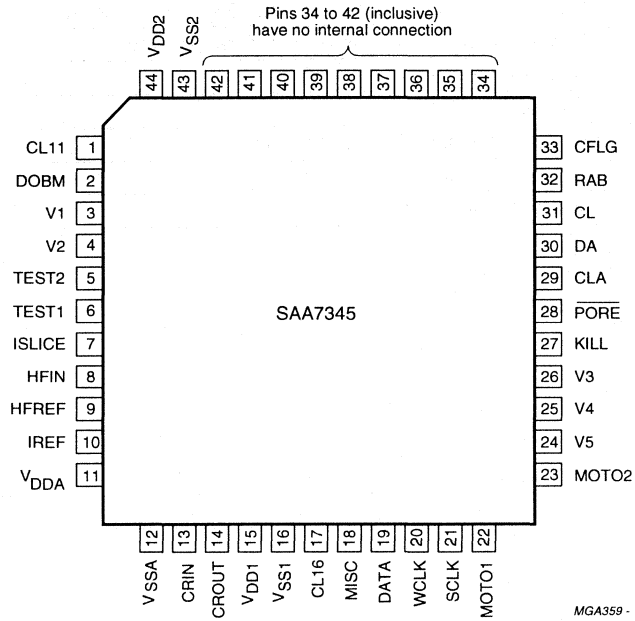


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Demodulator

FRAME SYNC PROTECTION

This circuit will detect the frame synchronization signals. Two synchronization counters are used in the SAA7345:

1. The coincidence counter which is used to detect the coincidence of successive syncs. It generates a Sync coincidence signal if 2 syncs are 588 ±1 EFM clocks apart.
2. The main counter is used to partition the EFM signal into 17-bit words. This counter is reset when:
   a) A Sync coincidence is generated.
   b) A sync is found within ±6 EFM clocks of its expected position.

The Sync coincidence signal is also used to generate the Lock signal which will go active HIGH when 1 Sync coincidence is found. It will reset to LOW when, during 61 consecutive frames, no Sync coincidence is found. This Lock signal is accessed via the status signal when the status control register (address 0010) is set to X100. See section on "Microcontroller interface" .

Data Slicer and Clock Regenerator

The SAA7345 has an integrated slice level comparator which is clocked by the crystal frequency clock. The slice level is controlled by an internal current source applied to an external capacitor under the control of the digital phase-locked loop (DPLL).

Regeneration of the bit clock is achieved with an internal fully digital PLL. No external components are required and the bit clock is not output. The PLL has two microcontroller control registers (addresses 1000 and 1001) for bandwidth and equalization.

For certain applications an offtrack input is necessary. If this flag is HIGH, the SAA7345 will assume that the servo is following on the wrong track, and will flag all incoming HF data as incorrect. The offtrack is input via the V1 pin when the versatile pins interface register (address 1100) bit 0 is set to logic 1.

EFM demodulation

The 14-bit EFM data and subcode words are decoded into 8-bit symbols.

Subcode data processing

Q-CHANNEL PROCESSING

The 96-bit Q-channel word is accumulated in an internal buffer. Sixteen bits are used to perform a Cyclic Redundancy Check (CRC). If the data is good, the SUBQREADY-I signal will go LOW. SUBQREADY-I can be read via the status signal when the status control register (address 0010) is set to X000 (normal reset condition). Good Q-channel data may be read via the microcontroller interface.

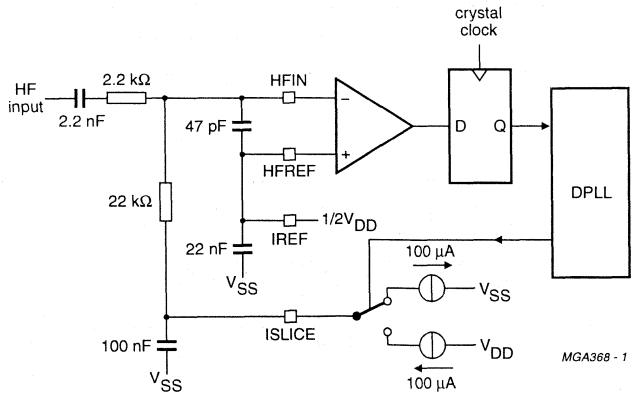


Fig.3 Data slicer showing typical application components.

OTHER SUBCODE CHANNELS

Data of the other subcode channels (Q to W) may be read via the V4 pin if the versatile pins interface register (address 1101) is set to XX01.

The format is similar to RS232. The subcode sync word is formed by a pause of 200 µs minimum. Each subcode byte starts with a logic 1 followed by 7 bits (Q to W). The gap between bytes is variable between 11.3 µs and 90 µs.

The subcode data is also available in the EBU output (DOBM) in a similar format.

Microcontroller interface

The SAA7345 has a 3-line microcontroller interface which is compatible with the digital servo IC TDA1301.

WRITING DATA TO SAA7345

The SAA7345 has thirteen 4-bit programmable configuration registers as shown in Table 2. These can be written to via the microcontroller interface using the protocol shown in Fig.5.

Write operation sequence

- RAB is held LOW by the microcontroller to hold the SAA7345 DA pin at high-impedance.
- Microcontroller data is clocked into the internal shift register on the LOW-to-HIGH clock transition CL.
- Data D (3 : 0) is latched into the appropriate control register [address bits A (3 : 0)] on the LOW-to-HIGH transition of RAB with CL HIGH.
- If more data is clocked into SAA7345 before the LOW-to-HIGH transition of RAB then only the last 8 bits are used.
- If less data is clocked into SAA7345, unpredictable operation will result.
- If the LOW-to-HIGH transition of RAB occurs with CL LOW, the command will be disregarded.

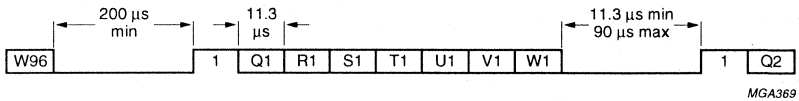


Fig.4 Subcode format and timing at V4 pin.

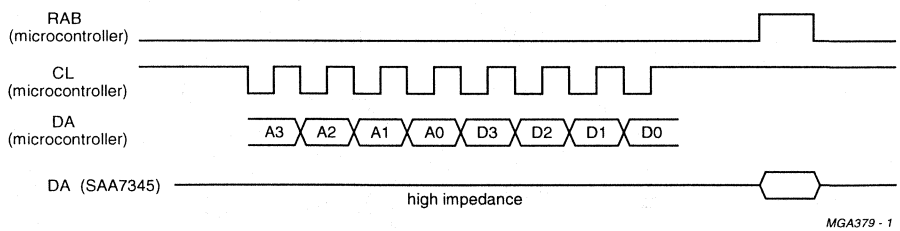
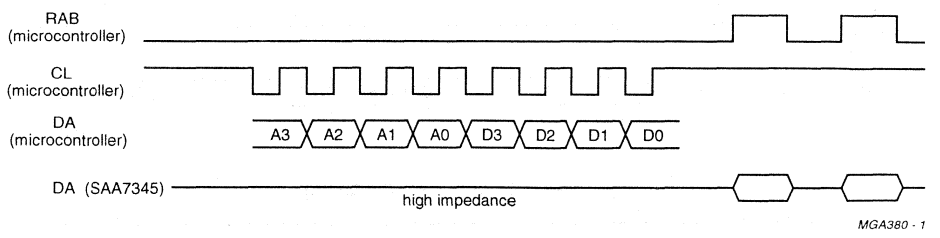


Fig.5 Microcontroller WRITE timing.

WRITING DATA TO SAA7345; REPEAT MODE

The same command can be repeated several times (e.g. for fade function) by applying extra RAB pulses as shown in Fig.6.



Note that CL must stay HIGH between RAB pulses.

Fig.6 Microcontroller WRITE timing; repeat mode.

READING STATUS INFORMATION FROM SAA7345

There are several internal status signals which can be made available on the DA line (Table 1).

Table 1 Internal status signals.

SIGNAL	DESCRIPTION
SUBQREADY-I	LOW if new subcode word is ready in Q-channel register.
MOTSTART1	HIGH if motor is turning at 75% or more of nominal speed.
MOTSTART2	HIGH if motor is turning at 50% or more of nominal speed.
MOTSTOP	HIGH if motor is turning at 12% or less of nominal speed.
PLL Lock	HIGH if Sync coincidence signals are found.
V1	Follows input on V1 pin.
V2	Follows input on V2 pin.
MOTOR-OV	HIGH if the motor servo output stage saturates.

The status signal to be output is selected by status control register (address 0010). The timing for reading the status signal is shown in Fig.7.

Status read operation sequence

- Write appropriate data to register 0010 to select required status signal.
- With RAB LOW; set CL LOW.
- Set RAB HIGH; this will instruct the SAA7345 to output status signal on DA.

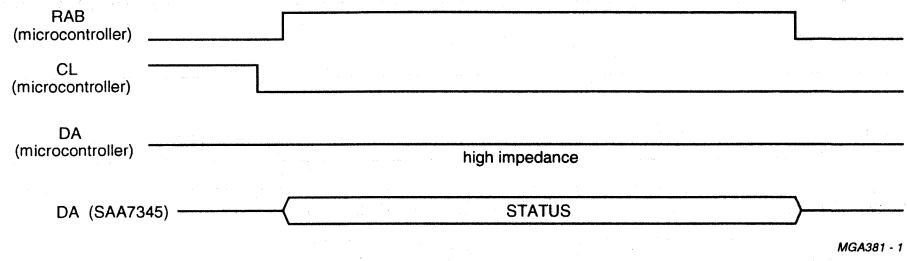


Fig.7 SAA7345 status READ timing.

READING Q-CHANNEL SUBCODE FROM SAA7345

To read Q-channel subcode from SAA7345, the SUBQREADY-I signal should be selected as status signal. The subcode read timing is shown in Fig.8.

Read subcode operation sequence

- Monitor SUBQREADY-I status signal.
- When this signal is LOW, and up to 2.3 ms after its LOW-to-HIGH transition, it is permitted to read subcode.
- Set CL LOW, SAA7345 will output first subcode bit (Q1).
- After subcode read starts, the microcontroller may take as long as it wants to terminate read operation.
- SAA7345 will output consecutive subcode bits after each HIGH-to-LOW transition of CL.
- When enough subcode has been read (1 to 96 bits), stop reading by pulling RAB LOW.

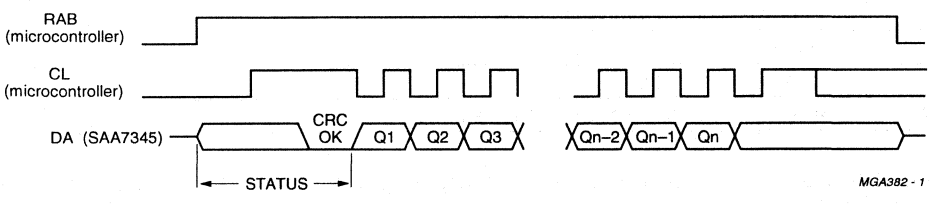


Fig.8 SAA7345 Q-channel subcode READ timing.

PEAK DETECTOR OUTPUT

In place of the CRC-bits (bits 81 to 96), the peak detector information is added to the Q-channel data. The peak information corresponds to the highest audio level (absolute value) and is measured on positive peaks. Only the most significant 8 bits of the peak level are given, in unsigned notation. Bits 81 to 88 contain the LEFT peak value (bit 88 = MSB) and bits 89 to 96 contain the RIGHT channel (bit 96 = MSB). Value is reset after reading Q-channel data.

Behaviour of the SUBQREADY-I signal

When the CRC of the Q-channel word is good, and no subcode is being read, the SUBQREADY-I signal will react as shown in Fig.9.

When the CRC is good and subcode is being read, the timing in Fig.10 applies.

If t_1 (SUBQREADY-I LOW to end of subcode read) is below 2.6 ms, then t_2 = 13.1 ms (i.e. the microcontroller can read all subcode frames if it completes the read operation within 2.6 ms after subcode ready).

If this criterion is not met, it is only possible to guarantee that t_3 will be below 26.2 ms (approximately).

If subcode frames with failed CRCs are present, the t_2 and t_3 times will be increased by 13.1 ms for each defective subcode frame.

Sharing the microcontroller interface

When the RAB pin is held LOW by the microcontroller, it is permitted to put any signal on the DA and CL lines (SAA7345 will set output DA to high-impedance). Under this circumstance these lines may be used for another purpose (e.g. TDA1301 microcontroller interface Data and Clock line, see Fig.11).

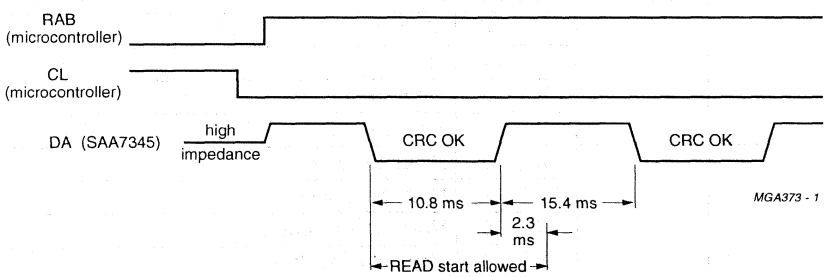


Fig.9 SUBQREADY-I timing when no subcode is read.

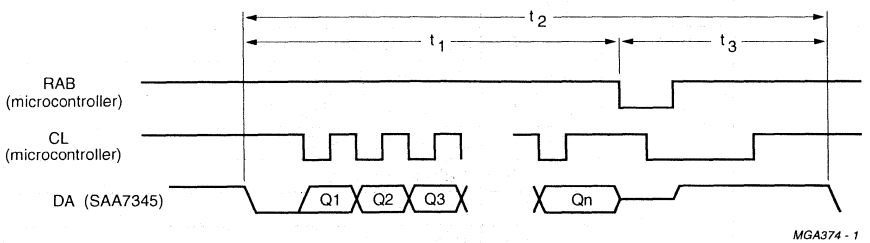


Fig.10 SUBQREADY-I timing when subcode is being read.

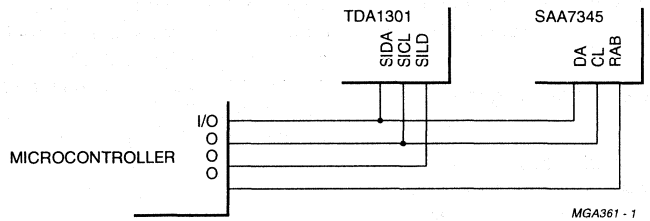


Fig.11 SAA7345 microcontroller interface application diagram.

Table 2 Command registers.
The 'INITIAL' column shows the power-on reset state.

REGISTER	ADDRESS	DATA	FUNCTION	INITIAL
Fade and Attenuation	0 0 0 0	X 0 0 0	Mute	Reset
		X 0 1 X	Attenuate	
		X 0 0 1	Full Scale	
		X 1 0 0	Step Down	
		X 1 0 1	Step Up	
Motor mode	0 0 0 1	X 0 0 0	Motor off mode	Reset
		X 0 0 1	Motor brake mode 1	
		X 0 1 0	Motor brake mode 2	
		X 0 1 1	Motor start mode 1	
		X 1 0 0	Motor start mode 2	
		X 1 0 1	Motor jump mode	
		X 1 1 1	Motor play mode	
		X 1 1 0	Motor jump mode 1	
		1 X X X	anti-windup active	
		0 X X X	anti-windup off	Reset
Status control	0 0 1 0	X 0 0 0	status = SUBQREADY-I	Reset
		X 0 0 1	status = MOTSTART1	
		X 0 1 0	status = MOTSTART2	
		X 0 1 1	status = MOTSTOP	
		X 1 0 0	status = PLL Lock	
		X 1 0 1	status = V1	
		X 1 1 0	status = V2	
		X 1 1 1	status = MOTOR-OV	
		0 X X X	L channel first at DAC (WCLK normal)	Reset
		1 X X X	R channel first at DAC (WCLK inverted)	

REGISTER	ADDRESS	DATA	FUNCTION	INITIAL
DAC output	0 0 1 1	1 0 1 0	I^2S CD-ROM mode	
		1 0 1 1	EIAJ; CD-ROM mode	
		1 1 0 X	I^2S; $4f_s$ mode	Reset
		1 1 1 1	I^2S; $2f_s$ mode	
		1 1 1 0	I^2S; f_s mode	
		0 0 0 X	EIAJ; 16-bit; $4f_s$	
		0 0 1 1	EIAJ; 16-bit; $2f_s$	
		0 0 1 0	EIAJ; 16-bit; f_s	
		0 1 0 X	EIAJ; 18-bit; $4f_s$	
		0 1 1 1	EIAJ; 18-bit; $2f_s$	
		0 1 1 0	EIAJ; 18-bit; f_s	
Motor gain	0 1 0 0	X 0 0 0	Motor gain G = 3.2	Reset
		X 0 0 1	Motor gain G = 4.0	
		X 0 1 0	Motor gain G = 6.4	
		X 0 1 1	Motor gain G = 8.0	
		X 1 0 0	Motor gain G = 12.8	
		X 1 0 1	Motor gain G = 16.0	
		X 1 1 0	Motor gain G = 25.6	
		X 1 1 1	Motor gain G = 32.0	
Motor bandwidth	0 1 0 1	X X 0 0	Motor f_4 = 0.5 Hz	Reset
		X X 0 1	Motor f_4 = 0.7 Hz	
		X X 1 0	Motor f_4 = 1.4 Hz	
		X X 1 1	Motor f_4 = 2.8 Hz	
		0 0 X X	Motor f_3 = 0.85 Hz	Reset
		0 1 X X	Motor f_3 = 1.71 Hz	
		1 0 X X	Motor f_3 = 3.42 Hz	
Motor output configuration	0 1 1 0	X X 0 0	Motor power maximum 37%	Reset
		X X 0 1	Motor power maximum 50%	
		X X 1 0	Motor power maximum 75%	
		X X 1 1	Motor power maximum 100%	
		0 0 X X	MOTO1, MOTO2 pins 3-state	Reset
		0 1 X X	Motor Pulse Width Modulation (PWM) mode	
		1 0 X X	Motor Pulse Density Modulation (PDM) mode	
		1 1 X X	Motor Compact Disc Video (CDV) mode	

REGISTER	ADDRESS	DATA	FUNCTION			INITIAL
			Loop BW (Hz)	Internal BW (Hz)	Low-pass BW (Hz)	
PLL loop filter bandwidth	1 0 0 0	0 0 0 0	1640	525	8400	
		0 0 0 1	3279	263	16800	
		0 0 1 0	6560	131	33600	
		0 1 0 0	1640	1050	8400	
		0 1 0 1	3279	525	16800	
		0 1 1 0	6560	263	33600	
		1 0 0 0	1640	2101	8400	
		1 0 0 1	3279	1050	16800	Reset
		1 0 1 0	6560	525	33600	
		1 1 0 0	1640	4200	8400	
		1 1 0 1	3279	2101	16800	
		1 1 1 0	6560	1050	33600	
PLL loop filter equalization	1 0 0 1	0 0 0 1	PLL 30 ns over-equalization			
		0 0 1 0	PLL 15 ns over-equalization			
		0 0 1 1	PLL nominal equalization			Reset
		0 1 0 0	PLL 15 ns under-equalization			
		0 1 0 1	PLL 30 ns under-equalization			
EBU output	1 0 1 0	X X 0 0	EBU data before concealment			
		X X 1 0	EBU data after concealment and fade			Reset
		X X 1 1	EBU off – output LOW			
		X 0 X X	Level II clock accuracy ($<1000 \times 10^{-6}$)			Reset
		X 1 X X	Level III clock accuracy ($>1000 \times 10^{-6}$)			
		0 X X X	Flags in EBU off			Reset
		1 X X X	Flags in EBU on			
Speed control	1 0 1 1	1 X X X	double-speed mode			
		0 X X X	single-speed mode			Reset
		X 0 X X	33.869 MHz crystal present			Reset
		X 1 X X	16.934 MHz crystal present			
		X X 0 0	standby 1: 'CD-STOP' mode (note 1)			Reset
		X X 1 0	standby 2: 'CD-PAUSE' mode (note 1)			
		X X 1 1	operating mode			
Versatile pins interface	1 1 0 0	X X X 1	offtrack input at V1			
		X X X 0	no offtrack input (V1 may be read via status)			Reset
		X X 0 X	Kill-L at KILL output, Kill-R at V3 output			
		X 0 1 X	V3 = 0; single Kill output			Reset
		X 1 1 X	V3 = 1; single Kill output			

REGISTER	ADDRESS	DATA	FUNCTION	INITIAL
Versatile pins interface	1 1 0 1	0 0 0 0	4-line motor (using V4, V5)	
		X X 0 1	Q to W subcode at V4	
		X X 1 0	V4 = 0	
		X X 1 1	V4 = 1	Reset
		0 1 X X	de-emphasis signal at V5	
		1 0 X X	V5 = 0	
		1 1 X X	V5 = 1	Reset

Note

1. Standby modes = CL, DA and RAB; normal operation.
   MISC, SCLK, WCLK, DATA, CL11 and DOBM; 3-state.
   CRIN, CROUT, CL16 and CLA; normal operation.
   V1, V2, V3, V4 and V5; normal operation.
   MOTO1 and MOTO2 - in standby 2 'CD-PAUSE'; normal operation.
   MOTO1 and MOTO2 - in standby 1 'CD-STOP'; held LOW in PWM mode; 3-state in PDM mode.

Error corrector

The error corrector carries out t = 2, e = 0 error corrections on both C1 (32 symbol) and C2 (28 symbol) frames. Four symbols are used from each frame as parity symbols. The strategy t = 2, e = 0 means that the error corrector can correct two erroneous symbols per frame and detect all erroneous frames.

The error corrector also contains a flag controller. Flags are assigned to symbols when the error corrector cannot ascertain if the symbols are definitely good. C1 generates output flags which are read (after de-interleaving) by C2, to help in the generation of C2 output flags.

The C2 output flags are used by the interpolator for concealment of non-correctable errors. They are also output via the EBU signal (DOBM) and the MISC output with I^2S for CD-ROM applications.

The flags output pin CFLG provides information on the state of all error correction and concealment flags.

Audio functions

De-emphasis and phase linearity

When de-emphasis is detected in the Q-channel subcode, the digital filter automatically includes a de-emphasis filter section. When de-emphasis is not required, a phase compensation filter section controls the phase linearity of the digital oversampling filter to $\leq \pm 1°$ within the band 0 to 16 kHz.

Digital oversampling filter

The SAA7345 contains a 2 to 4 times oversampling filter. The filter specification of the 4× oversampling filter is given in Table 2 and shown in Fig.12.

These attenuations do not include the sample and hold at the DAC output or the DAC post filter.

When using the oversampling filter, the output level is scaled –0.5 dB down, to avoid overflow on full-scale sinewave inputs (0 to 20 kHz).

Table 3 Digital filter passband characteristics.

PASSBAND	ATTENUATION
0 to 19 kHz	≤ 0.001 dB
19 to 20 kHz	≤ 0.03 dB

Table 4 Digital filter stopband characteristics.

STOPBAND	ATTENUATION
24.0 kHz	≥ 25 dB
24 to 27 kHz	≥ 38 dB
27 to 35 kHz	≥ 40 dB
35 to 64 kHz	≥ 50 dB
64 to 68 kHz	≥ 31 dB
68 kHz	≥ 35 dB
69 to 88 kHz	≥ 40 dB

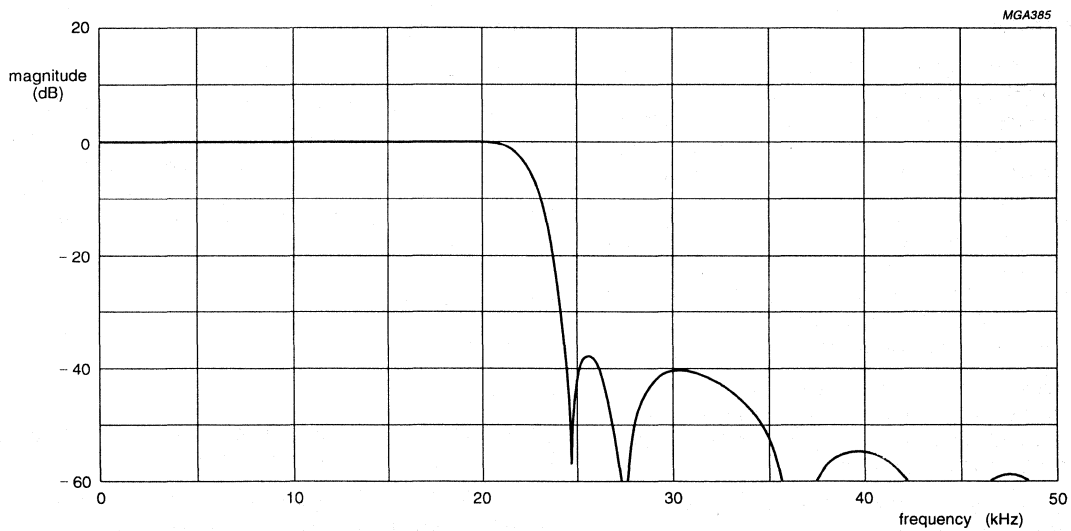


Fig.12 Digital filter characteristics.

CONCEALMENT

A 1-sample linear interpolator becomes active if a single sample is flagged as erroneous but cannot be corrected. The erroneous sample is replaced by a level midway between the preceding and following samples. Left and right channels have independent interpolators.

If more than one consecutive non-correctable sample is found, the last good sample is held. A 1-sample linear interpolation is then performed before the next good sample (see Fig.13).

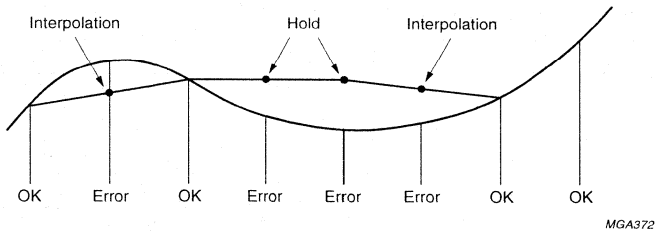


Fig.13 Concealment mechanism.

MUTE, ATTENUATION AND FADE

A digital level controller is present on the SAA7345 which performs the functions of soft mute, attenuation and fade.

Mute and Attenuation

Soft mute is activated by sending the Mute command to the fade control register (address 0000, data X000). The signal will reduced to zero in up to 128 steps (depending on the current position of the fade control), taking a maximum of 3 ms.

Attenuation (−12 dB) is activated by sending the Attenuate command to the fade control register (data X01X).

Attenuation and mute are cancelled by sending the Full Scale command to the fade control register (data X001). It will take 3 ms to ramp the output from mute to the full-scale level.

Fade

The audio output level is determined by the value of the internal fade counter.

$$\text{Level} = \frac{\text{counter}}{128} \times \text{maximum level}$$

- The counter is preset to 128 by the Full Scale command if no oversampling is required.
- The counter is preset to 120 (−0.5 dB scaling) by the Full Scale command if either $2f_s$ or $4f_s$ oversampling is programmed in the DAC output register (address 0011).
- The counter is preset to 32 by the Attenuate command.
- The counter is preset to 0 by the Mute command.

To control the fade counter in a continuous way, the step-up and step-down commands are available (fade control register data X101 and X100). They will increment or decrement the counter by 1 for each register write operation.

- When issuing more than 1 step-up or step-down command in sequence, the write repeat mode may be used (see Fig.6).
- A pause of at least 22 µs is necessary between any two step-up or step-down commands.
- When a step-up command is given when the fade counter is already at its full-scale value, the counter will not increment.

DAC Interface

The SAA7345 is compatible with a wide range of Digital-to-Analog Converters. Eleven formats are supported and are shown in Table 5.

All formats are MSB first. f_s is 44.1 kHz in single-speed mode and 88.2 kHz in double-speed mode.

Table 5 DAC interface formats.

MODE	DAC CONTROL REGISTER DATA	SAMPLE FREQUENCY	BITS	SCLK (MHz)	FORMAT	INTERPOLATION
1	1 0 1 0	f_s	16	$2.1168 \times n^{(1)}$	CD-ROM (I^2S)	no
2	1 0 1 1	f_s	16	$2.1168 \times n^{(1)}$	CD-ROM (EIAJ)[2]	no
3	1 1 1 0	f_s	16	$2.1168 \times n^{(1)}$	Philips I^2S – 16 bits	yes
4	0 0 1 0	f_s	16	$2.1168 \times n^{(1)}$	EIAJ – 16 bits	yes
5	0 1 1 0	f_s	18	$2.1168 \times n^{(1)}$	EIAJ – 18 bits	yes
6	0 0 0 X	$4f_s$	16	$8.4672 \times n^{(1)}$	EIAJ – 16 bits	yes
7	0 1 0 X	$4f_s$	18	$8.4672 \times n^{(1)}$	EIAJ – 18 bits	yes
8	1 1 0 X	$4f_s$	18	$8.4672 \times n^{(1)}$	Philips I^2S – 18 bits	yes
9	0 0 1 1	$2f_s$	16	$4.2336 \times n^{(1)}$	EIAJ – 16 bits	yes
10	0 1 1 1	$2f_s$	18	$4.2336 \times n^{(1)}$	EIAJ – 18 bits	yes
11	1 1 1 1	$2f_s$	18	$4.2336 \times n^{(1)}$	Philips I^2S – 18 bits	yes

Note

1. n = disc speed.
2. EIAJ is the abbreviation for: Electronic Industries Associated of Japan.

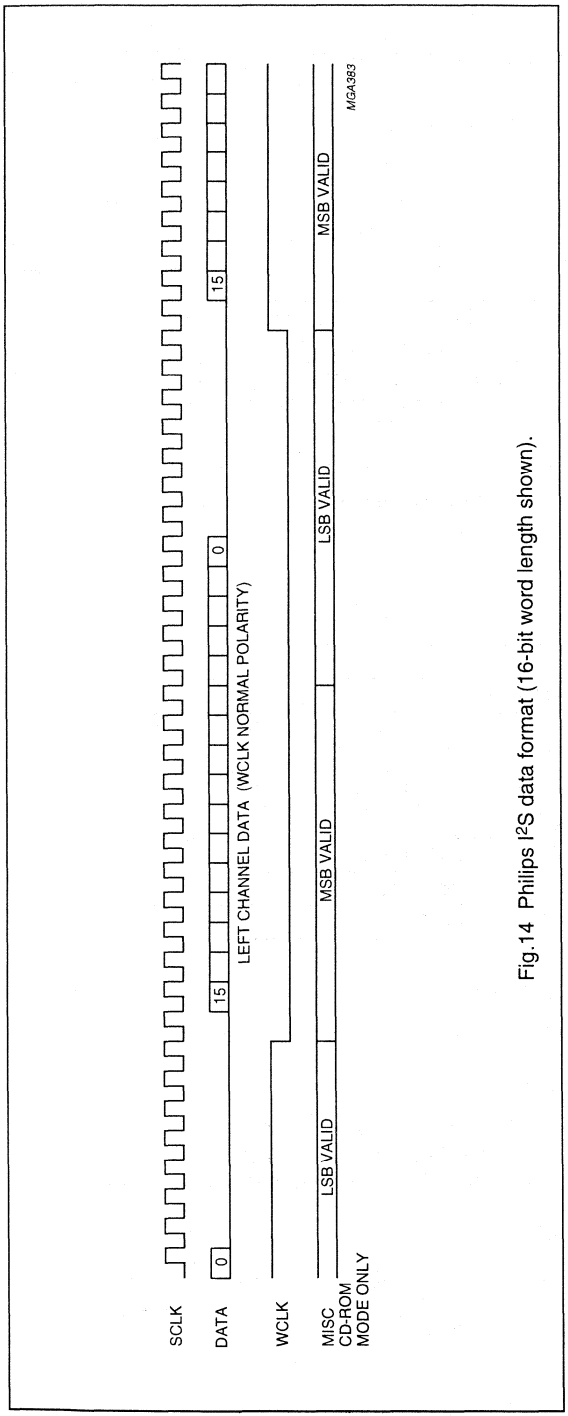


Fig.14 Philips I²S data format (16-bit word length shown).

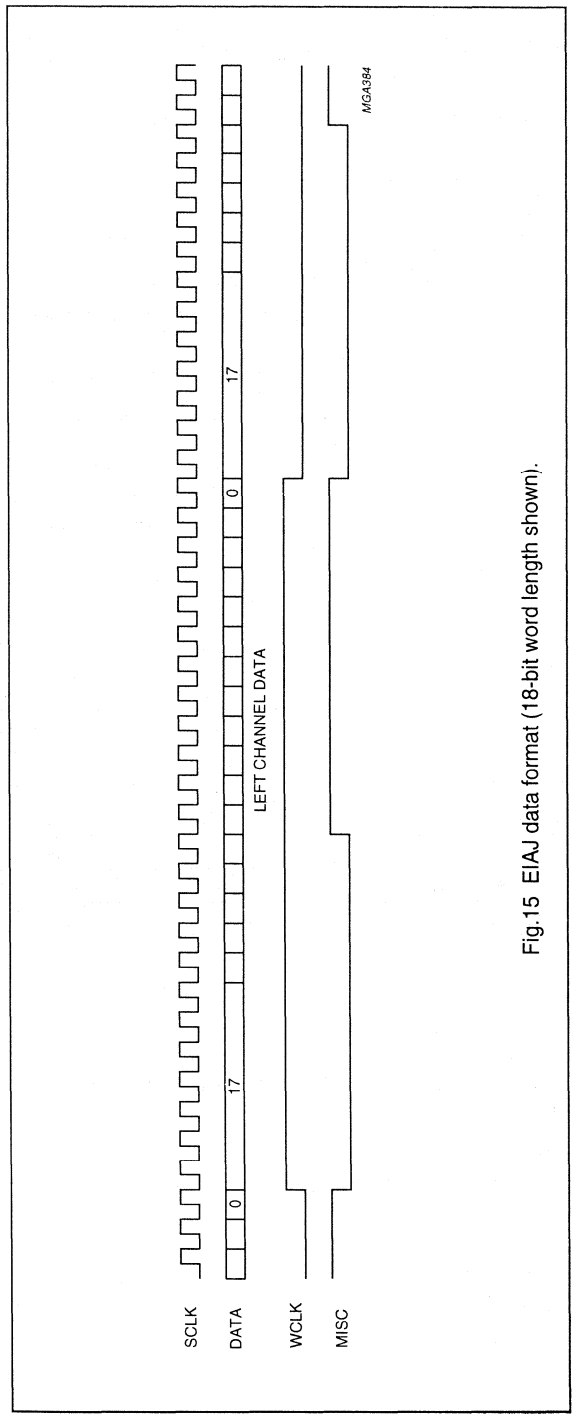


Fig.15 EIAJ data format (18-bit word length shown).

EBU interface

The biphase-mark digital output signal at pin DOBM is in accordance with the format defined by the *"IEC 958"* specification.

Three different modes can be selected via the EBU output control register (address 1010).

Table 6 EBU output modes.

EBU CONTROL REGISTER DATA	EBU OUTPUT AT DOBM PIN	EBU VALIDITY FLAG (BIT 28)
X X 1 1	DOBM pin held LOW	–
X X 0 0	data taken before concealment, mute and fade	HIGH if data is non-correctable (concealment flag)
X X 1 0	data taken after concealment, mute and fade	HIGH if data is non-correctable (concealment flag)

FORMAT

The digital audio output consists of 32-bit words (subframes) transmitted in biphase-mark code (two transitions for a logic 1 and one transition for a logic 0). Words are transmitted in blocks of 384 (see Table 7).

Table 7 EBU word format.

WORD	BITS	FUNCTION
Sync	0 to 3	–
Auxiliary	4 to 7	not used; normally zero
Error flags	4	CFLG error and interpolation flags when bit 3 of EBU control register is set to logic 1
Audio sample	8 to 27	first 4 bits not used (always zero)
Validity flag	28	valid = logic 0
User data	29	used for subcode data (Q to W)
Channel status	30	control bits and category code
Parity bit	31	even parity for bits 4 to 30

SYNC

The sync word is formed by violation of the biphase rule and therefore does not contain any data. Its length is equivalent to 4 data bits. The three different sync patterns indicate the following situations:

- Sync B:
  - Start of a block (384 words), word contains left sample.
- Sync M:
  - Word contains left sample (no block start).
- Sync W:
  - Word contains right sample.

AUDIO SAMPLE

Left and right samples are transmitted alternately.

VALIDITY FLAG

Audio samples are flagged (bit 28 = logic 1) if an error has been detected but was non-correctable. This flag remains the same even if data is taken after concealment.

USER DATA

Subcode bits Q until W from the subcode section are transmitted via the user data bit. This data is asynchronous with the block rate.

CHANNEL STATUS

The channel status bit is the same for left and right words. Therefore a block of 384 words contains 192 channel status bits. The category code is always CD. The bit assignment is shown in Table 8.

Table 8 EBU channel status.

WORD	BITS	FUNCTION
Control	0 to 3	copy of CRC checked Q-channel control bits 0 to 3; bit 2 is logic 1 when copy permitted; bit 3 is logic 1 when recording has pre-emphasis
Reserved mode	4 to 7	always zero
Category code	8 to 15	CD: bit 8 = logic 1; all other bits = logic 0
Clock accuracy	28 to 29	set by EBU control register: 00 = Level II 01 = Level III
Remaining	16 to 27 30 to 191	always zero

KILL circuit

The KILL circuit detects digital silence by testing for an all-zero or all-ones data word in the left or right channel before the digital filter. The output is switched active LOW when silence has been detected for at least 200 ms. Two modes are available, selected by the versatile pins register (address 1100):

1-PIN KILL MODE

Active LOW signal on KILL pin when digital silence has been detected on both LEFT and RIGHT channels for 200 ms.

2-PIN KILL MODE

Independent digital silence detection for left and right channels. The KILL pin is active LOW when digital silence has been detected in the LEFT channel for 200 ms, and V3 is active LOW when digital silence has been detected in the RIGHT channel for 200 ms.

When MUTE is active then the KILL output is forced LOW.

Spindle motor control

The spindle motor speed is controlled by a fully integrated digital servo. Address information from the internal ±8 frame FIFO and disc speed information are used to calculate the motor control output signals.

Several output modes are supported:

1. Pulse Density, 2-line (true complement output), 1 MHz sample frequency.
2. PWM output, 2-line, 22.05 kHz modulation frequency.
3. PWM-output, 4-line, 22.05 kHz modulation frequency.
4. CDV motor mode.

The modes are selected via the motor output configuration register (address 0110).

PULSE DENSITY MODE

In the Pulse Density mode the motor output pin MOTO1 is the pulse density modulated motor output signal. A 50% duty cycle corresponds with the motor not actuated, higher duty cycles mean acceleration, lower mean braking.

In this mode, the MOTO2 signal is the inverse of the MOTO1 signal. Both signals change state only on the edges of a 1 MHz internal clock signal.

Possible application diagrams are shown in Fig.16.

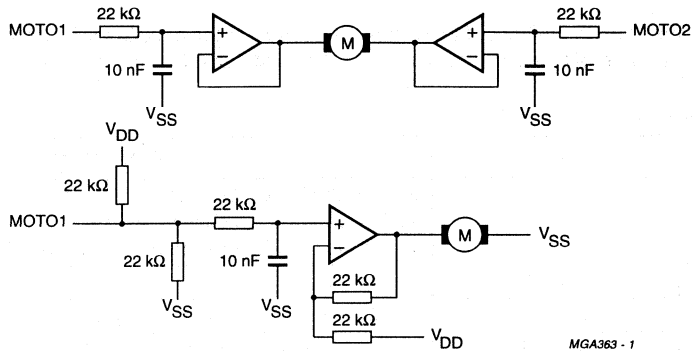


Fig.16 Motor pulse density application diagrams.

PWM MODE, 2-LINE

In the PWM mode the motor acceleration signal is put in pulse-width modulation form on the MOTO1 output and the motor braking signal is pulse-width modulated on the MOTO2 output.

Figure 17 shows the timing and Fig.18 a typical application diagram.

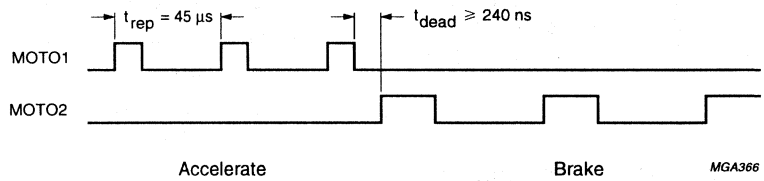


Fig.17 Motor 2-line PWM mode timing.

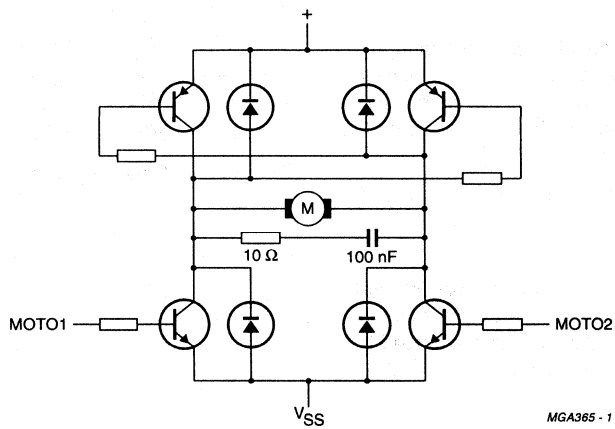


Fig.18 Motor 2-line PWM mode application diagram.

PWM MODE, 4-LINE

Using two extra outputs from the Versatile Pins Interface, it is possible to use the SAA7345 with a 4-input motor bridge. Figure 19 shows the timing and Fig.20 a typical application diagram.

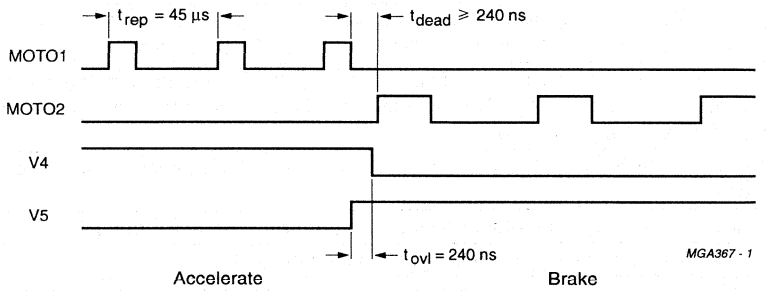


Fig.19 Motor 4-line PWM mode timing.

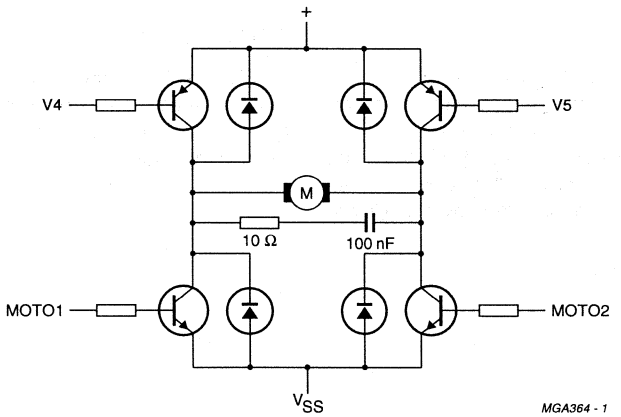


Fig.20 Motor 4-line PWM mode application diagram.

CDV MODE

In the CDV motor mode, the FIFO position will be put in pulse-width modulated form on the MOTO1 pin (carrier frequency 300 Hz) and the PLL frequency signal will be put in pulse-density modulated form on the MOTO2 pin (carrier frequency 4.23 MHz). The integrated motor servo is disabled in this mode.

Remark:

The PWM signal on MOTO1 corresponds to a total memory space of 20 frames, therefore the nominal FIFO position (half-full) will result in a PWM output of 60%.

OPERATION MODES

The motor servo has the operation modes as shown in Table 9 and is controlled by the motor mode register (address 0001).

Table 9 Operation modes.

MODE	DESCRIPTION
Start mode 1	Disc is accelerated by applying a positive voltage to the spindle motor. No decisions are involved and the PLL is reset. No disc speed information is available for the microcontroller.
Start mode 2	The disc is accelerated as in Start mode 1, however the PLL will monitor the disc speed. When the disc reaches 75% of its nominal speed, the controller will switch to Jump mode. The motor status signals are valid (register 0010).
Jump mode	Motor servo enabled but FIFO kept reset at 50%. The audio is muted but it is possible to read the subcode.
Jump mode 1	Similar to Jump mode but motor integrator is kept at zero. Used for long jumps.
Play mode	FIFO released after resetting to 50%. Audio mute released.
Stop mode 1	Disc is braked by applying a negative voltage to the motor. No decisions are involved.
Stop mode 2	The disc is braked as in Stop mode 1, but the PLL will monitor the disc speed. As soon as the disc reaches 12% of its nominal speed, the MOTSTOP status signal will go HIGH and switch the motor servo to off mode.
Off mode	Motor not steered.

POWER LIMIT

In Start mode 1, Start mode 2, Stop mode 1 and Stop mode 2, a fixed positive or negative voltage is applied to the motor. This voltage can be programmed as a percentage of the maximum possible voltage via the motor output configuration register (address 0110) to limit current drain during start and stop. The following power limits are possible:

- 100% of maximum (no power limit)
- 75% of maximum
- 50% of maximum
- 37% of maximum.

LOOP CHARACTERISTICS

The gain and cross-over frequencies of the motor control loop can be programmed via the motor gain and bandwidth registers (addresses 0100 and 0101). The possible parameter values are as follows:

Gain: 3.2, 4.0, 6.4, 8.0 12.8, 16, 26.6 or 32.

Cross-over frequency, f_4: –0.5, –0.7, –1.4 or –2.8 Hz.

Cross-over frequency, f_3: –0.85, –1.71 or –3.42 Hz.

FIFO OVERFLOW

If FIFO overflow occurs during Play mode (e.g. as a result of motor shock), the FIFO will be automatically reset to 50% and the audio interpolator is activated to minimize the effect of data loss.

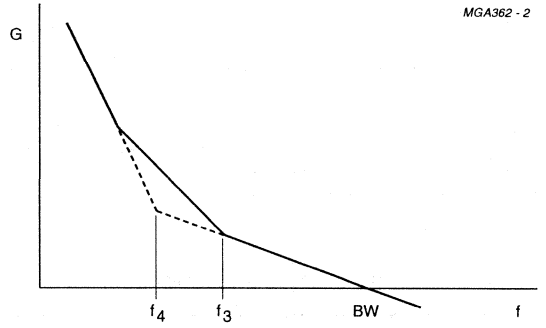


Fig.21 Motor servo mode diagram.

Versatile pins interface

The SAA7345 has five pins that can be reconfigured for different applications as shown in Table 10.

Table 10 Versatile pins.

SYMBOL	PIN	TYPE	CONTROL REGISTER ADDRESS	CONTROL REGISTER DATA	FUNCTION
V1	3	input	1 1 0 0	X X X 1	offtrack input (from digital servo)
				X X X 0	input may be read via status register (address 0010 data X101)
V2	4	input	–	–	input may be read via status register (address 0010 data X110)
V3	26	output	1 1 0 0	X X 0 X	kill output for right channel
				X 0 1 X	output = logic 0
				X 1 1 X	output = logic 1
V4	25	output	1 1 0 1	0 0 0 0	4-line motor drive (using V4 and V5)
				X X 0 1	Q-W subcode output
				X X 1 0	output = logic 0
				X X 1 1	output = logic 1
V5	24	output	1 1 0 1	0 1 X X	de-emphasis output (active HIGH)
				1 0 X X	output = logic 0
				1 1 X X	output = logic 1

Flags Output (CFLG) (open drain output)

A 1-bit flag signal is available at the CFLG pin. This signal shows the status of the error corrector and interpolator and is updated every frame (7.35 kHz).

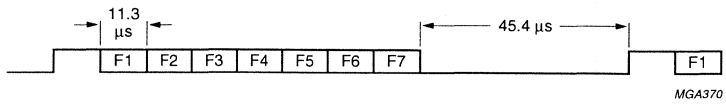


Fig.22 Flags output timing.

Table 11 Meaning of flag bits.

F1	F2	F3	F4	F5	F6	F7	MEANING
0	X	X	X	X	X	X	no absolute time sync
1	X	X	X	X	X	X	absolute time sync
X	0	0	X	X	X	X	C1 frame contained no errors
X	0	1	X	X	X	X	C1 frame contained 1 error
X	1	0	X	X	X	X	C1 frame contained 2 errors
X	1	1	X	X	X	X	C1 frame non-correctable
X	X	X	0	0	X	X	C2 frame contained no errors
X	X	X	0	1	X	X	C2 frame contained 1 error
X	X	X	1	0	X	X	C2 frame contained 2 errors
X	X	X	1	1	X	X	C2 frame non-correctable
X	X	X	X	X	0	0	no interpolations
X	X	X	X	X	0	1	at least one 1-sample interpolation
X	X	X	X	X	1	0	at least one hold and no interpolations
X	X	X	X	X	1	1	at least one hold and one 1-sample interpolation

ABSOLUTE TIME SYNC

The first flag bit (F1) is the absolute time sync signal. It is the FIFO-passed subcode-sync and relates the position of the subcode-sync to the audio data (DAC output).

The flag may be used for special purposes such as synchronization of different players.

FLAGS AT EBU OUTPUT

The CFLG flags are available on bit 4 of the EBU data format when bit 3 of the EBU output control register (address 1010) is set to logic 1.

Double speed mode

Double speed mode is programmed via the Speed control register (address 1011). It is possible to program double speed independent of clock frequency, but optimum performance is achieved with a 33.8688 MHz crystal or a ceramic resonator.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	−0.5	+6.5	V
$V_{I(max)}$	maximum input voltage		−0.5	V_{DD} + 0.5	V
V_O	output voltage		−0.5	+6.5	V
I_O	output current (continuous)		−	±20	mA
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−55	+125	°C
V_{es1}	electrostatic handling	note 2	−2000	+2000	V
V_{es2}	electrostatic handling	note 3	−200	+200	V

Notes

1. All V_{DD} and V_{SS} connections must be made externally to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a rise time of 15 ns.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 µH series inductor.

CHARACTERISTICS

V_{DD} = 3.4 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		3.4	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V	−	22	50	mA
Analog Front End (V_{DD} = 4.5 to 5.5 V); comparator inputs HFIN and HFREF						
f_{clk}	clock frequency		8	−	35	MHz
V_{th}	switching thresholds		1.2	−	V_{DD} − 0.4	V
Analog Front End (V_{DD} = 3.4 to 5.5 V); comparator inputs HFIN and HFREF						
f_{clk}	clock frequency		8	−	20	MHz
V_{tpt}	HFIN input voltage level		−	1.0	−	V
Digital inputs CL and RAB						
V_{IL}	LOW level input voltage		−0.3	−	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	−	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	−	+10	µA
C_I	input capacitance		−	−	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital inputs $\overline{PORE}$, V1 and V2						
V_{thr}	switching threshold voltage rising		–	–	$0.8V_{DD}$	V
V_{thf}	switching threshold voltage falling		$0.2V_{DD}$	–	–	V
V_{hys}	hysteresis voltage		–	$0.33V_{DD}$	–	V
R_{PU}	input pull-up resistance	V_I = 0 V	–	50	–	kΩ
C_I	input capacitance		–	–	10	pF
t_{rw}	reset pulse width	$\overline{PORE}$ only	1	–	–	µs
Digital outputs CL16 and CLA						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −1 mA	V_{DD} − 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	C_L = 20 pF; note 1	–	–	15	ns
t_f	output fall time	C_L = 20 pF; note 1	–	–	15	ns
Digital outputs V4 and V5						
V_{OL}	LOW level output voltage	V_{DD} = 4.5 V to 5.5 V; I_{OL} = 10 mA	0	–	1.0	V
		V_{DD} = 3.4 V to 5.5 V; I_{OL} = 5 mA	0	–	1.0	V
V_{OH}	HIGH level output voltage	V_{DD} = 4.5 V to 5.5 V; I_{OH} = −10 mA	V_{DD} − 1	–	V_{DD}	V
		V_{DD} = 3.4 V to 5.5 V; I_{OH} = −5 mA	V_{DD} − 1	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	C_L = 20 pF; note 1	–	–	15	ns
t_f	output fall time	C_L = 20 pF; note 1	–	–	15	ns
Open-drain output CFLG						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
I_{OL}	LOW level output current		–	–	2	mA
C_L	load capacitance		–	–	50	pF
t_f	output fall time	C_L = 20 pF; note 1	–	–	30	ns
Open-drain outputs KILL and V3						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
I_{OL}	LOW level output current		–	–	2	mA
C_L	load capacitance		–	–	50	pF
t_f	output fall time	C_L = 20 pF; note 1	–	–	15	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
3-state outputs MISC, SCLK, WCLK, DATA and CL11						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –1 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	C_L = 20 pF; note 1	–	–	15	ns
t_f	output fall time	C_L = 20 pF; note 1	–	–	15	ns
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
3-state outputs MOTO1, MOTO2 and DOBM						
V_{OL}	LOW level output voltage	V_{DD} = 4.5 V to 5.5 V; I_{OL} = 10 mA	0	–	1.0	V
		V_{DD} = 3.4 V to 5.5 V; I_{OL} = 5 mA	0	–	1.0	V
V_{OH}	HIGH level output voltage	V_{DD} = 4.5 V to 5.5 V; I_{OH} = –10 mA	V_{DD} – 1	–	V_{DD}	V
		V_{DD} = 3.4 V to 5.5 V; I_{OH} = –5 mA	V_{DD} – 1	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	C_L = 20 pF; note 1	–	–	10	ns
t_f	output fall time	C_L = 20 pF; note 1	–	–	10	ns
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
Digital input/output DA						
V_{IL}	LOW level input voltage		–0.3	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD} + 0.3	V
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –1 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	C_L = 20 pF; note 1	–	–	15	ns
t_f	output fall time	C_L = 20 pF; note 1	–	–	15	ns
Crystal oscillator input CRIN (external clock)						
g_m	mutual conductance at start-up		–	4	–	mS
R_O	output resistance at start-up		–	11	–	kΩ
C_I	input capacitance		–	–	10	pF
I_{LI}	input leakage current		–10	–	+10	µA
Crystal oscillator output CROUT (see Fig.26)						
f_{xtal}	crystal frequency		8	16.9344	35	MHz
C_{fb}	feedback capacitance		–	–	5	pF
C_O	output capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I^2S timing						
CLOCK OUTPUT SCLK (SEE FIG.23)						
t_{cy}	output clock period	sample rate = f_s	–	472.4	–	ns
		sample rate = $2f_s$	–	236.2	–	ns
		sample rate = $4f_s$	–	118.1	–	ns
t_H	clock HIGH time	sample rate = f_s	166	–	–	ns
		sample rate = $2f_s$	83	–	–	ns
		sample rate = $4f_s$	42	–	–	ns
t_L	clock LOW time	sample rate = f_s	166	–	–	ns
		sample rate = $2f_s$	83	–	–	ns
		sample rate = $4f_s$	42	–	–	ns
t_{su}	set-up time	sample rate = f_s	95	–	–	ns
		sample rate = $2f_s$	48	–	–	ns
		sample rate = $4f_s$	24	–	–	ns
t_h	hold time	sample rate = f_s	95	–	–	ns
		sample rate = $2f_s$	48	–	–	ns
		sample rate = $4f_s$	24	–	–	ns
I^2S timing (double speed)						
CLOCK OUTPUT SCLK (SEE FIG.23)						
t_{cy}	output clock period	sample rate = f_s	–	236.2	–	ns
		sample rate = $2f_s$	–	118.1	–	ns
		sample rate = $4f_s$	–	59.1	–	ns
t_H	clock HIGH time	sample rate = f_s	83	–	–	ns
		sample rate = $2f_s$	42	–	–	ns
		sample rate = $4f_s$	21	–	–	ns
t_L	clock LOW time	sample rate = f_s	83	–	–	ns
		sample rate = $2f_s$	42	–	–	ns
		sample rate = $4f_s$	21	–	–	ns
t_{su}	set-up time	sample rate = f_s	48	–	–	ns
		sample rate = $2f_s$	24	–	–	ns
		sample rate = $4f_s$	12	–	–	ns
t_h	hold time	sample rate = f_s	48	–	–	ns
		sample rate = $2f_s$	24	–	–	ns
		sample rate = $4f_s$	12	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Microcontroller interface timing (see Figs 24 and 25)						
INPUTS CL AND RAB						
t_L	input LOW time	single speed	500	–	–	ns
		double speed	260	–	–	ns
t_H	input HIGH time	single speed	500	–	–	ns
		double speed	260	–	–	ns
t_r	rise time	single speed	–	–	480	ns
t_f	fall time	double speed	–	–	240	ns
READ MODE						
t_{dRD}	delay time RAB to DA valid		0	–	50	ns
t_{dRZ}	delay time RAB to DA high-impedance		0	–	50	ns
t_{pd}	propagation delay CL to DA	single speed	700	–	980	ns
		double speed	340	–	500	ns
WRITE MODE						
t_{suD}	set-up time DA to CL	single speed; note 2	−700	–	–	ns
		double speed; note 2	−340	–	–	ns
t_{hD}	hold time CL to DA	single speed	–	–	980	ns
		double speed	–	–	500	ns
t_{suCR}	set-up time CL to RAB	single speed	260	–	–	ns
		double speed	140	–	–	ns
t_{dWZ}	delay time DA high-impedance to RAB		50	–	–	ns

Notes

1. Timing reference voltage levels are 0.8 V and V_{DD} − 0.8 V.
2. Negative set-up time means that data may change after clock transition.

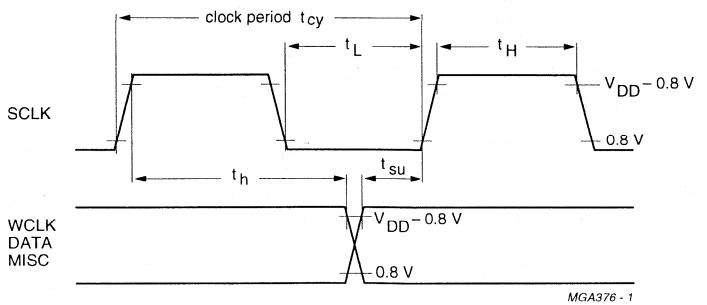


Fig.23 I^2S timing.

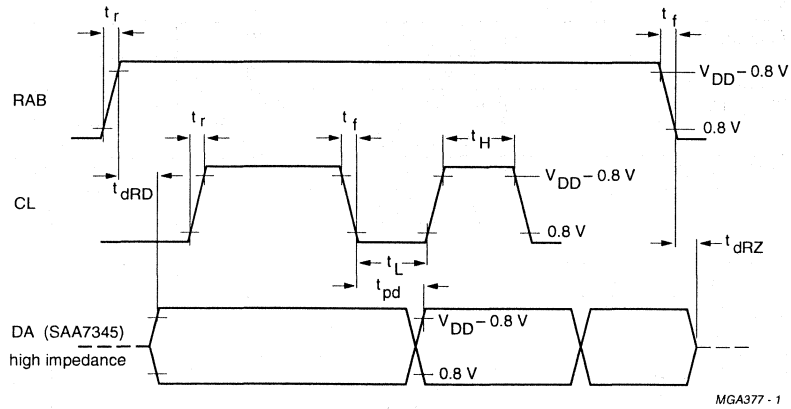


Fig.24 Microcontroller timing; READ mode.

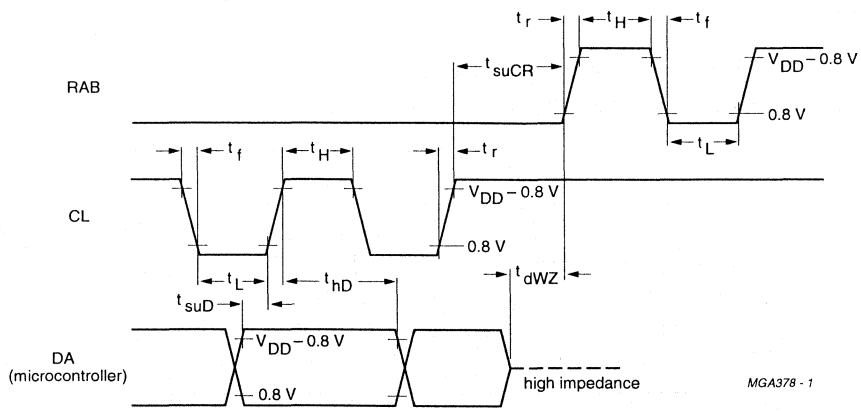


Fig.25 Microcontroller timing; WRITE mode.

APPLICATION INFORMATION

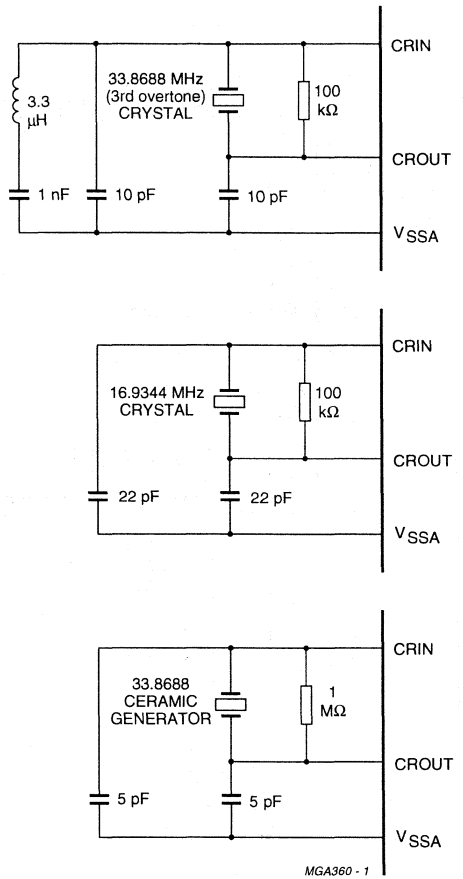
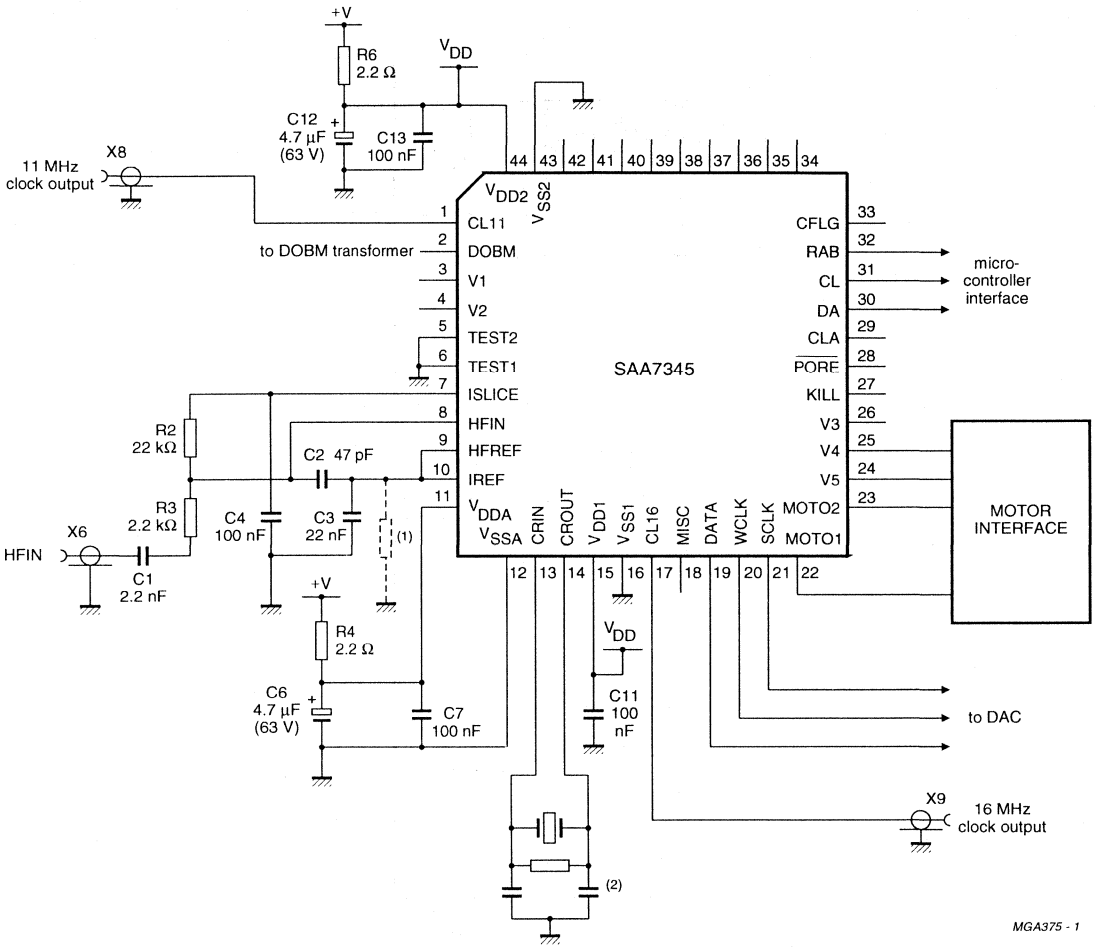


Fig.26 Application circuits for crystal oscillator.



(1) Diagram is for a 5 V application. For 3.4 V applications an additional resistor of 150 kΩ should be added between IREF (pin 10) and ground.
(2) For crystal oscillator circuit see Fig.26.

Fig.27 Typical SAA7345 application diagram.

Shock absorbing RAM addresser SAA7346

FEATURES

- Absorbs shocks from x, y and z directions
- Absorbs rotational shocks
- Absorbs multiple shocks per second
- Interfaces directly to compact disc decoders SAA7345, SAA7347 and SAA7370
- Multi-speed I^2S-bus input with single-speed I^2S-bus output
- Controls 1 or 4 MBit of external Dynamic Random Access Memory (DRAM)
- Easy serial interface for communication with common microcontrollers
- Software selectable shock detectors
- By-pass/power-down mode
- Kill interface for DAC deactivation
- Can be used for:
  - 'sampling' part of a disc
  - to reduce access pauses between jumps
  - to deliver a programmable delay
  - to generate a fixed audio rate from Constant Angular Velocity (CAV) discs.

GENERAL DESCRIPTION

The SAA7346 can be used to make a CD player insensitive to shocks. To do this, SAA7346 operates closely with a standard 1 Mbit or 4 Mbit DRAM. Audio data is stored inside the DRAM and during shocks the data of the DRAM can be played. The SAA7346 functions as a customized DRAM controller with serial I/O and on-board shock detectors.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	3.3	5.0	5.5	V
I_{DD}	supply current	–	12	–	mA
f_{clk}	clock frequency	–	16.9344	–	MHz
$f_{i(clk)}$	I^2S input word clock frequency	44.1	88.2	176.4	kHz
$f_{o(clk)}$	I^2S output word clock frequency	44.1	88.2	176.4	kHz
T_{amb}	operating ambient temperature	−40	–	+85	°C
T_{stg}	storage temperature	−65	–	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7346H	44	QFP(1)	plastic	SOT307-2

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* are followed. The pocketbook can be ordered using the code 9398 510 34011.

BLOCK DIAGRAM

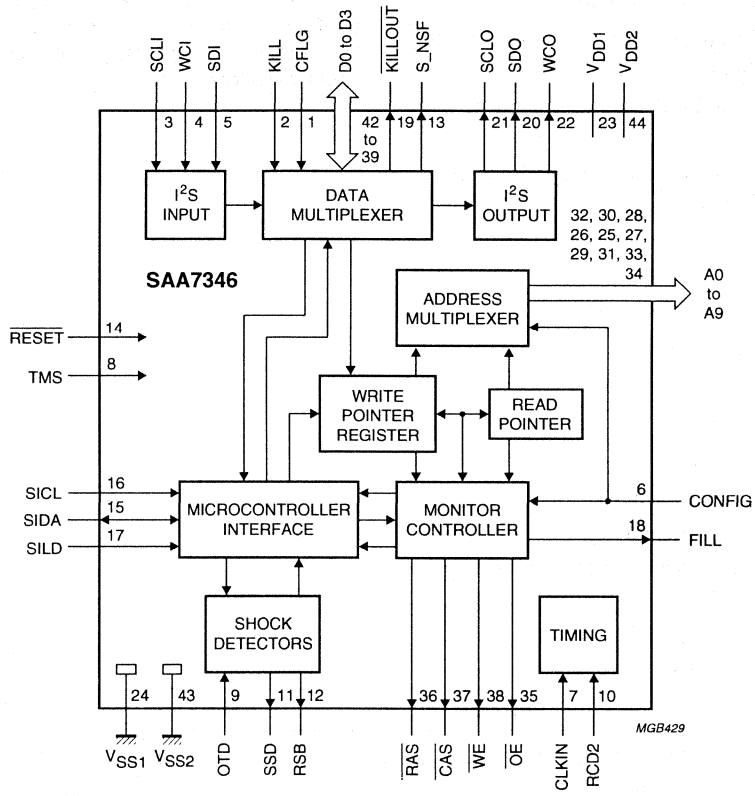


Fig.1 Simplified SAA7347 block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CFLG	1	correction flag input from CD decoder
KILL	2	kill input
SCLI	3	multi-speed I^2S bit clock input
WCI	4	multi-speed I^2S word clock input
SDI	5	multi-speed I^2S data input
CONFIG	6	external DRAM select input; HIGH 4 Mbit, LOW 1 Mbit
CLKIN	7	16.9344 MHz system clock input
TMS	8	test mode select input; active HIGH
OTD	9	on/off track detector input
RCD2	10	DRAM read cycle divide-by-2 input; active HIGH
SSD	11	shock detected output; active HIGH when shock is detected
RSB	12	rotational shock busy output; active HIGH when rotational shock is detected
S_NSF	13	synthetic new subcode frame output
$\overline{\text{RESET}}$	14	reset enable input; active LOW
SIDA	15	microcontroller interface input/output data line
SICL	16	microcontroller interface clock input
SILD	17	microcontroller interface $\overline{\text{read}}$/write input
FILL	18	FIFO write enable output; active HIGH
$\overline{\text{KILLOUT}}$	19	open drain output; active LOW; when in by-pass mode $\overline{\text{KILLOUT}}$ equals KILL
SDO	20	I^2S data output
SCLO	21	I^2S bit clock output
WCO	22	I^2S word clock output
V_{DD1}	23	supply voltage 1
V_{SS1}	24	supply ground 1
A4	25	DRAM address bus output 4
A3	26	DRAM address bus output 3
A5	27	DRAM address bus output 5
A2	28	DRAM address bus output 2
A6	29	DRAM address bus output 6
A1	30	DRAM address bus output 1
A7	31	DRAM address bus output 7
A0	32	DRAM address bus output 0
A8	33	DRAM address bus output 8
A9	34	DRAM address bus output 9
$\overline{\text{OE}}$	35	DRAM enable output; active LOW
$\overline{\text{RAS}}$	36	DRAM row address strobe output; active LOW
$\overline{\text{CAS}}$	37	DRAM column address strobe output; active LOW
$\overline{\text{WE}}$	38	DRAM write enable output; active LOW

SYMBOL	PIN	DESCRIPTION
D3 to D0	39 to 42	DRAM data bus inputs/outputs
V_{SS2}	43	supply ground 2
V_{DD2}	44	supply voltage 2

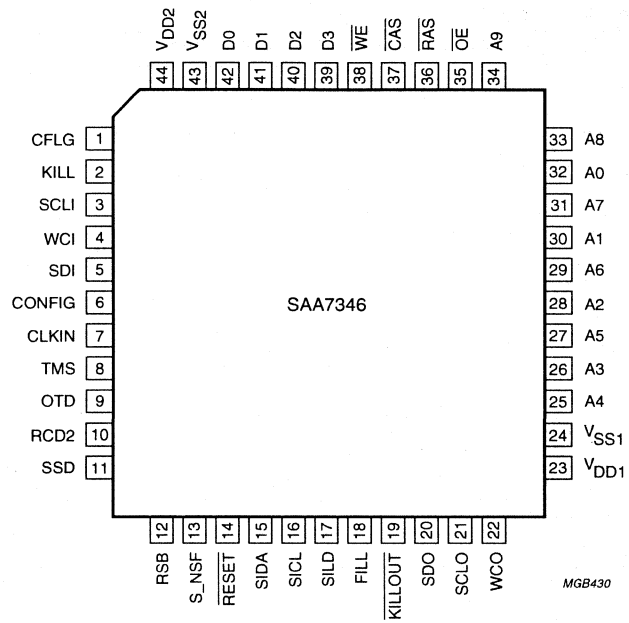


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

I²S input/output interfaces

The SAA7346 contains an asynchronous serial input and a serial output interface. The serial operation of the interfaces is under hardware control of the external circuitry and uses the I²S protocol. The output presents a continuous clock signal SCLO (typically 2.8224 MHz) which is divided from the system clock, and a word select signal WCO, typically 44.1 kHz (f_s), which is used to distinguish between right and left channels. When in by-pass mode WCO and SCLO are the same as the input interface signals WCI and SCLI, enabling data to pass through the SAA7346. Since the serial input port is asynchronous the device is independent of the CD decoder clock speed and enables the word clock to vary from $1.1 \times f_s$ to $4 \times f_s$ (typically $2 \times f_s$). This is a requirement of any electronic shock absorbing system since the disc must be rotating faster than usual to assure the FIFO is full to absorb a shock. The falling edge of WCO indicates the start of a new transfer. Data is exchanged over the SDI and SDO pins. The SAA7346 is compatible with a variety of DAC ICs.

New subcode frame regeneration

The SAA7346 has a digital phase-locked loop (PLL) system which decodes the F1 and F6 flags, from the first 1-bit signal generated by the CD decoder correction flag output shown in Fig.3. The F1 flag is the absolute time sync signal of the New Subcode Frame (NSF). It relates

the position of the subcode-sync to the audio data. This signal determines the accuracy with which the SAA7346 sews audio data together after a shock. When the CD decoder preforms a jump the NSF will be missed. The PLL system will insert the missing pulse. The resulting signal is the S_NSF which can be used as a time out for reading the subcode from the decoder shown in Fig.4. The S_NSF is available externally and the NSF flag can be read via the serial microcontroller interface. The F6 flag indicates at least one hold has occurred in the decoder's error corrector and interpolator. The shock processor uses this signal to evaluate whether a shock has occurred.

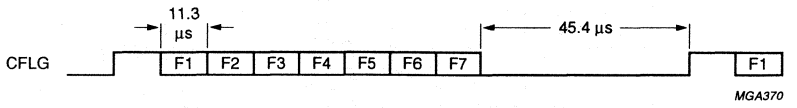


Fig.3 CFLG input timing diagram.

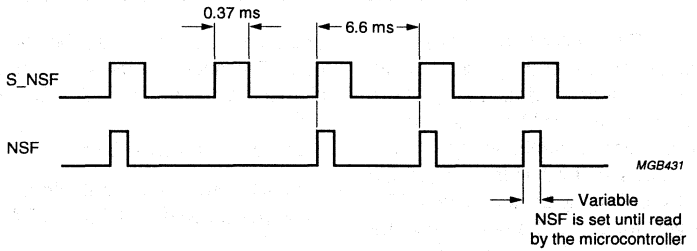


Fig.4 S_NSF output timing diagram; n = 2.

Shock processor

The shock processor determines whether a shock has occurred by processing all the shock detectors. The SAA7346 will enter shock mode and set SSD when the:

- µCsd flag is set by the microcontroller in the command register
- OTD input is active while the jmp_bz flag is not set
- RSB output is set while the e_rot_sd flag is set
- NSF pulse is lost and the full flag is not read by the microcontroller from the status register.

When the target position has been found the microcontroller should set the PFB flag in the command register. The SAA7346 will respond by clearing the SSD flag and start refilling. If CFLG still indicates a hold, the decoder is rolling out of its FIFO. RSB will be set which sets SSD again thus the FIFO will not start refilling. The microcontroller should jump one track back and look for the correct target position again. When the motor speed is stable and the decoder does not roll out of its FIFO, the audio data will be glued together.

SSD will be reset whenever the microcontroller sets PFB or the flush flags in the command register, or when the FIFO empties while the echo flag is LOW. Note if the microcontroller wants SSD to be clear for a while the shock detectors should be inhibited.

FIFO controller and monitor

The SAA7346 uses a state machine to control and monitor the conditions of the FIFO shown in Fig.5.

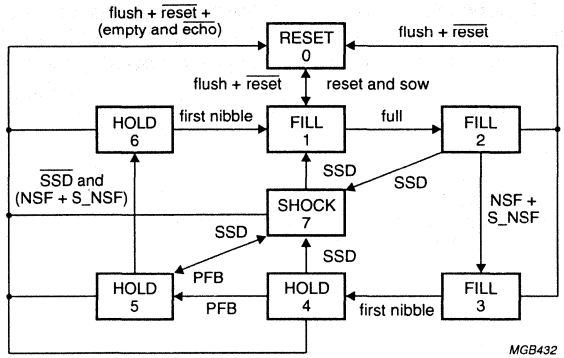


Fig.5 State machine flow diagram.

During normal operation the FIFO will fill up because writing is carried out twice as fast as reading; this is the fill mode. If the FIFO is full the monitor will detect and set the full flag. At the same time the fill flag will be reset thus preventing audio data from being written in to the FIFO. When the microcontroller reads the full flag from the status register, the servo control should jump back one track. The microcontroller enters a wait loop until the same absolute time subcode frame turns by again; this is the hold mode. When the spot is found again the microcontroller should set the PFB flag in the command register and the SAA7346 will resume writing to the DRAM. While in fill mode the write pointer address is saved at the end of each subcode frame. When the player exists hold mode it restores the saved address and continues writing after the last sample.

When a shock is detected the SAA7346 will enter shock mode. The shock mode will last until the PFB is set by the microcontroller or the FIFO is flushed, reset or runs empty.

Microcontroller interface

The SAA7346 has a 3-line microcontroller interface which is compatible with TDA1301, TDA1303 and SAA7345.

Writing data to the SAA7346

The SAA7346 command register is shown in Table 1. This can be written to via the microcontroller interface as shown in Fig.6. The command register flags functions are shown in Table 2.

Table 1 SAA7346 microcontroller interface registers.

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Command	flush	bypass	echo	jmp_bz	otd_p	e_rot_sd	µCsd	PFB
Status	Lm	Lm1	FRM_ER	NSF	full	empty	SSD	fill

Table 2 Command register flag functions.

COMMAND	DESCRIPTION
Flush	Flush, when set, will empty the FIFO, reset the read and write pointer addresses. Then writing will resume to the FIFO. Flag reset automatically.
Bypass	Bypass, when set, will power down the SAA7346. The I²S interface passes input to output directly. The parallel interface port controls $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{OE}$ which are pulled HIGH. KILL passes directly to $\overline{KILLOUT}$. When exiting by-pass mode the FIFO is automatically flushed.
Echo	Echo, when set, will cause the FIFO contents to be continuously played until the correct position is found again.
jmp_bz	Jump busy, when set, indicates a jump is being preformed. The OTD shock detector input will be disabled. After the jump has finished the flag should be reset by a write.
otd_p	OTD polarity enable. Enables the polarity of the OTD input to be switched from active HIGH set, active LOW not set.
e_rot_sd	Enable rotational shock detection, when set, will detect shocks whenever the decoder rolls out of its internal FIFO.
µCsd	Microcontroller shock detected is set when the microcontroller has detected a shock.
PFB	Position Found Back, when set, indicates that the microcontroller has found the absolute time frame after a shock or hold cycle. The audio data will sew together and the flag reset automatically.

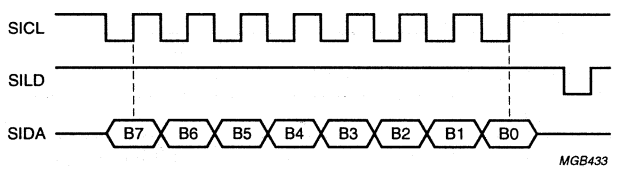


Fig.6 Microcontroller WRITE timing.

Writing operation sequence:

- SILD is held HIGH by the microcontroller.
- Microcontroller data is clocked into the internal command register on the LOW-to-HIGH clock transition of SICL.
- SILD is pulled LOW by the microcontroller to latch-in data to the command register.
- SICL and SILD are pulled HIGH by the microcontroller to indicate that communications have finished.

READING STATUS OF SAA7346

The SAA7346 has a status register shown in Table 1. This can be read via the microcontroller interface shown in Fig.7. The internal status signals are made available on the SIDA pin and are shown in Table 3.

Table 3 Internal status signals.

STATUS	DESCRIPTION
Lm and Lm1	The two Most Significant Bits (MSB) of the FIFO. These can be used to display the FIFO length or correct the subcode time information. The FIFO length is shown in Table 4.
FRM_ER	Framing error flag is set when: 1. The microcontroller did not accept the previous subcode flag on time. When this occurs the NSF flag will be set together with FRM_ER. 2. The S_NSF generated signal does not coincide with the NSF signal generated by the decoder. When this occurs there has been a FIFO overflow in the decoder or a jump. Framing error flag is reset when status register is read.
NSF	New subcode frame is set when an absolute sync is recovered from the CFLG input. Reset when status register is read. If the NSF is still set at the next occurrence of a subcode frame, FRM_ER will be set indicating that the microcontroller has lost a frame.
Full	Full is set when the FIFO is full. When the flag is set the microcontroller must jump back to the previous track. Reset when status register is read.
Empty	Empty is set when the FIFO is emptied during hold or shock modes. DRAM writing should resume immediately unless echo is set in the command register. If set, writing can only resume when PFB or flush are set in the command register. The latter will cause a discontinuity in music. Note when set there is a complete word left in the FIFO giving the SAA7346 controller time to switch to fill mode.
SSD	Set shock detect is set when SAA7346 detects a shock.
Fill	Fill is set when writing data to the DRAM or by setting the command register flags PFB or flush. Reset internally when full or SSD are set.

Table 4 FIFO length as a function of CONFIG, Lm and Lm1.

CONFIG	Lm	Lm1	FIFO LENGTH (s)
0	0	0	0.00 to 0.19
0	0	1	0.19 to 0.39
0	1	0	0.39 to 0.58
0	1	1	0.58 to 0.78
1	0	0	0.00 to 0.75
1	0	1	0.75 to 1.50
1	1	0	1.50 to 2.25
1	1	1	2.25 to 2.97

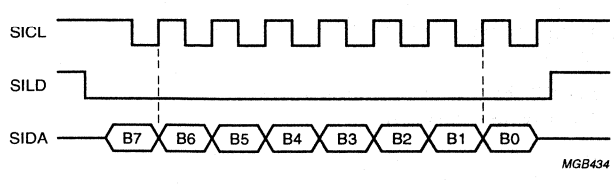


Fig.7 Microcontroller READ timing.

Read operation sequence:

- SILD is held LOW by the microcontroller.
- Status information is clocked from the internal status register on the LOW-to-HIGH clock transition of SICL.
- SICL and SILD are pulled HIGH by the microcontroller to indicate that communications have finished.

DRAM interface

The SAA7346 may be connected to all standard 80 ns, 1M × 4 bit or 256K × 4 bit fast page mode DRAMs. The best performance can be expected with the 4 Mbit DRAM. The CONFIG input selects the DRAM configuration either HIGH 4 Mbit or LOW 1 Mbit format. The SAA7346 converts audio data from serial to parallel and stores it as 4 bits. The addresses for read or write actions are calculated by separate read and write pointers which are multiplexed onto a 4 bits address bus. The control signal outputs associated with the parallel inputs/outputs are shown in Table 5.

Table 5 Command register flag functions.

COMMAND	DESCRIPTION
$\overline{WE}$	indicates write enable action
$\overline{RAS}$	row address strobe
$\overline{CAS}$	column address strobe
$\overline{OE}$	output buffer enable for external memory during cycle.

When the SAA7346 leaves bypass mode where all parallel Port control lines are pulled HIGH, the device initiates a DRAM power-up routine in accordance with the JEDEC standard.

System clock

The system clock input, CLKIN, recommended input signal is 16.9344 MHz. The accuracy of this clock influences the accuracy of the I^2S output, therefore the performance of the DAC and hence audio quality. The system clock is divided by 384 to derive the I^2S output word clock, WCO divided by 8 to derive the I^2S output bit clock, SCLO. Therefore whatever clock jitter the user introduces on the CLKIN signal will be reflected in the WCO and SCLO outputs.

Reset

Reset should be applied for four system clock cycles. Reset will:

- Clear SSD
- Clear the command register but leave the bypass flag set.

After a reset has been applied the SAA7346 will start-up in bypass mode.

Kill interface

The kill interface can be used to deactivate the DAC. The kill input is passed directly to the $\overline{KILLOUT}$ output when the bypass flag in the command register is set. When the flag is not set $\overline{KILLOUT}$ is generated by the SAA7346. It is LOW after leaving bypass mode, a reset or a FIFO flush. It will be LOW until the first error free word is read from the FIFO. The kill input has no effect or function when the bypass flag is not set.

Read cycle divide (RCD2)

The RCD2 input enables the modes of operation shown in Table 6. When RCD2 is HIGH the DRAM-read requests are halved allowing I^2S output speeds to vary. The factor n is called the over-speed factor.

Table 6 SAA7346 I²S output speeds.

RCD2	I²S INPUT SPEED	I²S OUTPUT SPEED	APPLICATION
LOW	CAV(1)	n = 1	CAV CDROM player with standard audio speed
LOW(2)	n = 1	n = 1	delay line feature
LOW	n = 2	n = 1	shock proof CD player
LOW	n = 4	n = 1	high data rate CDROM/CDI player with standard audio speed
HIGH	n = 2	n = ½	musicians feature
HIGH	n = 4	n = ½	musicians feature

Notes

1. CAV with n = 4 speed at outer edge of disc; n = 1.5 at inner edge of disc.
2. To build-up a delay, RCD2 should be made HIGH temporarily for twice the delay time.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	0	6.5	V
P_{max}	maximum power dissipation	–	500	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−40	+85	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	80	K/W

CHARACTERISTICS

V_{DD} = 3.3 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		3.3	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5.0 V	–	12	–	mA
I_{DDb}	bypass supply current	V_{DD} = 5.0 V; bypass mode	–	4	–	mA
I_{DDq}	quiescent supply current		–	–	100	µA
Digital inputs						
INPUTS: WCI, SDI, CLKIN, OTD AND RCD2; NORMAL CMOS						
V_{IL}	LOW level input voltage		−0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 V to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INPUT CLKIN						
f_{clk}	system clock frequency		–	16.9344	–	MHz
t_H	system clock HIGH time		35	–	65	ns
t_r	system clock rise time	0.8 V to (V_{DD} – 0.8 V)	–	–	20	ns
t_f	system clock fall time	(V_{DD} – 0.8 V) to 0.8 V	–	–	20	ns
INPUTS: CFLG, KILL, CONFIG AND SILD; WITH PULL-UP						
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
R_{PU}	input pull-up resistance	V_I = 0 V	–	50	–	kΩ
C_I	input capacitance		–	–	10	pF
INPUT TMS; WITH PULL-DOWN						
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
R_{PD}	input pull-down resistance	$V_I = V_{DD}$	–	50	–	kΩ
C_I	input capacitance		–	–	10	pF
INPUTS: $\overline{\text{RESET}}$, SCLI AND SICL; SCHMITT-TRIGGER						
V_{thr}	switching threshold voltage rising		–	–	$0.8V_{DD}$	V
V_{thf}	switching threshold voltage falling		$0.2V_{DD}$	–	–	V
V_{hys}	hysteresis voltage		–	$0.33V_{DD}$	–	V
C_I	input capacitance		–	–	10	pF
INPUT $\overline{\text{RESET}}$						
t_{RW}	RESET pulse width; active LOW		236	–	–	ns
Digital outputs						
OUTPUTS: FILL, S_NSF, RSB AND SSD; PUSH-PULL						
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OL} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.8 V to (V_{DD} – 0.8 V); C_L = 50 pF	–	–	15	ns
t_f	output fall time	(V_{DD} – 0.8 V) to 0.8 V; C_L = 50 pF	–	–	15	ns
OUTPUTS: SDO, SCLO, WCO, $\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, A0 TO A9; SLEW RATE PUSH-PULL						
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OL} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.8 V to (V_{DD} – 0.8 V); C_L = 50 pF	–	–	20	ns
t_f	output fall time	(V_{DD} – 0.8 V) to 0.8 V; C_L = 50 pF	–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OUTPUT $\overline{\text{KILLOUT}}$; OPEN DRAIN						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.4	V
I_O	output current		–	–	2	mA
C_L	load capacitance		–	–	50	pF
t_f	output fall time	(V_{DD} – 0.8 V) to 0.8 V; C_L = 50 pF	–	–	30	ns
INPUTS/OUTPUTS: D0 TO D3; NORMAL CMOS WITH SLEW RATE CONTROLLED PUSH-PULL						
V_{IL}	LOW level input voltage		–0.3	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 V to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OL} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.8 V to (V_{DD} – 0.8 V); C_L = 50 pF	–	–	20	ns
t_f	output fall time	(V_{DD} – 0.8 V) to 0.8 V; C_L = 50 pF	–	–	20	ns
INPUT/OUTPUT SIDA; NORMAL CMOS WITH PUSH-PULL						
V_{IL}	LOW level input voltage		–0.3	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 V to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OL} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.8 V to (V_{DD} – 0.8 V); C_L = 50 pF	–	–	15	ns
t_f	output fall time	(V_{DD} – 0.8 V) to 0.8 V; C_L = 50 pF	–	–	15	ns
I^2S timing						
RECEIVER (SEE FIG.9)						
Clock input SCLI						
T_{cy}	clock cycle time		118.1[1]	236.2[2]	472.4[3]	ns
t_H	clock HIGH time		41.3[1]	–	–	ns
t_L	clock LOW time		41.3[1]	–	–	ns
Inputs: SDI and WCI						
t_{su}	set-up time		23.6	–	–	ns
t_h	hold time		10	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TRANSMITTER (SEE FIG.8)						
Clock output SCLO						
T_{cy}	clock cycle time		–	472.4[3]	944.8[4]	ns
t_H	clock HIGH time		165.3	–	–	ns
t_L	clock LOW time		165.3	–	–	ns
Outputs: SDO and WCO						
t_d	delay time		–	–	377	ns
t_h	hold time		40	–	–	ns
Microcontroller interface timing (see Figs 12 and 13)						
INPUTS: SICL AND SILD						
t_H	input HIGH time		180	–	–	ns
t_L	input LOW time		180	–	–	ns
t_r	rise time	0.8 V to (V_{DD} – 0.8 V)	–	–	240	ns
t_f	fall time	(V_{DD} – 0.8 V) to 0.8 V	–	–	240	ns
Read mode (see Fig.12)						
t_d	delay time SILD to SIDA valid		120	–	–	ns
t_{pd}	propagation delay time SICL to SIDA		–	–	110	ns
Write mode (see Fig.13)						
t_{su1}	set-up time SIDA to SICL		40	–	–	ns
t_h	hold time SICL to SIDA		–	–	180	ns
t_{su2}	set-up time SICL to SILD		180	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DRAM interface timing (see Figs 14 and 15)						
T_{cy}	read or write cycle time		160	–	–	ns
t_{CAC}	access time from $\overline{CAS}$		–	–	20	ns
t_{OAC}	access time from $\overline{OE}$		–	–	20	ns
t_{h3}	$\overline{OE}$ to data input hold time		0	–	–	ns
t_{RH}	$\overline{RAS}$ HIGH time		70	–	–	ns
t_{RL}	$\overline{RAS}$ LOW time		80	–	10000	ns
t_{h1}	$\overline{RAS}$ hold time		20	–	–	ns
t_{h2}	$\overline{RAS}$ hold time to $\overline{OE}$ LOW		20	–	–	ns
t_{CL}	$\overline{CAS}$ LOW time		20	–	10000	ns
t_{h4}	$\overline{CAS}$ hold time		80	–	–	ns
t_{CRd}	delay time from $\overline{CAS}$ HIGH to $\overline{RAS}$		10	–	–	ns
t_{RCd}	delay time from $\overline{RAS}$ to $\overline{CAS}$		25	–	–	ns
t_{Rd}	$\overline{RAS}$ to column address delay time		20	–	–	ns
t_{su1}	row address set-up time		0	–	–	ns
t_{RAh}	row address hold time		15	–	–	ns
t_{su2}	column address set-up time		0	–	–	ns
t_{CAh}	column address hold time		20	–	–	ns
t_{Rh}	column address hold time from $\overline{RAS}$ LOW		60	–	–	ns
t_{l}	column address to $\overline{RAS}$ lead time		40	–	–	ns
t_{RCh}	read command hold time		0	–	–	ns
t_{RRh}	read command hold time to $\overline{RAS}$		12	–	–	ns
t_{Wsu}	write command set-up time		0	–	–	ns
t_{Wh1}	write command hold time		15	–	–	ns
t_{WL}	write command LOW time		15	–	–	ns
t_{Wh2}	write command hold time from $\overline{RAS}$		60	–	–	ns
t_{WCl}	write command to $\overline{CAS}$ lead time		20	–	–	ns
t_{WRl}	write command to $\overline{RAS}$ lead time		20	–	–	ns
t_{Dsu}	data output set-up time		0	–	–	ns
t_{Dh}	data output hold time		15	–	–	ns
t_{DRh}	data output hold time from $\overline{RAS}$		60	–	–	ns

Notes

1. n = 4.
2. n = 2.
3. n = 1.
4. n = ½.

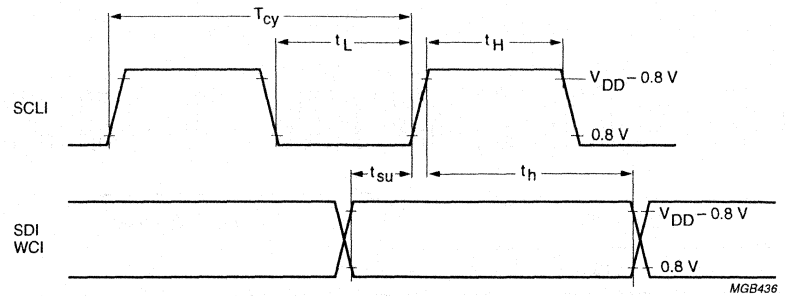


Fig.8 I²S input timing.

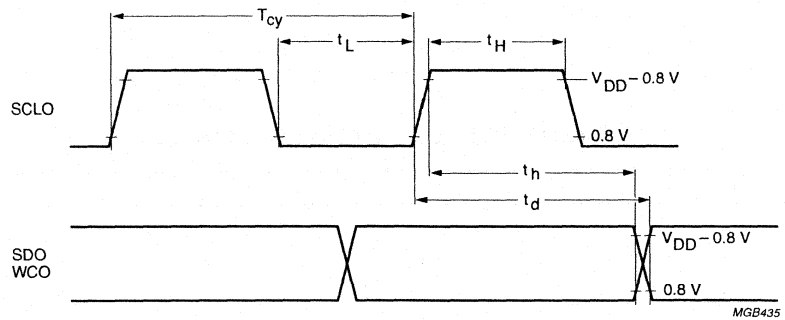


Fig.9 I²S output timing.

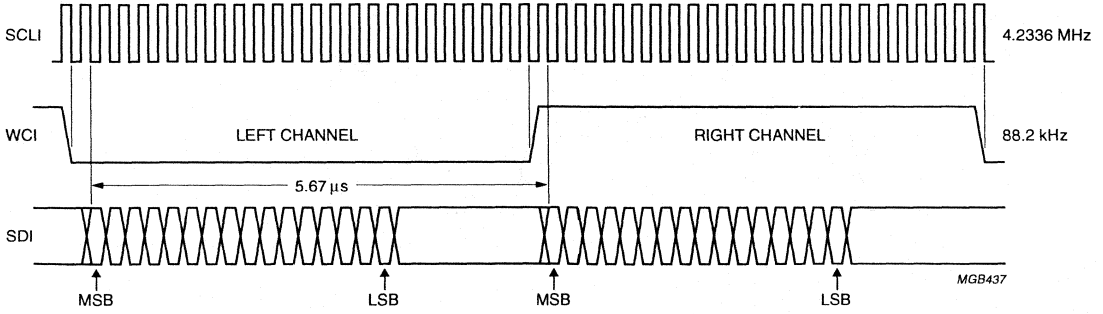


Fig.10 Typical I²S data input waveform; f = 4.2 MHz; n = 2.

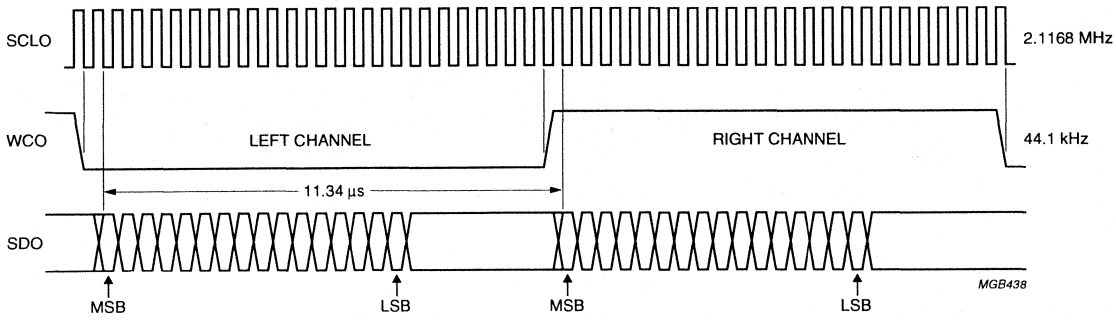


Fig.11 Typical I²S data output waveform; f = 2.1 MHz; n = 1.

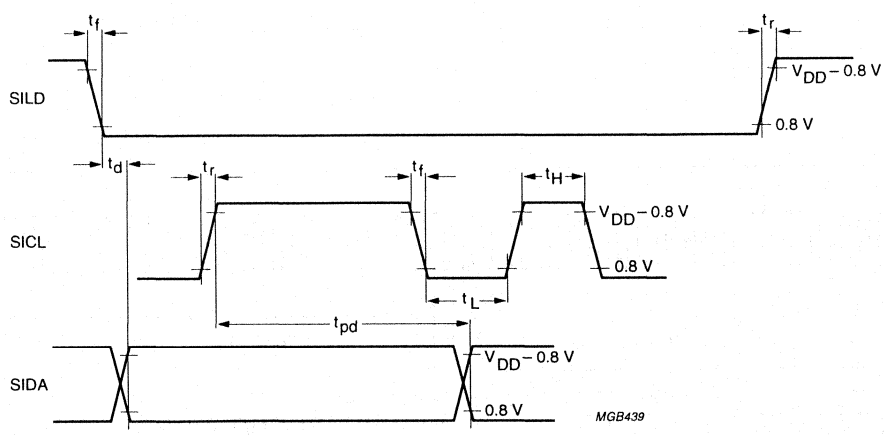


Fig.12 Microcontroller timing; READ mode.

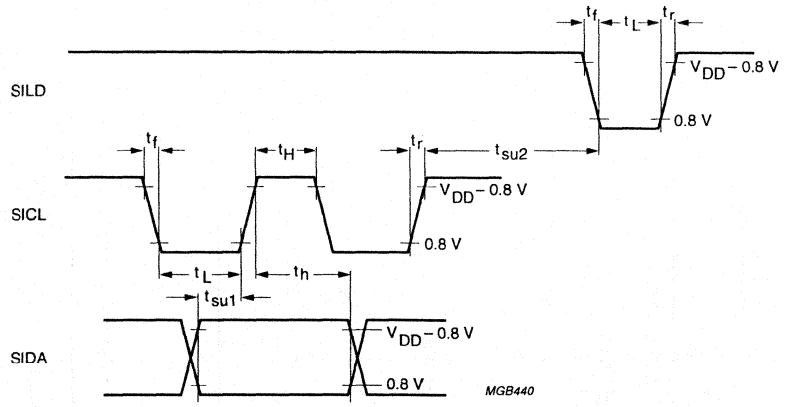


Fig.13 Microcontroller timing; WRITE mode.

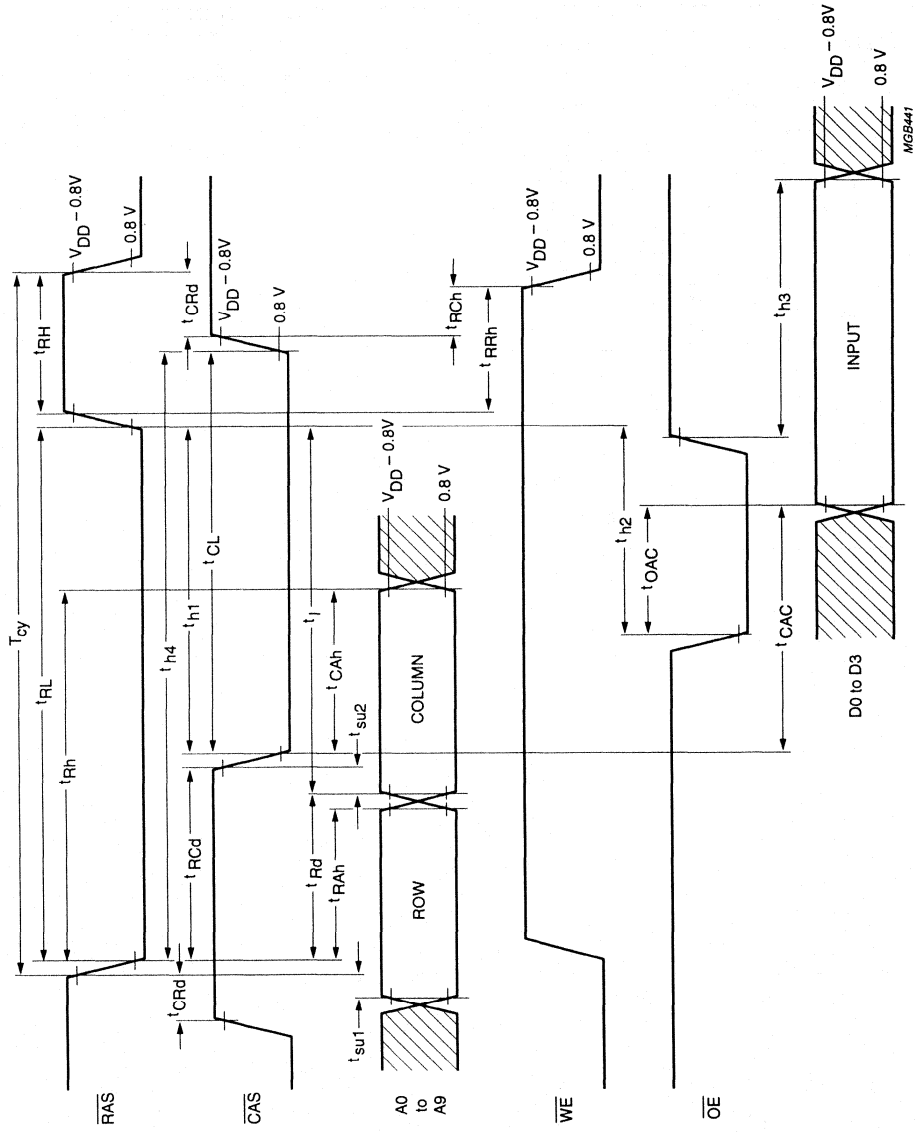


Fig.14 READ cycle timing.

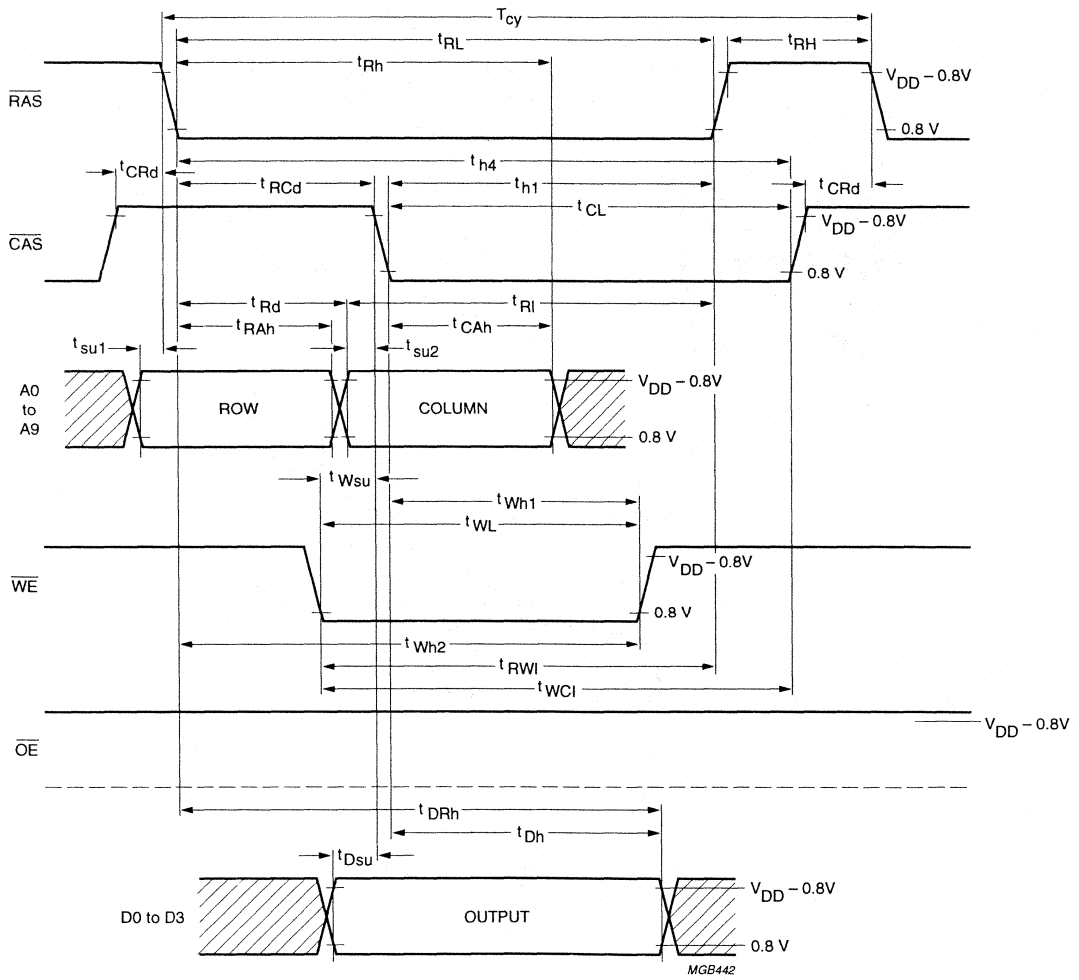


Fig.15 WRITE cycle timing.

APPLICATION INFORMATION

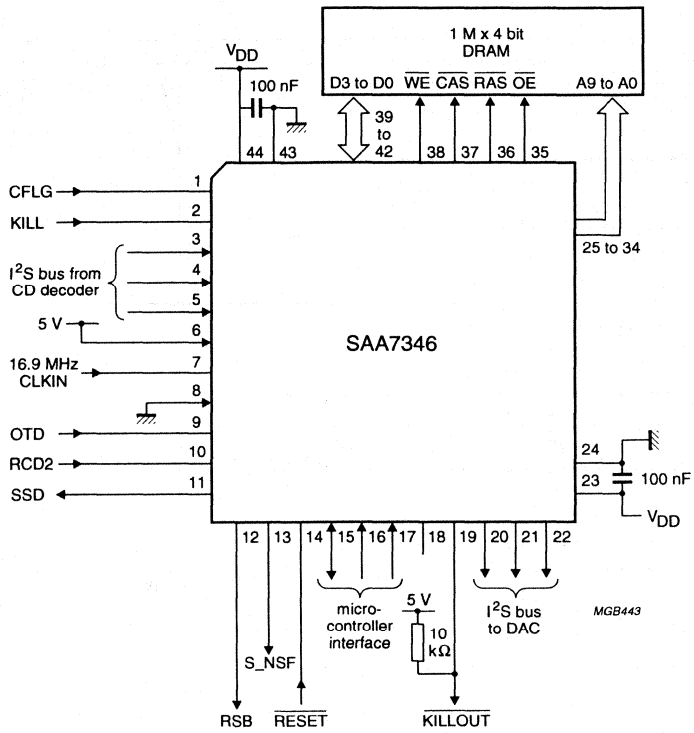
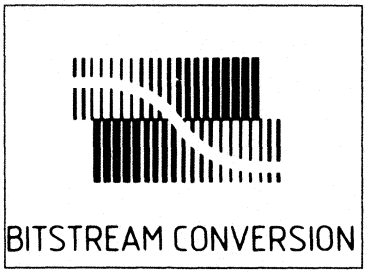


Fig.16 SAA7346 application diagram.

20-bit input bitstream conversion DAC for digital audio systems

SAA7350



FEATURES

- Up to 20-bit input
- Variety of interface formats (Japanese and I²S)
- Choice of two system clock frequencies
- Sampling frequency from 16 kHz to 53 kHz
- Third order noise shaping to increase signal-to-noise ratio
- Bitstream conversion, using switched capacitor one-bit DAC
- Differential mode output configuration
- Single power supply operation (+5 V)
- −10 to +70 °C operating temperature range
- Output interface for TDA1547

GENERAL DESCRIPTION

The SAA7350 is a CMOS digital-to-analog converter using Philips bitstream conversion technique. The device is designed for mid/high performance digital audio systems (particularly compact disc). The device also can be used with the TDA1547 device for top performance digital audio systems.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range	4.5	5.0	5.5	V
f_{XTAL}	crystal frequency (256 f_s)	-	11.2896	-	MHz
f_{XTAL}	crystal frequency (384 f_s)	-	16.9344	-	MHz
DR	dynamic range	93	98	-	dB
THD	total harmonic distortion	-	−96	−93	dB
	digital silence	-	−103	−100	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7350GP	44	QPF	plastic	SOT205AG

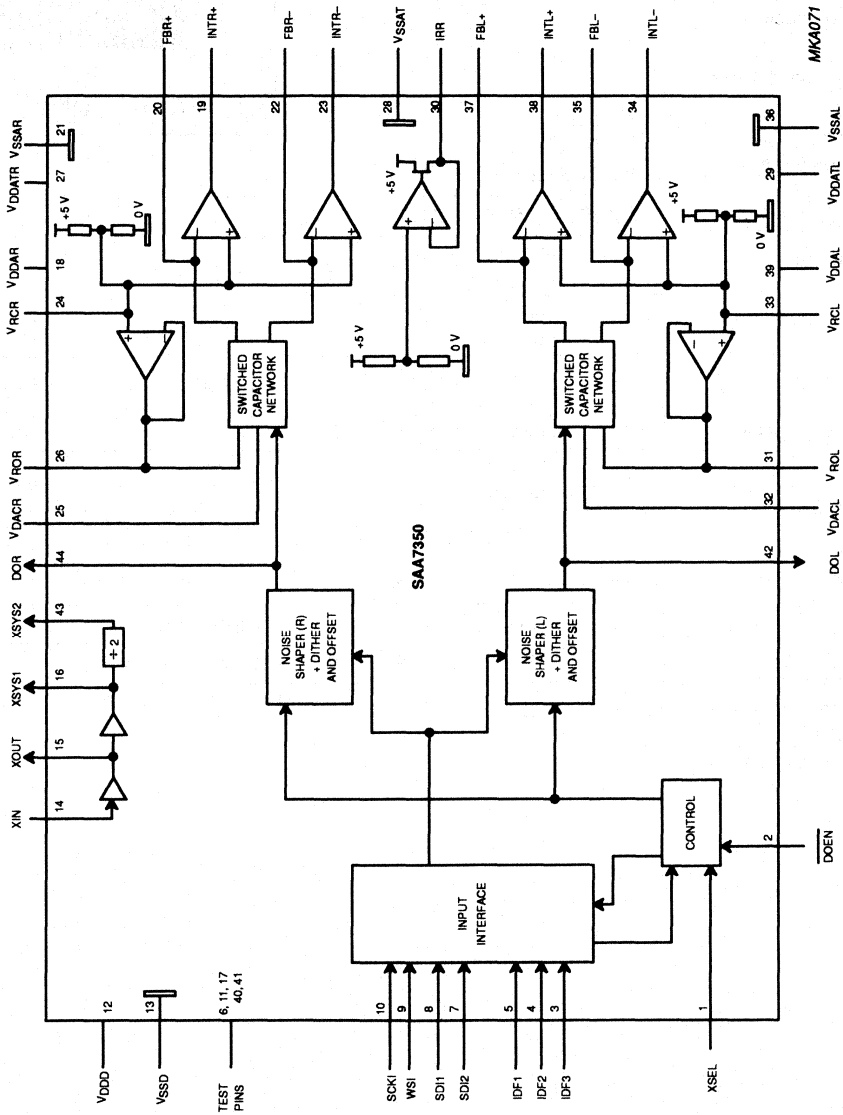


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
XSEL	1	crystal frequency select; this pin is used to select the master crystal frequency as follows: XSEL HIGH = 384 f_s, XSEL LOW = 256 f_s; if unconnected the pin will default HIGH
$\overline{DOEN}$	2	one-bit digital output enable; when LOW, the one-bit code outputs are made available for TDA1547; if unconnected the pin will default HIGH
IDF3, IDF2, IDF1	3, 4, 5	input data format; these three pins determine the input format the device is to operate in (see functional description); if unconnected these pins will default HIGH (i.e. burst clock mode)
TEST4	6	test 4; this pin should be left open-circuit
SDI2	7	serial data input; used in simultaneous mode only (for the right channel signal); when not used, this pin will be internally pulled HIGH
SDI1	8	serial data input; this should be a 16, 18 or 20-bit linear 2's complement PCM signal; in simultaneous mode this pin is used for the left channel signal
WSI	9	serial input word select signal; signifies whether data word is for the left or right channel; can be either f_s, 2 f_s, 4 f_s or 8 f_s where f_s is the system sampling frequency; f_s can be between 16 kHz and 53 kHz
SCKI	10	bit clock input for the serial input interface
TEST1	11	test 1; this pin should be left open-circuit
V_{DDD}	12	+5 V power supply for the digital section
V_{SSD}	13	ground connection for the digital section
XIN	14	crystal oscillator input
XOUT	15	crystal oscillator output
XSYS1	16	buffered oscillator output
TEST5	17	test 5; in normal operation this pin should be tied LOW
V_{DDAR}	18	analog 5 V supply for right channel
INTR+	19	output from the right positive switched-capacitor integrator; input to differential operational amplifier
FBR+	20	feedback connection for the right positive switched-capacitor integrator
V_{SSAR}	21	0 V supply for right channel
FBR-	22	feedback connection for the right negative switched-capacitor integrator
INTR-	23	output from the right negative switched-capacitor integrator; input to differential operational amplifier
V_{RCR}	24	high impedance voltage reference for right channel inputs; typically $V_{DDAR}/2$
V_{DACR}	25	reference voltage supply for right channel DAC's; normally this will beconnected to V_{SS}
V_{ROR}	26	right channel voltage reference output; typically $V_{DDAR}/2$
V_{DDATR}	27	5 V supply for right channel analog timing
V_{SSAT}	28	0 V supply for left and right channel analog timing
V_{DDATL}	29	5 V supply for left channel analog timing
IRR	30	24 kΩ bias resistor connection for the reference current generator circuit

PINNING

SYMBOL	PIN	DESCRIPTION
V_{ROL}	31	left channel voltage reference output; typically $V_{DDAL}/2$
V_{DACL}	32	reference voltage supply for left channel DAC; normally this will be connected to V_{SS}
V_{RCL}	33	high impedance voltage reference for left channel inputs and for bias current generator; typically $V_{DDAL}/2$
INTL-	34	output from the left negative switched-capacitor integrator; input to differential operational-amplifier
FBL-	35	feedback connection for the left negative switched-capacitor integrator
V_{SSAL}	36	0 V supply for left channel
FBL+	37	feedback connection for the left positive switched-capacitor integrator
INTL+	38	output from the left positive switched-capacitor integrator; input to differential operational-amplifier
V_{DDAL}	39	analog 5 V supply for left channel
TEST2	40	test 2; this pin should be left open-circuit
TEST3	41	test 3; this pin should be left open-circuit
DOL	42	digital output left; left channel one-bit code for TDA1547; when disabled this pin will be driven LOW
XSYS2	43	output clock at a frequency of half the master clock frequency
DOR	44	digital output right; right channel one-bit code for TDA1547; when disabled this pin will be driven LOW

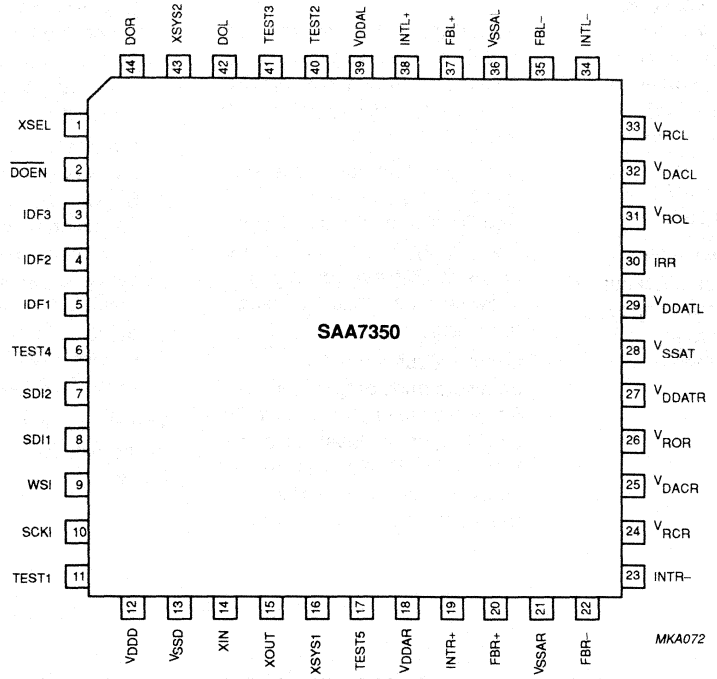


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

General

The SAA7350 bitstream conversion CMOS DAC contains a flexible interface supporting a variety of formats. This enables it to be used with a number of available digital filters with wordlengths of up to 20 bits and upsampling up to 8 f_s. The system sampling frequency (f_s) can be between 16 kHz and 53 kHz.

The analog section contains four one-bit DACs operated in differential mode to achieve high performance signal-to-noise ratio, channel separation and total harmonic distortion.

Input interface

The SAA7350 supports the following modes:

- I²S with dataword rates of f_s, 2 f_s or 4 f_s with wordlengths of up to 20 bits (see Fig. 3). A minimum of 16 bit-clock cycles per word is required.
- Sony serial format for dataword rate of f_s, 2 f_s or 4 f_s with wordlengths of 16, 18 or 20 bits (see Fig. 4). As this format idles on the MSB it is necessary to know how many bits are being transmitted.
- Simultaneous mode for dataword rates of f_s, 2 f_s, 4 f_s or 8 f_s with wordlengths of up to 20 bits idling on the least significant bit (see Fig. 5). A minimum of 16 bit-clock cycles per word is required.
- Simultaneous mode for dataword rates of f_s, 2 f_s, 4 f_s and 8 f_s with wordlengths of 18 or 20 bits idling on the MSB (see Fig. 6). As this format idles on the MSB it is necessary to know how many bits are being transmitted.
- Simultaneous mode for dataword rates of f_s, 2 f_s, 4 f_s or 8 f_s with wordlengths of up to 20 bits using burst clocks (see Fig. 7). A minimum of 16 bit-clock cycles is required. This mode is restricted to having the bit clock at less than or equal to half the master clock frequency supplied to the SAA7350.

The choice of these formats is given by the pins IDF1 to IDF3 as shown below.

Input data formats

IDF3	IDF2	IDF1	format
0	0	0	I²S format up to 20 bits
0	0	1	Sony serial format 16 bits
0	1	0	Sony serial format 18 bits
0	1	1	Sony serial format 20 bits
1	0	0	simultaneous format idling on LSB up to 20 bits
1	0	1	simultaneous format idling on MSB 18 bits
1	1	0	simultaneous format idling on MSB 20 bits
1	1	1	simultaneous format burst clock up to 20 bits

The transfer on the serial input has to be synchronous to the master clock.

Clock frequency

The device can run at an input clock frequency of either 384 f_s or 256 f_s (pin XSEL) outputting a system clock at the same frequency on XSYS1 and half input clock frequency on XSYS2. f_s can be between 16 kHz and 53 kHz.

Noise shaping

Third order noise shaping is implemented on the SAA7350 to give an improved signal-to-noise ratio. DC offset and out-of-band dither is added to prevent idle patterns in the audio band.

Bitstream conversion DAC

The digital-to-analogue conversion in the SAA7350 is performed using the Philips bitstream conversion technique. The input from the digital filter is oversampled to 8 f_s by means of a digital sample and hold and converted to a 1-bit pulse density modulated (PDM) signal. A switched capacitor technique is used for the bitstream conversion to convert the PDM signal to an analog signal. A fixed charge is either added or subtracted from the virtual earth node of an integrator . As this output is a continuous time output a highly symmetrical operational amplifier is used to give a low distortion figure.

In order to increase the output signal-to-noise ratio and THD performance, internal operational-amplifiers are provided so that the device is operated in differential mode. With this technique, any common mode signals cancel thus improving the signal-to-noise ratio and total harmonic distortion.

TDA1547 interface

The SAA7350 can also be used to provide oversampling and noise shaping for the TDA1547. One-bit codes and clock outputs are supplied for inputs to the TDA1547.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage; note 1	−0.5	+6.5	V
V_I	DC input voltage	−0.5	+6.5	V
I_{IK}	DC input diode current	-	±20	mA
V_O	DC output voltage	−0.5	+6.5	V
I_O	DC output source or sink current	-	±20	mA
I_{DD} or I_{SS}	DC V_{DD} or V_{SS} current (total)	-	±0.5	A
T_{stg}	storage temperature range	−65	+150	°C
T_{amb}	operating ambient temperature range	−10	+70	°C
V_{es}	electrostatic handling; note 2	−1000	+1000	V

Notes to the limiting values

1. All V_{DD} and V_{SS} pins must be connected externally to the same power supply unit.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; f_{XTAL} = 384 f_s; f_s = 44.1 kHz unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	supply voltage (analog)		4.5	5.0	5.5	V
I_{DDA}	supply current (analog)		-	45	70	mA
V_{DDD}	supply voltage (digital)		4.5	5.0	5.5	V
I_{DDD}	supply current (digital)		-	30	50	mA
Digital part:						
Inputs: SCKI, WSI, SDI1						
V_{IL}	LOW level input voltage	note 1	−0.5	-	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	-	V_{DD} + 0.5	V
I_{LI}	input leakage current	note 2	−10	0	+10	µA
C_I	input capacitance		-	-	10	pF
Inputs: XSEL, SD12, $\overline{\text{DOEN}}$, IDF1, IDF2, IDF3		note 3				
V_{IL}	LOW level input voltage	note 1	−0.5	-	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	-	V_{DD} + 0.5	V
Z_I	pull-up impedance		-	50	-	kΩ
C_I	input capacitance		-	-	10	pF
Crystal oscillator input: XIN						
V_{IL}	LOW level input voltage	note 1	−0.5	-	+1.5	V
V_{IH}	HIGH level input voltage	note 1	3.5	-	V_{DD} + 0.5	V
I_{LI}	input leakage current	note 2	−10	0	+10	µA
C_I	input capacitance		-	-	10	pF
Outputs: XSYS1						
V_{OL}	LOW level output voltage	note 1	−0.5	-	+0.4	V
V_{OH}	HIGH level output voltage	note 1	2.4	-	V_{DD} + 0.5	V
C_L	load capacitance		-	-	35	pF
Outputs: XSYS2, DOL, DOR						
V_{OL}	LOW level output voltage		-	-	0.5	V
V_{OH}	HIGH level output voltage		V_{DD} - 0.5	-	-	V
C_L	load capacitance		-	-	20	pF
Crystal oscillator: input XIN/output XOUT						
f_{XTAL}	operating frequency XTAL	note 4	4.096	256 f_s or 384 f_s	20.35	MHz
G_m	mutual conductance	100 kHz	1.5	-	-	mA/V
G_v	small signal voltage gain	$G_v = G_m \times R_o$	3.5	-	-	V/V
C_I	input capacitance		-	-	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal oscillator: input XIN/output XOUT						
C_{FB}	feedback capacitance		-	-	5	pF
C_O	output capacitance		-	-	10	pF
I_{LI}	input leakage current	note 2	−10	-	+10	μA
Timing						
External clock input: XIN						
f_c	input frequency		4.096	256 f_s or 384 f_s	20.35	MHz
t_r	input rise time	note 5	-	-	10	ns
t_f	input fall time	note 5	-	-	10	ns
t_{HIGH}	input HIGH time (relative to clock period)	at 1.5 V	30	-	70	%
System clock output: XSYS1		note 6				
t_r	output rise time	note 5	-	-	10	ns
t_f	output fall time	note 5	-	-	10	ns
t_{HIGH}	output HIGH time (relative to clock period)	note 7	-	50	-	%
Data outputs: DOL, DOR		see Fig.8; note 8				
t_r	data output rise time		-	10	15	ns
t_f	data output fall time		-	10	15	ns
t_{SU}	data output set-up time		0	-	-	ns
t_{HD}	data output hold time		25	-	-	ns
Data clock output: XSYS2		see Fig. 8; note 8				
t_r	clock output rise time		-	5	10	ns
t_f	clock output fall time		-	5	10	ns
t_{HIGH}	clock output HIGH time	note 9	40	-	-	ns
t_{LOW}	clock output LOW time	note 9	40	-	-	ns
Input timing		see Fig.9				
Clock input: SCKI						
f_{ci}	input clock frequency		0.256	-	20.35	MHz
msr	mark space ratio		40:60	-	60:40	
Word select input: WSI						
f_i	input frequency		14.4	-	424	kHz
Data inputs: SDI1, SDI2/word select input: WSI						
$t_{SU;DAT}$	input set-up time		-	20	-	ns
$t_{HD;DAT}$	input hold time (relative to SCKI)		0	-	-	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog part						
Reference voltage source: VRC						
V_{ref}	high-impedance reference voltage level		-	2.5	-	V
Outputs: INTL+, INTL-, INTR+, INTR-		notes 10 and 11				
$V_{AO(RMS)}$	output level at 0 dB (RMS value)	note 12	-	0.9	-	V
$V_{DIFF(RMS)}$	application output level at 0 dB (RMS value)	note 13	1.62	1.80	1.98	V
DAC performance		note 12				
DR	dynamic range		93	98	-	dB
THD + N	total harmonic distortion	at 0 dB/1 kHz	-	−96	−93	dB
	digital silence		-	−103	−100	dB
a	channel separation	1 kHz	-	100	-	dB
RR	power supply rejection ratio to V_{DD}		-	60	-	dB
	channel matching	note 14	-	-	±0.25	dB
le	linearity	0 to −100 dB	-	±1	-	dB

Notes to the characteristics

1. Minimum V_{IL}, V_{OL} and maximum V_{IH}, V_{OH} are peak values to allow for transients.
2. I_{LIMIN} and I_{LOMIN} measured at V_I = 0 V; I_{LIMAX} and I_{LOMAX} measured at $V_I = V_{DD}$.
3. Pins XSEL and SDI2 are internally pulled high when not connected. XSEL HIGH indicates a crystal frequency of 384 f_s.
4. f_XTAL is a multiple of the system sampling frequency f_s. f_s can be between 16 and 53 kHz.
5. Reference levels = 0.8 V and 2.0 V.
6. Output times are measured with a capacitve load of 35 pF. XSYS2 is half the master clock frequency. See Fig.10 for relative clock timings.
7. t_{HIGH} valid only when used with XTAL, with 50% input mark space ratio. XSYS1 t_{HIGH} is measured at $V_{DD}/2$.
8. Output times are measured with a capacitive load of 20 pF. XSYS2 is half the master clock frequency. Data output hold time is relative to XSYS2.
9. XSYS2 output HIGH/LOW times are for 20.35 MHz. Minimum value for 16.934 MHz is 49 ns.
10. Device measured in differential mode with external components shown in recommended application diagram (see Figs 13 and 14). It should be noted that for 1.80 mV output, feedback resistors R16a, R17a, R16b, R17b should be 31.6 kΩ. Application diagram shows preferred type range values of 30 kΩ which give 1.80 x 30/31.6 = 1.70 mV.
11. Maximum load (excluding feedback) is 10 kΩ, 100 pF to VRO (V_{ref}). Dynamic output impedance is typically 150 Ω.
12. Output level tracks linearly with sampling frequency (f_s). DAC performance quoted for 18-bit, 4 f_s input.
13. Application output level measured at output from first operational-amplifier stage in Figs 13 and 14.
14. With matched external components.

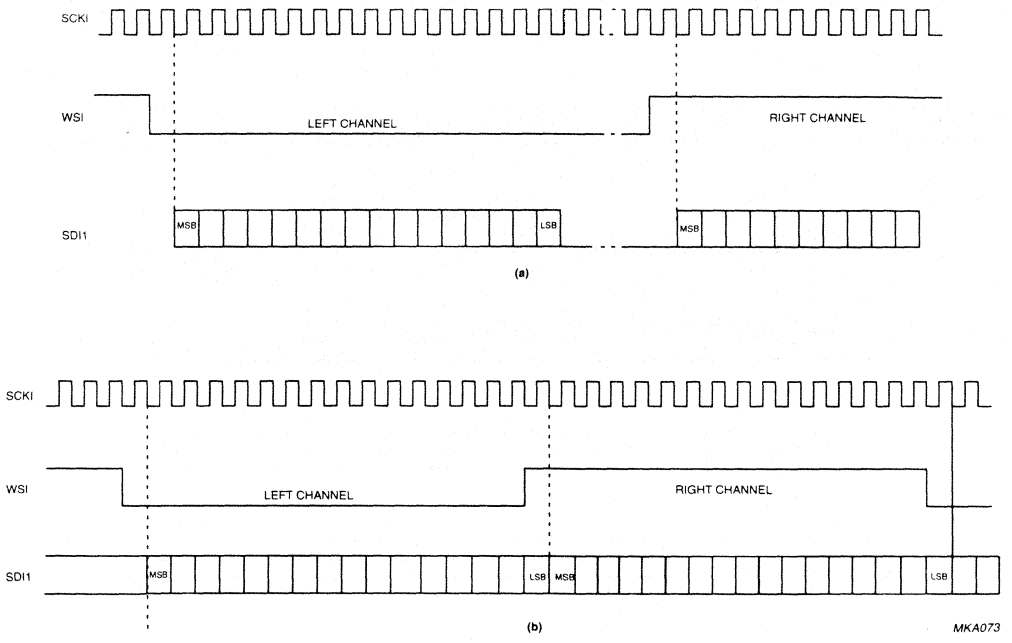


Fig.3 I²S 4 fs input formats.

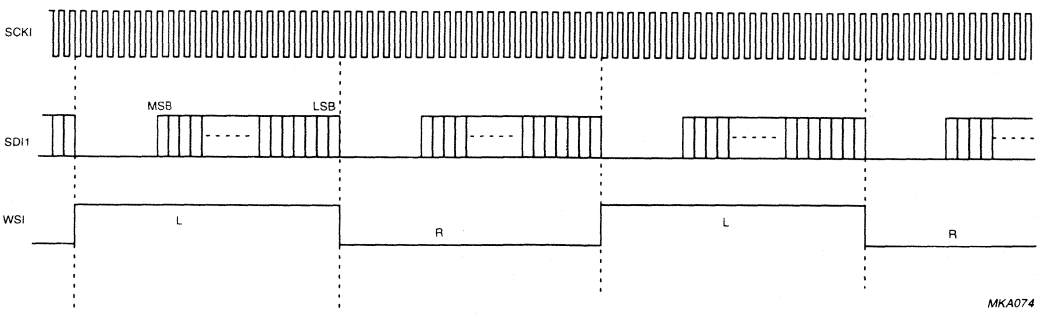


Fig.4 Sony serial input format.

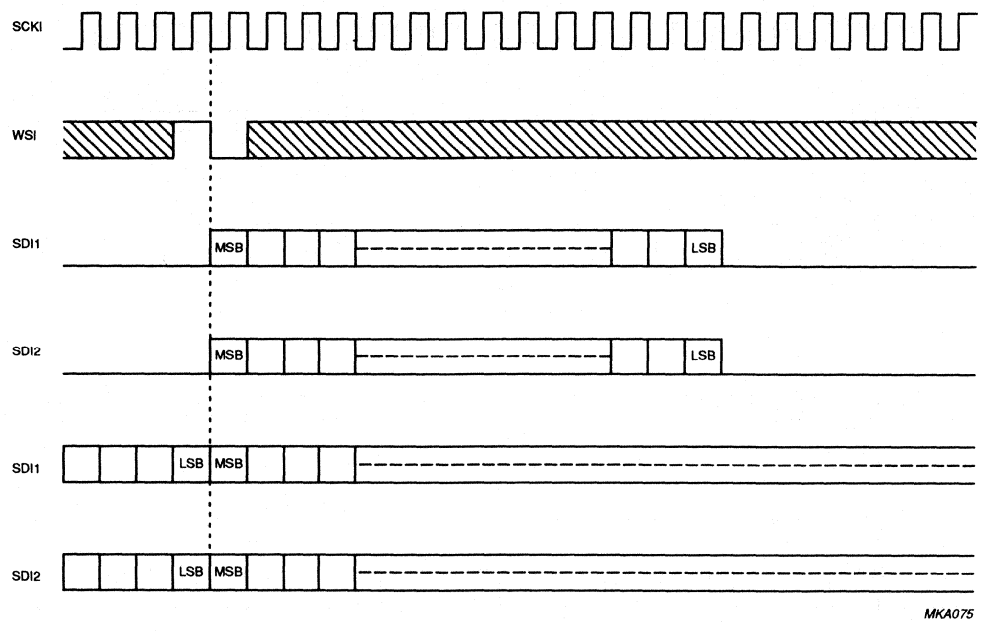


Fig.5 Simultaneous mode input format - continuous clock idling on LSB.

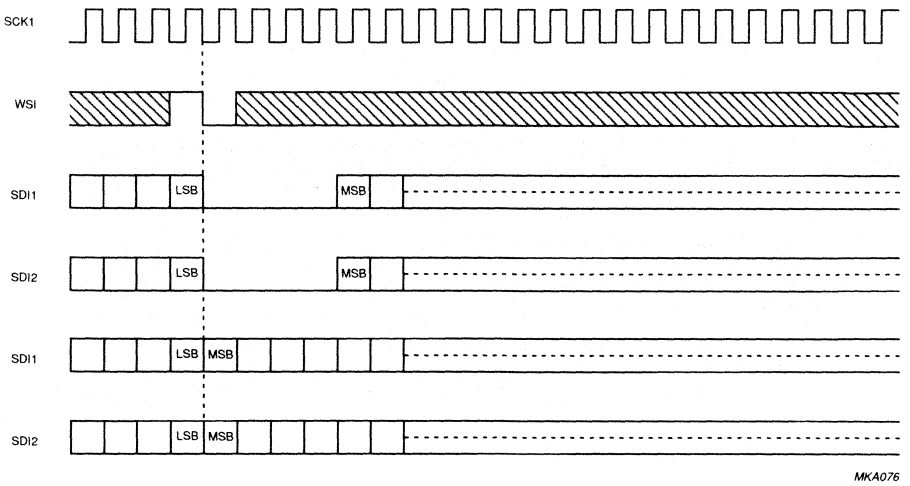


Fig.6 Simultaneous mode input format - continuous clock idling on MSB.

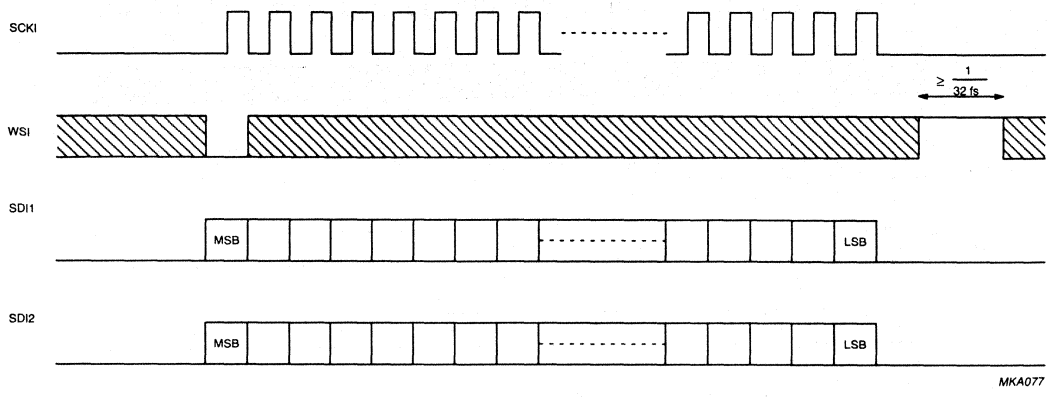


Fig.7 Simultaneous burst clock input format.

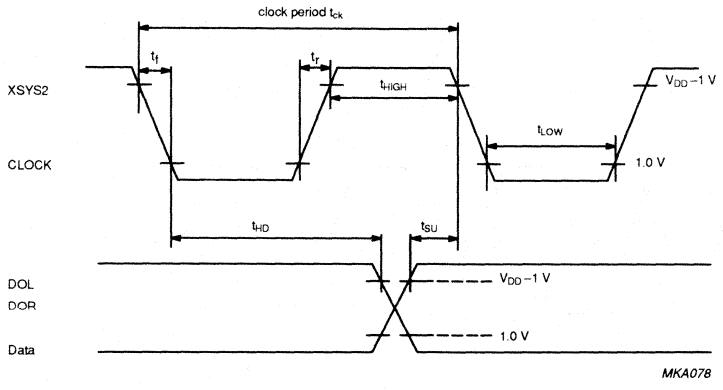


Fig.8 One bit code timing.

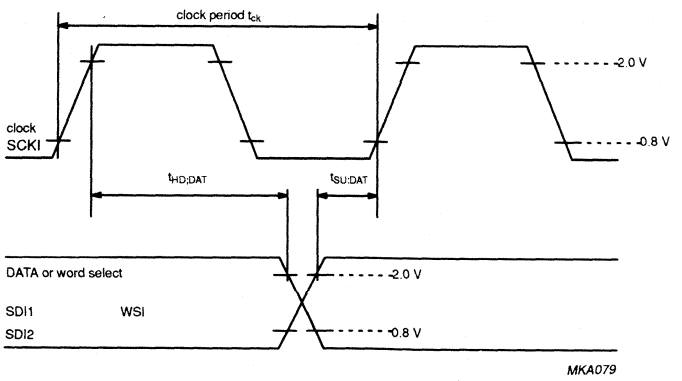


Fig.9 Input timing (valid for all input modes).

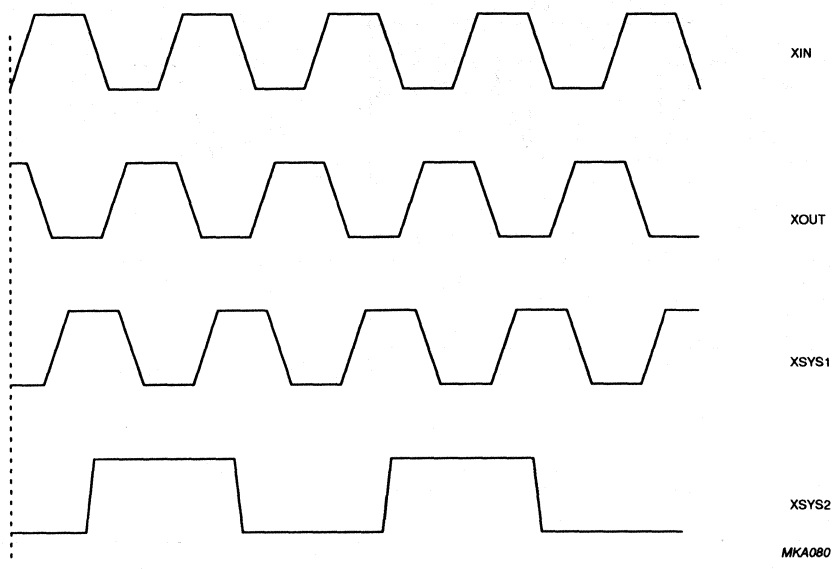


Fig.10 Relative clock timing.

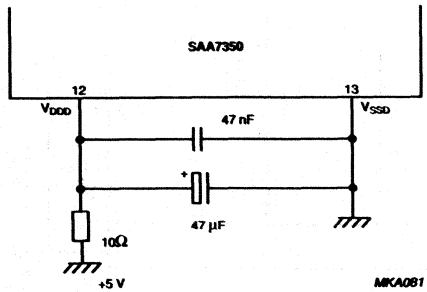


Fig.11 Digital voltage supply.

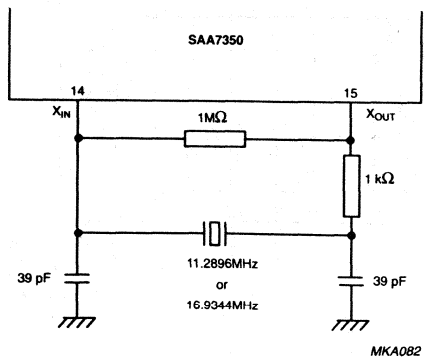


Fig.12 Crystal oscillator.

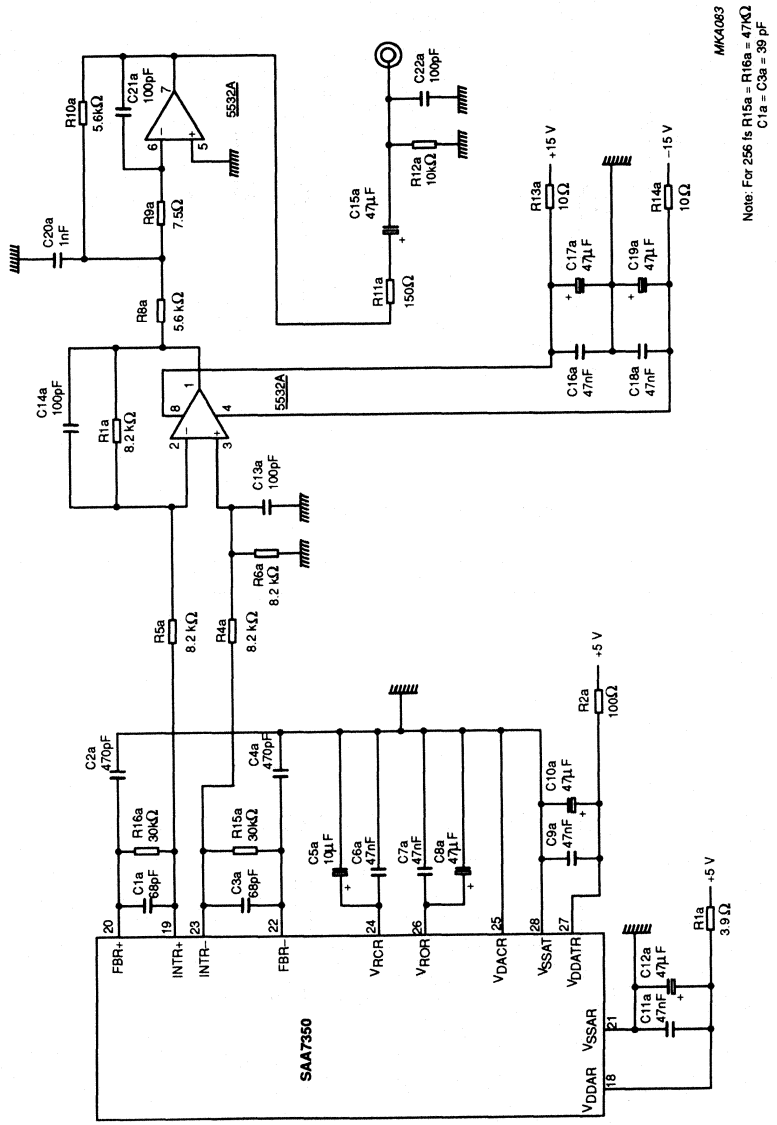


Fig.13 SAA7350 application circuit - analog section right channel (384 fs, 44.1 kHz).

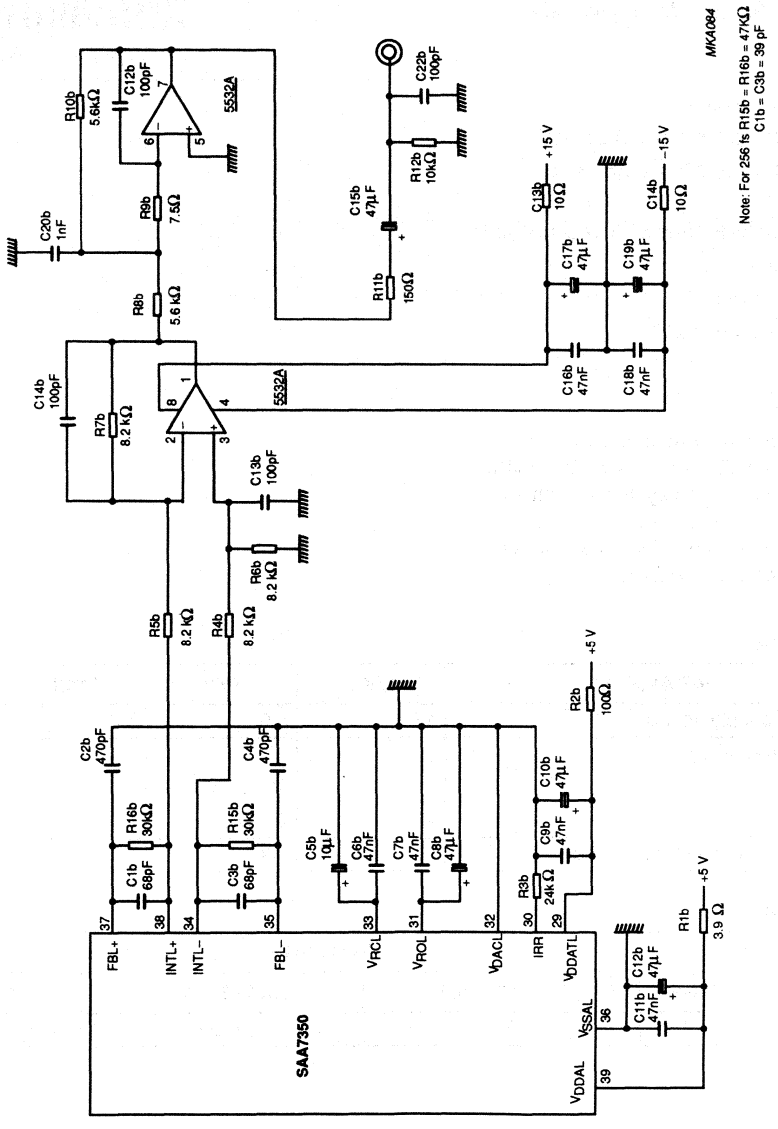
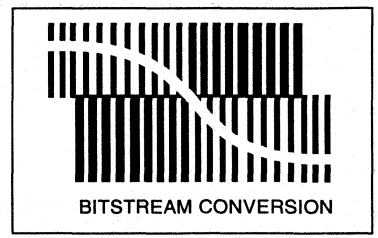


Fig.14 SAA7350 application circuit - analog section left channel (384 fs, 44.1 kHz).

Bitstream conversion ADC for digital audio systems

SAA7360



FEATURES

- Stereo input
- Single-ended input
- Uncommitted input buffer for filtering and pre-scaling
- Fully differential ADC using 3rd order Sigma-Delta modulation
- 128 times oversampling
- Four stage digital decimation filter
- Switchable high pass filter to remove DC offsets
- 16-bit or 18-bit selectable output in a multiple of formats
- Sampling rates between 18 kHz and 53 kHz supported
- Master or slave operation
- Choice of 2 crystal frequencies
- Single power supply operation (+5 V).

GENERAL DESCRIPTION

The SAA7360 is a CMOS analog-to-digital converter using Philips bitstream conversion technique. The device is designed for digital audio playback systems, such as digital amplifiers, CD-recordable and Digital Compact Cassette (DCC). The device is a complementary device to the SAA7350 bitstream conversion DAC.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5.0	5.5	V
f_{XTAL}	crystal frequency				
	$256f_s$	–	11.2896	–	MHz
	$512f_s$	–	22.5792	–	MHz
THD + N	total harmonic distortion + noise	–	–90	–85	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7360GP	44	QFP	plastic	SOT205A

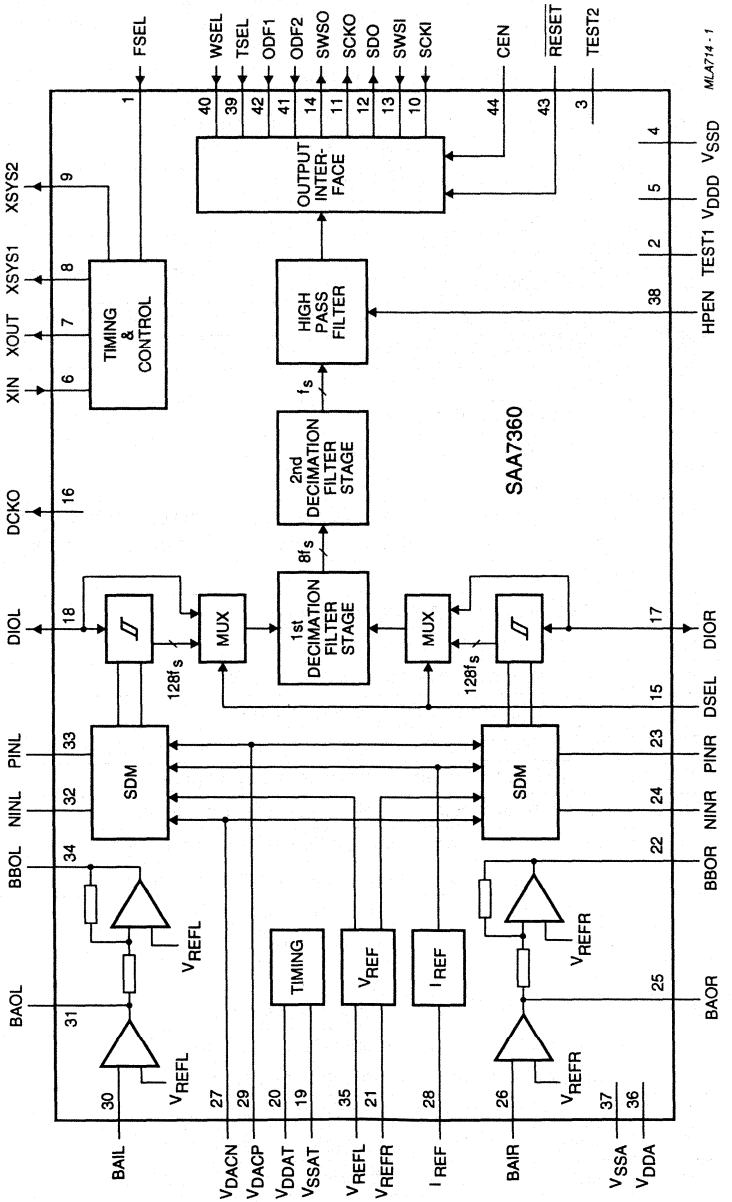


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FSEL	1	Crystal frequency select input. This pin is used to select the master crystal frequency as follows: FSEL HIGH = $256f_s$, FSEL LOW = $512f_s$. If unconnected the pin will default HIGH.
TEST1	2	Test input 1. This pin should be left open-circuit.
TEST2	3	Test input 2. This pin should be left open-circuit.
V_{SSD}	4	Ground supply for the digital section.
V_{DDD}	5	+5 V supply for the digital section.
XIN	6	Crystal oscillator input.
XOUT	7	Crystal oscillator output.
XSYS1	8	System clock output.
XSYS2	9	Output clock at a frequency half the system clock frequency.
SCKI	10	Serial interface clock input.
SCKO	11	Serial interface clock output.
SDO	12	Serial interface data output.
SWSI	13	Serial interface word select input.
SWSO	14	Serial interface word select output.
DSEL	15	Input for selecting between the internally generated 1-bit code (DSEL HIGH) or an externally generated 1-bit code (DSEL LOW). If unconnected this pin defaults HIGH.
DCKO	16	1-bit code clock output.
DIOR	17	1-bit code input/output (right channel).
DIOL	18	1-bit code input/output (left channel).
V_{SSAT}	19	Ground supply for the analog timing section.
V_{DDAT}	20	+5 V supply for the analog timing section.
V_{REFR}	21	+2.5 V reference generator for the right channel analog section.
BBOR	22	Output of right channel buffer operational amplifier "B".
PINR	23	Positive input to right channel Sigma-Delta modulator.
NINR	24	Negative input to right channel Sigma-Delta modulator.
BAOR	25	Output of right channel buffer operational amplifier "A".
BAIR	26	Input of right channel buffer operational amplifier "A".
V_{DACN}	27	Negative voltage reference level input for the DACs.
I_{REF}	28	Current reference output.
V_{DACP}	29	Positive voltage reference level input for the DACs.
BAIL	30	Input of left channel buffer operational amplifier "A".
BAOL	31	Output of left channel buffer operational amplifier "A".
NINL	32	Negative input to left channel Sigma-Delta modulator.
PINL	33	Positive input to left channel Sigma-Delta modulator.
BBOL	34	Output of left channel buffer operational amplifier "B".
V_{REFL}	35	+2.5 V reference generator for the left channel analog section.
V_{DDA}	36	+5 V supply for the analog section.

SYMBOL	PIN	DESCRIPTION
V_{SSA}	37	Ground supply for the analog section.
HPEN	38	High pass filter enable input. (HPEN HIGH = enabled). If unconnected this pin defaults HIGH.
TSEL	39	Input to select master (TSEL LOW) or slave (TSEL HIGH) operation of the serial interface. If unconnected this pin defaults HIGH.
WSEL	40	Input to indicate 16-bit (WSEL HIGH) or 18-bit (WSEL LOW) output data word length of the serial interface. If unconnected this pin defaults HIGH.
ODF2, ODF1	41, 42	Serial interface format inputs. These two pins determine the interface format in which the device will operate (see FUNCTIONAL DESCRIPTION). If unconnected these pins will default HIGH (I^2S format).
$\overline{RESET}$	43	Power-on reset input (active LOW) to mute the digital output during power on.
CEN	44	Chip enable input. This pin, when LOW, disables the operation of the device and 3-states the outputs of the serial interface bus. This enables the connection of one of more devices to the output bus. If unconnected this pin defaults HIGH.

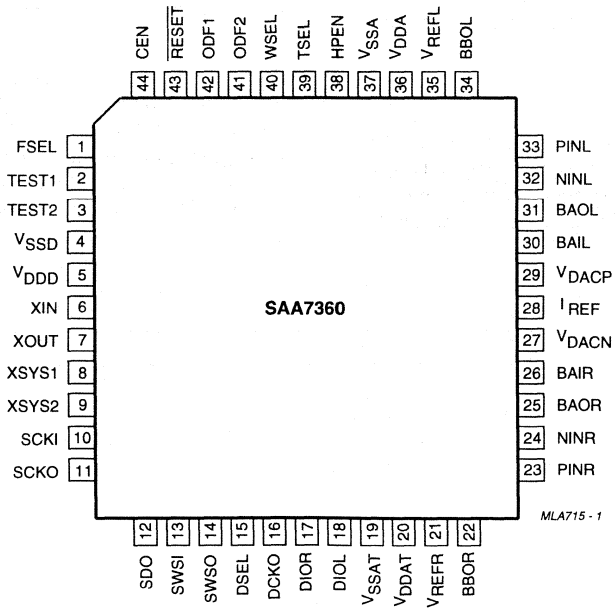


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The SAA7360 is a bitstream conversion CMOS ADC for digital audio systems. The device consists of a input buffer which can be configured by the user for pre-scaling and anti-aliasing, a third order Sigma- Delta modulator with a performance of better than 90 dB THD + Noise, and decimation filters with anti-aliasing suppression of greater than 93 dB and in band ripple of less than 0.0002 dB. The device outputs data in a number of formats compatible with a range of manufacturers.

Clock frequency

The SAA7360 can operate in either master or slave mode (CMOS input drive levels). The clock can be either $256f_s$ or $512f_s$ (where f_s is the sampling frequency) indicated via pin FSEL. System clock outputs equal to the input frequency (XSYS1) and half the input frequency (XSYS2) are provided to drive other ICs in the system. All performance parameters track with f_s which can vary between 18 kHz and 53 kHz without degradation of performance.

Input buffer

The input buffer stage consists of an uncommitted input operational amplifier ("A") and a committed unity gain operational amplifier ("B") to perform a single-to-double ended conversion for the differential ADC. The input buffer can be configured for pre-scaling and second order anti-aliasing filtering. The scaling should be performed so as to provide a maximum of 1 V RMS at the output of the operational amplifier.

Sigma-Delta modulator

The analog-to-digital conversion is performed by a third order Sigma-Delta modulator, which outputs a 1-bit code at $128f_s$ with a distortion plus noise figure of greater than 90 dB. The modulator is scaled so that a 0 dB input results in an output of –3 dB, at the 1-bit outputs.

Digital decimation filter

The left and right channel 1-bit codes from the ADC are decimated from $128f_s$ to $1f_s$ in four stages of filtering. The first filter stage decimates by a factor of $16f_s$ to $8f_s$ using a fourth order comb type filter. The other three filter stages consist of three cascaded half-band filters each decimating by a factor of two. The half-band filter decimating from $8f_s$ to $4f_s$ has a gain of +2 dB to compensate for the –3 dB through the analog part and allow a headroom of 1 dB to prevent clipping with DC offsets.

The overall response of the digital decimation filter is a pass band from $0f_s$ to $0.454f_s$ (20 kHz at f_s = 44.1 kHz f_s) with ripple less than 0.0002 dB and a transition band of $0.454f_s$ to $0.544f_s$. All frequencies between $0.544f_s$ and $64f_s$ which could result in aliasing into the base band are attenuated by greater than –93 dB.

Table 1 Output data formats.

ODF2	ODF1	MODE
0	0	test
0	1	format 1
1	0	format 2
1	1	I^2S

High-pass filter

The operational amplifiers in the Sigma-Delta modulator can cause a small DC offset to be present in the 1-bit code passed to the digital section. This can result in the possibility of clicks when switching between devices and the recording of DC offsets which can upset offsets introduced in filters and noise shaping DACs in the playback path. A switchable high-pass filter is included on the IC after the decimation filter stage to allow the user to remove these DC offsets (selectable via pin HPEN). The filter does not affect the decimation process. The filter is 1st order high pass with the following specification:

Corner frequency (–3 dB): 1.7 Hz
Ripple: none
At 20 Hz: –0.03 dB, 5 degree phase deviation
Above 100 Hz: < 0.00002 dB, < 1 degree
Noise floor: –116 dB

Output interface

The output interface can operate in master or slave mode selectable by pin TSEL. Master mode drives pins SWSO (word select), SCKO (bit clock) and SDO (data output). Slave mode receives the word clock on pin SWSI and the bit clock on pin SCKI. In slave mode the internal circuitry runs on the incoming bit clock and therefore cannot operate with burst clocks. Slave mode causes the pins SWSO and SCKO to be 3-stated allowing systems to connect SWSO and SCKO to pins SWSI and SCKI respectively for applications where the device has to operate in master and slave modes. The bit clock in master mode is at $32f_s$ for 16-bit output, and $64f_s$ for 18-bit output. In slave mode the bit clock is a minimum of $32f_s$ and a maximum of $64f_s$.

Three output formats are supported, IIS and two pseudo I^2S modes common in digital audio ADC systems. These formats are shown in Figure 3. Selection of the three formats is given in Table 1. 16-bit or 18-bit output words can be chosen (via pin WSEL).

Reset

When pin $\overline{\text{RESET}}$ is held LOW then the data outputs are set to zero. The $\overline{\text{RESET}}$ pin operates as a Schmitt trigger, enabling a power-on reset function by using an external RC cicuit.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	note 1	–0.5	+6.5	V
V_I	DC input voltage		–0.5	+6.5	V
I_{IK}	DC input diode current		–	±20	mA
V_O	DC output voltage		–0.5	V_{DD}+0.5	V
I_O	DC output source or sink current		–	±20	mA
I_{DD} or I_{SS}	total DC V_{DD} or V_{SS} current		–	±0.5	A
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C
V_{es}	electrostatic handling	note 2	–1500	+1500	V
V_{es}	electrostatic handling	note 3	–100	+100	V

Notes

1. All V_{DD} and V_{SS} pins must be externally connected to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a rise time of 15 ns.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 µH series inductor.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; $f_{XTAL} = 256f_s$; f_s = 44.1 kHz unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current		–	39	–	mA
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDD}	digital supply current		–	43	–	mA
P_{tot}	total power consumption		–	410	–	mW
Digital part: Inputs						
FSEL, HPEN, DSEL, TSEL, WSEL, ODF2, ODF1, CEN						
V_{IL}	LOW level input voltage	note 1	−0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DDD} +0.5	V
Z_I	input impedance		–	35	–	kΩ
C_I	input capacitance		–	–	10	pF
$\overline{\text{RESET}}$						
V_{IL}	LOW level input voltage	note 1	−0.5	–	$+0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage	note 1	$0.6V_{DDD}$	–	V_{DDD} +0.5	V
ΔV_I	input hysteresis		0.2	–	–	V
I_{LI}	input leakage current	note 2	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
SCKI, SWSI						
V_{IL}	LOW level input voltage	note 1	−0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DDD} +0.5	V
I_{LI}	input leakage current		−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
Crystal oscillator input XIN						
V_{IL}	LOW level input voltage		−0.5	–	$+0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	–	V_{DDD} +0.5	V
I_{LI}	input leakage current	note 2	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
SWSO, SCKO, SDO						
V_{OL}	LOW level output voltage	−400 μA; note 1	–	–	+0.4	V
V_{OH}	HIGH level output voltage	20 μA; note 1	2.4	–	–	V
C_L	load capacitance		–	–	50	pF
I_{LI}	leakage current in 3-state	note 2	−10	–	+10	μA
XSYS1, XSYS2						
V_{OL}	LOW level output voltage	−400 μA; note 1	–	–	0.4	V
V_{OH}	HIGH level output voltage	20 μA; note 1	2.4	–	–	V
C_L	load capacitance		–	–	35	pF
DCKO						
V_{OL}	LOW level output voltage	−400 μA; note 1	–	–	1.0	V
V_{OH}	HIGH level output voltage	20 μA; note 1	V_{DDD} −1.0	–	–	V
C_L	load capacitance		–	–	20	pF
Input/Outputs						
DIOR, DIOL						
V_{IL}	LOW level input voltage	note 1	−0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DDD} +0.5	V
Z_I	input impedance		–	35	–	kΩ
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	−400 μA; note 1	–	–	1.0	V
V_{OH}	HIGH level output voltage	20 μA; note 1	V_{DDD} −1.0	–	–	V
C_L	load capacitance		–	–	20	pF
Crystal oscillator						
Input XIN; Output XOUT						
f_{XTAL}	crystal operating frequency	note 3	4.608	$256f_s$ or $512f_s$	27.136	MHz
G_m	mutual conductance	100 kHz	1.5	–	–	mA/V
G_v	small signal voltage gain	$G_v = G_m \times R_o$	–	3.5	–	V/V
C_I	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	–	5	pF
C_O	output capacitance		–	–	10	pF
I_{LI}	input leakage current	note 2	−10	–	+10	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
External clock input XIN						
f_c	input frequency	note 3	4.608	$256f_s$ or $512f_s$	27.136	MHz
t_r	input rise time	V_{IL} to V_{IH}	–	–	10	ns
t_f	input fall time	V_{IH} to V_{IL}	–	–	10	ns
msr	mark-space ratio					
	in slave mode	$256f_s$	45	–	55	%
	in slave mode	$512f_s$	40	–	60	%
System clock output						
XSYS1, XSYS2 (note 4)						
t_r	output rise time	V_{OL} to V_{OH}	–	–	15	ns
t_f	output fall time	V_{OH} to V_{OL}	–	–	15	ns
t_{HIGH}	output HIGH time (relative to clock period)	note 5	40	50	60	%
1-bit code outputs (see Fig.4) 1–bit code inputs (see Fig.5)						
Clock: DCKO						
t_{cor}	clock output rise time	note 6	–	–	15	ns
t_{cof}	clock output fall time	note 6	–	–	15	ns
t_{coh}	clock output HIGH time		45	–	–	ns
t_{col}	clock output LOW time		45	–	–	ns
Data: DIOL, DIOR						
t_{dor}	data output rise time	note 6	–	–	15	ns
t_{dof}	clock output fall time	note 6	–	–	15	ns
t_{dod}	data output delay time (relative to DCKO)	note 6	–30	–	+30	ns
t_{dir}	data input rise time		–	–	20	ns
t_{dif}	data input fall time		–	–	20	ns
t_{dis}	data input set-up time (relative to DCKO)		30	–	–	ns
t_{dih}	data input hold time (relative to DCKO)		30	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial data outputs (see Fig.6)						
Clock: SCKO						
t_r	clock output rise time	note 7	–	–	30	ns
t_f	clock output fall time	note 7	–	–	30	ns
Word select: SWSO						
t_r	word select output rise time	note 7	–	–	30	ns
t_f	word select output fall time	note 7	–	–	30	ns
t_{SR}	word select output set-up time	note 8	100	–	–	ns
t_{HR}	word select output hold time	note 8	100	–	–	ns
Clock: SCKI (note 9)						
t_r	clock input rise time		–	–	100	ns
t_f	clock input fall time		–	–	100	ns
t_{HC}	clock input HIGH time		50	–	–	ns
t_{LC}	clock input LOW time		50	–	–	ns
Word select: SWSI (note 9)						
t_r	word select input rise time		–	–	100	ns
t_f	word select input fall time		–	–	100	ns
t_{SR}	word select input set-up time	note 10	100	–	–	ns
t_{HR}	word select input hold time	note 10	100	–	–	ns
Data: SDO						
t_r	data output rise time	note 7	–	–	30	ns
t_f	data output fall time	note 7	–	–	30	ns
t_{dod}	data output delay time	note 10	–100	–	+100	ns
t_{SR}	data output set-up time	note 8	100	–	–	ns
t_{HR}	data output hold time	note 8	100	–	–	ns
Analog part						
Voltage reference						
V_{REFL}, V_{REFR}						
V_I	input voltage		–5%	$V_{DDA}/2$	5%	V
Current reference						
I_{REF} (note 11)						
I_O	output current		–	V_{DDA}/ (2 x 13 kΩ)	–	A
DAC reference						
Input: V_{DACN}						
V_I	input voltage		–	V_{SSA}	–	V
Input: V_{DACP}						
V_I	input voltage		–	V_{DDA}	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sigma-Delta modulator						
Inputs: PINR, NINR, PINL, NINL						
$V_{I(RMS)}$	input voltage (RMS value)	note 12	–	1	–	V
ADC performance (note 13)						
THD + N	total harmonic distortion	at –1 dB digital output; note 14	–	–90 (0.003%)	–85 (0.0056%)	dB
DR	dynamic range	note 14	93	97	–	dB
α	channel separation	at 1 kHz; note 15	–	100	–	dB
G	gain		–1.5	–1	–0.5	dB
gd	group delay (in pass band)	note 16	–	1.25	–	ms

Notes

1. Minimum V_{IL}, V_{OL} and maximum V_{IH}, V_{OH} are peak values to allow for transients.
2. I_{LI} minimum and I_{LO} minimum measured at $V_I = 0$ V; I_{LI} maximum and I_{LO} maximum measured at $V_I = V_{DDD}$.
3. f_{XTAL} is a multiple of the system sampling frequency f_s which can vary between 18 kHz and 53 kHz.
4. Output times are measured with a capacitve load of 35 pF. XSYS2 is half the master clock frequency.
5. t_{HIGH} valid only when used with XTAL, with 50% input mark space ratio. XSYS1 t_{HIGH} is measured at $V_{DDD}/2$.
6. Output times are measured with a capacitive load of 20 pF.
7. Output times are measured with a capacitive load of 50 pF.
8. Relative to SCKO in master mode.
9. In slave mode the number of SCKI clocks in each channel should be less than 33 and the same in both. The polarity of SWSI indicates left/right channel.
10. Relative to SCKI in slave mode.
11. I_{REF} connected to 0 V via a 13 kΩ resistor.
12. The maximum recommended input voltage (referred to as 0 dB) yields a –1 dB output (relative to full-scale digital swing). The input voltage scales with $V(V_{DACP}) - V(V_{DACN})$; almost equal to V_{DDA}, hence:

$$V_I(0\ dB) = \frac{[V(V_{DACP}) - V(V_{DACN})]}{5} V_{RMS}$$

13. Device measured with external components shown in recommended application diagram Fig.7.
14. Typical values are for 18-bit performance, minimum/maximum values are for 16-bit performance.
15. This is the ratio (in dB) of the digital output amplitude of single tone, in one channel, to the digital output amplitude of the same tone in the measurement channel. this definition presupposes that the channels have the same gain.
16. $Group\ delay = \frac{(55.5 \pm 1)}{f_s}$, where f_s is the output sampling frequency. Typical value given is for f_s = 44.1 kHz.

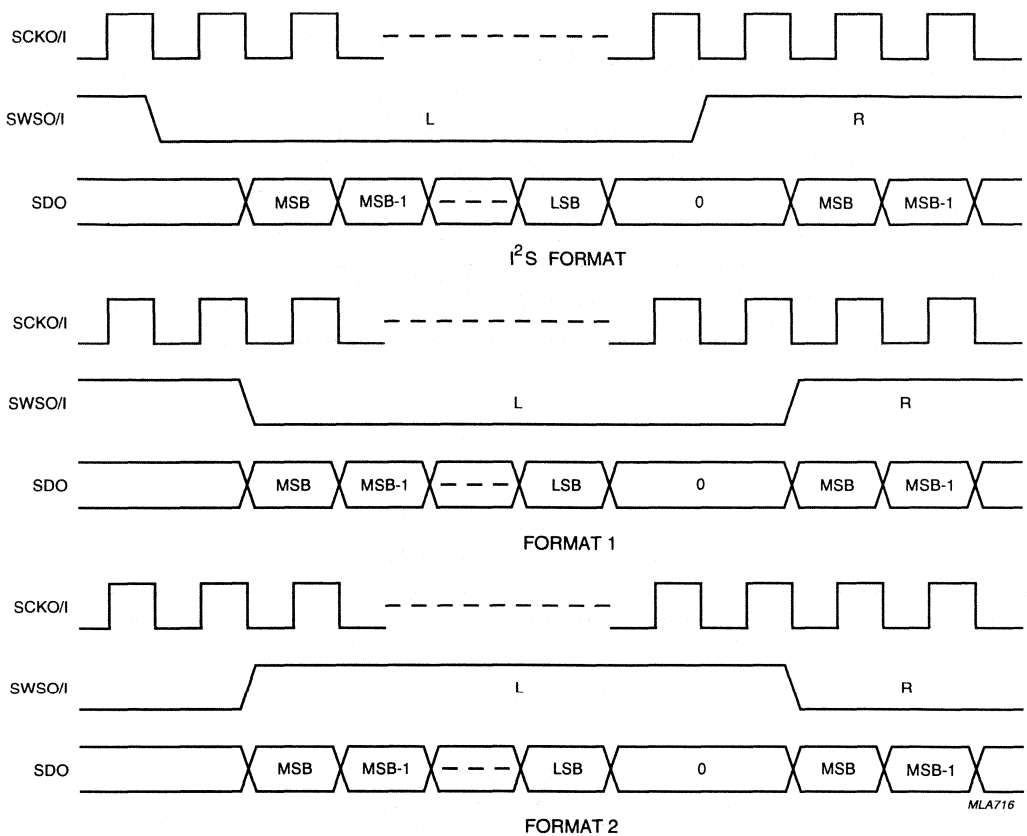


Fig.3 Output interface modes.

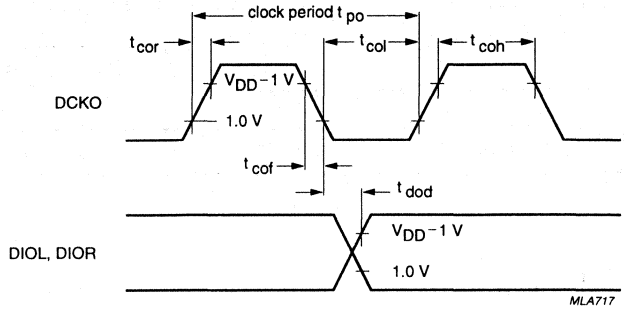


Fig.4 One bit code output timing.

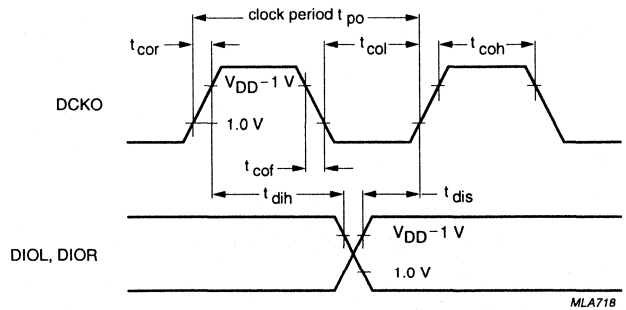


Fig.5 One bit code input timing.

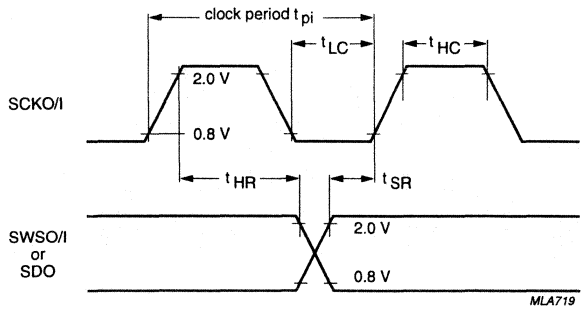
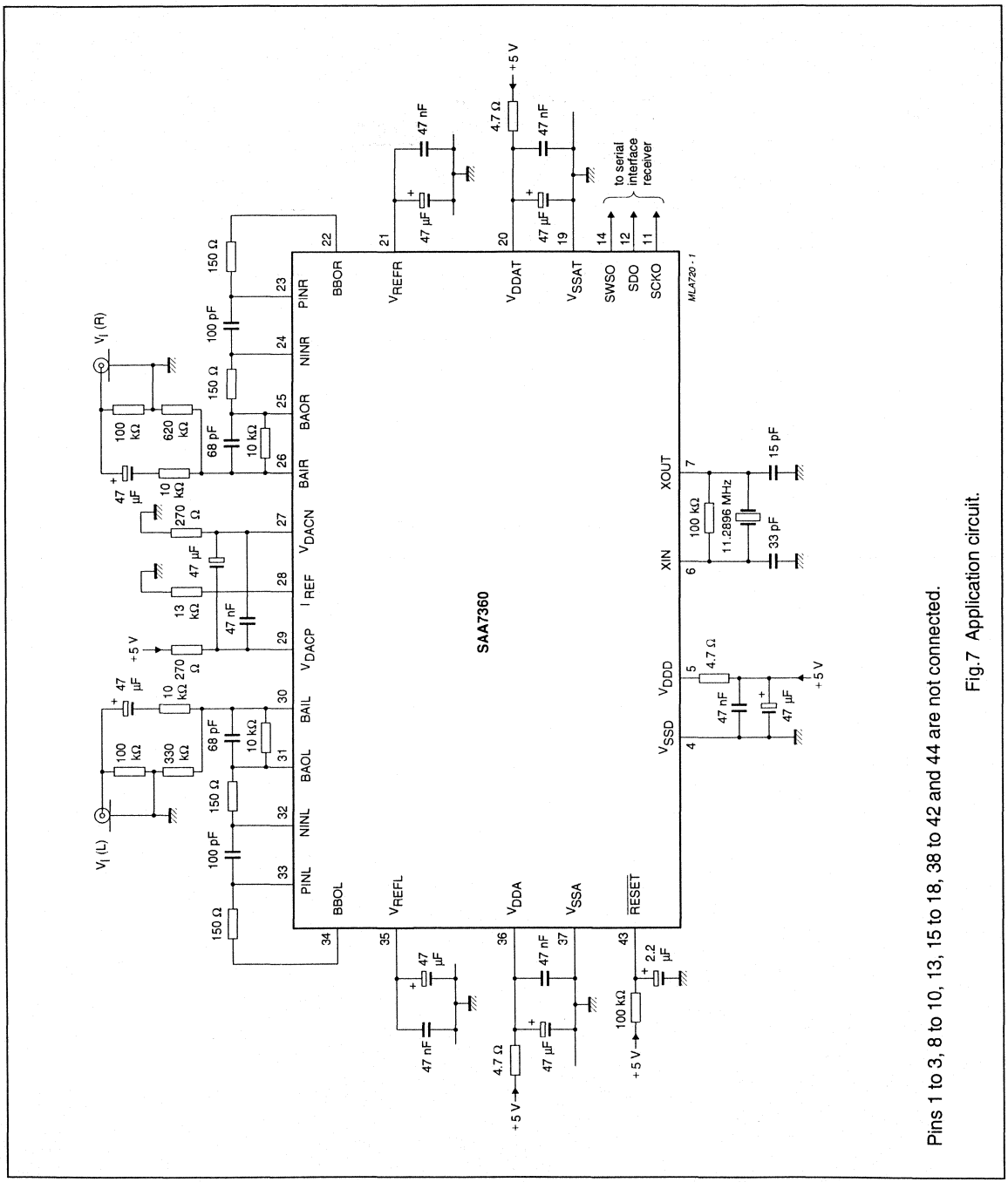


Fig.6 Serial output timing.

APPLICATION INFORMATION



Pins 1 to 3, 8 to 10, 13, 15 to 18, 38 to 42 and 44 are not connected.

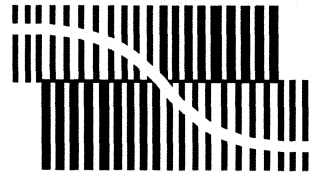
Fig.7 Application circuit.

Bitstream conversion ADC for digital audio systems

SAA7366

FEATURES

- Integrated buffers for simple interfacing to analog inputs
- 4 flexible serial interface modes
- Overload detection of digital signal ≥−1 dB amplitude
- Selectable high-pass filter
- 18-bit serial output
- 3.4 to 5.5 V operation of digital part
- Standby mode
- SO24 package
- Small non-critical PCB layout.



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The SAA7366 is a CMOS cost effective stereo analog-to-digital converter (ADC) using the Philips bitstream conversion technique.

APPLICATIONS

The device is designed for digital acquisition of analog audio signals for digital audio systems such as:

- CD-recordable
- Digital Compact Cassette (DCC)
- Digital Audio Tape (DAT).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	3.4	5.0	5.5	V
V_{DDA}	analog supply voltage	4.5	5.0	5.5	V
f_i	clock input frequency	4.608	12.288	13.568	MHz
THD + N	total harmonic distortion + noise	–	–	−80	dB
DR	dynamic range	90	–	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7366T	24	SO24L	plastic	SOT137A

BLOCK DIAGRAM

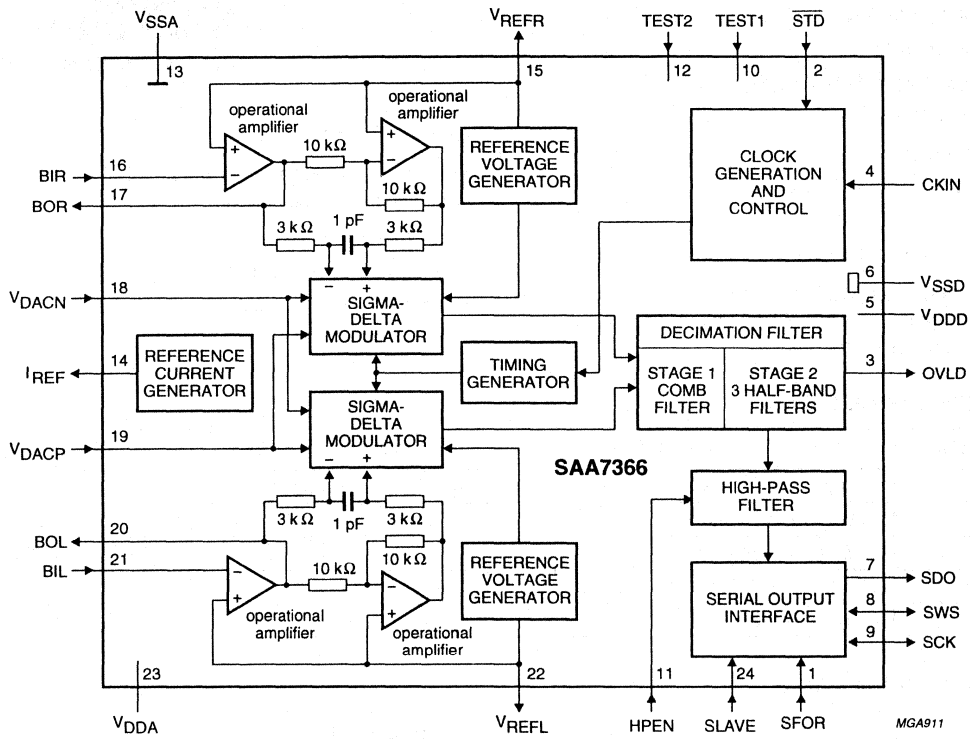


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SFOR	1	Serial interface output format select. Output format is selected as follows: SFOR HIGH = Format 1; SFOR LOW = Format 2.
$\overline{STD}$	2	Standby mode input (active LOW).
OVLD	3	Overload indication output. This pin indicates whether the internal digital signal is within 1 dB of maximum. In standby mode this output is high impedance.
CKIN	4	System clock input.
V_{DDD}	5	Supply for the digital section (3.4 to 5.5 V).
V_{SSD}	6	Ground supply for the digital section.
SDO	7	Serial interface data output. In standby mode this output is high impedance.
SWS	8	Serial interface word select signal. In master mode this pin outputs the serial interface word select signal. In slave mode this pin is the word select input to the serial interface. In standby mode this pin is always an input (high impedance).
SCK	9	Serial interface clock. In master mode this pin outputs the serial interface bit clock. In slave mode this pin is the input for the external bit clock. In standby mode this output is high impedance.
TEST1	10	Test input 1. This pin should be left open-circuit.
HPEN	11	High-pass filter enable input. (HPEN HIGH = enabled). If unconnected this pin defaults HIGH.
TEST2	12	Test input 2. This pin should be left open-circuit.
V_{SSA}	13	Ground supply for the analog section.
I_{REF}	14	Current reference output node.
V_{REFR}	15	$\frac{1}{2}V_{DDA}$ reference generator output for the right channel analog section.
BIR	16	Buffer operational amplifier inverting input for right channel.
BOR	17	Buffer operational amplifier output for right channel.
V_{DACN}	18	Negative 1-bit DAC reference voltage input, connected to 0 V.
V_{DACP}	19	Positive 1-bit DAC reference voltage input, connected to +5 V.
BOL	20	Buffer operational amplifier output for left channel.
BIL	21	Buffer operational amplifier inverting input for left channel.
V_{REFL}	22	$\frac{1}{2}V_{DDA}$ reference generator output for the left channel analog section.
V_{DDA}	23	Supply for the analog section.
SLAVE	24	Serial interface operating output mode master/slave select as follows: HIGH = slave mode; LOW = master mode. If unconnected the pin will default LOW.

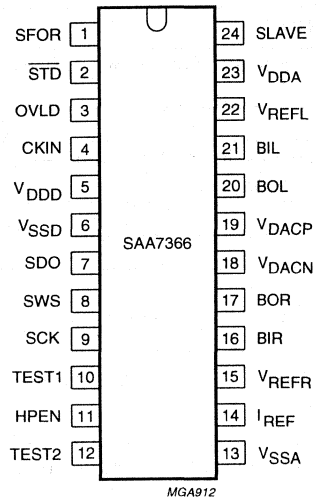


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The SAA7366 is a bitstream conversion CMOS ADC for digital audio systems. The conversion is achieved using a third order Sigma-Delta modulator (SDM), operating at 128 times the output sample frequency (f_s). The high oversampling ratio greatly simplifies the design of the analog input anti-alias filter. In most cases the internal buffer operational amplifier, configured as a low-pass filter will suffice. The 1-bit code from the Sigma-Delta modulator is filtered and down-sampled (decimated) to $1f_s$ in two stages of filtering. An optional high-pass filter is provided to remove DC, if required. The device has been designed with ease of use, low board area and low application costs in mind.

Clock frequency

The external clock, input on pin CKIN, operates at 256 times f_s, which can range from 18 kHz to 53 kHz.

Input buffer

Two input buffers are provided, one for each channel, for signal amplitude matching, signal buffering and anti-alias filter purposes. These are configured for inverting use. Access is provided by pins BIL, BIR (inverting inputs) and BOL, BOR (outputs) for left and right channels respectively. By the choice of feedback component values, the application signal amplitude can be matched to the requirements of the ADC. Typically the operational amplifiers are configured as low-pass filters with a gain of 1 and a pole at approximately $5f_s$.

Remark: The complete ADC is non-inverting. Hence a positive DC input (referenced to V_{ref}) will yield a positive digital output.

Input level

The overall system gain is proportional V_{DDA}, or more accurately $\{V(V_{DACP}) - V(V_{DACN})\}$. For convenience the ADC input signal amplitude is defined as that amplitude seen on BOL or BOR, the operational amplifier outputs (i.e. the input to the Sigma-Delta modulator). Also, the 0 dB input level is defined as that which provides a −1 dB (actually −1.08 dB) digital output, relative to full-scale swing. This offset provides headroom to accommodate small random DC offsets without causing the digital output to clip.

Hence:

$$V_I(0\ dB) = \frac{V(V_{DACP}) - V(V_{DACN})}{5} = V\ (RMS)$$

The user of the IC should ensure, that when all sources of signal amplitude variation are taken into account, the maximum input signal should conform to the 0 dB level. If not, clipping may occur. In the event that the maximum signal level cannot be pre-determined, e.g. a live microphone input, the average signal level should be set at −10 to −20 dB down. The exact value will depend on the application and the balance between head room and operating signal-to-noise ratio.

Behaviour during overload

As defined earlier the maximum input level for normal operation is 0 dB. If the input level exceeds this value clipping may occur. Infringements are limited to the maximum permitted positive or negative values, $2^{17} - 1$ or -2^{17} respectively. If the high-pass filter has been enabled the clipped output samples may have non-maximum values due to the removal of the DC content. Input signals in the range of 0 to 1 dB may or may not be clipped depending on the values of DC dither and small random offsets in the analog circuitry.

When using the recommended application circuitry, clipping will initially be observed on negative peaks due to the use of negative DC dither.

The maximum level of overload that can be safely tolerated is application circuit dependent. In the case of the

recommended circuit the following applies: the inverting operational amplifier inputs BIL/BIR are protected from excessive voltages (currents) by diodes to V_{DDA} and V_{SSA}. These have absolute maximum ratings of $I_{IK} = \pm 20$ mA, with a safe practical limit of ±2 mA. Given the input resistor of 10 kΩ, ±2 mA diode current and the operation of the operational amplifier a maximum signal (applied to the input resistor) of ±30 V can be handled safely. This level represents an overload of 26 dB.

During overload the in-band portion of the waveform will be correctly converted. The out-of-band portion will be limited as detailed above.

Sigma-Delta modulator

The SAA7366 has two third order Sigma-Delta modulators with a quantization noise floor of approximately −104 dB. The scaling of the feedback has been optimized for stable operation even during overload. Thus with a maximum signal swing of 0 V to V_{DDA} on the input the digital output remains well behaved, i.e. it does not burst into random oscillation. During overload the output is simply a clipped version of the input. The gain of this stage is −4.95 dB.

Decimation filter

Decimation from $128f_s$ is performed in two stages. The first stage is a comb filter, which decimates from 128 to $8f_s$. The second stage, consists of 3 half-band filters, each decimating by a factor of 2.

The overall characteristics are given in Table 1.

Table 1 Overall filter characteristics.

ITEM	CONDITION	VALUE (dB)
Pass band ripple	0 to $0.45f_s$ Hz	±0.1
	0.45 to $0.47f_s$	−0.5
Stop band	$>0.55f_s$	−60
Dynamic range	0 to $0.42f_s$	110
Gain	DC	3.87

High-pass filter

An optional high-pass filter is provided to remove unwanted DC components. The operation is selected when HPEN is HIGH. The filter has the characteristics given in Table 2.

Table 2 High-pass filter characteristics.

ITEM	CONDITION	VALUE (dB)
Pass band ripple		none
Pass band gain		0
Droop	at $0.00045f_s$	0.029
Attenuation at DC	at $0.00000036f_s$	>40
Dynamic range	0 to $0.45f_s$	116

Serial interface

The serial interface provides 2 formats in both master and slave modes (see Figs 3 and 4). In both modes the interface provides up to 18 significant bits of output data per channel.

During standby mode ($\overline{STD}$ = LOW) all interface pins are in their high-impedance state. On recovery from standby the serial data output SDO is held LOW until valid data is available from the decimation filter. This time depends on whether the high-pass filter is selected or not as follows:

HPEN = 0; $T = 1024/f_s$, T = 21.3 ms when f_s = 48 kHz

HPEN = 1; $T = 8192/f_s$, T = 170.6 ms when f_s = 48 kHz

Overload Detection Indication (OVLD)

The OVLD output is used to indicate whenever the data, in either the left or right channel, is within 1 dB of the maximum possible digital swing. When this condition is detected the OVLD output is forced HIGH for at least $512f_s$ cycles (10.6 ms at f_s = 48 kHz). This time-out is reset for each infringement.

Standby mode ($\overline{STD}$)

The $\overline{STD}$ pin activates a power saving mode when the device function is not required. This pin can also be used as a chip enable, as follows.

On a HIGH-to-LOW transition, of the $\overline{STD}$ pin, the internal control circuitry starts a timed power-down sequence. This takes approximately 32 system clock cycles to complete. Transitions on $\overline{STD}$ which are shorter than 32 clock cycles have an indeterminate effect. However, the device will always recover correctly.

During standby the following occurs:

- The internal logic clock is disabled
- The serial interface pins are forced to high impedance
- The OVLD output is forced LOW
- The analog circuitry is disabled
- The nominal external analog node voltages are maintained by a low-power circuit. This feature ensures a fast recovery from standby mode.

On a LOW-to-HIGH transition the device reverts back to its normal function. This process takes approximately 32 system clock cycles. Before SDO is enabled the output data is forced LOW. SDO remains LOW until good data is available from the decimation filter.

The $\overline{STD}$ pin has a Schmitt-trigger input. A simple power-on reset function can be effected using an external capacitor to V_{SSD} and resistor to V_{DDD}.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	note 1	−0.5	+6.5	V
V_I	DC input voltage		−0.5	+6.5	V
I_{IK}	DC input diode current		–	±20	mA
V_O	DC output voltage		−0.5	V_{DD} + 0.5	V
I_O	DC output source or sink current		–	±20	mA
I_{DDtot}	total DC supply current		–	±0.5	A
I_{SStot}	total DC supply current		–	±0.5	A
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C
V_{es1}	electrostatic handling	note 2	−2000	+2000	V
V_{es2}	electrostatic handling	note 3	−200	+200	V

Notes

1. V_{SSD} and V_{SSA} pins must be externally connected to a common potential.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a rise time of 15 ns.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

V_{DDD} = 3.4 to 5.5 V; V_{DDA} = 4.5 to 5.5 V; T_{amb} = −40 to +85 °C; f_s = 18 to 53 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	f_s = 48 kHz	–	13	–	mA
V_{DDD}	digital supply voltage		3.4	5.0	5.5	V
I_{DDD}	digital supply current	f_s = 48 kHz	–	56	–	mA
P_{tot}	total power consumption	f_s = 48 kHz	–	345	–	mW

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{STD}	standby supply current		–	65	–	μA
P_{STD}	standby power consumption		–	325	–	μW
Digital part: inputs						
SFOR, SLAVE AND HPEN						
V_{IL}	LOW level input voltage	note 1	−0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DDD} + 0.5	V
I_{LI}	input leakage current	note 2	−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
CLKIN						
V_{IL}	LOW level input voltage		−0.5	–	$+0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	–	V_{DDD} + 0.5	V
I_{LI}	input leakage current	note 2	−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
$\overline{STD}$ (SCHMITT-TRIGGER)						
V_{IL}	LOW level input voltage	note 1	−0.5	–	$+0.4V_{DDD}$	V
V_{IH}	HIGH level input voltage	note 1	2.4	–	V_{DDD} + 0.5	V
ΔV_I	input hysteresis		–	600	–	mV
I_{LI}	input leakage current	note 2	−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
Digital part: Input/Outputs						
SWS AND SCK						
V_{IL}	LOW level input voltage	note 1	−0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DDD} + 0.5	V
I_{LI}	leakage current in 3-state	note 2	−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_O = −400 μA; note 1	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 20 μA; note 1	2.4	–	–	V
C_L	output load capacitance		–	–	50	pF
Digital part: Outputs						
OVLD						
V_{OL}	LOW level output voltage	I_O = −400 μA; note 1	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 20 μA; note 1	2.4	–	–	V
C_L	output load capacitance		–	–	50	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SDO						
V_{OL}	LOW level output voltage	I_O = −400 µA; note 1	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 20 µA; note 1	2.4	–	–	V
I_{LI}	leakage current in 3-state	note 2	−10	–	+10	µA
C_L	output load capacitance		–	–	50	pF
Digital part: timing						
CKIN						
t_r	clock input rise time		–	–	10	ns
t_f	clock input fall time		–	–	10	ns
f_i	clock input frequency	note 3	4.608	12.288	13.568	MHz
msr	mark-to-space ratio	$f_s > 32$ kHz	40	–	60	%
		$f_s \leq 32$ kHz	30	–	70	%
Serial interface master and slave modes (see Figs 5, 6 and 7)						
SCK						
t_r	clock rise time	note 4	–	–	50	ns
t_f	clock fall time	note 4	–	–	50	ns
t_L	clock LOW time	T = 1/64f_s	0.40T	–	0.60T	
t_H	clock HIGH time	T = 1/64f_s	0.40T	–	0.60T	
f_{clk}	clock frequency	master mode	64f_s	64f_s	64f_s	
		slave mode	–	–	64f_s	
t_{idle}	burst clock idle time	slave mode; T = 1/f_s	0	–	0.05T	
SWS						
t_r	word select rise time	note 4	–	–	50	ns
t_f	word select fall time	note 4	–	–	50	ns
t_{wL}	word select LOW time	T = 1/f_s	0.45T	0.50T	0.55T	
t_{wH}	word select HIGH time	T = 1/f_s	0.45T	0.50T	0.55T	
f_{wc}	word select frequency		1f_s	1f_s	1f_s	
t_d	word select delay from SCK	master mode	−50	–	+50	ns
t_d	word select delay from SCK	slave mode	50	–	–	ns
t_{su}	word select set-up time to SCK	slave mode	150	–	–	ns
SDO						
t_h	data output hold time		100	–	–	ns
t_{su}	data output set-up time		100	–	–	ns
t_r	data output rise time	note 4	–	–	50	ns
t_f	data output fall time	note 4	–	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog part (V_{DDD} = V_{DDA} = 5 V; T_{amb} = 25 °C; f_s = 48 kHz)						
VOLTAGE REFERENCE: V_{REFL} AND V_{REFR}						
V_O	output voltage		$0.475V_{DDA}$	$0.5V_{DDA}$	$0.525V_{DDA}$	V
Z_n	DC impedance	normal mode	–	750	–	Ω
Z_s	DC impedance	standby mode	–	100	–	kΩ
CURRENT REFERENCE: I_{REF}						
V_O	output voltage		–	$0.5V_{DDA}$	–	V
I_O	output current	R = 33 kΩ	–	76	–	μA
DAC REFERENCE: V_{DACN}						
V_I	input voltage		–	V_{SSA}	–	V
V_{DACP}						
V_I	input voltage		–	V_{DDA}	–	V
BUFFER OPERATIONAL AMPLIFIERS: BIL, BOL, BIR AND BOR						
V_{offset}	input offset voltage		–	< ±10	–	mV
R_{LmaX}	maximum load resistance; (drive capability)	decoupled to V_{REF}	–	10	–	kΩ
Z_O	output impedance		–	100	–	Ω
THD + N	total harmonic distortion plus noise	f = 0 to 20 kHz	–	–85	–	dB
ADC PERFORMANCE; NOTE 5						
t_{gd}	group delay	$T = 1/f_s$	tbf	–	tbf	μs
α_{sb}	stop band attenuation	$f > 0.546f_s$	60	–	–	dB
DR	dynamic range	note 6	90	–	–	dB
THD + N	total harmonic distortion plus noise	note 7	–	–	–80	dB
S/N	signal-to-noise ratio	A-weighted	–	tbf	–	dB
α_{cs}	channel separation	note 8	–	tbf	–	dB
G	gain	note 9	–1.2	–1	–0.8	dB

Notes

1. Minimum V_{IL}, V_{OL} and maximum V_{IH}, V_{OH} are peak values to allow for transients.
2. I_{LImin} and I_{LOmin} measured at V_I = 0 V; I_{LImax} and I_{LOmax} measured at $V_I = V_{DDD}$.
3. f_i is a multiple (×256) of the system sampling frequency (f_s) which can vary between 18 kHz and 53 kHz.
4. C_L = 50 pF (valid for master mode only).
5. Device measured with external components shown in recommended application diagram Fig.8.
6. Input is 1 kHz and –60 dB.
7. Input is 1 kHz and 0 dB.
8. Measured by applying a 1 kHz, 0 dB signal to one channel and monitoring the level of 1 kHz (fundamental) on the other channel.
9. See also Section "Input level" of Chapter "Functional description"; valid for left or right channel.

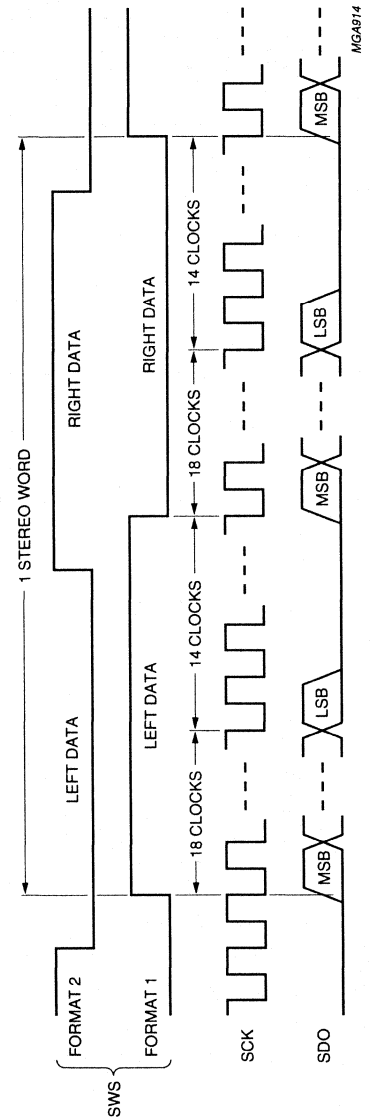


Fig.3 Serial interface master mode format.

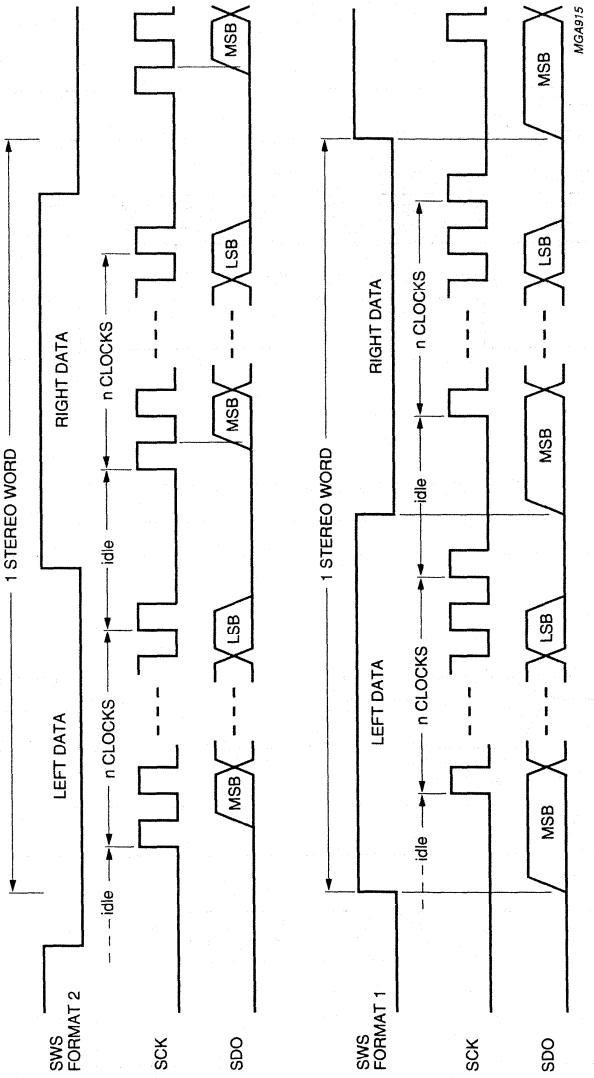


Fig.4 Serial interface slave mode formats.

1 < n < 33.
Up to 18 significant bits are available.

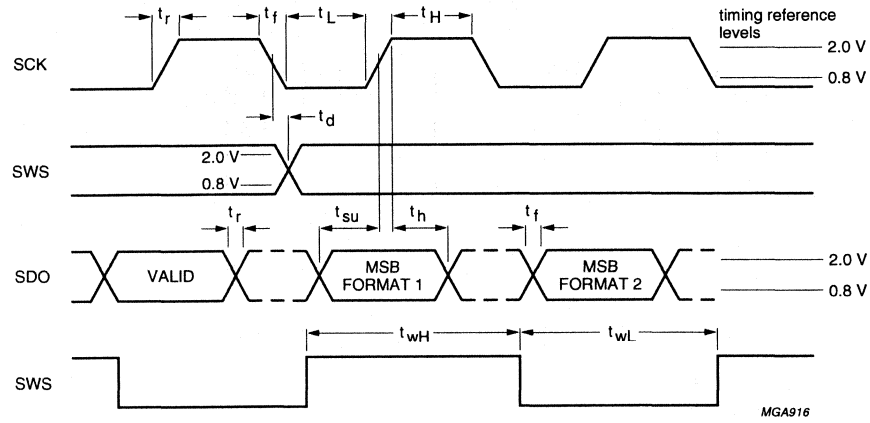


Fig.5 Serial interface master mode timing.

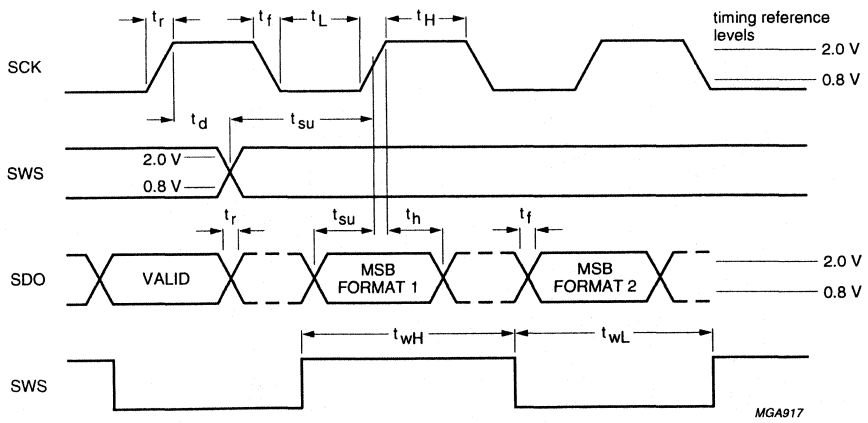


Fig.6 Serial interface slave mode timing.

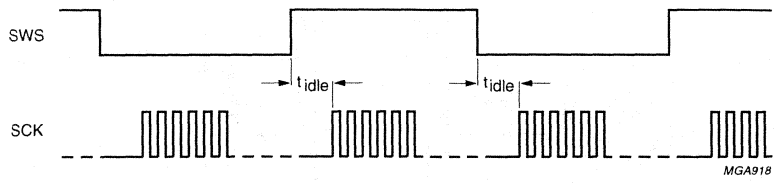
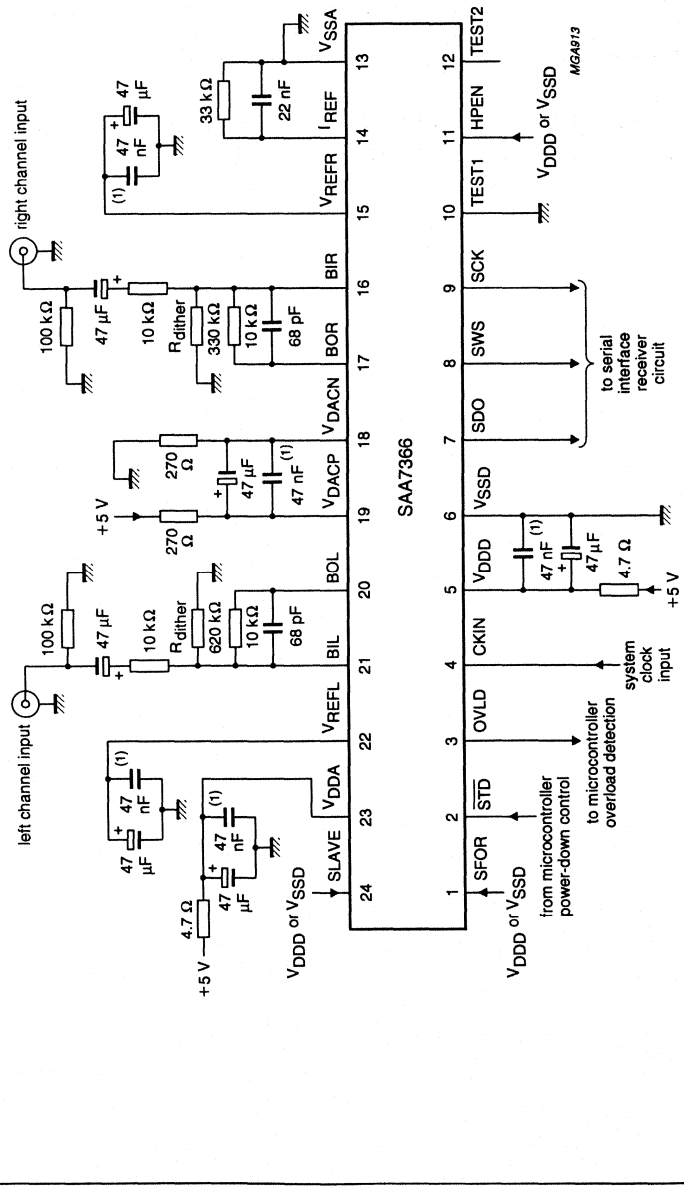


Fig.7 Serial interface slave mode burst clock.

APPLICATION INFORMATION



(1) These capacitors should preferably be surface mounted components located as close as possible to the device pins.

Fig.8 Application circuit.

DIGITAL SATELLITE RADIO BROADCASTING TUNER DECODER (SAT-2)

GENERAL DESCRIPTION

The SAA7500 performs a decoder function for digital satellite sound broadcasting tuners. It is designed to decode one of 16 stereo channels broadcasting audio signals in accordance with the German standard - **Technische Richtlinie ARD/ZDF Nr. 3R1.**

Features

- Clock recovery
- Differential decoding
- Main frame synchronization
- Swapping half-frames in case of inversion
- Unscrambling
- Demultiplexing
- Subframe synchronization
- Error correction and concealment
- Scale factor decoding with error correction
- Shift into the original values using the scale factors
- Mute in case of synchronization loss

QUICK REFERENCE DATA

parameter	symbol	min.	max.	unit
Supply voltage	V_{DD}	4.5	5.5	V
Power dissipation	P_{tot}		500	mW
Clock frequency	T_{20N}	20.48		MHz

PACKAGE OUTLINE

68-lead plastic leaded chip carrier (PLCC); 'pocket' version (SOT188AA).

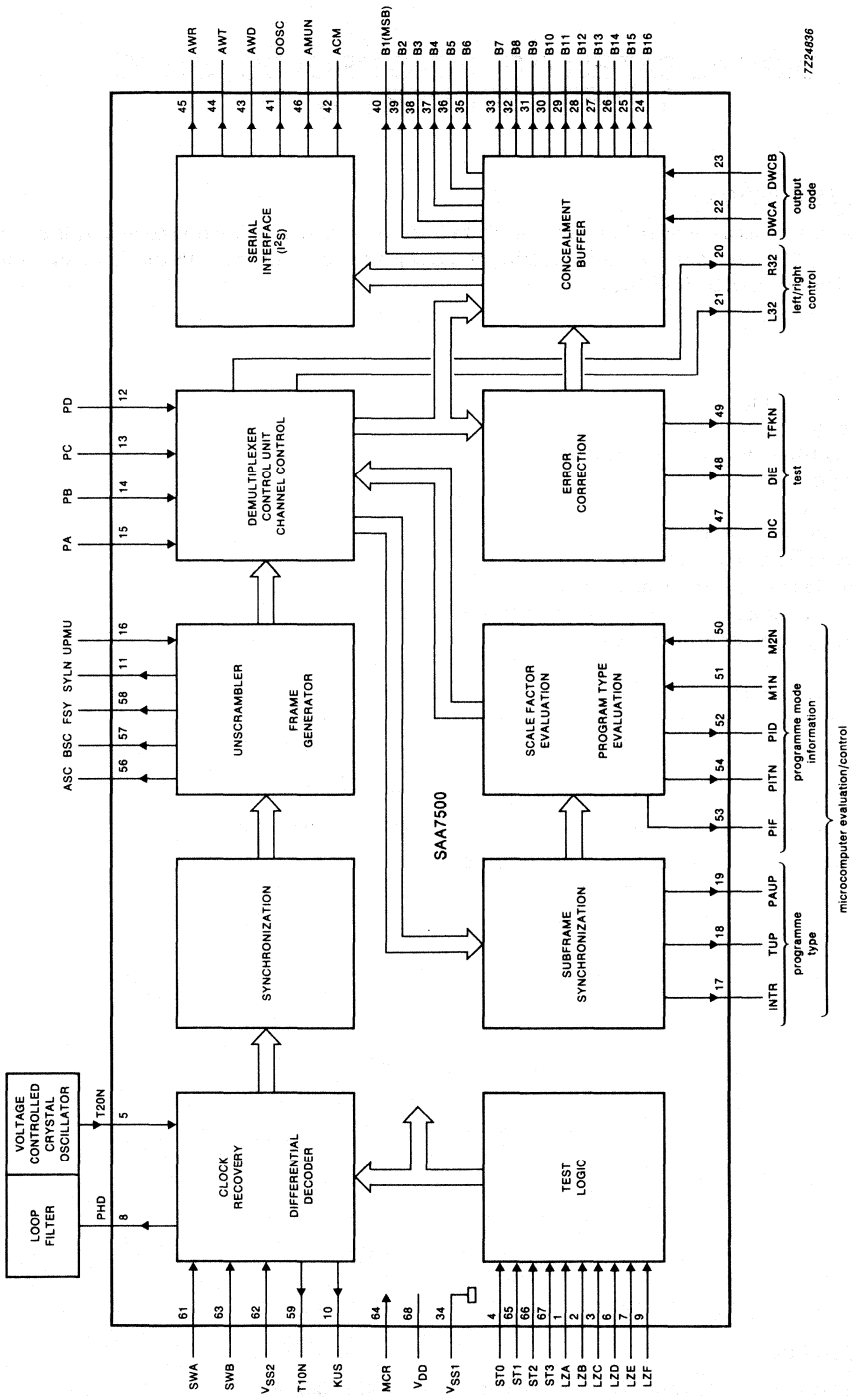


Fig.1 Block diagram.

PINNING

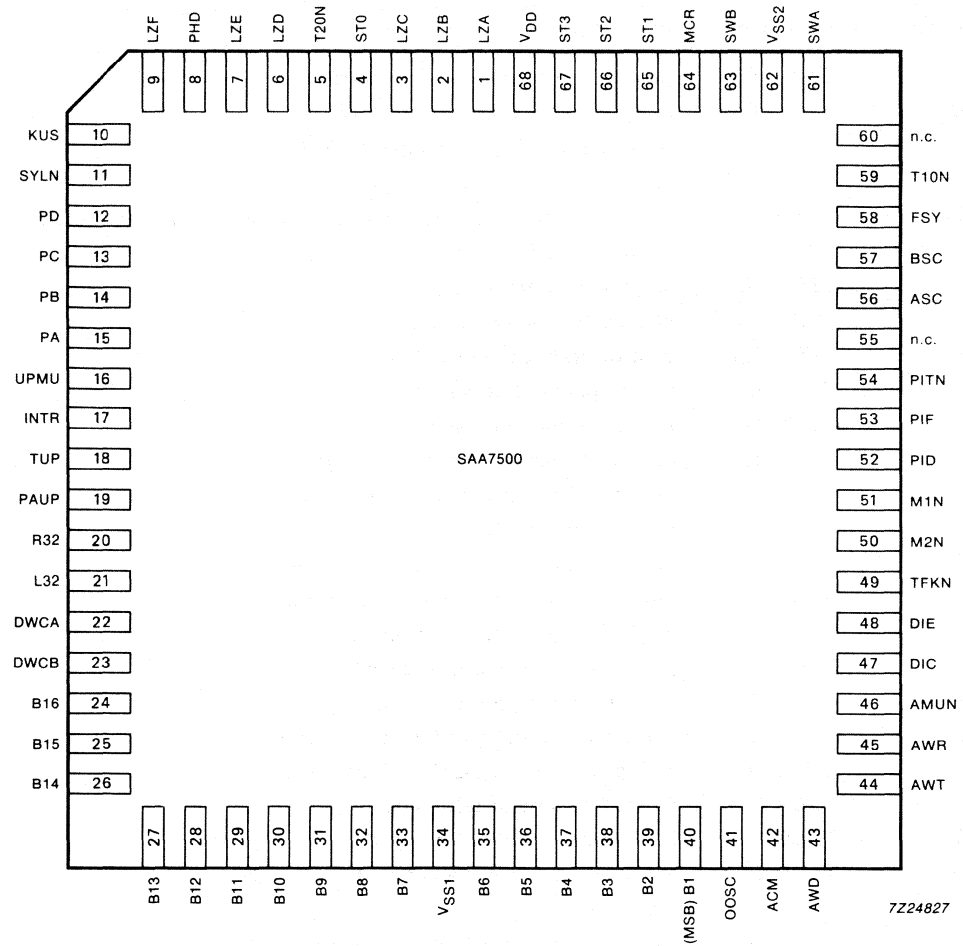


Fig.2 Pinning diagram; for pin functions see next page.

Pin functions

(1) = CMOS level input. (2) = TTL level input. (3) = CMOS level input with pull down resistor.

pin no.	mnemonic		description
1	LZA	I(3)	phase adjustment for the internal clock.
2	LZB	I(3)	phase adjustment for the internal clock.
3	LZC	I(3)	phase adjustment for the internal clock.
4	ST0	I(3)	control input for testing.
5	T20N	I(1)	20.48 MHz clock input from voltage controlled oscillator (VCX).
6	LZD	I(3)	control input for testing.
7	LZE	I(3)	control input for testing.
8	PHD	O	phase control signal for VCX.
9	LZF	I(3)	control input for testing.
10	KUS	O	test output (A'B' swap).
11	SYLN	O	synchronization indication flag.
12	PD	I(2)	programme number input selector (MSB)
13	PC	I(2)	programme number input selector.
14	PB	I(2)	programme number input selector.
15	PA	I(2)	programme number input selector (LSB).
16	UPMU	I(2)	mute input (controlled by microcomputer).
17	INTR	O	interrupt flag for microcomputer.
18	TUP	O	programme type interface (clock).
19	PAUP	O	programme type interface (data).
20	R32	O	multiplex control signal for right channel.
21	L32	O	multiplex control signal for left channel.
22	DWCA	I(3)	DA-converter mode select input.
23	DWCB	I(3)	DA-converter mode select input.
24-33	B16-7	O	audio data for parallel interface, bits 16 (LSB) to 7.
34	V_{SS1}	I	ground (supply).
35-40	B6-1	O	audio data for parallel interface, bits 6 to 1 (MSB).
41	OOSC	O	4.096 MHz clock output.
42	ACM	O	concealment flag (for SAA7220P/C).
43	AWD	O	audio data (for SAA7220P/C).
44	AWT	O	bit clock (for SAA7220P/C).
45	AWR	O	word select signal (for SAA7220P/C).
46	AMUN	O	mute signal (for SAA7220P/C).
47	DIC	O	data output for testing.
48	DIE	O	data output for testing.

pin no.	mnemonic		description
49	TFKN	O	burst clock for test data.
50	M2N	I(2)	channel mode select input.
51	M1N	I(2)	channel mode select input.
52	PID	O	programme information (PI) interface output (data).
53	PIF	O	programme information (PI) interface output (window signal).
54	PITN	O	programme information (PI) interface output (clock).
55	n.c.		not connected.
56	ASC	O	data output for 10.24 Mbit/s interface.
57	BSC	O	data output for 10.24 Mbit/s interface.
58	FSY	O	window signal for 10.24 Mbit/s interface.
59	T10N	O	10.24 MHz clock output.
60	n.c.		not connected.
61	SWA	I(2)	10.24 Mbit/s data input.
62	V_{SS2}	I	ground (screen).
63	SWB	I(2)	10.24 Mbit/s data input.
64	MCR	I(1)	master reset.
65	ST1	I(3)	control input for testing.
66	ST2	I(3)	control input for testing.
67	ST3	I(3)	control input for testing and mode select for 10.24 Mbit/s interface.
68	V_{DD}	I	power supply.

FUNCTIONAL DESCRIPTION

General

The SAA7500 has been designed to decode 16 stereo channel sound broadcasting signals in accordance with the German standard - **Technische Richtlinie ARD/ZDF Nr. 3R1.** The channel carrying the sound broadcast programme is selected and converted into an intermediate frequency by a frontend. The signal is then amplified and demodulated (4 PSK (Phase Shift Keying) with carrier recovery). The outputs from the demodulator are two differential coded signals that are input into the SAA7500. The SAA7500 decoder outputs the audio data, of the selected stereo or mono channel, as linear quantized 16-bit audio samples.

Selection of the desired audio channel, as well as stereo or mono mode, is controlled by inputs PA, PB, PC and PD. These inputs may be driven directly by switches or controlled by a microcomputer.

When under the control of a microcomputer, the SAA7500 transmits serial data to the microcomputer on the type of programme (16 stereo or 32 mono). The corresponding synchronization of the subframe is partly performed by the SAA7500 (every 2 ms) and at a higher level by the microcomputer (every 16 ms). The SAA7500 also sends to the microcomputer, programme information code data together with its clock and window signal.

The circuit automatically performs the system error correction and concealment. In the transmit error rate range of 0 to 3×10^{-3} a theoretical C/N (carrier-to-noise ratio) gain of about 6 dB is obtained. The residual error rate is nearly zero for transmit error rates $\leqslant 3 \times 10^{-4}$.

The remaining functions, such as clock recovery, main and subframe synchronization and scale factor decoding, are protected in a similar manner so that they will not influence the residual error rate.

Clock recovery

The baseband signals A' and B' are connected to the SWA and SWB inputs of the SAA7500. For clock recovery, the phase of the incoming data streams is compared with T10N (half the oscillator frequency). The output of the phase comparator (PHD) controls, by means of the loop filter, the voltage controlled oscillator (both are external to the IC) and thus its output signal T20N.

For energy dispersal, for example, in modulation pauses or with constant signals, the data streams are scrambled during generation. The exceptions are the synchronization words and the special service bits. In order that the phase correspondence between the recovered system clock (T10N) and the input signals A' and B' can be adjusted to a minimum bit error rate (BER), a programmable phase shifter is provided (inputs LZA, LZB, LZC and ST3).

The differential decoder logic delivers the original data streams which may be exchanged depending on the number of mixer stages on the transmission channel. The polarity of the two synchronization words will indicate if this is necessary, if so the two data streams will be automatically switched over.

Synchronization

Using the synchronization circuit, the incoming data streams are first searched for 11-bit Barker codewords. The synchronization circuit permits two errors for both synchronization words, which guards against failure of the synchronization word. If the synchronization word has been detected, the following data is examined at frame length intervals to see if the synchronization word is repeated. If it is repeated, it is acknowledged as a synchronization word (window check) and an internal frame pulse generator takes over further control. There is also a synchronization word failure control which initiates a renewed synchronization word search and mutes the AF output if four successive synchronization word failures occur.

To enhance the performance the result from the error correction circuit is used as an additional input to the synchronization circuit. This is to avoid extra errors through synchronization loss in the case of relative high, but for reception acceptable, bit error rates. This will not affect the rapid detection of

a very high bit error rate or the non-synchronization of the data stream. The decoder will function correctly with a bit error rate up to 3×10^{-3}.

Demultiplexer

After synchronization, the beginning of a frame is marked and the digital signals are defined as to their assignment. First the non-scrambled special service bit from the half frame A is taken out. The rest of both half frames are unscrambled and demultiplexed so that each half frame is split into two substreams with a rate of 5.12 Mbit/s (see Technische Richtlinie ARD/ZDF Nr. 3R1, main frame specification). Using the inputs from the synchronization circuit and the programme selector (inputs PA, PB, PC and PD) the demultiplexer locks on to the selected programme block and generates all the control signals required for further signal processing.

Error correction

The error correction circuit provides for exact identification of two errors in a 63/44 BCH block and correction of the incorrect bits. In the event of more than two errors the identification circuit can identify incorrect BCH blocks with up to five errors.

The BCH block is operated on by a syndrome calculator, the result controls the lines of an error correction matrix. The output of this matrix corrects (inverts) the incorrect bits when data is shifted out from its buffer. The BCH block is then fed through a second syndrome calculator. In the event of more than two errors the result of the whole calculation will be other than zero. This information provides the concealment in the next stages.

The two adjacent samples related to the detected incorrect sample are added and divided by two, the result replaces the incorrect sample (interpolation). In the event of successive bad samples the last corrected sample is held until a good sample is detected (hold function). A high error frequency in the event of synchronization loss will activate the muting function and set the output data to zero.

This information, if concealment is not active, is used in the synchronization circuit as described in that section. When the samples are correct it can be assumed that the synchronization is also correct.

Scale factor, programme type evaluation and shift sunction

The transmitted samples are returned to their original range of values by the scale factor, which is obtained by decoding the ZI-subframe. The start of this frame is coupled to the start of the special services frame, synchronization for this frame uses the same principle as for the main frame. In the scale factor evaluation unit the BCH 14/6 code words (three times transmitted) are fed into a majority selection circuit working at bit level. Subsequently the error check and the correction of a maximum of two errors is carried out.

The SAA7500 contains the synchronization word detection and error check for the subframe synchronization word with its repetition time of 2 ms. The programme type evaluation with its superior synchronization has to be performed external to the chip, for example, by a microcomputer. For this purpose data is available in 8-bit blocks at a serial interface (INTR, PAUP and TUP; block rate = 4000/s). The same microcomputer can also perform the programme selection (inputs PA, PB, PC and PD).

At the input to the concealment buffer the corrected 11 bits (MSB) are combined with the 3 unprotected transmitted bits (LSB). The scale factor determines the required shift-back operations needed to convert the transmitted values back into the original values. Voids that occur are filled with noughts or ones corresponding to the sign bit. The shift-back and filling of voids ensures that no incorrect bits occur above the range defined by the scale factor. The upper 16 bits represent the regenerated audio sample.

FUNCTIONAL DESCRIPTION (continued)

Digital-to-analogue conversion and interfaces

The SAA7500 enables different DAC systems to be used. For control of the SAA7220P/C and TDA1541 a 2.5 external divider must be connected to the 20.48 MHz clock signal to produce the required 8.192 MHz clock signal.

A serial interface is built in with the following outputs: bit clock (AWT), word select (AWR) and audio data (AWD). In addition the mute signal (AMUN) and the concealment flag (ACM) are also available. The SAA7220P/C and TDA1541 are equipped with a digital audio interface for domestic use equivalent to 'IEC proposal No. 84 (secretariat 28; from June 1985)'.
For DACs with a parallel interface in a multiplex mode the audio data are available at the B1(MSB)-B16 outputs. The multiplexing is controlled by the L32 and R32 outputs. Using the mode outputs DWCA and DWCB the code (offset binary or two's complement) and polarity can be selected.

Additional information, including the scale factor is available through the programme information (PI) interface (PID, PITN and PIF). Another interface, using the ASC, BSC and T10N outputs, makes available signals from the differential decoder. These signals are used for bit error measurement and an optimized phase adjustment of the internal clock (refer to 'clock recovery' section).

An optional application of the control signals for mute and concealment operations is possible using the outputs AMUN and ACM. For the mute signal a different time relationship to the unwanted unwanted pulse with very low C/N values may be obtained.

The external application of the concealment signal is recommended; if an additional interpolation is required between additional samples with different levels in the external circuitry (such as the SAA7220P/C).

Truth tables

Table 1 Delay adjustment

pins 1 to 3

LZC	LZB	LZA	delay
0	0	0	$4 \times \tau$
0	0	1	$3 \times \tau$
0	1	0	$2 \times \tau$
0	1	1	$1 \times \tau$
1	0	0	$0 \times \tau$
1	0	1	$-1 \times \tau$
1	1	0	$-2 \times \tau$
1	1	1	$-3 \times \tau$

$\tau \approx 1.5$ x gate delay time (NAND)

Table 2 Master reset

pin 64

MCR	function
0	operation
1	master reset

Table 3 Mute

pin 16

UPMU	function
0	no
1	yes

Table 4 Programme number

pins 12 to 15

PD	PC	PB	PA	programme no.
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
.	.	.	.	.
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

Table 5 Phase control signal

pin 8

PHD	phase
0	lead phase
1	lag phase

Table 6 Synchronization indication

pin 11

SYLN	synchronization
0	yes
1	no

Table 7 Mode select for data outputs ASC and BSC for 10.24 Mbit/s interface

pin 67

ST3	data ASC/BSC
0	after unscrambler
1	before unscrambler

Table 8 Data converter mode select B1(MSB) to B16

pins 22 and 23

DWCB	DWCA	DA converter mode
0	0	compl. offset binary
0	1	offset binary
1	0	compl. 2's complement
1	1	2's complement

Table 9 Channel mode select

pins 50 and 51

M2N	M1N	channel mode
0	0	mono (1 + 2)
0	1	mono R(2)
1	0	mono L(1)
1	1	stereo

Table 10 Concealment

pin 42

ACM	function
0	no
1	yes

Table 11 Mute

pin 46

AMUN	mute
0	yes
1	no

Table 12 Interrupt

pin 47

INTR	interrupt
0	no
1	yes

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	7.0	V
Input voltage range*	V_I	−0.5	V_{DD} + 0.5	V
Input current	I_I	−	± 10	mA
Output current	I_O	−	± 10	mA
Supply current in V_{SS}	I_{SS}	−	28	mA
Supply current in V_{DD}	I_{DD}	−	28	mA
Total power dissipation	P_{tot}	−	500	mW
Operating ambient temperature range	T_{amb}	−25	+85	°C
Storage temperature range	T_{stg}	−55	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling, however, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices (see Handling MOS Devices).

The PLCC-68 package can only be guaranteed with soldering temperatures up to a maximum of 235 °C.

* V_{DD} + 0.5 must not exceed 7.0 V.

DC CHARACTERISTICS

T_{amb} = 0 °C to +70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	4.5	–	5.5	V
Supply current	Fig.10	I_{DD}	–	12.5	–	mA
Quiescent supply current	note 1	I_{DDq}	–	–	50	μA
Inputs I(1)						
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Input current LOW	note 2	$-I_{IL}$	–	–	10	μA
Input current HIGH	note 2	I_{IH}	–	–	10	μA
Inputs I(2)						
Input voltage LOW		V_{IL}	–	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	–	V
Input current LOW	note 2	$-I_{IL}$	–	–	10	μA
Input current HIGH	note 2	I_{IH}	–	–	10	μA
Inputs I(3)						
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Pull down resistor		R_I	25	50	100	kΩ
Outputs O						
Output voltage LOW	$-I_{OL}$ = 1 mA	V_{OL}	–	–	0.5	V
Output voltage HIGH	I_{OH} = 1 mA	V_{OH}	4.0	–	–	V

Notes to DC characteristics

1. T_{amb} = 25 °C, all inputs at V_{SS} or V_{DD}, all outputs open.
2. At 25 °C max. 1 μA.

AC CHARACTERISTICS

T_{amb} = 0 to + 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
T20N clock pulse	Fig.3					
Pulse width HIGH		t_{WH}	15	20	–	ns
Pulse width LOW		t_{WL}	15	22	–	ns
T20N pulse period		t_{P20}	48	48.8	–	ns
Data input timing	Fig.4					
Set-up time for data SWA and SWB to T10N	note 1	t_{SWL}	–	50	–	ns
T10N pulse period T_{PSW}	note 2	t_{P10}	–	97.6	–	ns
Main frame timing	Fig.5					
Main frame sync pulse		t_{SYNC}	–	$11t_{P10}$	–	ns
Audio data timing	Fig.6					
Audio sample repetition time		t_{SAMP}	–	31.25	–	μs
Load pulse width HIGH		t_{LPH}	–	6.25	–	μs
Audio data hold		t_{ADH}	–	1	–	μs
I²S timing	Fig.7					
Frequency AWT signal		f_{AWT}	–	1.024	–	MHz
Audio sample repetition time		t_{SAMP}	–	31.25	–	μs
PI interface timing	Fig.8					
Frequency PITN signal		f_{PITN}	–	32	–	kHz
PITN pulse period		t_{PITN}	–	31.25	–	μs
PIF pulse width HIGH		t_{PIFH}	–	$22t_{PITN}$	–	μs
PIF pulse period		t_{ZI}	–	2	–	ms
Output timing Programme type interface	Fig.9					
INTR pulse period		t_{INTR}	–	250	–	μs
INTR pulse width HIGH		t_{PINH}	–	31.25	–	μs

Notes to AC characteristics

1. Due to noise, the period t_{SWL} may occasionally vary between 30 and 70 ns.
2. Due to noise, the period time t_{PSW} may occasionally vary between 77.6 and 117.6 ns.

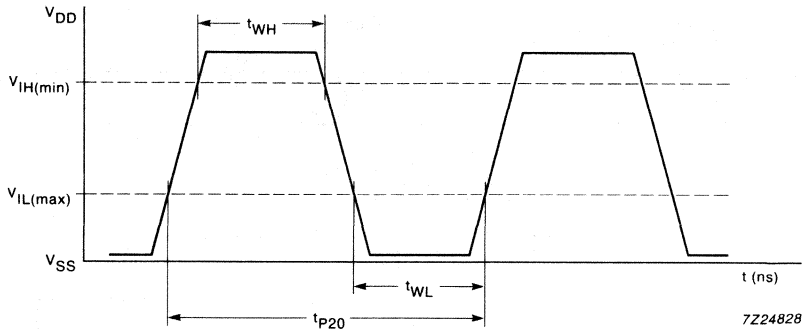


Fig.3 Waveform at clock input T20N (pin 5).

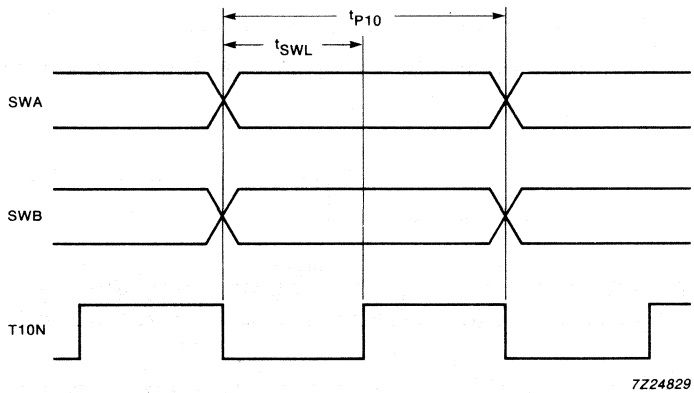


Fig.4 Data input timing (pins 59, 61 and 63).

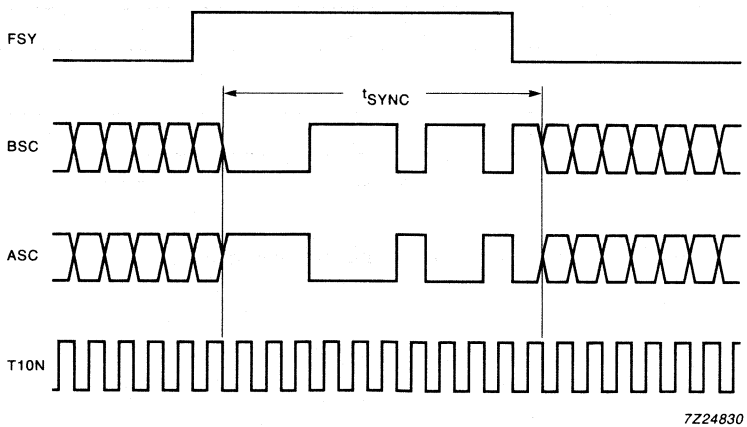


Fig.5 Output timing for 10.24 Mbit/s interface (pins 56, 57, 58 and 59).

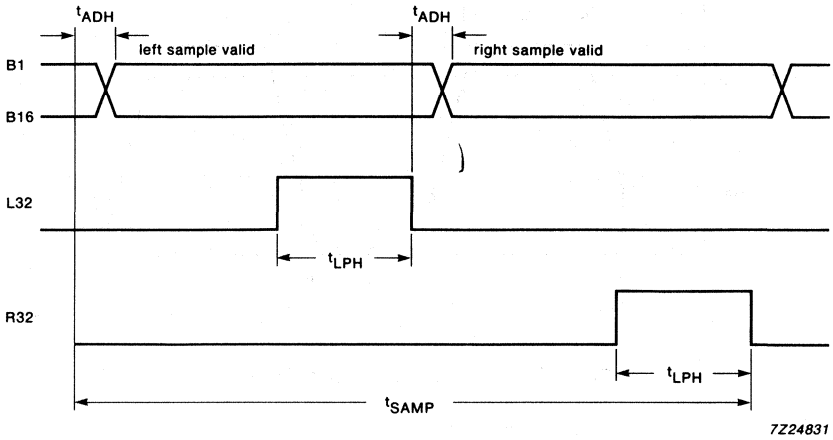


Fig.6 Audio data timing parallel out (pins 40 to 35, 33 to 24, 21 and 20).

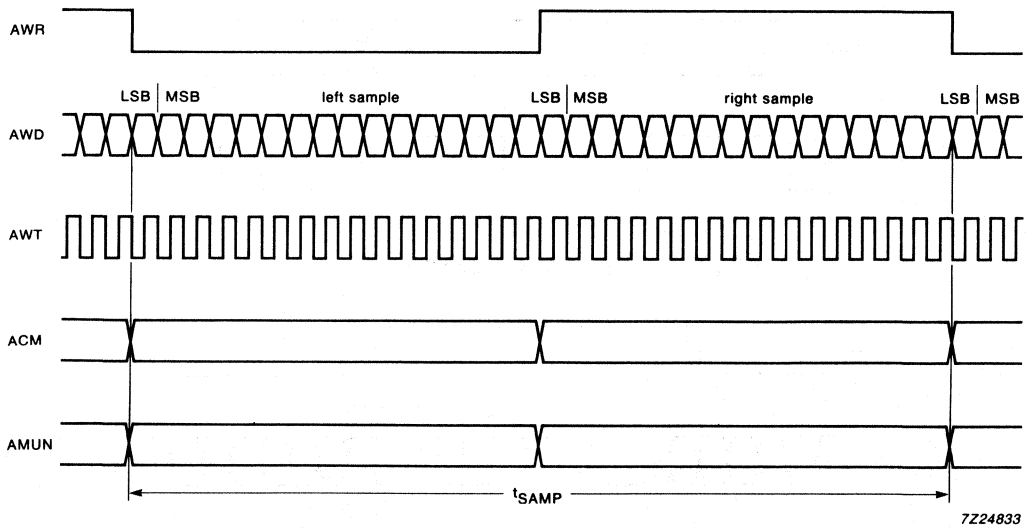


Fig.7 Inter-IC Sound (I^2S) timing and mute and interpolation flags (pins 42 to 46).

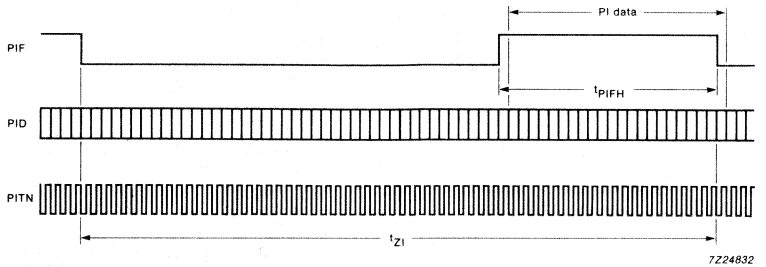
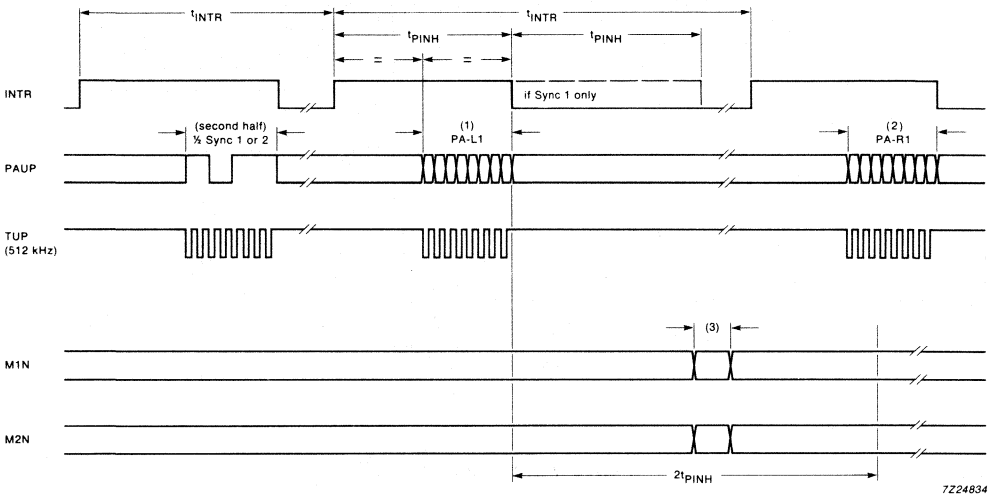


Fig.8 PI interface timing (pins 52 to 54).



(1) Programme type - left
(2) Programme type - right
(3) This time is approximately 10 μs

Fig.9 Output timing programme type interface (pins 17 to 19).

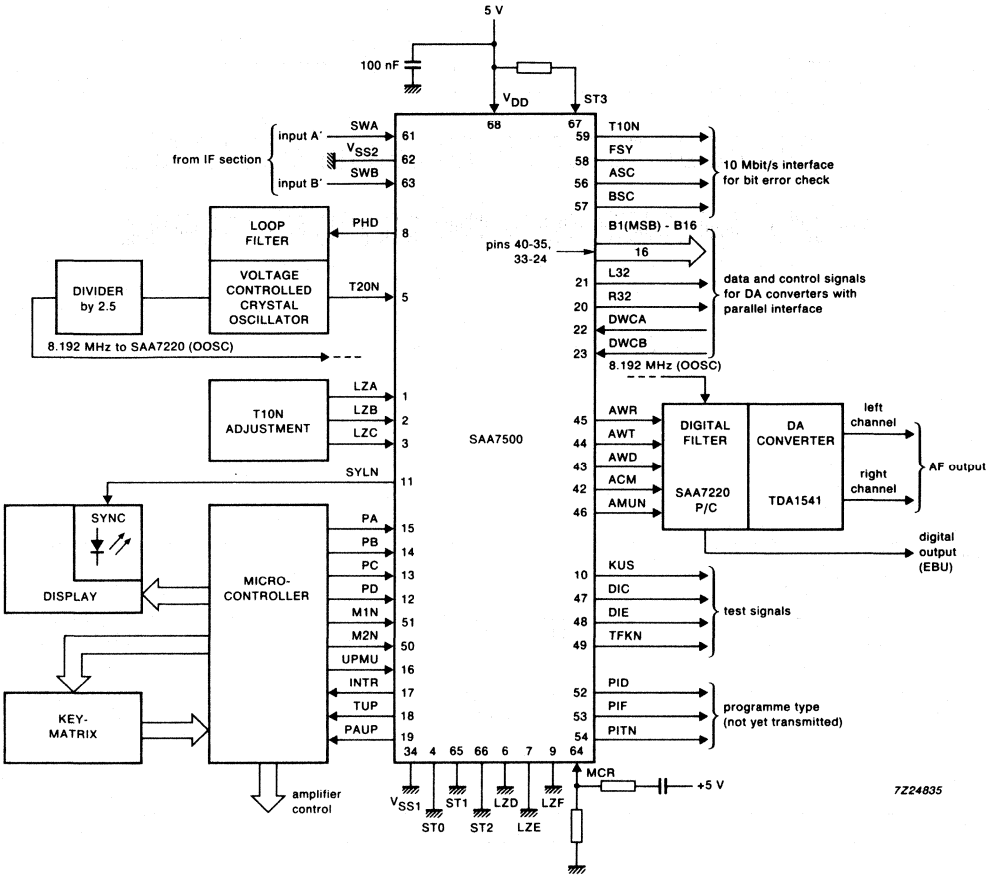


Fig.10 Application proposal.

Digital satellite radio broadcasting tuner decoder

SAA7501

FEATURES

- Clock recovery
- Differential decoding
- Main frame synchronization
- Swapping half-frames in event of inversion
- Unscrambling
- Demultiplexing
- Subframe synchronization
- Error correction and concealment
- Scale factor decoding with error correction
- Shift into the original values using the scale factors
- Mute in event of synchronization loss.

GENERAL DESCRIPTION

The SAA7501 performs a decoder function for digital satellite sound broadcasting tuners. It is designed to decode one of 16 stereo channels broadcasting audio signals in accordance with the German standard – **Technische Richtlinie ARD/ZDF No. 3R1.**

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.5	V
P_{tot}	total power dissipation	–	500	mW
f_{T20N}	clock frequency	20.48	–	MHz

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7501WP	68	PLCC	plastic	SOT188

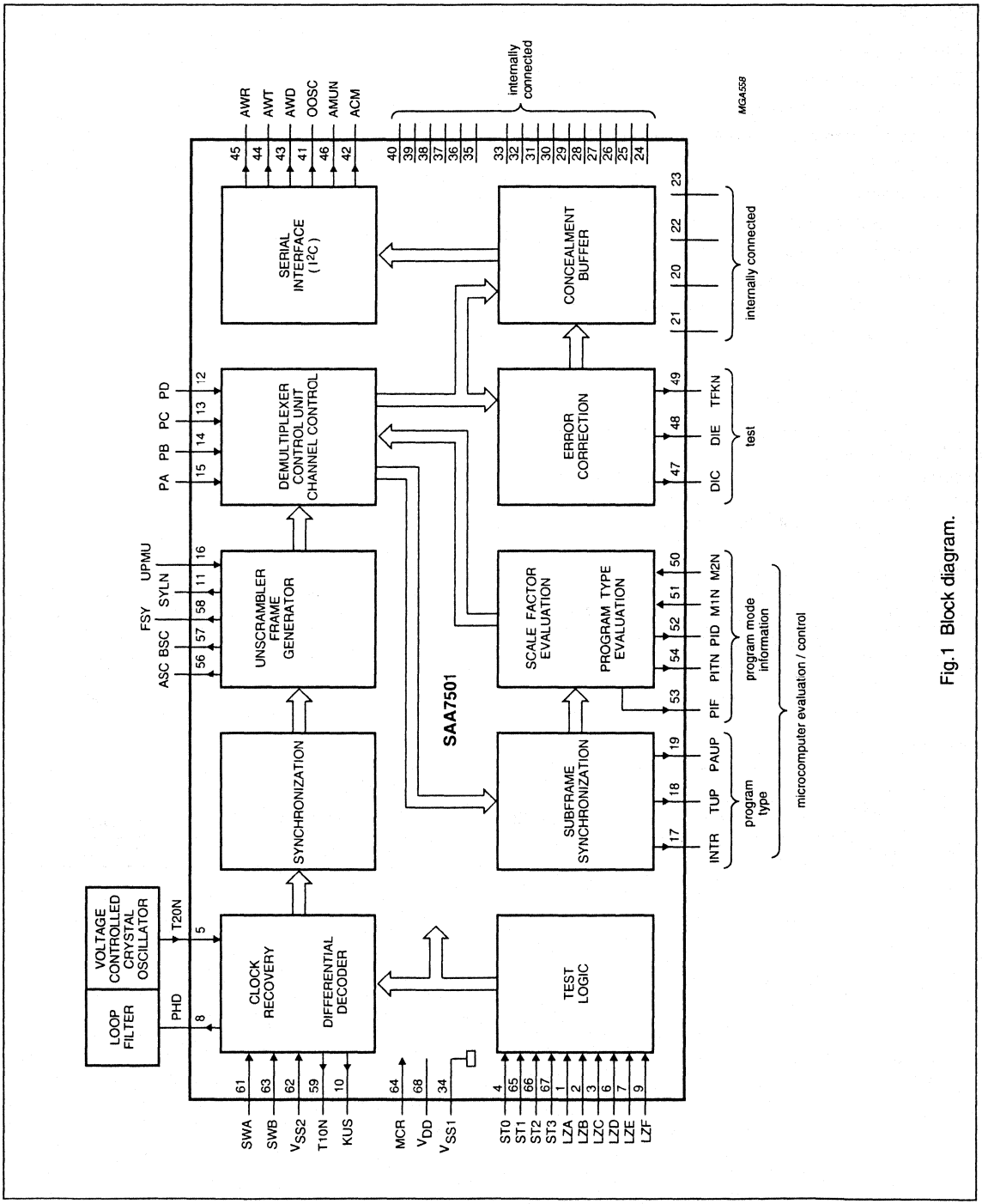


Fig.1 Block diagram.

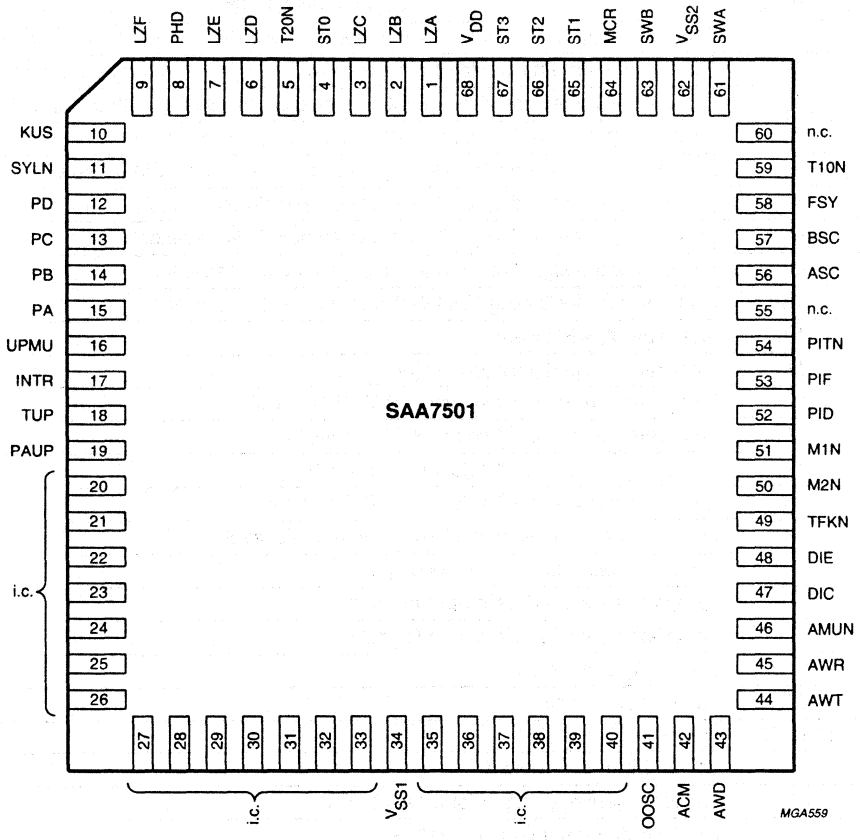


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
LZA	1	phase adjustment input for the internal clock (CMOS level with pull-down resistor)
LZB	2	phase adjustment input for the internal clock (CMOS level with pull-down resistor)
LZC	3	phase adjustment input for the internal clock (CMOS level with pull-down resistor)
ST0	4	control input for testing (CMOS level with pull-down resistor)
T20N	5	20.48 MHz clock input from voltage controlled oscillator (CMOS level)
LZD	6	control input for testing (CMOS level with pull-down resistor)
LZE	7	control input for testing (CMOS level with pull-down resistor)
PHD	8	phase control signal output for voltage controlled oscillator
LZF	9	control input for testing (CMOS level with pull-down resistor)
KUS	10	test output; A'B' swap
SYLN	11	synchronization indication flag output
PD	12	program number input selector; MSB (TTL level)
PC	13	program number input selector (TTL level)
PB	14	program number input selector (TTL level)
PA	15	program number input selector; LSB (TTL level)
UPMU	16	mute input; controlled by microcomputer (TTL level)
INTR	17	interrupt flag output for microcomputer
TUP	18	program type interface output for clock
PAUP	19	program type interface output for data
i.c.	20 to 33	internally connected
V_{SS1}	34	ground supply input
i.c.	35 to 40	internally connected
OOSC	41	4.096 MHz clock output
ACM	42	concealment flag output for SAA7220P/C
AWD	43	audio data output for SAA7220P/C
AWT	44	bit clock output for SAA7220P/C
AWR	45	word select signal output for SAA7220P/C
AMUN	46	mute signal output for SAA7220P/C
DIC	47	data output for testing
DIE	48	data output for testing
TFKN	49	burst clock output for test data
M2N	50	channel mode select input (TTL level)
M1N	51	channel mode select input (TTL level)
PID	52	program information (PI) interface output for data
PIF	53	program information (PI) interface output for window signal
PITN	54	program information (PI) interface output for clock
n.c.	55	not connected
ASC	56	data output for 10.24 Mbit/s interface
BSC	57	data output for 10.24 Mbit/s interface

SYMBOL	PIN	DESCRIPTION
FSY	58	window signal output for 10.24 Mbit/s interface
T10N	59	10.24 MHz clock output
n.c.	60	not connected
SWA	61	10.24 Mbit/s data input (TTL level)
V_{SS2}	62	screen ground input
SWB	63	10.24 Mbit/s data input (TTL level)
MCR	64	master reset input (CMOS level)
ST1	65	control input for testing (CMOS level with pull-down resistor)
ST2	66	control input for testing (CMOS level with pull-down resistor)
ST3	67	control input for testing and mode select for 10.24 Mbit/s interface (CMOS level with pull-down resistor)
V_{DD}	68	power supply input

FUNCTIONAL DESCRIPTION

General

The SAA7501 has been designed to decode 16 stereo channel sound broadcasting signals in accordance with the German standard – **Technische Richtlinie ARD/ZDF No. 3R1.** The channel carrying the sound broadcast program is selected and converted into an intermediate frequency by a front end. The signal is then amplified and demodulated {4 PSK (Phase Shift Keying) with carrier recovery}. The outputs from the demodulator are two differential coded signals that are input to the SAA7501. The SAA7501 decoder outputs the audio data, of the selected stereo or mono channel, as linear quantized 16-bit audio samples.

Selection of the desired audio channel, and stereo or mono mode, is controlled by inputs PA, PB, PC and PD. These inputs may be driven directly by switches or controlled by a microcomputer.

When under the control of a microcomputer, the SAA7501 transmits serial data to the microcomputer on the type of program (16 stereo or 32 mono). The corresponding synchronization of the subframe is partly performed by the SAA7501 (every 2 ms) and at a higher level by the microcomputer (every 16 ms). The SAA7501 also sends to the microcomputer, program information code data together with its clock and window signal.

The circuit automatically performs the system error correction and concealment. In the transmit error rate range of 0 to 3×10^{-3} a theoretical C/N (carrier-to-noise ratio) gain of approximately 6 dB is obtained. The residual error rate is almost zero for transmit error rates $\leq 3 \times 10^{-4}$.

The remaining functions, such as clock recovery, main and subframe synchronization and scale factor decoding, are protected in a similar manner so that they will not influence the residual error rate.

Clock recovery

The baseband signals A' and B' are connected to the SWA and SWB inputs of the SAA7501. For clock recovery, the phase of the incoming data streams is compared with T10N (half the oscillator frequency). The output of the phase comparator (PHD) controls, by means of the loop filter, the voltage controlled oscillator (both are external to the IC) and thus its output signal T20N.

For energy dispersal, for example, in modulation pauses or with constant signals, the data streams are scrambled during generation. The exceptions are the synchronization words and the special service bits. In order that the phase correspondence between the recovered system clock (T10N) and the input signals A' and B' can be adjusted to a minimum bit error rate (BER), a programmable phase shifter is provided (inputs LZA, LZB, LZC and ST3).

The differential decoder logic delivers the original data streams which may be exchanged depending on the number of mixer stages on the transmission channel. The polarity of the two synchronization words will indicate if this is necessary, if so the two data streams will be automatically switched over.

Synchronization

Using the synchronization circuit, the incoming data streams are first searched for 11-bit Barker code words. The synchronization circuit permits two errors for both synchronization words, which guards against failure of the synchronization word. If the synchronization word has been detected, the following data is examined at frame length intervals to see if the synchronization word is repeated. If it is repeated, it is acknowledged as a synchronization word (window check) and an internal frame pulse generator takes over further control. There is also a synchronization word failure control which initiates a renewed synchronization word search and mutes the AF output if four successive synchronization word failures occur.

To enhance the performance the result from the error correction circuit is used as an additional input to the synchronization circuit. This is to avoid extra errors through synchronization loss in the event of relative high, but for reception acceptable, bit error rates. This will not affect the rapid detection of a very high bit error rate or the non-synchronization of the data stream. The decoder will function correctly with a bit error rate up to 3×10^{-3}.

Demultiplexer

After synchronization, the beginning of a frame is marked and the digital signals are defined as to their assignment. First the non-scrambled special service bit from the half-frame A is taken out. The rest of both half-frames are unscrambled and demultiplexed so that each half-frame is split into two substreams with a rate of 5.12 Mbit/s (see Technische Richtlinie ARD/ZDF Nr. 3R1, main frame specification). Using the inputs from the synchronization circuit and the program selector (inputs

PA, PB, PC and PD) the demultiplexer locks on to the selected program block and generates all the control signals required for further signal processing.

Error correction

The error correction circuit provides for exact identification of two errors in a 63/44 BCH block and correction of the incorrect bits. In the event of more than two errors the identification circuit can identify incorrect BCH blocks with up to five errors.

The BCH block is operated on by a syndrome calculator, the result controls the lines of an error correction matrix. The output of this matrix corrects (inverts) the incorrect bits when data is shifted out from its buffer. The BCH block is then fed through a second syndrome calculator. In the event of more than two errors the result of the whole calculation will be other than zero. This information provides the concealment in the next stages.

The two adjacent samples related to the detected incorrect sample are added and divided by two, the result replaces the incorrect sample (interpolation). In the event of successive bad samples the last corrected sample is held until a good sample is detected (hold function). A high error frequency in the event of synchronization loss will activate the muting function and set the output data to zero.

This information, if concealment is not active, is used in the synchronization circuit as described in that section. When the samples are correct it can be assumed that the synchronization is also correct.

Scale factor, program type evaluation and shift function

The transmitted samples are returned to their original range of values by the scale factor, which is obtained by decoding the ZI-subframe. The start of this frame is coupled to the start of the special services frame, synchronization for this frame uses the same principle as for the main frame. In the scale factor evaluation unit the BCH 14/6 code words (transmitted three times) are fed into a majority selection circuit operating at bit level. Subsequently the error check and the correction of a maximum of two errors is carried out.

The SAA7501 contains the synchronization word detection and error check for the subframe synchronization word with its repetition time of 2 ms. The program type evaluation with its superior synchronization has to be performed external to the chip, for example, by a microcomputer. For this purpose data is available in 8-bit blocks at a serial interface (INTR, PAUP and TUP; block rate = 4000/s). The same microcomputer can also perform the program selection (inputs PA, PB, PC and PD).

At the input to the concealment buffer the corrected 11 bits (MSB) are combined with the 3 unprotected transmitted bits (LSB). The scale factor determines the required shift-back operations required to convert the transmitted values back into the original values. Voids that occur are filled with noughts or ones corresponding to the sign bit. The shift-back and filling of voids ensures that no incorrect bits occur above the range defined by the scale factor. The upper 16 bits represent the regenerated audio sample.

Digital-to-analog conversion and interfaces

The SAA7501 enables different DAC systems to be used. For control of the SAA7220P/C and TDA1541 a 2.5 external divider must be connected to the 20.48 MHz clock signal to produce the required 8.192 MHz clock signal.

A serial interface is built in with the following outputs: bit clock (AWT), word select (AWR) and audio data (AWD). In addition the mute signal (AMUN) and the concealment flag (ACM) are also available. The SAA7220P/C and TDA1541 are equipped with a digital audio interface for domestic use equivalent to 'IEC proposal No. 84 (secretariat 28; from June 1985)'.

Additional information, including the scale factor is available through the program information (PI) interface (PID, PITN and PIF). Another interface, using the ASC, BSC and T10N outputs, makes available signals from the differential decoder. These signals are used for bit error measurement and an optimized phase adjustment of the internal clock (refer to **Clock recovery** section).

An optional application of the control signals for mute and concealment operations is possible using the outputs AMUN and ACM. For the mute signal a different time relationship to the unwanted pulse with very low C/N values may be obtained.

The external application of the concealment signal is recommended; if an additional interpolation is required between additional samples with different levels in the external circuitry (such as the SAA7220P/C).

Truth tables

Table 1 Delay adjustment (pins 1 to 3).

LZC	LZB	LZA	DELAY
0	0	0	4 x τ
0	0	1	3 x τ
0	1	0	2 x τ
0	1	1	1 x τ
1	0	0	0 x τ
1	0	1	−1 x τ
1	1	0	−2 x τ
1	1	1	−3 x τ

Where: $\tau \approx$ 1.5 x gate delay time (NAND).

Table 2 Master reset (pin 64).

MCR	FUNCTION
0	operation
1	master reset

Table 3 Mute (pin 16).

UPMU	FUNCTION
0	no
1	yes

Table 4 Program number (pins 12 to 15).

PD	PC	PB	PA	PROGRAM NUMBER
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
.	.	.	.	.
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

Table 5 Phase control signal (pin 8).

PHD	PHASE
0	lead phase
1	lag phase

Table 6 Synchronization indication (pin 11).

SYLN	SYNCHRONIZATION
0	yes
1	no

Table 7 Mode select for data outputs ASC and BSC for 10.24 Mbit/s interface (pin 67).

ST3	DATA ASC/BSC
0	after unscrambler
1	before unscrambler

Table 8 Channel mode select (pins 50 and 51).

M2N	M1N	CHANNEL MODE
0	0	mono (1 + 2)
0	1	mono R (2)
1	0	mono L (1)
1	1	stereo

Table 9 Concealment (pin 42).

ACM	FUNCTION
0	no
1	yes

Table 10 Mute (pin 46)

AMUN	MUTE
0	yes
1	no

Table 11 Interrupt (pin 47)

INTR	INTERRUPT
0	no
1	yes

LIMITING VALUES

In accordance with the Absolute Rating Maximum System (IEC134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	7.0	V
V_I	input voltage (note 1)	−0.5	V_{DD} +0.5	V
I_I	input current	–	±10	mA
I_O	output current	–	±10	mA
I_{SS}	supply current in V_{SS}	–	28	mA
I_{DD}	supply current in V_{DD}	–	28	mA
P_{tot}	total power dissipation	–	500	mW
T_{amb}	operating ambient temperature	−25	+85	°C
T_{stg}	storage temperature	−55	+150	°C

Note

1. V_{DD} +0.5 must not exceed 7 V.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling, however, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices (see Handling MOS Devices).

The PLCC-68 package can only be guaranteed with soldering temperatures up to a maximum of 235 °C.

DC CHARACTERISTICS

T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		4.5	–	5.5	V
I_{DD}	supply current		–	12.5	–	mA
I_{DDq}	quiescent supply current	note 1	–	–	50	µA
Inputs (CMOS level)						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_{IL}	LOW level input current	note 2	–	–	–10	µA
I_{IH}	HIGH level input current	note 2	–	–	10	µA
Inputs (TTL level)						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2	–	–	V
I_{IL}	LOW level input current	note 2	–	–	–10	µA
I_{IH}	HIGH level input current	note 2	–	–	10	µA
Inputs (CMOS level with pull-down resistor)						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
R_I	pull-down resistor		25	50	100	kΩ
Outputs						
V_{OL}	LOW level output voltage	I_{OL} = –1 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = 1 mA	4.0	–	–	V

Notes

1. T_{amb} = 25 °c; all inputs at V_{SS} or V_{DD}; all outputs open-circuit.
2. At 25 °C maximum 1 µA.

AC CHARACTERISTICS

T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T20N clock pulse (see Fig.3)						
t_{WH}	pulse width HIGH		15	20	–	ns
t_{WL}	pulse width LOW		15	22	–	ns
t_{P20}	T20N pulse period		48	48.8	–	ns
Data input timing (see Fig.4)						
t_{SWL}	set-up time for data SWA and SWB to T10N	note 1	–	50	–	ns
t_{P10}	T10N pulse period t_{PSW}	note 2	–	97.6	–	ns
Main frame timing (see Fig.5)						
t_{SYNC}	main frame sync pulse		–	$11t_{P10}$	–	ns
I²S timing (see Fig.6)						
f_{AWT}	frequency AWT signal		–	1.024	–	MHz
t_{SAMP}	audio sample repetition time		–	31.25	–	µs
PI interface timing (see Fig.7)						
f_{PITN}	frequency PTIN signal		–	32	–	kHz
t_{PITN}	PTIN pulse period		–	31.25	–	µs
t_{PIFH}	PIF pulse width HIGH		–	$22t_{PITN}$	–	µs
t_{ZI}	PIF pulse period		–	2	–	ms
Output timing Program type interface (see Fig.8)						
t_{INTR}	INTR pulse period		–	250	–	µs
t_{PINH}	INTR pulse width HIGH		–	31.25	–	µs

Notes

1. Due to noise, the period t_{SWL} may occasionally vary between 30 and 70 ns.
2. Due to noise, the period t_{PSW} may occasionally vary between 77.6 and 117.6 ns.

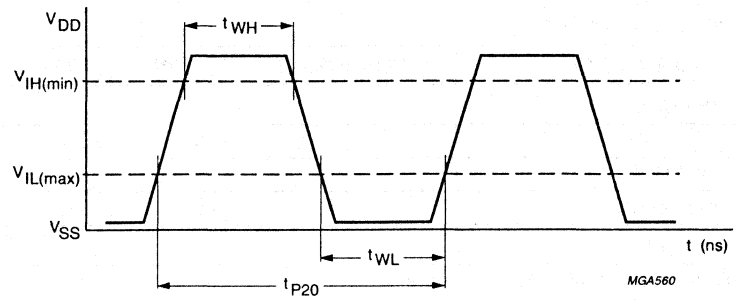


Fig.3 Waveform at clock input T20N (pin 5).

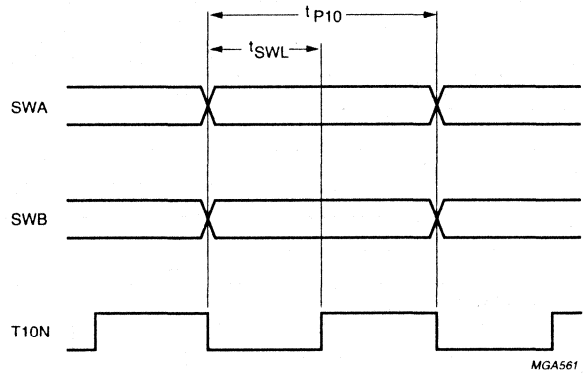


Fig.4 Data input timing (pins 59, 61 and 63).

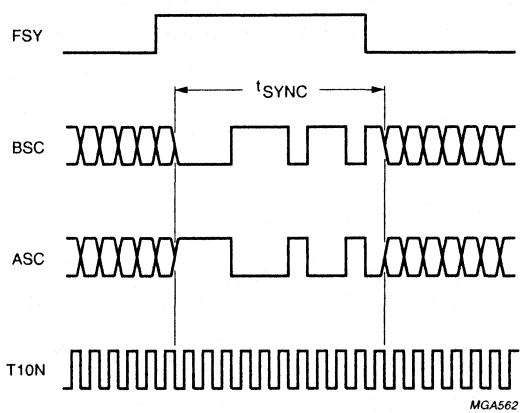


Fig.5 Output timing for 10.24 Mbit/s interface (pins 56, 57, 58 and 59).

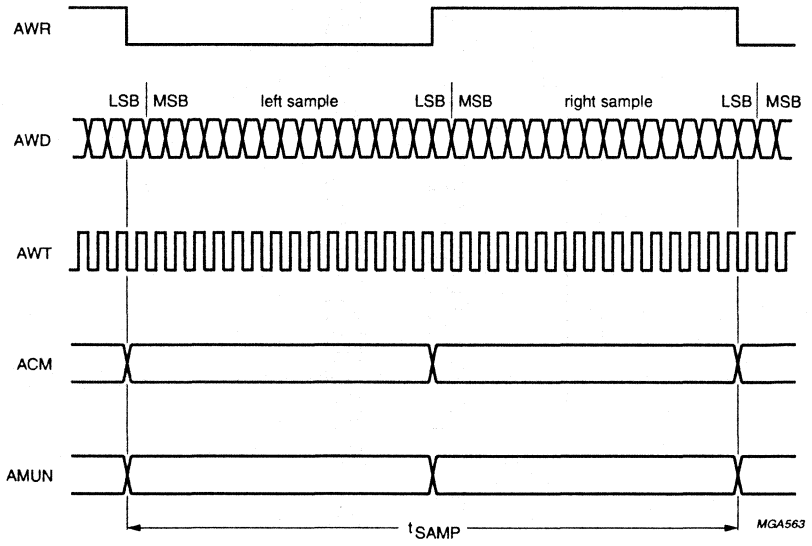


Fig.6 Inter-IC Sound (I²S) timing and mute and interpolation flags (pins 42 to 46).

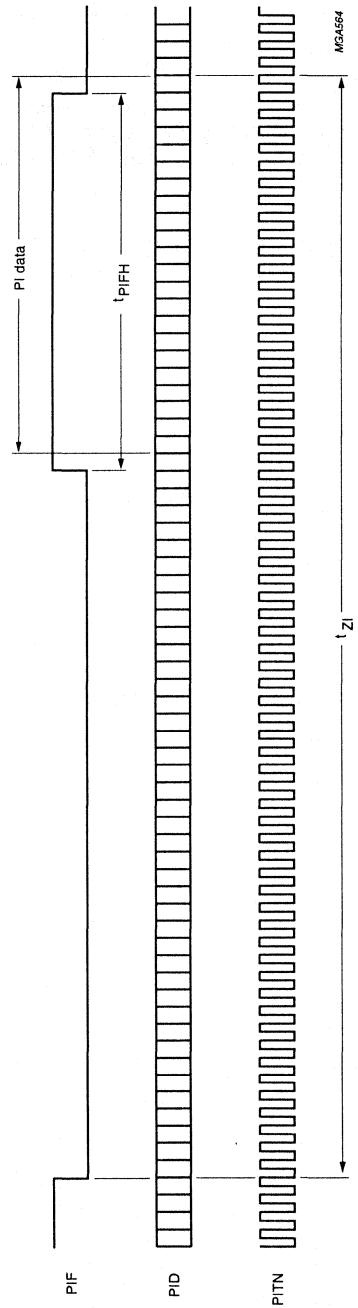
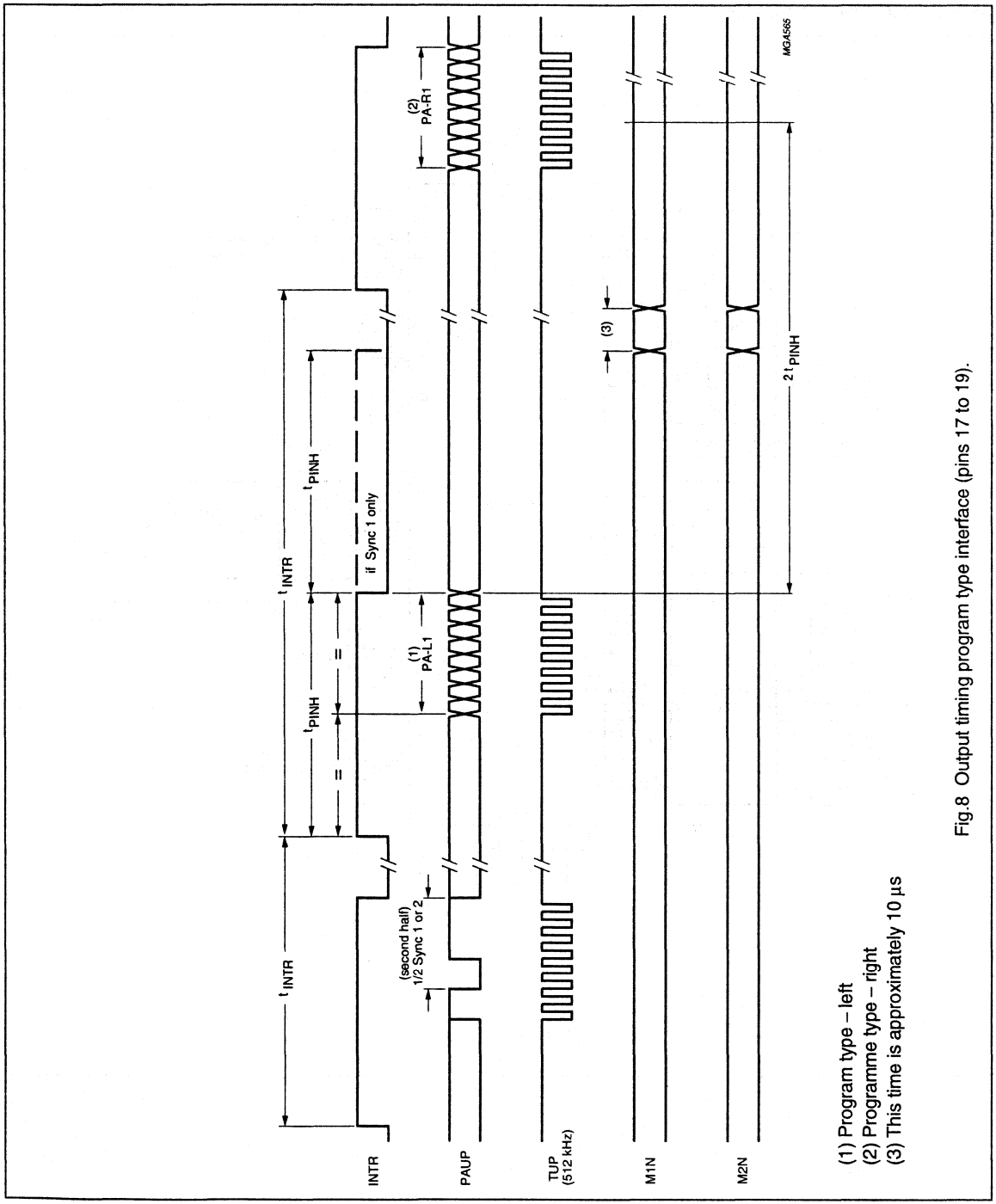


Fig.7 PI interface timing (pins 52 to 54).



(1) Program type – left
(2) Programme type – right
(3) This time is approximately 10 µs

Fig.8 Output timing program type interface (pins 17 to 19).

APPLICATION INFORMATION

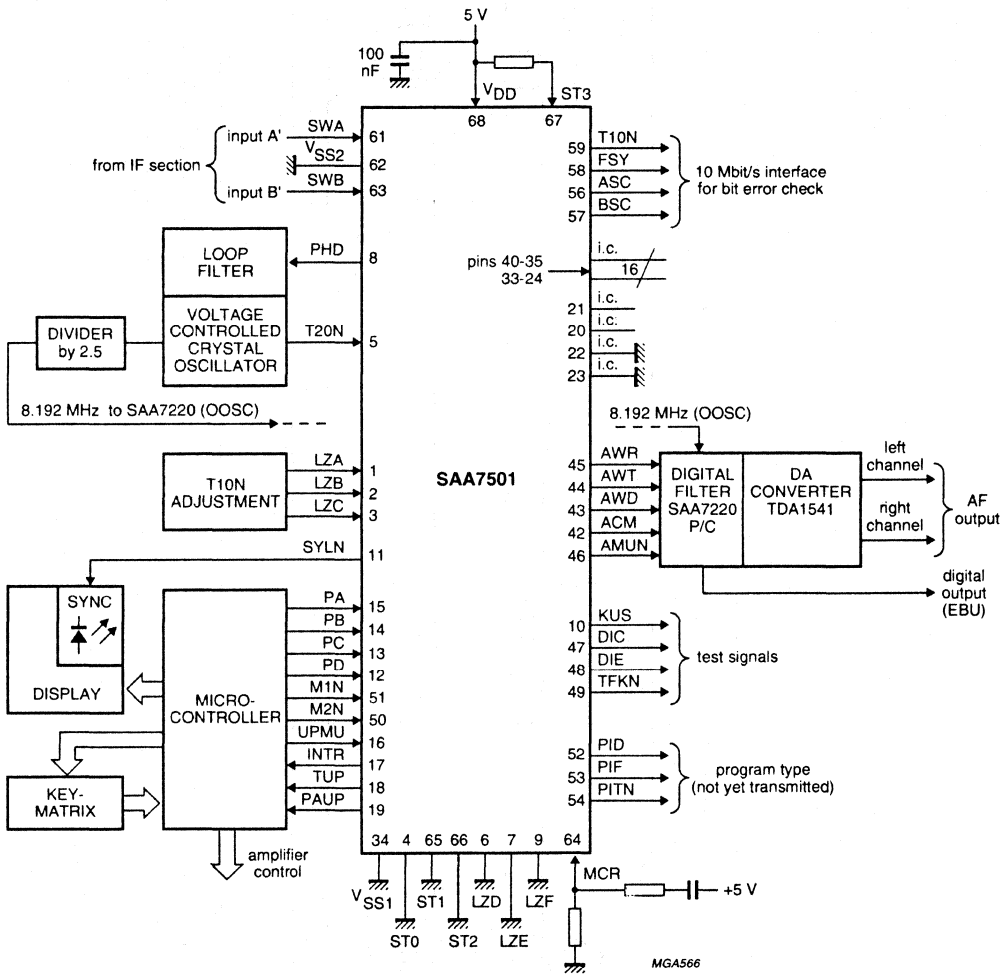


Fig.9 Application diagram.

Digital audio processing IC (DAPIC) SAA7740H

FEATURES

Hardware

- Two digital inputs and two digital outputs in the I²S-bus format (i.e. 4 audio channels)
- Independent input/output interfaces
- Slave input/output interfaces
- Slave processing
- I²C-bus microcontroller interface
- DC filtering at the inputs
- One programmable 2nd-order digital filter unit
- Two multiply accumulate processor units (24 × 16-bit/MAC)
- DRAM interface and address computation unit for external delay lines
- On-chip coefficient and external delay line address storage
- Hardware controlled soft mute via the MUTE pin
- Hardware controlled soft demute via the RESET pin.
- Operating ambient temperature; −40 to +85 °C

Software

- 5-band parametric equalizer with selectable centre frequency, slope setting and boost/cut gain settings from −12 to +12 dB
- Stereo width control from mono to stereo to spatial stereo
- Stereo Hall-effects for field acoustics, such as concert halls, with 8 coefficients and 8 delayed taps per channel
- External delay line processing for delays up to 1 second
- Reverberation with selectable reverberation time (up to 5 seconds) and energy
- Three different surround sound programs to obtain a spatial effect on 4 loudspeakers
- Passive DOLBY surround processing with the addition of an external dynamic noise reduction IC
- Karaoke processing
- Dual 16th-order correction filtering
- Quad 8th-order correction filtering
- Digital volume and balance control
- Soft controlled soft mute/demute via the microcontroller interface
- Input switching matrix
- Output rear and front switching matrix.

APPLICATIONS

- Digital amplifiers
- Audio combination sets
- Car audio systems
- TV audio channels.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DD(tot)}$	total DC supply voltage	all V_{DD} pins	4.5	5.0	5.5	V
$I_{DD(tot)}$	total DC supply current	f_{xtal} = 16.9344 MHz	–	60	–	mA
f_{xtal}	input crystal frequency		12.288	16.9344	21.7	MHz
P_{tot}	total power dissipation	f_{xtal} = 16.9344 MHz	–	0.3	–	W
T_{amb}	operating ambient temperature		−40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7740H	QFP64[1]	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the "*Quality Reference Handbook*" (order number 9398 510 63011) are followed.

BLOCK DIAGRAM

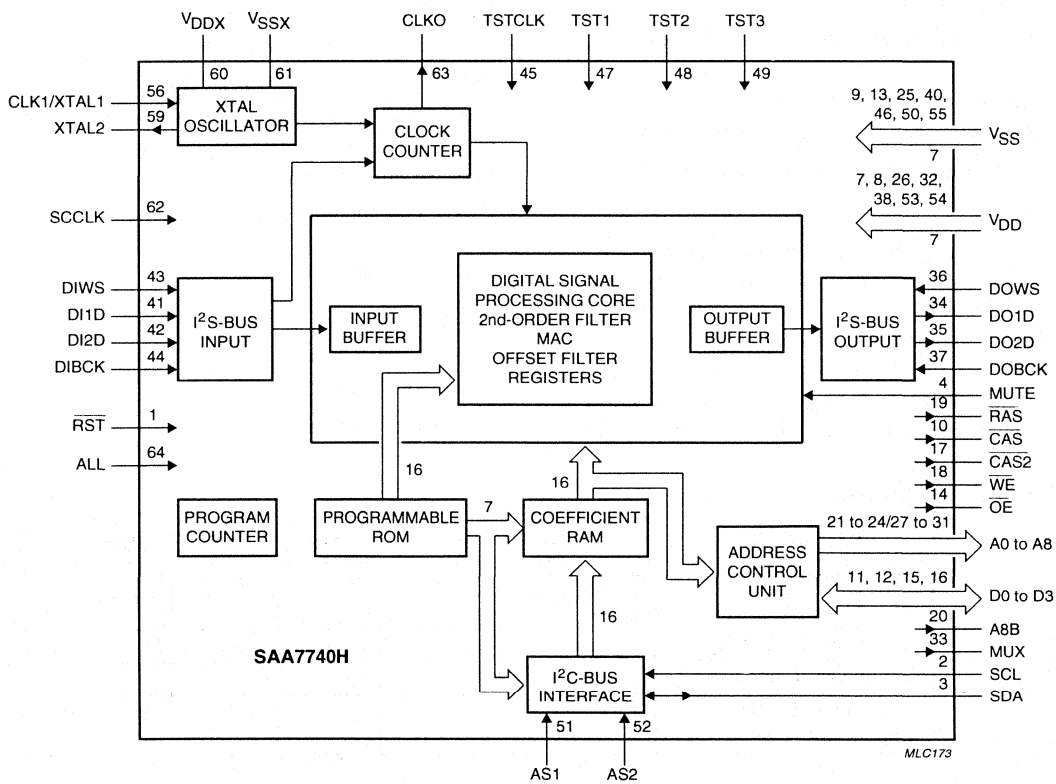


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{RST}$	1	reset input (active LOW)
SCL	2	serial clock input (I^2C-bus)
SDA	3	serial data input/output (I^2C-bus)
MUTE	4	mute input (active HIGH)
n.c.	5	not connected
n.c.	6	not connected
V_{DD}	7	supply voltage
V_{DD}	8	supply voltage
V_{SS}	9	ground supply
$\overline{CAS}$	10	column address strobe (DRAM) (active LOW)
D0	11	input/output data bus line 0 (DRAM)
D1	12	input/output data bus line 1 (DRAM)
V_{SS}	13	ground supply
$\overline{OE}$	14	output buffer enable (DRAM) (active LOW)
D2	15	input/output data bus line 2 (DRAM)
D3	16	input/output data bus line 3 (DRAM)
$\overline{CAS2}$	17	second column address strobe (active LOW)
$\overline{WE}$	18	write enable (DRAM) (active LOW)
$\overline{RAS}$	19	row address strobe (DRAM) (active LOW)
A8B	20	inverse MSB address line output (DRAM)
A8	21	address line output 8 (DRAM)
A7	22	address line output 7 (DRAM)
A6	23	address line output 6 (DRAM)
A5	24	address line output 5 (DRAM)
V_{SS}	25	ground supply
V_{DD}	26	supply voltage
A4	27	address line output 4 (DRAM)
A3	28	address line output 3 (DRAM)
A2	29	address line output 2 (DRAM)
A1	30	address line output 1 (DRAM)
A0	31	address line output 0 (DRAM)
V_{DD}	32	supply voltage
MUX	33	address latch strobe output (SRAM)

SYMBOL	PIN	DESCRIPTION
DO1D	34	digital audio output 1 (I^2S-bus)
DO2D	35	digital audio output 2 (I^2S-bus)
DOWS	36	digital audio input word select
DOBCK	37	digital audio input serial bit clock
V_{DD}	38	supply voltage
n.c.	39	not connected
V_{SS}	40	ground supply
DI1D	41	digital audio input 1 (I^2S-bus)
DI2D	42	digital audio input 2 (I^2S-bus)
DIWS	43	digital audio input word select
DIBCK	44	digital audio input serial bit clock
TSTCLK	45	clock input for test mode (should be tied LOW)
V_{SS}	46	ground supply
TST1	47	test pin input 1 (should be tied LOW)
TST2	48	test pin input 2 (should be tied LOW)
TST3	49	test pin input 3 (should be tied LOW)
V_{SS}	50	ground supply
AS1	51	address select input 1 (I^2C-bus)
AS2	52	address select input 2 (I^2C-bus)
V_{DD}	53	supply voltage
V_{DD}	54	supply voltage
V_{SS}	55	ground supply
CLK1/XT AL1	56	clock or crystal input
n.c.	57	not connected
n.c.	58	not connected
XTAL2	59	crystal output 2
V_{DDX}	60	crystal supply voltage
V_{SSX}	61	crystal ground supply
SCCLK	62	scan test clock input (should be tied LOW)
CLKO	63	clock signal output
ALL	64	mode select input (should be tied HIGH)

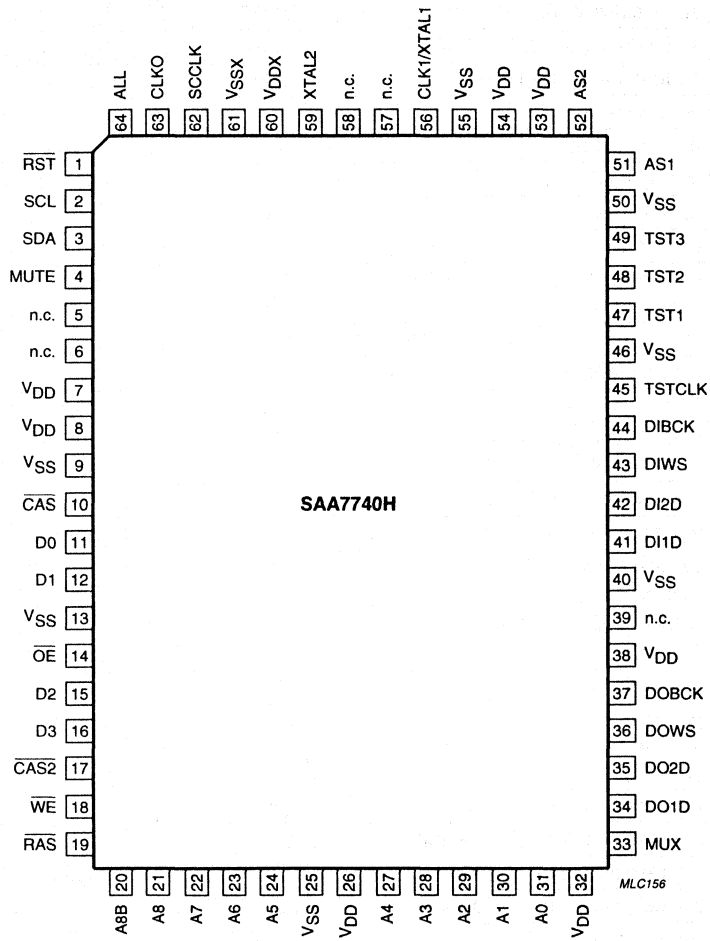


Fig.2 Pinning diagram.

GENERAL DESCRIPTION

The SAA7740H is a function-specific digital signal processor. The device is capable of performing processing for listening-environments such as equalization, hall-effects, reverberation, surround-sound and digital volume/balance control. The SAA7740H can also be reconfigured (in a dual and quad filter mode) so that it can be used as a digital filter with programmable characteristics.

For reasons of silicon efficiency, the SAA7740H realises most functions directly in hardware. The flexibility exists in the possibility to download function parameters, correction coefficients and various configurations from a host microcontroller (see Fig.1). The parameters can be passed in real time and all functions can be switched on simultaneously.

The communication with a host microcontroller conforms with the standard I^2C-bus format. The SAA7740H accepts 2 digital stereo signals in the I^2S-bus format at audio sampling frequency (f_{as}) and provides 2 digital stereo outputs.

Mode description

The SAA7740H can be set in four basic modes of operation.

GENERAL DAPIC MODE

In the general DAPIC mode two variants are available (see Figs 3 and 4). In this mode the DAPIC accepts 2 stereo input signals. DC filtering is performed on the inputs before further processing. On one of the stereo inputs a 5-band graphic equalization can be performed. The stereo image of this signal can be controlled from mono to stereo.

In the first variant (see Fig.3) a stereo hall-effect can be added to the signal by means of direct reflections. In the second variant (see Fig.4) a reverberation effect can be added to the signal by means of exponential decaying reflections. Surround-sound can then be created for the rear loudspeakers. The surround-sound module is also able to provide karaoke.

The surround-sound module accepts the second stereo input, a microphone signal can be added via the 5-band equalizer. At the output, each of the 4 channels can be individually delayed via the external DRAM. The interfacing and addressing of the DRAM is performed by the DAPIC.

The applications for the general mode are digital amplifiers, audio combination sets and TV audio channels.

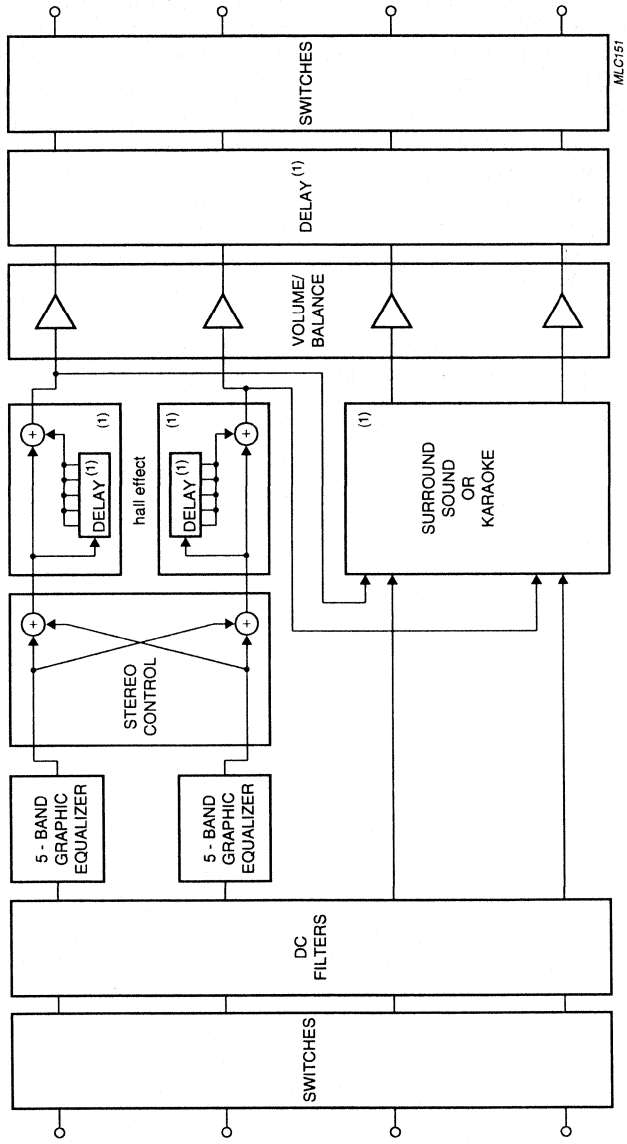


Fig.3 General DAPIC mode with hall-effect.

(1) External DRAM.

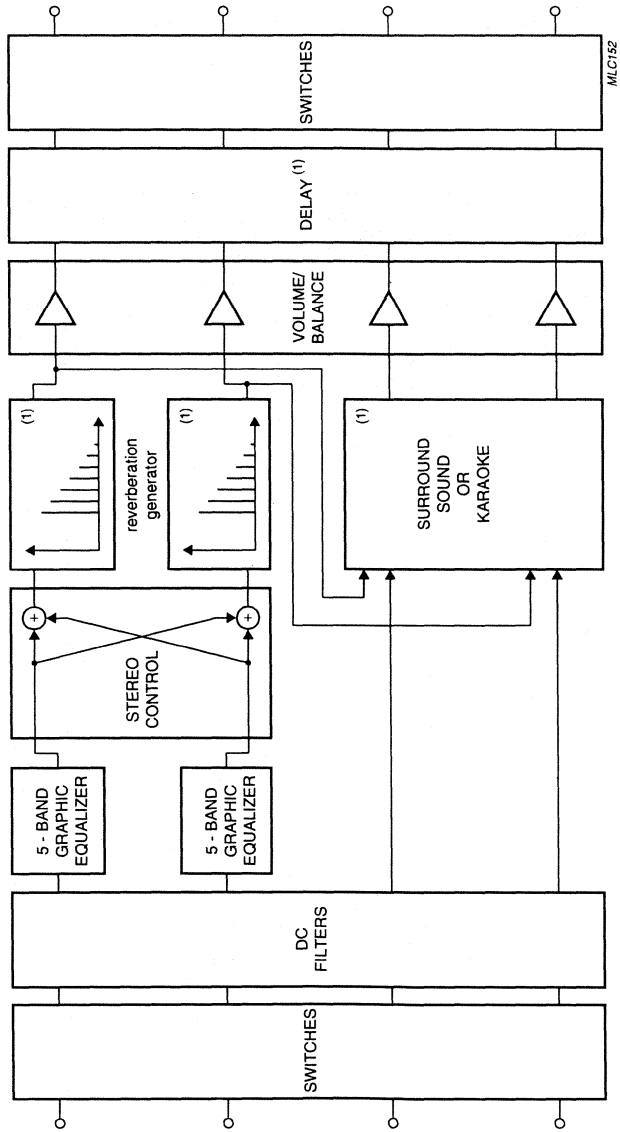


Fig.4 General DAPIC mode with reverberation.

(1) External DRAM.

DUAL-FILTER MODE

In the dual-filter mode one mono signal is accepted (see Fig.5.) The input can be selected from either one of the 2 stereo inputs (from the left or right input channel). DC filtering is performed at the input before further processing. Two separate corrections, in parallel, can be performed by means of an 8-band graphic equalizer. 16 poles and 16 zeros can be selected arbitrarily from the Z-domain. At the output, one of the channels can be delayed internally by the DAPIC. The two corrected outputs can be added to either one of the two stereo outputs.

The application for this mode is in loudspeaker correction.

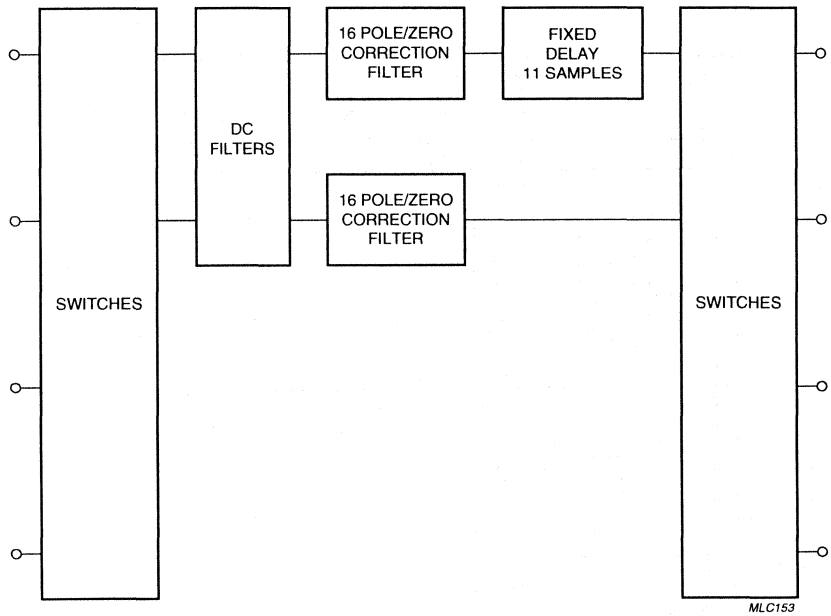


Fig.5 Dual filter mode.

QUAD-FILTER MODE

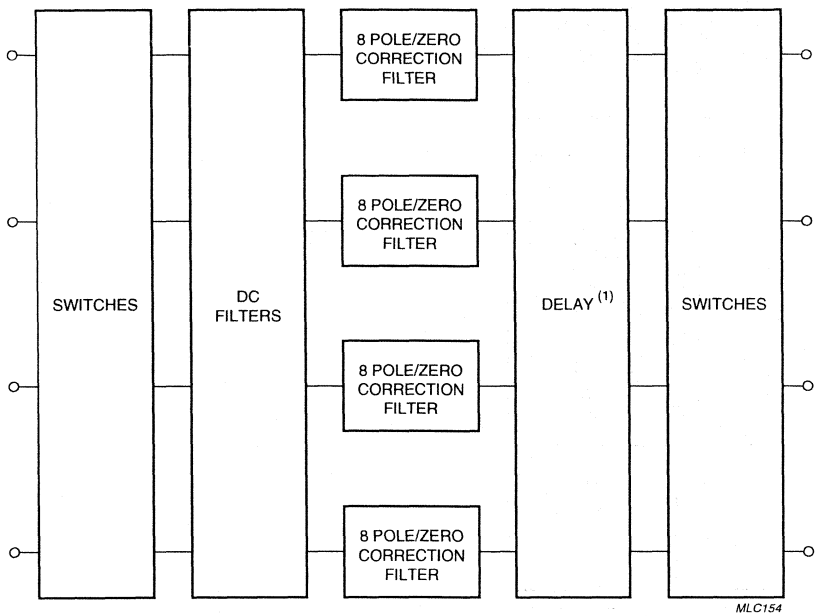
In the quad-filter mode two stereo signals are accepted (see Fig.6). DC filtering is performed at the inputs before further processing. A correction can be performed on the input signals using a 4-band graphic equalizer, i.e. 8 poles and 8 zeros can be placed arbitrarily in the Z-domain. At the output, different delays can be applied to the 4 channels via the external DRAM. The interfacing and addressing of the DRAM is performed by the DAPIC.

The application for this mode is in 4-channel correction applications such as car and home audio systems.

STEREO EXPANSION MODE

In the stereo expansion mode one stereo signal is accepted (see Fig.7). DC filtering is performed at the inputs before further processing. A 4-band graphic equalization is first performed after which a complex stereo expansion is applied. A room effect can be added by the addition of early reflections.

The applications for this mode are in the headphone out-of-head and incredible stereo applications.



(1) External DRAM.

Fig.6 Quad filter mode.

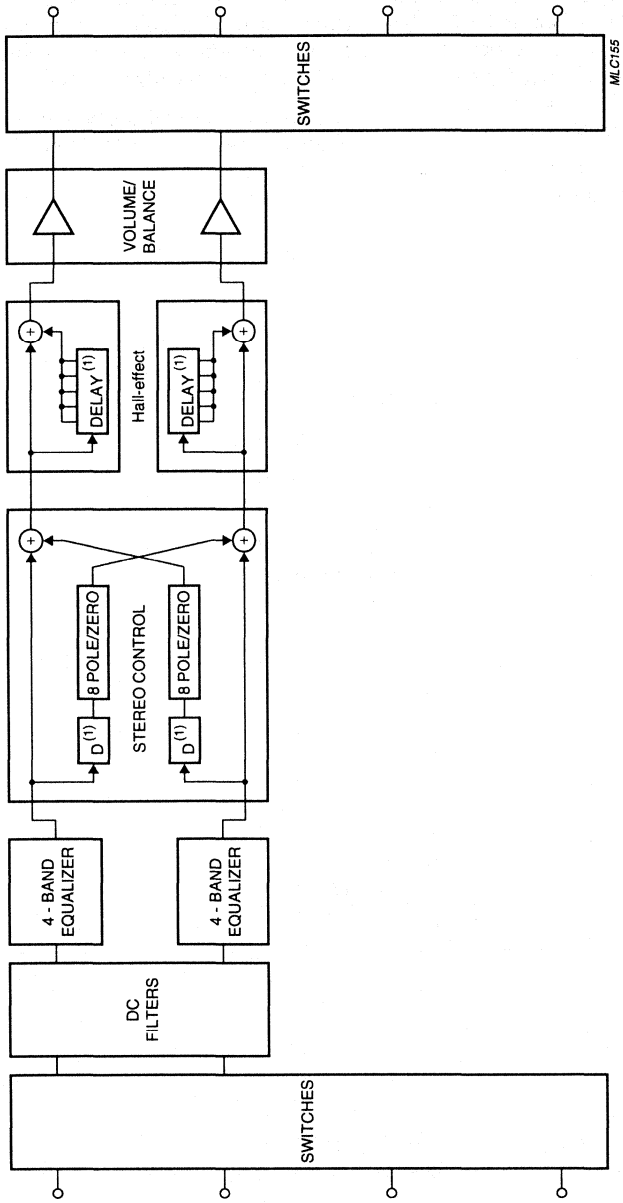


Fig.7 Stereo expansion mode.

(1) External DRAM.

FUNCTIONAL DESCRIPTION

The SAA7740H is used as a slave device. The internal operation is automatically synchronized with the word select clock of the incoming data (I^2S-bus format). Within an input frame of data, at f_{as}, 384 clock cycles are needed to compute a stereo output sample. The external clock therefore, should be minimum $384f_{as}$. External clocks which generate more than 384 clocks cycles will cause the processor to return to a wait state.

The external clock can be either a crystal connected directly to the DAPIC, or any clock generated in the system which contains DAPIC.

The I^2S-bus

Two I^2S-bus inputs and outputs are available on the DAPIC. The serial clock (DIBCK and DOBCK) and the word select (DIWS and DOWS) are applied from an external source. The two inputs and outputs are fully synchronized. However, the inputs do not have to be synchronized with the outputs. The clock and word select signals can be separated at the input and output.

The input and output buses support word lengths in accordance with the I^2S-bus standard. Up to 20 significant bits can be read by the DAPIC. Zeros will be added at the LSB position should less than 20 bits be applied. If more than 20 bits are applied the extra LSBs will be ignored. The stereo word rate (f_{as}) can be either 32, 44.1 or 48 kHz.

Because the DAPIC is a slave device it can only be connected to a master I^2S-bus transmitter or receiver (see Chapter "Timing characteristics" and Fig.8).

I^2C-bus control (SCL and SDA)

The I^2C-bus interface is used to control the operation of the DAPIC for the audio signal processing and write the coefficients and the external delay line addresses of the different signal processing algorithms. New coefficients are updated in real time to the internal RAM.

The transfer byte organization is as follows:

start condition

first byte (8 bits)

acknowledge (1 bit)

second byte (8 bits)

acknowledge (1 bit)

third to tenth byte (8 bits)

acknowledge (1 bit)

stop condition.

The first byte is the address of the I^2C-bus device being addressed. If the device detects its address it answers with an acknowledge by pulling down the data line (SDA) for one clock period (SCL line). The second byte contains the address of the internal RAM to which the first new coefficient should have written. The data will then be transmitted. Each new word (coefficient) is 2 bytes wide. Up to four words of data can be written within one transfer. Should the mode of the feature register be addressed then only one data word will be transferred.

Because the I^2C-bus (on the DAPIC) is a slave receiver bus, the clock has to be generated by the host microcontroller.

Table 1 I^2C-bus slave address.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	1	1	0	AS2[1]	AS1[1]	0

Note

1. AS1 and AS2 are the hardware (pin) programmable address bits. When the device detects this address it will respond with an acknowledge pulse on the SDA line.

DRAM interface

The DRAM interface contains a nibble wide data bus, a 9-bit wide address bus and all necessary control signals to enable the different DRAM configurations.

Timing of the control signals $\overline{RAS}$, $\overline{CAS}$, $\overline{CAS2}$, A8B, $\overline{OE}$ and $\overline{WE}$ is related to the applied clock frequency of the DAPIC. The important timing parameters are the page mode cycle time ($t_{cy;CAS}$), the access time ($t_{acc;RAS}$), the refreshing rate and the maximum value for $\overline{RAS}$ to $\overline{CAS}$ delay time ($t_{dRAS;CAS}$) (see Chapter "Timing characteristics" and Fig.9). A read/write operation will always be executed in the page mode (one row address and four column addresses) because every data transfer consists of 4 nibbles.

The refresh time of the DRAM (t_{rfsh}) must be greater than;

$t_{rfsh} > (2^{addr}/3f_{as})$ ms

where 'addr' is the number of physical address lines and f_{as} is measured in kHz.

For fast DRAMs, the maximum value for $\overline{RAS}$ and $\overline{CAS}$ is important.

Different DRAM combinations can be connected to the DAPIC. The smallest DRAM is a 64 × 4-bit (256 kbits) RAM. For this configuration, 16K data words can be stored. When this RAM is connected to the DAPIC, the MSB address signal (A8) can be felt floating.

The DAPIC can address up to 1 Mbit DRAMs. However, RAMs greater than 1 Mbit can also be connected. This, therefore, implies that the redundant address lines of the RAM must be fixed to V_{DD} or V_{SS} or must be joined with one of the other address pins.

The choice of a 256 kbit or a 1 Mbit DRAM device must be indicated by a flag bit residing in the start address control word of the different delay lines.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	DC supply voltage (each supply pin)		−0.5	+6.5	V
ΔV_{DD}	voltage difference between V_{DD} and V_{DDX}		−	550	mV
I_{IK}	DC input clamp diode current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	−	±10	mA
I_{OK}	DC output clamp diode current (output type 4 mA)	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V	−	±20	mA
I_O	DC output sink or source current (output type 4 mA)	$-0.5 < V_O < V_{DD} + 0.5$ V	−	±20	mA
I_{DD}	DC supply current per pin		−	50	mA
I_{SS}	DC supply current per pin		−	50	mA
LTCH	latch-up protection	CIC specification/ test method	100	−	mA
P_O	power dissipation per output		−	100	mW
P_{tot}	total power dissipation		−	1	W
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{es}	electrostatic discharge	note 1	−3000	+3000	V
		note 2	−300	+300	V

Notes

1. Human body model: C = 100 pF; R = 1.5 kΩ.
2. Machine model: C = 200 pF; L = 2.5 μH; R = 0 Ω.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
Rth j-a	thermal resistance from junction to ambient in free air	tbf	K/W

DC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDn}	DC supply voltage (pins 7, 8, 26, 32, 38, 53, 54 and 60)		4.5	5.0	5.5	V
$I_{DD(tot)}$	total of all DC supply current pins	f_{xtal} = 16.9344 MHz	–	60	–	mA
P_{tot}	total power dissipation	f_{xtal} = 16.9344 MHz	–	300	–	mW
V_{IH}	HIGH level input voltage (pins 1, 3, 4, 11, 12, 15, 16, 36, 37, 41 to 45, 47 to 49, 51, 52, 62 and 64)		$0.7V_{DD}$	–	–	V
V_{IL}	LOW level input voltage (pins 1, 3, 4, 11, 12, 15, 16, 36, 37, 41 to 45, 47 to 49, 51, 52, 62 and 64)		–	–	$0.3V_{DD}$	V
$V_{th(pos)}$	Schmitt trigger positive-going threshold (pin 2)		–	–	$0.8V_{DD}$	V
$V_{th(neg)}$	Schmitt trigger negative-going threshold (pin 2)		$0.2V_{DD}$	–	–	V
V_{HY}	hysteresis voltage (pin 2)		–	$0.33V_{DD}$	–	V
V_{OH}	HIGH level output voltage (pins 10 to 12, 14 to 24, 27 to 31, 33 to 35 and 63)	V_{DD} = 4.5 V; I_O = 4 mA	4.0	–	–	V
V_{OL}	LOW level output voltage (pins 10 to 12, 14 to 24, 27 to 31, 33 to 35 and 63)	V_{DD} = 4.5 V; I_O = 4 mA	–	–	0.5	V
I_{LI}	input leakage current (pins 1, 2, 4, 36, 37, 41 to 45, 47 to 49, 51, 52 and 62)	V_{DD} = 0 or 5.5 V	–	–	±1	µA
I_{ZO}	output leakage current; 3-state (pins 3, 11, 12, 15 and 16)	V_{DD} = 0 or 5.5 V	–	–	±5	µA
R_{pd}	internal pull-down resistance to V_{SS} (pin 64)	V_I = V_{DD}	17	–	134	kΩ
$t_{r(i)}$	input rise time	V_{DD} = 5.5 V	–	6	200	ns
$t_{f(i)}$	input fall time	V_{DD} = 5.5 V	–	6	200	ns
$t_{r(o)}$	output rise time for LOW-to-HIGH transition	V_{DD} = 4.5 V; T_{amb} = 85 °C; C_L = pF; pins 11, 12, 15 and 16	–	–	$9.5 + 0.4C_L$	ns
		V_{DD} = 4.5 V; T_{amb} = 85 °C; C_L = pF; pins 10, 14, 17 to 24, 27 to 31, 33 to 35 and 63	–	–	$8.5 + 0.4C_L$	
$t_{f(o)}$	output fall time for HIGH-to-LOW transition	V_{DD} = 4.5 V; T_{amb} = 85 °C; C_L = pF; pins 11, 12, 15 and 16	–	–	$11 + 0.5C_L$	ns
		V_{DD} = 4.5 V; T_{amb} = 85 °C; C_L = pF; pins 10, 14, 17 to 24, 27 to 31, 33 to 35 and 63	–	–	$9.0 + 0.5C_L$	ns

AC CHARACTERISTICS

V_{DDX} = 5 V; T_{amb} = +25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{xtal}	crystal input frequency	$\geq 384f_{as}$	12.288	16.9344	21.7	MHz
α_f	spurious frequency attenuation		20	–	–	dB
I_{59}	crystal current output (pin 59)	slave mode only	–	–	–	mA
g	transconductance at maximum current		–	0.4	–	mS
V_{xtal}	voltage across crystal		–	500	–	mV
C_L	load capacitance		–	–	15	pF
$\frac{1}{2}T_{clk}$	half clock period of external clock		23	–	–	ns

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{HC}	pulse width HIGH, DIBCK and DOBCK	110	–	ns
t_{LC}	pulse width LOW, DIBCK and DOBCK	110	–	ns
t_r	DIBCK and DOBCK rise time	–	20	ns
t_f	DIBCK and DOBCK fall time	–	20	ns
t_{h1}	DIWS and DOWS hold time	10	–	ns
t_{su1}	DIWS and DOWS set-up time	20	–	ns
t_{h2}	DI1D and DI2D hold time	10	–	ns
t_{su2}	DI1D and DI2D set-up time	20	–	ns
t_{acc}	DI1D and DI2D access time	–	25 + 0.5C_L in pF	ns
DRAM timing				
$\frac{1}{2}T_{clk}$	half clock period	23	–	ns
$t_{p;RAS}$	$\overline{RAS}$ precharge time	$4 \times \frac{1}{2}T_{clk} - 12$	–	ns
$t_{W;RAS}$	$\overline{RAS}$ pulse width	$16 \times 4\frac{1}{2}T_{clk} - 12$	–	ns
$t_{su;RA}$	row address set-up time	$\frac{1}{2}T_{clk} - 8$	–	ns
$t_{h;RA}$	row address hold time	$\frac{1}{2}T_{clk} - 12$	–	ns
$t_{dRAS;CAS}$	$\overline{RAS}$ to $\overline{CAS}$ delay time	$2 \times \frac{1}{2}T_{clk} - 14$	–	ns
$t_{h;CAS}$	$\overline{CAS}$ hold time	$4 \times \frac{1}{2}T_{clk} - 12$	–	ns
$t_{h;RAS}$	$\overline{RAS}$ hold time	$2 \times \frac{1}{2}T_{clk} - 12$	–	ns
$t_{RAS;CA}$	$\overline{RAS}$ to column address	–	$\frac{1}{2}T_{clk} + 8$	ns
$t_{hCA;RAS}$	column address hold time from $\overline{RAS}$	$5 \times \frac{1}{2}T_{clk} - 11$	–	ns
$t_{hCA;RASp}$	column address hold time from $\overline{RAS}$ precharge	$\frac{1}{2}T_{clk} - 12$	–	ns
$t_{lCA;RAS}$	column address to $\overline{RAS}$ lead time	$3 \times \frac{1}{2}T_{clk} - 8$	–	ns
$t_{pCAS;RAS}$	$\overline{CAS}$ to $\overline{RAS}$ precharge time	$4 \times \frac{1}{2}T_{clk} - 14$	–	ns
$t_{su;CA}$	column address set-up time	$\frac{1}{2}T_{clk} - 8$	–	ns

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$t_{h1CA;CAS}$	column address hold time to $\overline{CAS}$	$3 \times \frac{1}{2}T_{clk} - 14$	–	ns
$t_{h2CA;CAS}$	column address hold time to $\overline{CAS}$ precharge	$\frac{1}{2}T_{clk} - 15$	–	ns
$t_{W;CAS}$	$\overline{CAS}$ pulse width	$2 \times \frac{1}{2}T_{clk} - 14$	–	ns
$t_{p;CAS}$	$\overline{CAS}$ precharge time	$2 \times \frac{1}{2}T_{clk} - 11$	–	ns
$t_{cy;CAS}$	$\overline{CAS}$ page mode cycle time	$4 \times \frac{1}{2}T_{clk}$	–	ns
$t_{acc;CA}$	access time from column address	–	$3 \times \frac{1}{2}T_{clk} - 20$	ns
$t_{acc;CAS}$	access time from $\overline{CAS}$	–	$2 \times \frac{1}{2}T_{clk} - 24$	ns
$t_{acc;RAS}$	access time from $\overline{RAS}$	–	$4 \times \frac{1}{2}T_{clk} - 22$	ns
$t_{hDAT;CAS}$	data hold time from $\overline{CAS}$	2	–	ns
$t_{rcy;def}$	read cycle definition time	$4 \times \frac{1}{2}T_{clk} - 10$	–	ns
$t_{su;DAT}$	data input set-up time	$\frac{1}{2}T_{clk} - 8$	–	ns
$t_{h;DAT}$	data input hold time	$3 \times \frac{1}{2}T_{clk} - 16$	–	ns
$t_{hDAT;RAS}$	data input hold time from $\overline{RAS}$	$5 \times \frac{1}{2}T_{clk} - 15$	–	ns
$t_{wcy;def}$	write cycle definition time	$2 \times \frac{1}{2}T_{clk} - 12$	–	ns
t_{off}	output data disable time	–	$\frac{1}{2}T_{clk} + 8$	ns

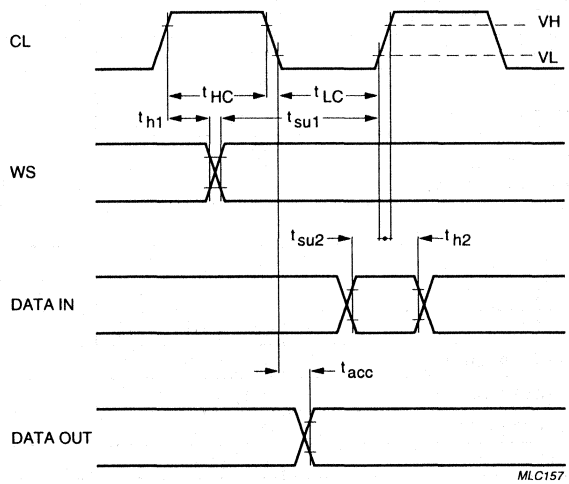


Fig.8 Timing diagram I²S-bus.

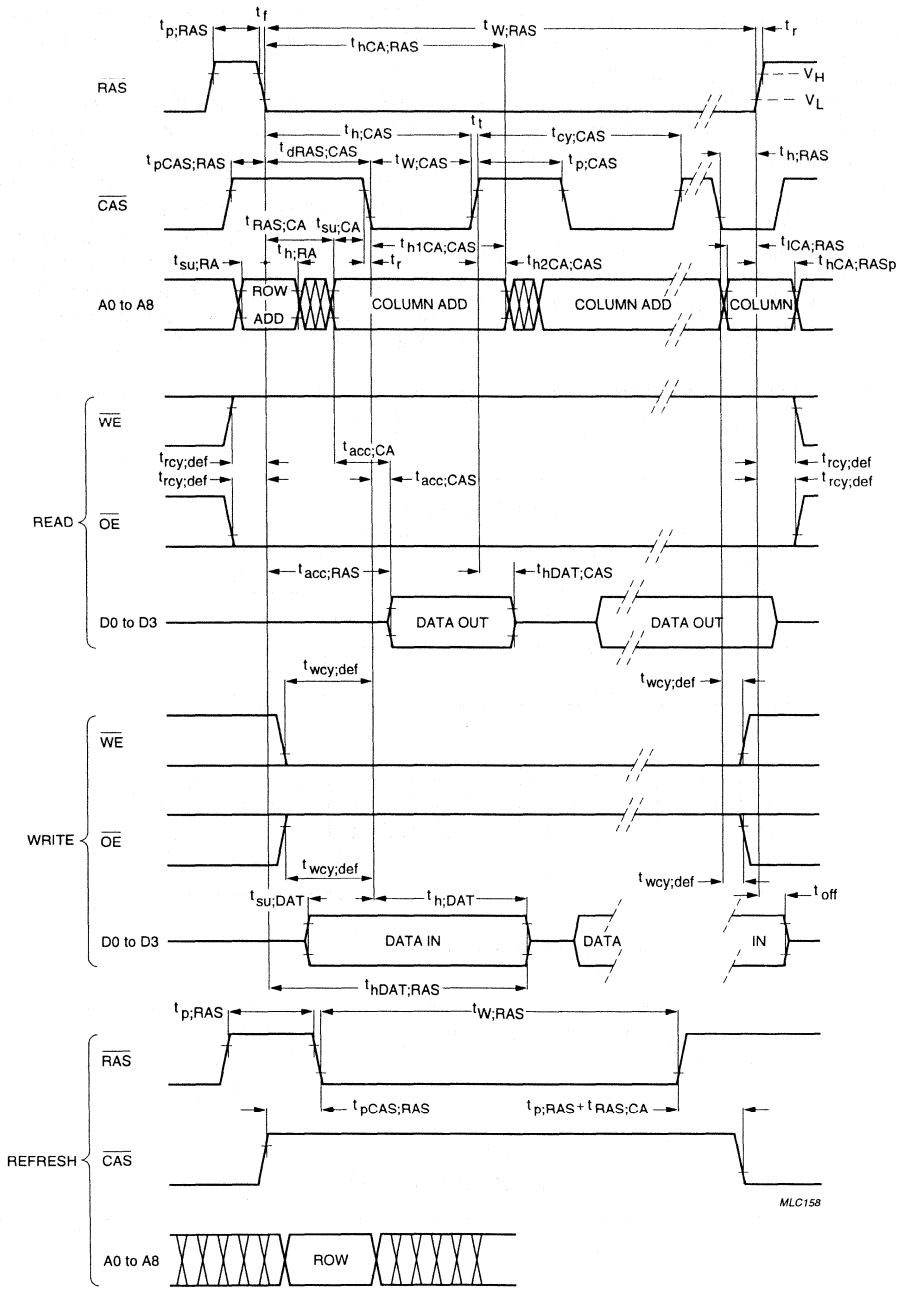


Fig.9 Timing diagram DRAM interface.

I²S-BUS PROTOCOL

The I²S-bus digital interface is used for communication to external digital sources. It is a 3-line serial bus with one line each for data, clock and word select. Figure 10 illustrates an excerpt from the Philips I²S-bus specification interface report with respect to general timing and format of the bus. Word select (WS) at logic 0 signifies the left channel and logic 1 the right channel.

The serial data is transmitted in two's complement with MSB first. One clock period after the negative edge of the WS line, the MSB of the left channel is transmitted. Data is synchronized on the negative edge of the clock and latched on the positive edge.

Two data line have been implemented as input from an external processor for the four audio channels. Because of this configuration the DAPIC operates in the following manner.

The I²S-bus input block reads 4 samples (left and right samples of the front and rear channel) and stores the information into the register file. The operators read from the register file, process the data and store the intermediate results back into the register file. If a delay line is required, the external RAM will need to be accessed. The output samples are read from the register file and are passed via the fade unit to the I²S-bus output block. The same operation is repeated for each incoming audio sample.

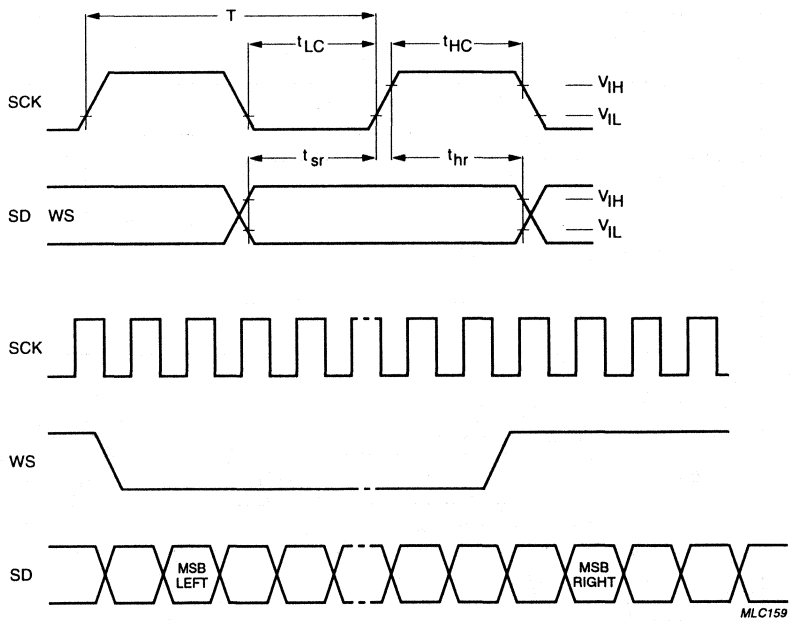


Fig.10 I²S-bus timing format.

I²C-BUS PROTOCOL

The I²C-bus is intended for 2-way, 2-line communication between different ICs or modules. The two lines are the serial data line (SDA) and the serial clock line (SCL). Both lines must be connected to the supply rail via a pull-up resistor when connected to the output stages of a microcontroller. Data transfer can only be initiated when the bus is not busy. Full details of the I²C-bus are given in the document *"The I²C-bus and how to use it"*. This document may be ordered using the code 9398 393 40011.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulses as changes in the data line at this time will be interpreted as control signals. The maximum clock frequency is 100 kHz (see Fig.11).

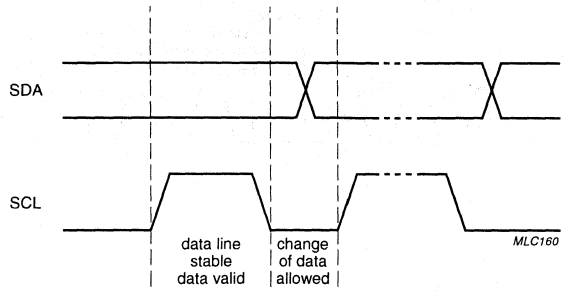


Fig.11 Bit transfer on the I²S bus.

Start and stop condition

In the start and stop condition the data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the stop condition (P) (see Fig.12).

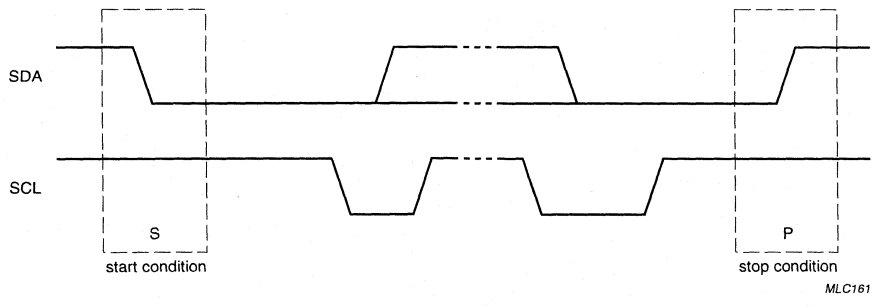


Fig.12 Start and stop conditions.

Data transfer

A device generating a message is a 'transmitter', a device receiving a message is a 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the device are the 'slaves' (see Fig.13).

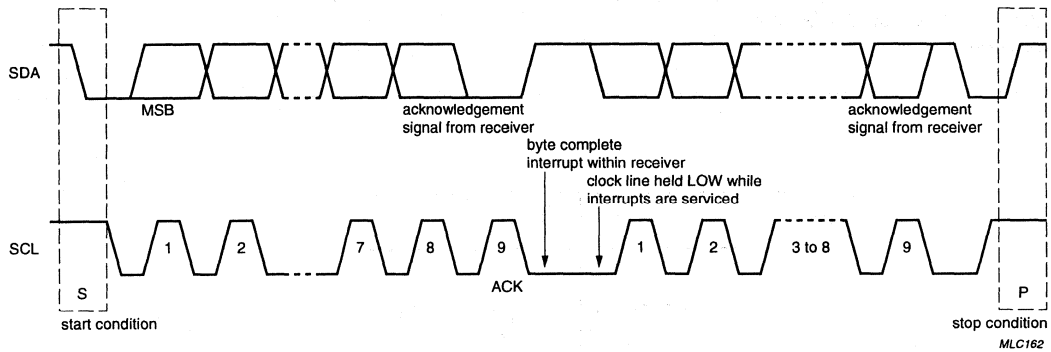


Fig.13 Data transfer on the I²C-bus.

Acknowledge

The number of data bytes that are transferred between the start and stop conditions, from transmitter to receiver, is unlimited. Each byte is followed by an acknowledge bit. The acknowledge bit is a HIGH level bit placed on the bus by the transmitter, whereas the master generates an extra acknowledge bit which is related to the clock pulse. A slave receiver which is addressed must generate an acknowledge bit after the reception of each byte. The master must also generate an acknowledge bit after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Set-up and hold times must also be taken into account. A master receiver must signal an end-of-data to the transmitter. This is achieved by not generating an acknowledge on the last byte that has been clocked out of the slave. In this condition the transmitter must leave the data line HIGH to enable the master to generate a stop condition (see Fig.14).

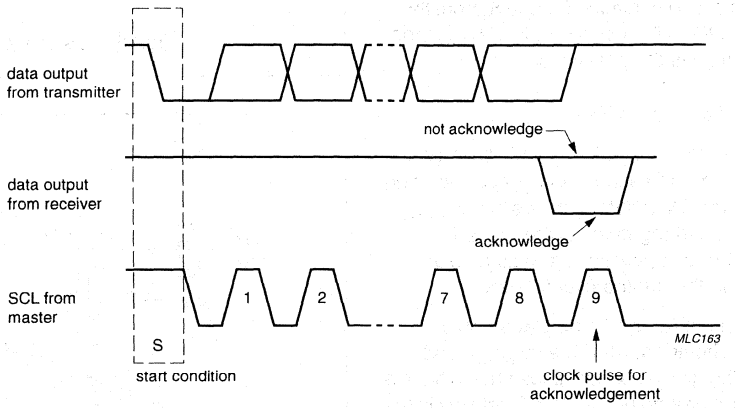


Fig.14 Acknowledge on the I²C-bus.

APPLICATION INFORMATION

Clock circuit and oscillator

The clock generation of the SAA7740H is designed to accommodate two main modes, the master and the slave.

In the master mode, the DAPIC is the master in the system. The clock is generated by connecting a crystal to the oscillator pins CLK1/XTAL1 and XTAL2 (see Fig.15).

In the slave mode, the DAPIC is supplied as a slave. The external clock should be connected to the oscillator at pin CLK1/XTAL1 (see Fig.16).

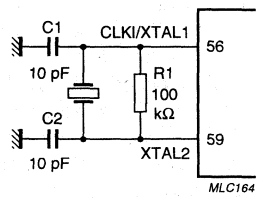


Fig.15 Master mode.

Crystal oscillator supply

The power supply for the oscillator is separate from the other supply line. This is to minimize feedback from the ground bounce of the IC to the oscillator. Pin V_{SSX} is the ground supply and V_{DDX} is the positive supply.

Power supply connection and EMC

The SAA7740H has in total 8 positive supply lines (V_{DD}) including V_{DDX}, and 8 ground supply lines (V_{SS}) including V_{SSX}. For correct current distribution all positive supply lines should be connected together on the printed circuit-board. The ground supply lines should also be connected together on the printed circuit-board.

To minimize radiation the IC should be placed on a double-layer printed circuit-board with a large ground plane on one side. The ground supply lines should have a short connection to the ground plane. An LC network in the positive supply lines can be used as a high frequency filter.

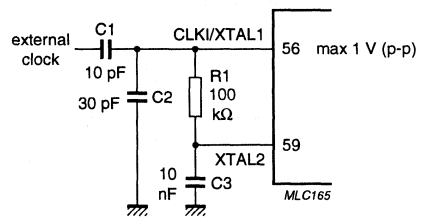


Fig.16 Slave mode.

Test mode connections

Pins SCCLK, TSTCLK, TST1, TST2 and TST3 are used to put the IC in the test mode and to test the internal connections. In the application these pins must be connected to ground.

INTERFERENCE AND NOISE SUPPRESSION CIRCUIT FOR FM RECEIVERS

GENERAL DESCRIPTION

The TDA1001B is a monolithic integrated circuit for suppressing interference and noise in FM mono and stereo receivers.

Features

- Active low-pass and high-pass filters
- Interference pulse detector with adjustable and controllable response sensitivity
- Noise detector designed for FM i.f. amplifiers with ratio detectors or quadrature detectors
- Schmitt trigger for generating an interference suppression pulse
- Active pilot tone generation (19 kHz)
- Internal voltage stabilization

QUICK REFERENCE DATA

Supply voltage (pin 9)	V_P	typ.	12 V
Supply current (pin 9)	I_P	typ.	14 mA
A.F. input signal handling (pin 1) (peak-to-peak value)	$V_{i(p-p)}$	typ.	1 V
Input resistance (pin 1)	R_i	min.	35 kΩ
Voltage gain (V_{1-16}/V_{6-16})	G_v	typ.	0,5 dB
Total harmonic distortion	THD	typ.	0,25 %
Bandwidth	B	typ.	70 kHz
Suppression pulse threshold voltage (peak value); $R_{13} = 0$	$V_{i(tr)OM}$	typ.	19 mV
Suppression pulse duration	t_s	typ.	27 μs
Supply voltage range (pin 9)	V_P		7,5 to 16 V
Operating ambient temperature range	T_{amb}		−30 to +80 °C

PACKAGE OUTLINE

TDA1001B: 16-lead DIL; plastic (SOT38).
TDA1001BT: 16-lead mini-pack; plastic (SO16; SOT109A).

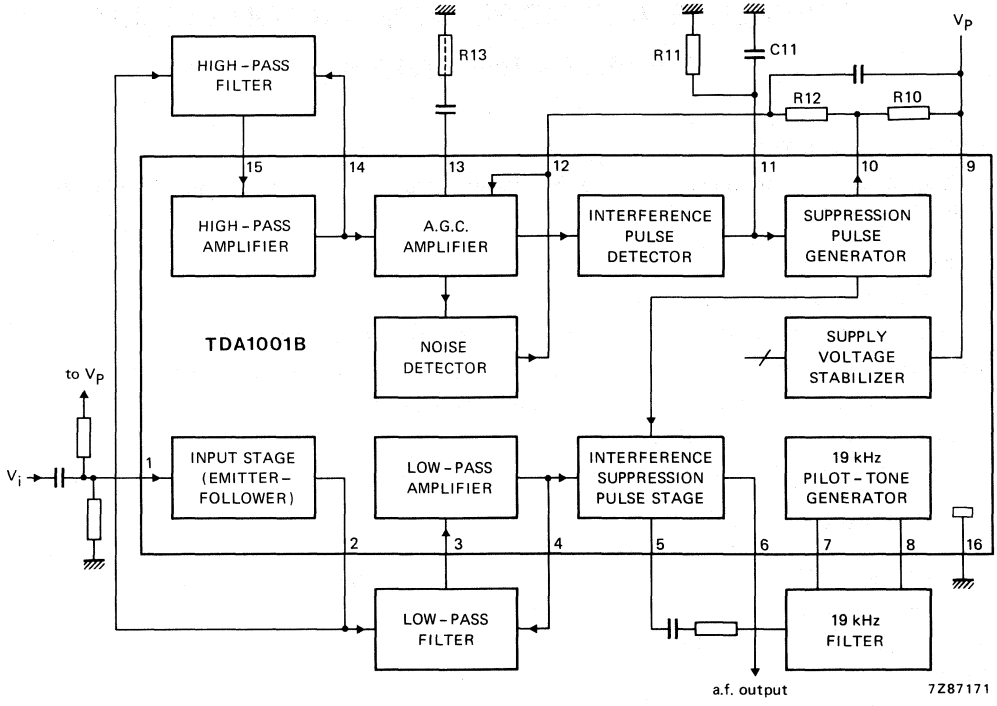


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	V_P	max.	18 V
Input voltage (pin 1)	V_{1-16}	max.	V_P V
Output current (pin 6)	I_6	max.	1 mA
	$-I_6$	max.	15 mA
Total power dissipation	see derating curves Fig. 2		
Storage temperature range	T_{stg}	−65 to +150	°C
Operating ambient temperature range	T_{amb}	−30 to +80	°C

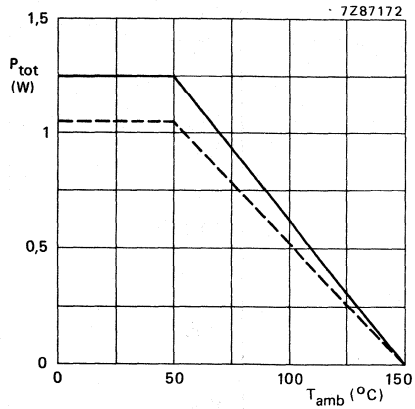


Fig. 2 Power derating curves.
——— in plastic DIL (SOT-38) package (TDA1001B)
– – – – – in plastic mini-pack (SO-16; SOT-109A) package (TDA1001BT); mounted on a ceramic substrate of 50 x 15 x 0,7 mm.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Input stage					
Input impedance (pin 1) f = 40 kHz	$\|Z_{i1}\|$	–	45	–	kΩ
Input resistance (pin 1) with pin 2 not connected	R_{i1}	–	600	–	kΩ
Input bias current (pin 1) $V_{1\text{-}16}$ = 4,8 V	I_{i1}	–	6	15	μA
Output resistance (pin 2) unloaded	R_{o2}		low-ohmic		
Internal emitter resistance	$R_{2\text{-}16}$	–	5,6	–	kΩ
Low-pass amplifier					
Input resistance (pin 3)	R_{i3}	10	–	–	MΩ
Input bias current (pin 3)	I_{i3}	–	–	7	μA
Output resistance (pin 4)	R_{o4}	–	–	5	Ω
Voltage gain (V_4/V_3)	$G_{v4/3}$	–	1,1	–	
Suppression pulse stage					
Input offset current at pin 5 during the suppression time t_s	I_{io5}	–	50	200	nA
Output stage					
Output resistance (pin 6)	R_{o6}		low-ohmic		
Internal emitter resistance	$R_{6\text{-}16}$		6	–	kΩ
Current gain (I_5/I_6)	$G_{i5/6}$	–	85	–	dB
Pilot tone generation (19 kHz)					
Input impedance (pin 8)	$\|Z_{i8}\|$	–	–	1	Ω
Output impedance (pin 7) pin 8 open	$\|Z_{o7}\|$	150	–	–	kΩ
Output bias current (pin 7)	I_{o7}	0,7	1	1,3	mA
Current gain (I_7/I_8)	$G_{i7/8}$	–	3	–	
High-pass amplifier					
Input resistance (pin 15)	R_{i15}	10	–	–	MΩ
Input bias current (pin 15)	I_{i15}	–	–	7	μA
Output resistance (pin 14)	R_{o14}	–	–	5	Ω
Voltage gain ($V_{14/15}$)	$G_{v14/15}$	–	1,4	–	

parameter	symbol	min.	typ.	max.	unit
A.G.C. amplifier; interference and noise detectors					
Internal resistance (pins 13 and 14)	$R_{13\text{-}14}$	1,5	2,0	2,5	kΩ
Operational threshold voltage (uncontrolled); peak value (pin 14) of the interference pulse detector	$\pm V_{14int\ m}$	–	15	–	mV
of the noise detector	$\pm V_{14n\ m}$	–	6,5	–	mV
Output voltage (peak value; pin 11)	$V_{11\text{-}16M}$	5,2	5,8	6,4	V
Output control current (pin 12) (peak value)	I_{12M}	150	200	250	μA
Output bias current (pin 12)	I_{o12}	–	2,5	6	μA
Input threshold voltage for onset of control (pin 12)	$V_{12\text{-}9}$	360	425	500	mV
($V_{i(tr)O}$ + 3 dB)	or:	–	$0{,}66V_{BE}$	–	mV
Suppression pulse generation (Schmitt trigger)					
Switching threshold (pin 11) 1: gate disabled	$V_{11\text{-}16}$	–	3,2	–	V
2: gate enabled	$V_{11\text{-}16}$	–	2,0	–	V
Switching hysteresis	$\Delta V_{11\text{-}16}$	–	1,2	–	V
Input offset current (pin 11)	I_{io11}	–	–	100	nA
Output current (pin 10) gate disabled; peak value	I_{o10M}	0,6	1	1,4	mA
Reverse output current (pin 10)	I_{R10}	–	–	2	μA
Sensitivity (pin 10)	$V_{10\text{-}16}$	2,5	–	–	V

APPLICATION INFORMATION

V_P = 12 V; T_{amb} = 25 °C; f = 1 kHz; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 9)	V_P	7,5	12	16	V
Quiescent supply current (pin 9)	I_P	10	14	18	mA
Signal path					
D.C. input voltage (pin 1)	$V_{1\text{-}16}$	–	4,5	–	V
Input impedance (pin 1); f = 40 kHz	$\lvert Z_{i1}\rvert$	35	–	–	kΩ
D.C. output voltage (pin 6)	$V_{6\text{-}16}$	2,4	2,8	–	V
Output resistance (pin 6)	R_{o6}		low-ohmic		
Voltage gain (V_6/V_1)	$G_{v6/1}$	0	0,5	1	dB
–3 dB point of low-pass filter	$f_{(-3dB)}$	–	70	–	kHz
Sensitivity for THD < 0,5% (peak-to-peak value)	$V_{i(p\text{-}p)}$	1,2	1,8	–	V
Residual interference pulse after suppression (see Fig. 3); pin 7 to ground; $V_{i(tr)M}$ = 100 mV; (peak-to-peak value)	$V_{6\text{-}16(p\text{-}p)}$	–	–	3	mV
Interference suppression at R13 = 0; notes 5 and 6; $V_{i(rms)}$ = 30 mV; f = 19 kHz (sinewave); $V_{i(tr)M}$ = 60 mV; f_r = 400 Hz	α_{int}	20	30	–	dB
Interference processing					
Input signal at pin 1; output signal at pin 10					
Suppression pulse threshold voltage; control function OFF (pin 9 connected to pin 12); r.m.s. value; note 1					
measured with sinewave input signal f = 120 kHz; $-V_{10\text{-}9} > 1$ V					
at R13 = 0 Ω	$V_{i(tr)rms}$	8	11	14	mV
at R13 = 2,7 kΩ	$V_{i(tr)rms}$	18	28,5	40	mV
voltage difference for safe triggering/ non-triggering (r.m.s. value)	$\Delta V_{i(rms)}$	–	1	–	mV
measured with interference pulses f = 400 Hz (see Fig. 3); peak value					
at R13 = 0 Ω	$V_{i(tr)M}$	–	19	–	mV
at R13 = 2,7 kΩ	$V_{i(tr)M}$	–	45	–	mV
Suppression pulse duration (note 2)	t_s	24	27	30	μs

parameters	symbol	min.	typ.	max.	unit
Noise threshold feedback control (notes 1 and 3)					
Noise input voltage (r.m.s. value) f = 120 kHz sinewave					
for $V_{12\text{-}9}$ = 300 mV					
at R13 = 0 Ω	$V_{ni(rms)}$	2,3	3,3	4,3	mV
at R13 = 2,7 kΩ	$V_{ni(rms)}$	–	8,2	–	mV
for $V_{12\text{-}9}$ = 425 mV ($V_{i(tr)O}$ + 3 dB)					
at R13 = 0 Ω	$V_{ni(rms)}$	–	7,3	–	mV
at R13 = 2,7 kΩ	$V_{ni(rms)}$	–	16,5	–	mV
for $V_{12\text{-}9}$ = 560 mV ($V_{i(tr)O}$ + 20 dB)					
at R13 = 0 Ω	$V_{ni(rms)}$	33	45	57	mV
at R13 = 2,7 kΩ	$V_{ni(rms)}$	–	107	–	mV
Amplification control voltage by interference intensity (note 4)					
$V_{i(rms)}$ = 50 mV; f = 19 kHz; $V_{i(tr)M}$ = 300 mV; r.m.s. value					
at repetition frequency f_r = 1 kHz	$V_{o6(rms)}$	49	–	56	mV
at repetition frequency f_r = 16 kHz	$V_{o6(rms)}$	45	–	65	mV

Notes to application information

1. The interference suppression and noise feedback control thresholds can be determined by R13 or a capacitive voltage divider at the input of the high-pass filter and they are defined by the following formulae:
   $V_{i(tr)} = (1 + R13/R_S) \times V_{i(tr)O}$ in which $R_S = 2\ k\Omega$;
   $V_{ni} = (1 + R13/R_S) \times V_{niO}$ in which $R_S = 2\ k\Omega$.
2. The suppression pulse duration is determined by C11 = 2,2 nF and R11 = 6,8 kΩ.
3. The characteristic of the noise feedback control is determined by R12 (and R10).
4. The feedback control of the interference suppression threshold at higher repetition frequencies is determined by R10 (and R12).
5. The 19 kHz generator can be adjusted with $R_{7\text{-}16}$ (and $R_{7\text{-}8}$). Adjustment is not required if components with small tolerances are used e.g. $\Delta R < 1\%$ and $\Delta C < 2\%$.
6. Measuring conditions:
   The peak output noise voltage ($V_{no\ m}$, CCITT filter) shall be measured at the output with a de-emphazing time T = 50 μs (R = 5 kΩ, C = 10 nF); the reference value of 0 dB is $V_{o\ int}$ with the 19 kHz generator short-circuited (pin 7 grounded).

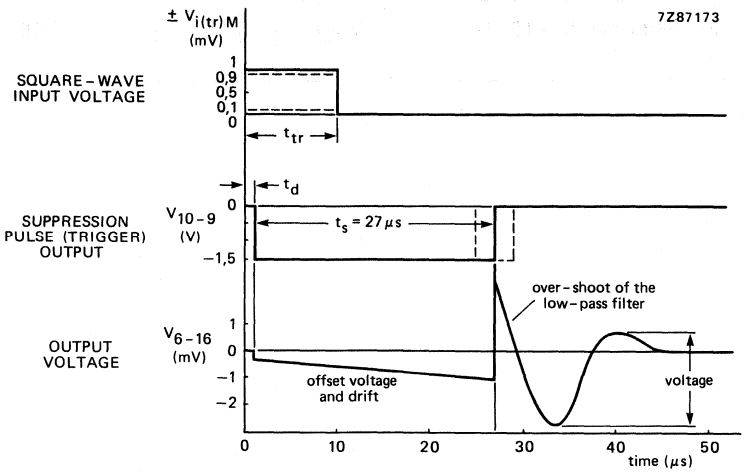


Fig. 3 Measuring signal for interference suppression; at the input (pin 1) a square-wave is applied with a duration of t_{tr} = 10 μs and with rise and fall times $t_r = t_f$ = 10 ns.

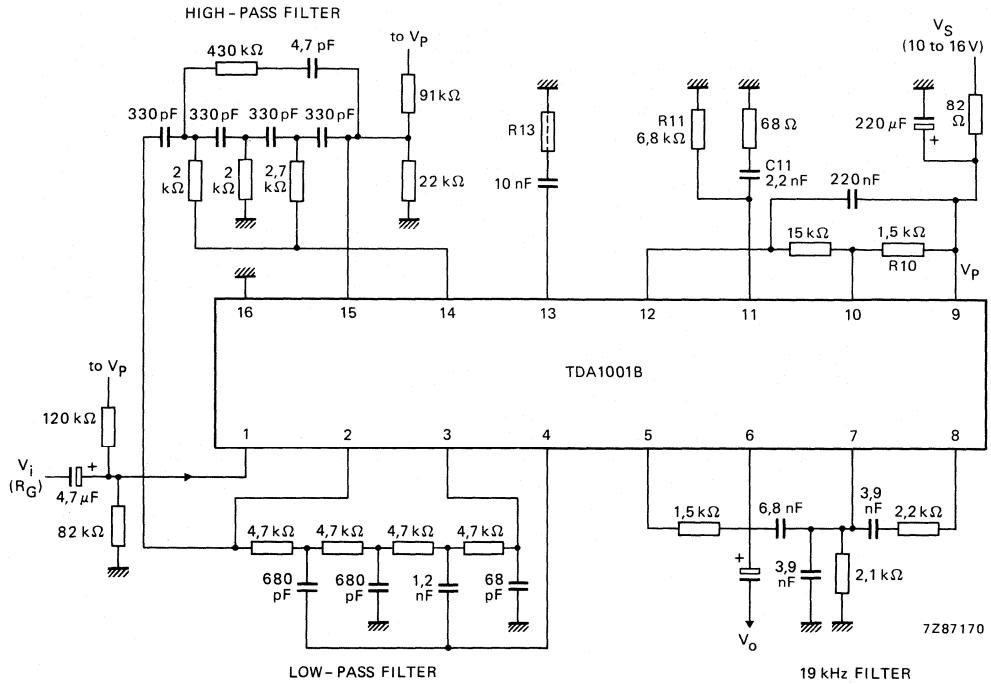


Fig. 4 Application circuit diagram.

6 W AUDIO POWER AMPLIFIER IN CAR APPLICATIONS
10 W AUDIO POWER AMPLIFIER IN MAINS-FED APPLICATIONS

The TDA1010A is a monolithic integrated class-B audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a 6 W car radio amplifier for use with 4 Ω and 2 Ω load impedances. The wide supply voltage range and the flexibility of the IC make it an attractive proposition for record players and tape recorders with output powers up to 10 W.

Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- low-cost external components
- good ripple rejection
- thermal protection

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 24 V
Repetitive peak output current	I_{ORM}	max.	3 A
Output power at pin 2; d_{tot} = 10%			
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	6,4 W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	6,2 W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,4 W
V_P = 14,4 V; R_L = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ.	9 W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2 %
Input impedance			
preamplifier (pin 8)	$\lvert Z_i \rvert$	typ.	30 kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ.	20 kΩ
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	31 mA
Sensitivity for P_o = 5,8 W; R_L = 4 Ω	V_i	typ.	10 mV
Operating ambient temperature	T_{amb}		−25 to + 150 °C
Storage temperature	T_{stg}		−55 to + 150 °C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

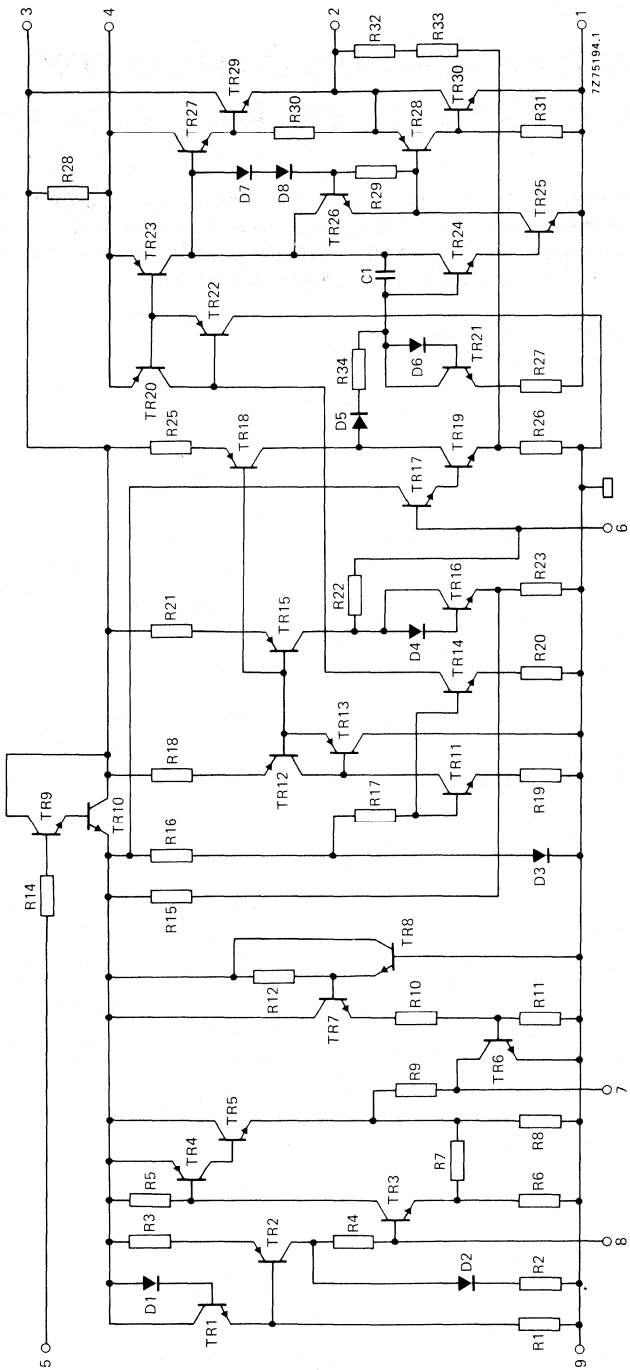


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24 V
Peak output current	I_{OM}	max.	5 A
Repetitive peak output current	I_{ORM}	max.	3 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−25 to + 150 °C
A.C. short-circuit duration of load during sine-wave drive; without heatsink at V_P = 14,4 V	t_{sc}	max.	100 hours

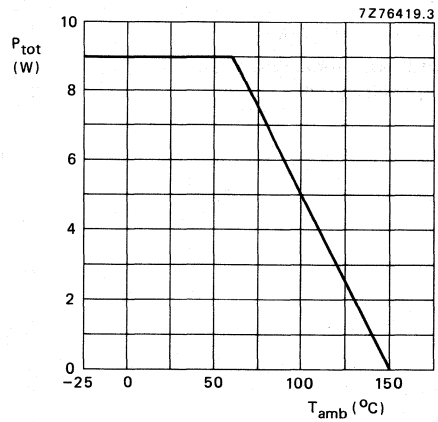


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 14,4 V; R_L = 2 Ω; T_{amb} = 60 °C maximum; thermal shut-down starts at T_j = 150 °C. The maximum sine-wave dissipation in a 2 Ω load is about 5,2 W. The maximum dissipation for music drive will be about 75% of the worst-case sine-wave dissipation, so this will be 3,9 W. Consequently, the total resistance from junction to ambient

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{3{,}9} = 23\ \text{K/W}.$$

Since $R_{th\ j\text{-}tab}$ = 10 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W,

$R_{th\ h\text{-}a}$ = 23 − (10 + 1) = 12 K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P	6 to 24	V
Repetitive peak output current	I_{ORM}	< 3	A
Total quiescent current at V_P = 14,4 V	I_{tot}	typ. 31	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power (see Fig. 4) at d_{tot} = 10%; measured at pin 2; with bootstrap			
V_P = 14,4 V; R_L = 2 Ω (note 1)	P_o	typ. 6,4	W
V_P = 14,4 V; R_L = 4 Ω (note 1 and 2)	P_o	> 5,9 typ. 6,2	W W
V_P = 14,4 V; R_L = 8 Ω (note 1)	P_o	typ. 3,4	W
V_P = 14,4 V; R_L = 4 Ω; without bootstrap	P_o	typ. 5,7	W
V_P = 14,4 V; R_L = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ. 9	W
Voltage gain			
preamplifier (note 3)	G_{v1}	typ. 24 21 to 27	dB dB
power amplifier	G_{v2}	typ. 30 27 to 33	dB dB
total amplifier	$G_{v\,tot}$	typ. 54 51 to 57	dB dB
Total harmonic distortion at P_o = 1 W	d_{tot}	typ. 0,2	%
Efficiency at P_o = 6 W	η	typ. 75	%
Frequency response (−3 dB)	B	80 Hz to 15	kHz
Input impedance			
preamplifier (note 4)	$\lvert Z_i \rvert$	typ. 30 20 to 40	kΩ kΩ
power amplifier (note 5)	$\lvert Z_i \rvert$	typ. 20 14 to 26	kΩ kΩ
Output impedance of preamplifier; pin 7 (note 5)	$\lvert Z_o \rvert$	typ. 20 14 to 26	kΩ kΩ
Output voltage preamplifier (r.m.s. value) d_{tot} < 1% (pin 7) (note 3)	$V_{o(rms)}$	> 0,7	V
Noise output voltage (r.m.s. value; note 6)			
R_S = 0 Ω	$V_{n(rms)}$	typ. 0,3	mV
R_S = 8,2 kΩ	$V_{n(rms)}$	typ. 0,7 < 1,4	mV mV
Ripple rejection at f = 1 kHz to 10 kHz (note 7)	RR	> 42	dB
at f = 100 Hz; C2 = 1 μF	RR	> 37	dB
Sensitivity for P_o = 5,8 W	V_i	typ. 10	mV
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ. 30	mA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Up to $P_o \leqslant 3$ W : $d_{tot} \leqslant 1\%$.
3. Measured with a load impedance of 20 kΩ.
4. Independent of load impedance of preamplifier.
5. Output impedance of preamplifier ($|Z_o|$) is correlated (within 10%) with the input impedance ($|Z_i|$) of the power amplifier.
6. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
7. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude: 2 V).
8. The tab must be electrically floating or connected to the substrate (pin 9).

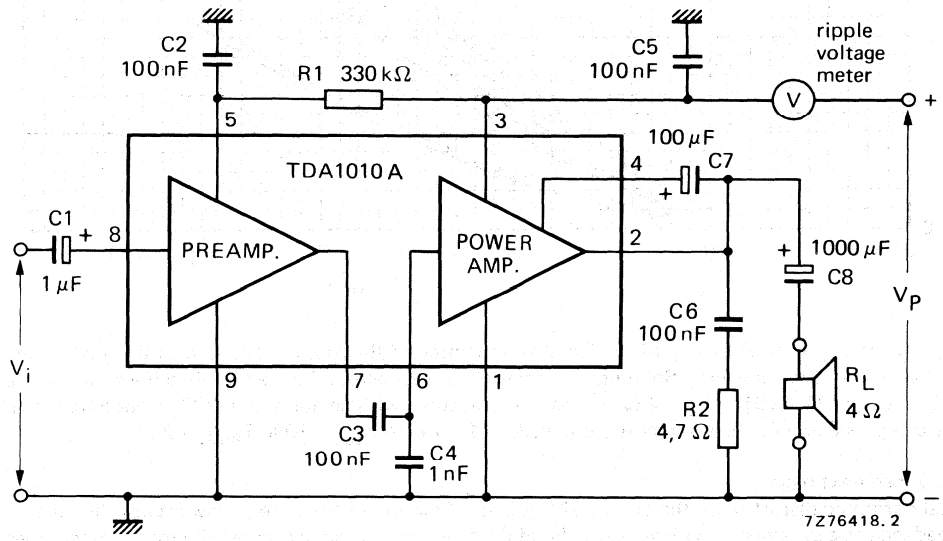


Fig. 3 Test circuit.

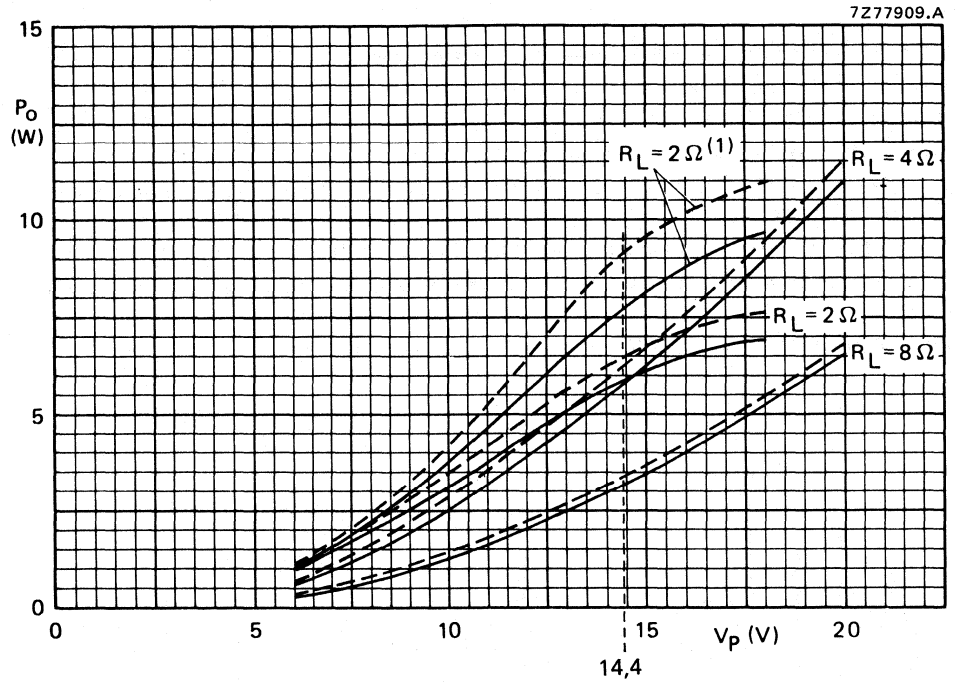


Fig. 4 Output power of the circuit of Fig. 3 as a function of the supply voltage with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\,\Omega$ (1) has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, d_{tot} = 10%, T_{amb} = 25 °C.

Fig. 5 See next page.
Total harmonic distortion in the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\,\Omega$ (1) has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, V_P = 14,4 V.

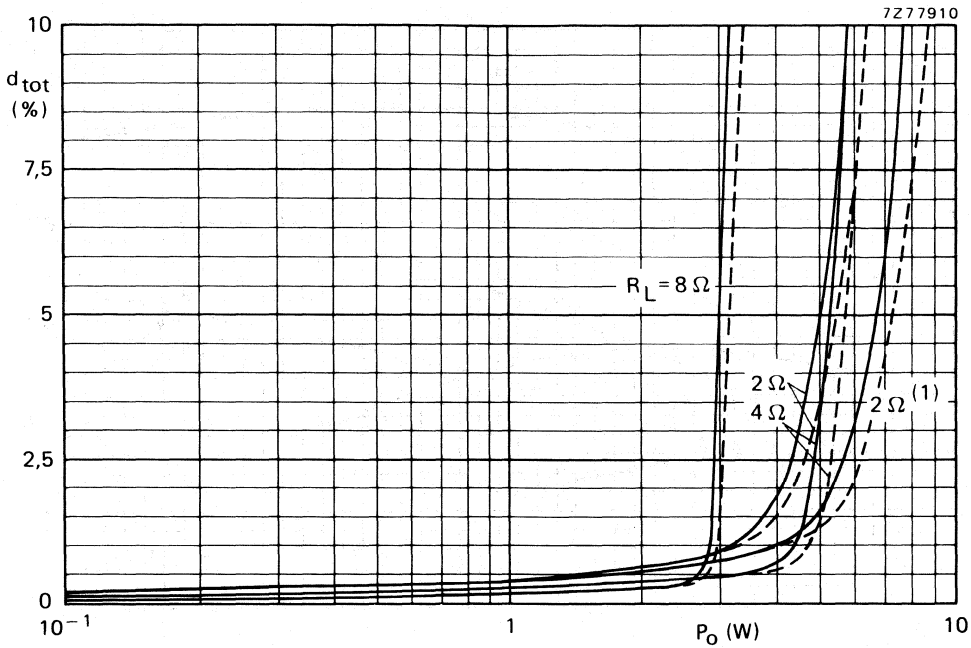


Fig. 5 For caption see preceding page.

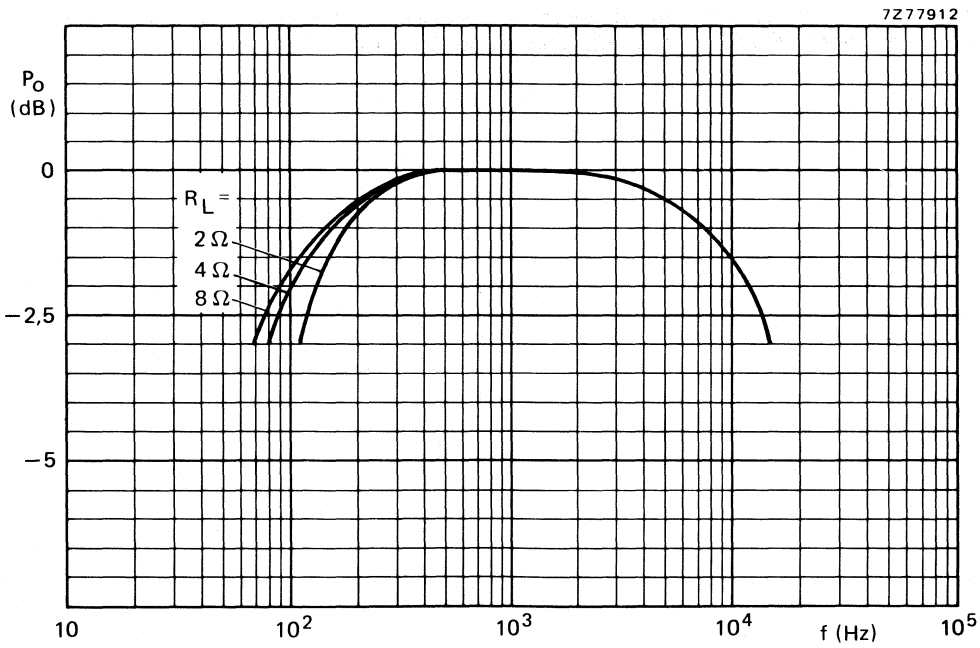


Fig. 6 Frequency characteristics of the circuit of Fig. 3 for three values of load impedance; typical values. P_O relative to 0 dB = 1 W; V_P = 14,4 V.

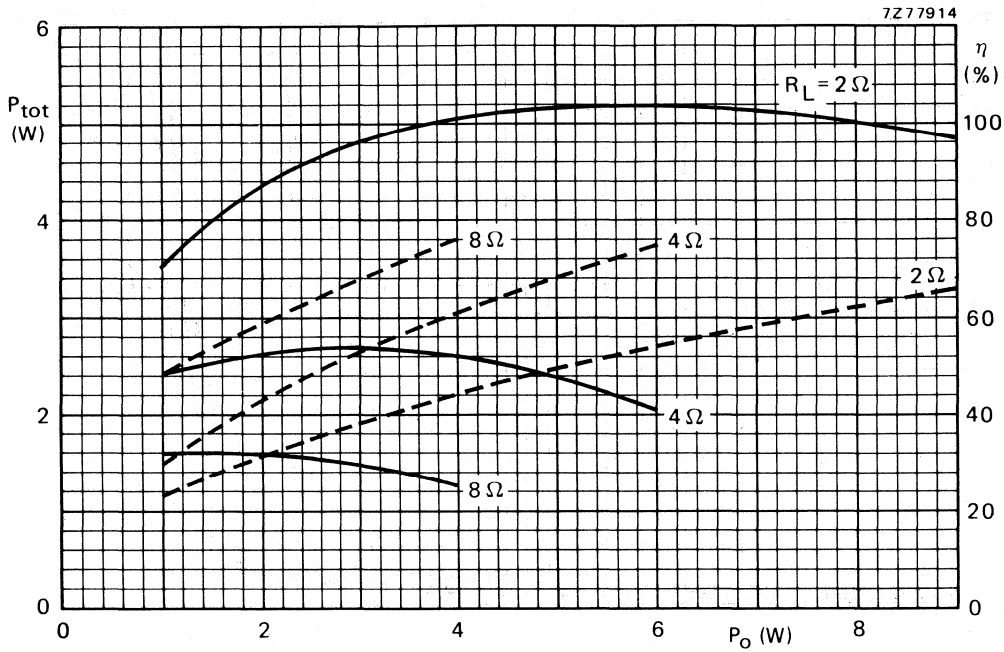


Fig. 7 Total power dissipation (solid lines) and the efficiency (dashed lines) of the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter (for $R_L = 2\,\Omega$ an external bootstrap resistor of 220 Ω has been used); typical values. $V_P = 14{,}4$ V; f = 1 kHz.

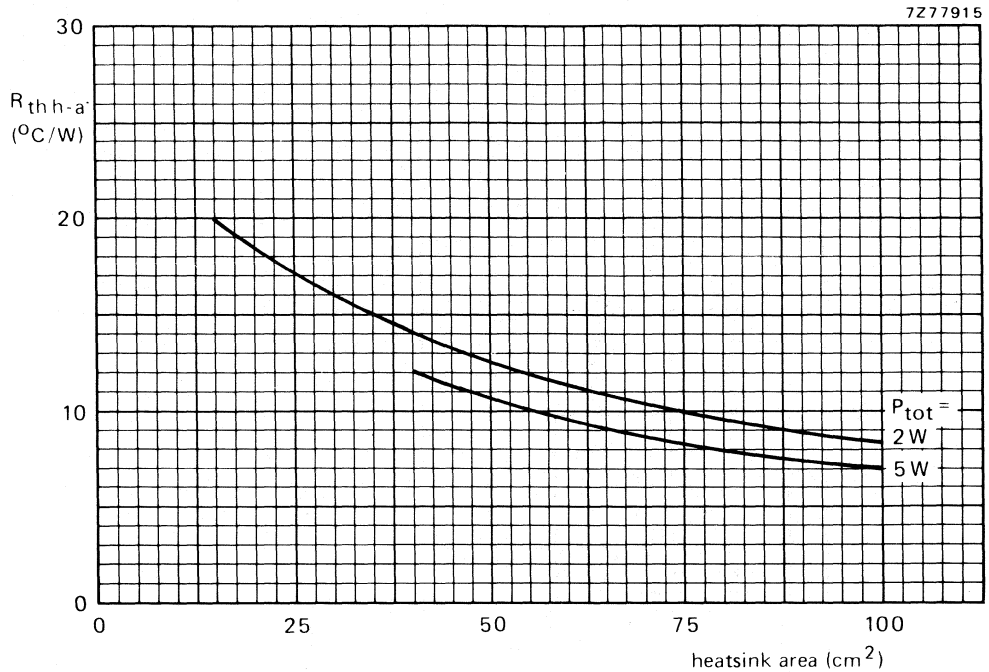


Fig. 8 Thermal resistance from heatsink to ambient of a 1,5 mm thick bright aluminium heatsink as a function of the single-sided area of the heatsink with the total power dissipation as a parameter.

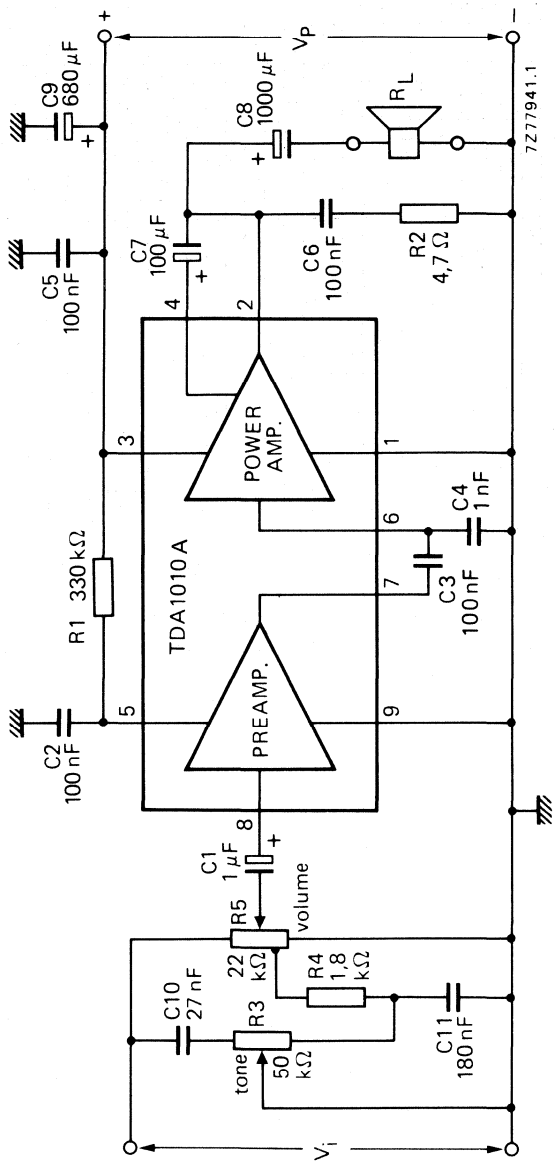


Fig. 9 Complete mono audio amplifier of a car radio.

APPLICATION INFORMATION

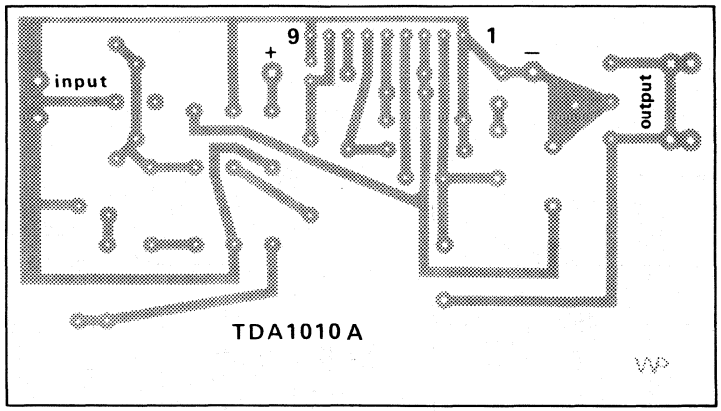


Fig. 10 Track side of printed-circuit board used for the circuit of Fig. 9; p.c. board dimensions 92 mm x 52 mm.

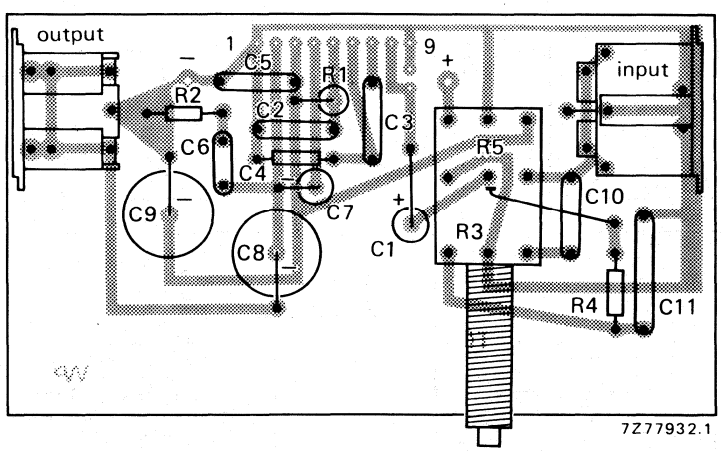


Fig. 11 Component side of printed-circuit board showing component layout used for the circuit of Fig. 9.

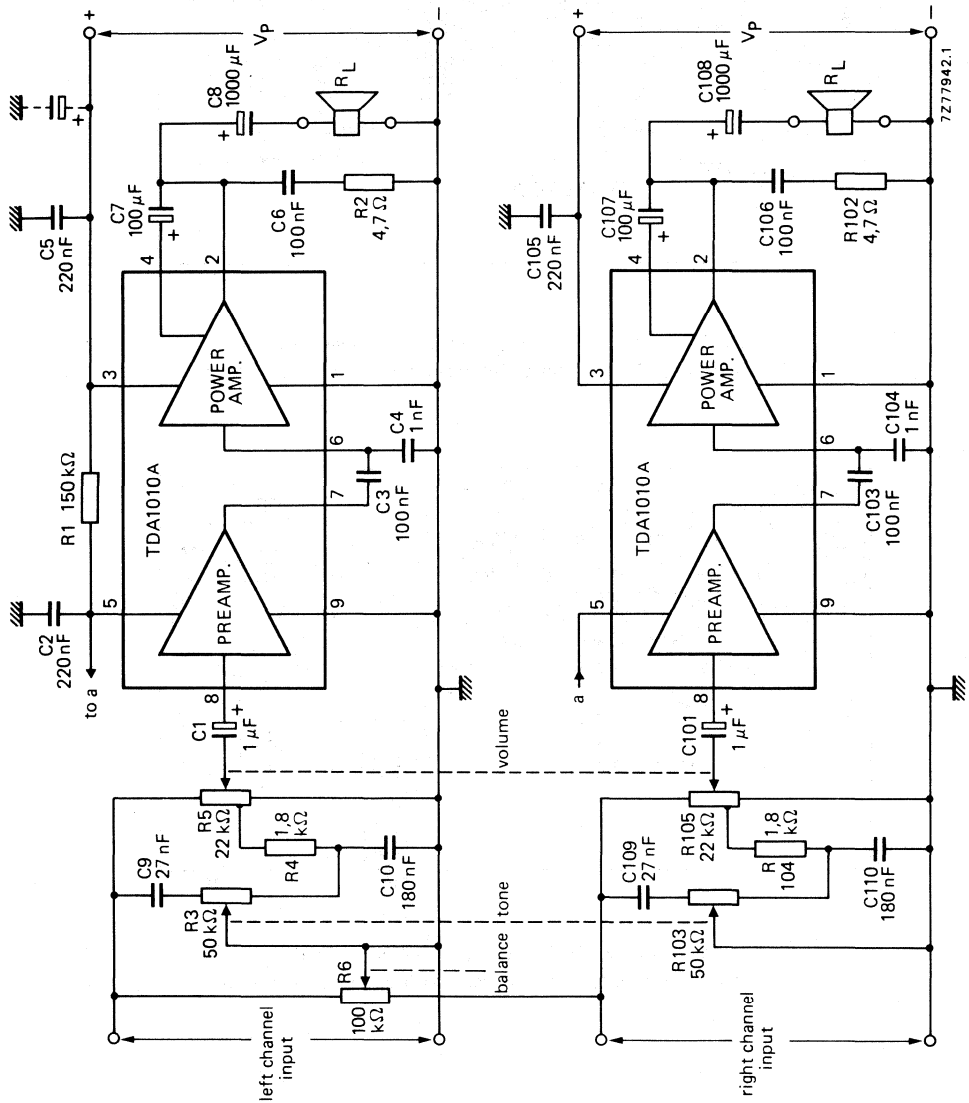


Fig. 12 Complete stereo car radio amplifier.

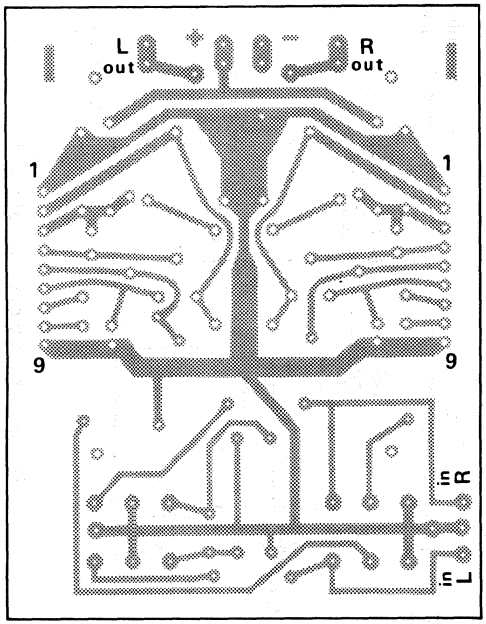


Fig. 13 Track side of printed-circuit board used for the circuit of Fig. 12; p.c. board dimensions 83 mm x 65 mm.

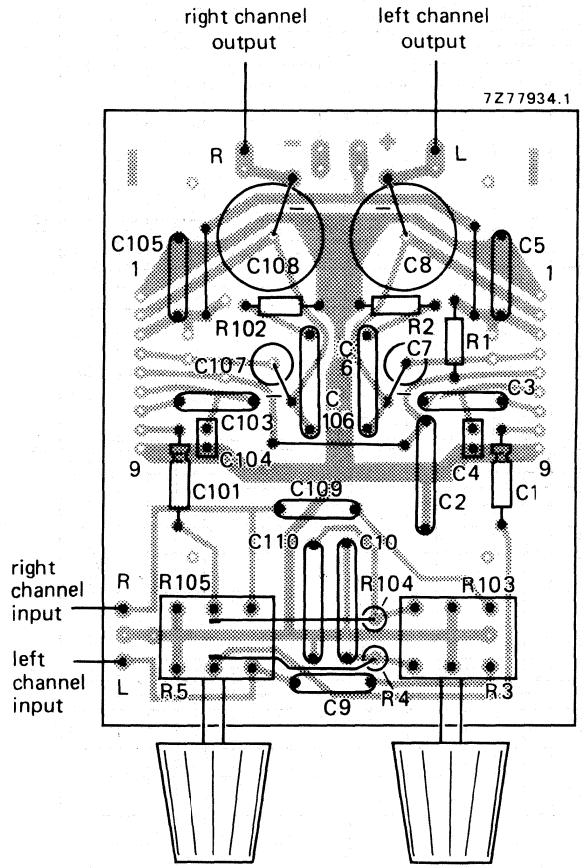


Fig. 14 Component side of printed-circuit board showing component layout used for the circuit of Fig. 12. Balance control is not on the p.c. board.

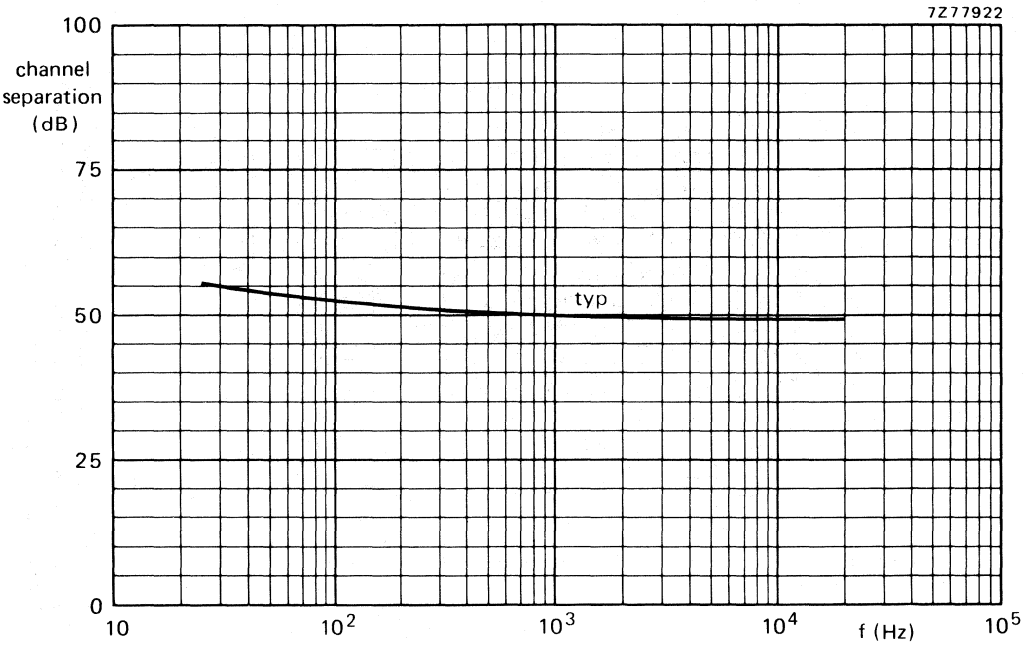


Fig. 15 Channel separation of the circuit of Fig. 12 as a function of the frequency.

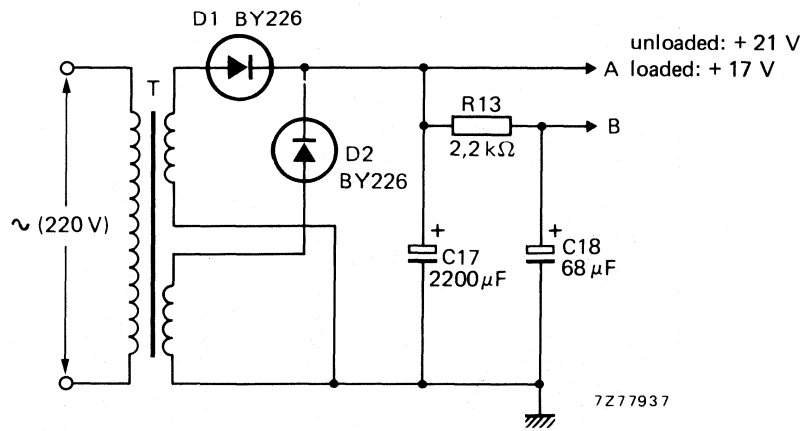


Fig. 16 Power supply of circuit of Fig. 17.

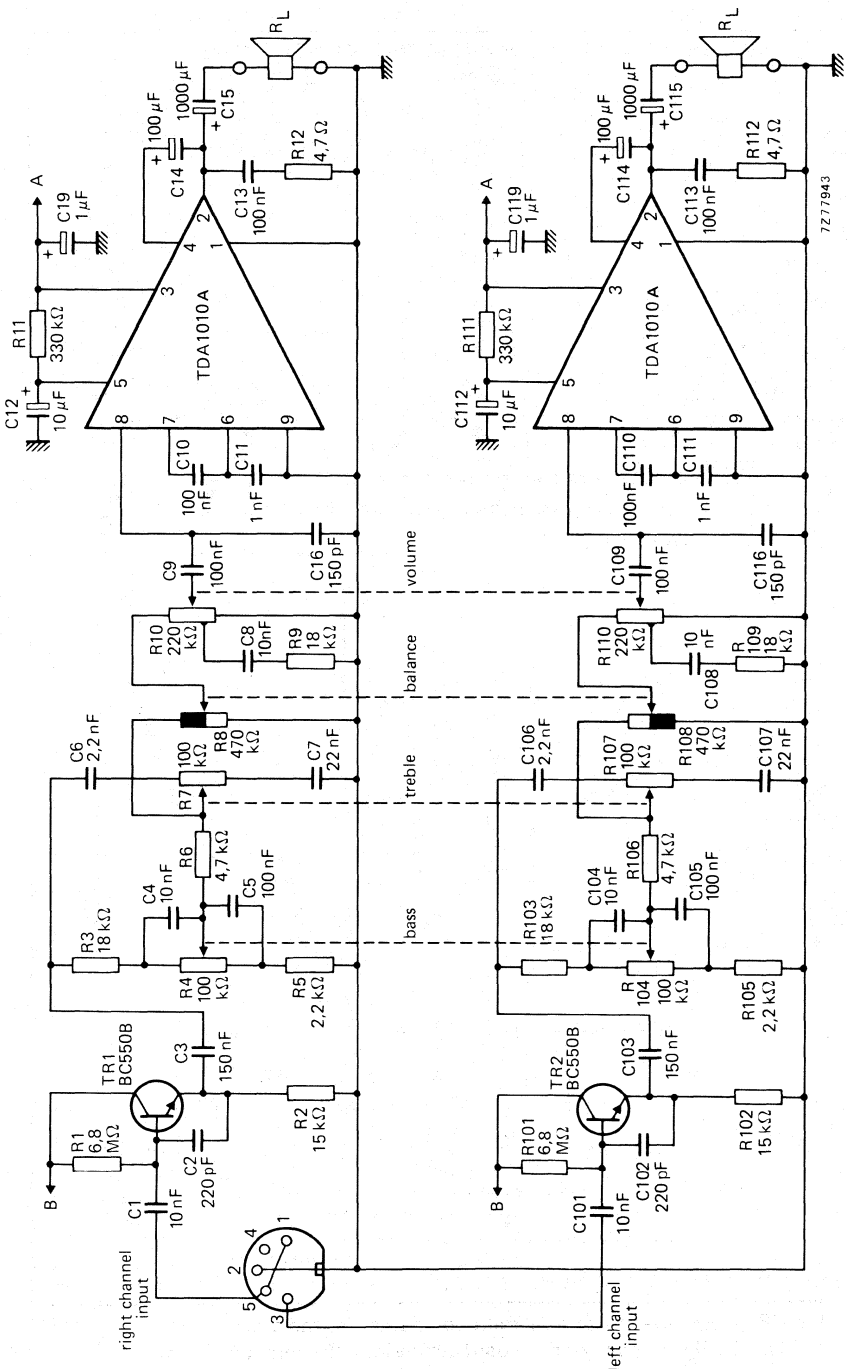


Fig. 17 Complete mains-fed ceramic stereo pick-up amplifier; for power supply see Fig. 16.

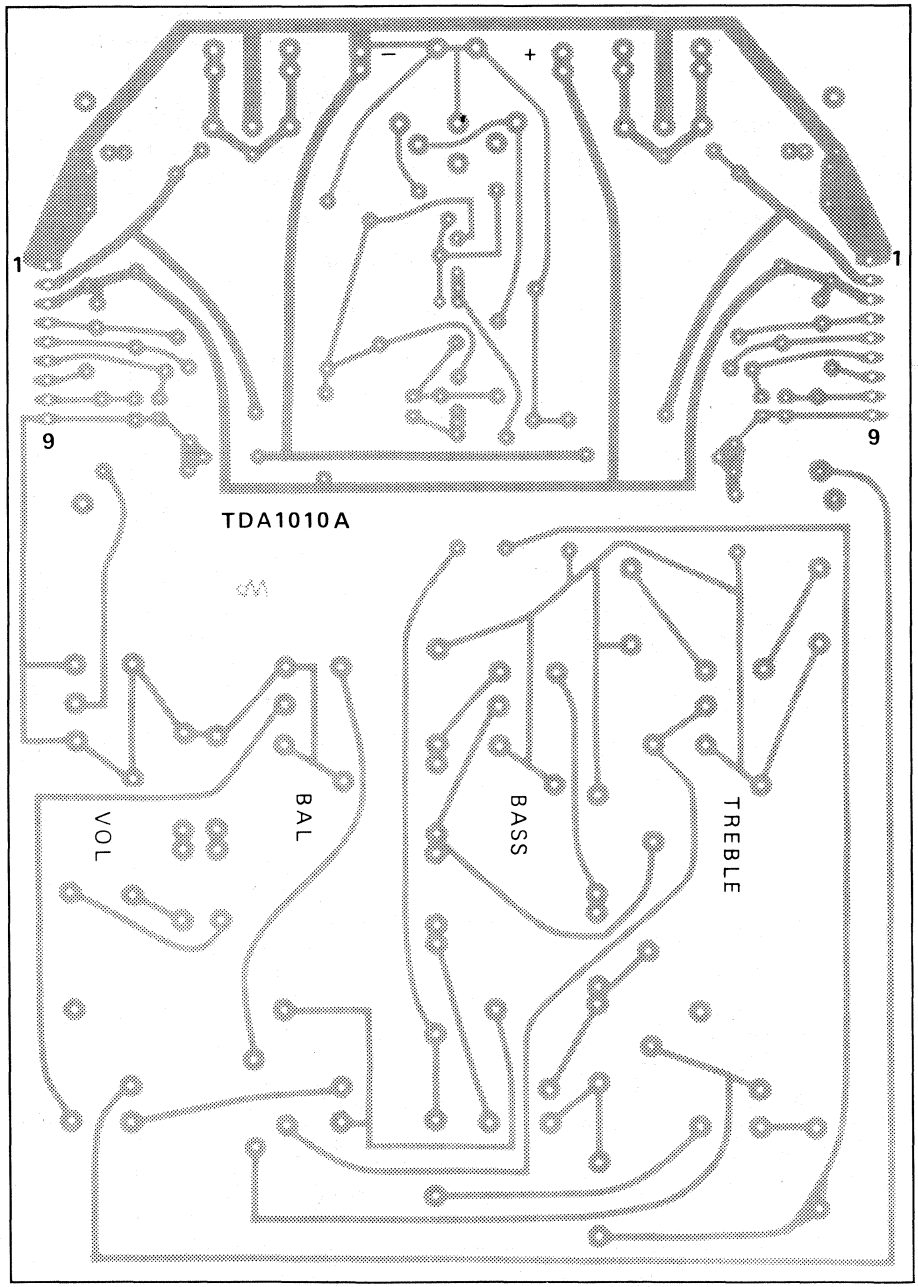


Fig. 18 Track side of printed-circuit board used for the circuit of Fig. 17 (Fig. 16 partly); p.c. board dimensions 169 mm x 118 mm.

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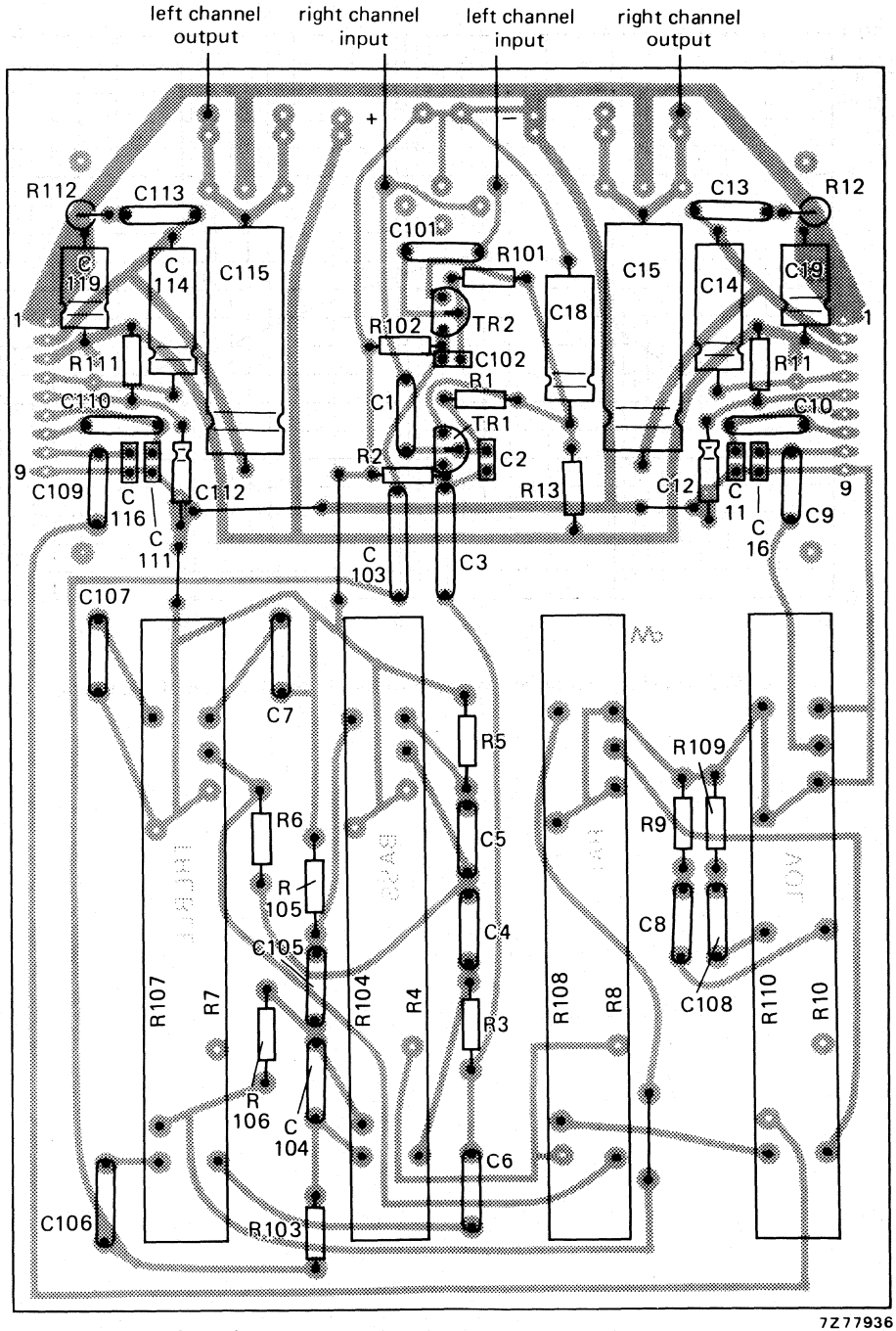


Fig. 19 Component side of printed-circuit board showing component layout used for the circuit of Fig. 17 (Fig. 16 partly).

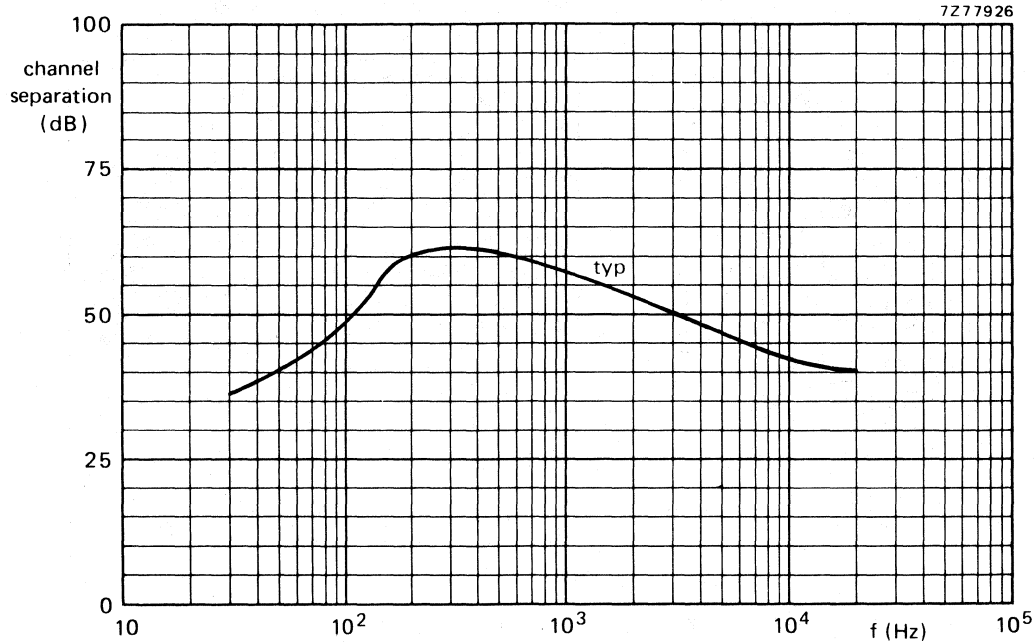


Fig. 20 Channel separation of the circuit of Fig. 17 as a function of frequency.

2 TO 6 W AUDIO POWER AMPLIFIER

The TDA1011 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The device can deliver up to 6 W into 4 Ω at 16 V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24 V makes this circuit very suitable for d.c. and a.c. apparatus, while the very low applicable supply voltage of 3,6 V permits 6 V applications.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P	3,6 to 20	V
Peak output current	I_{OM}	max. 3	A
Output power at d_{tot} = 10%			
V_P = 16 V; R_L = 4 Ω	P_o	typ. 6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	typ. 4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ. 0,2	%
Input impedance			
preamplifier (pin 8)	$\lvert Z_i \rvert$	> 100	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ. 20	kΩ
Total quiescent current	I_{tot}	typ. 14	mA
Operating ambient temperature	T_{amb}	−25 to + 150	°C
Storage temperature	T_{stg}	−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

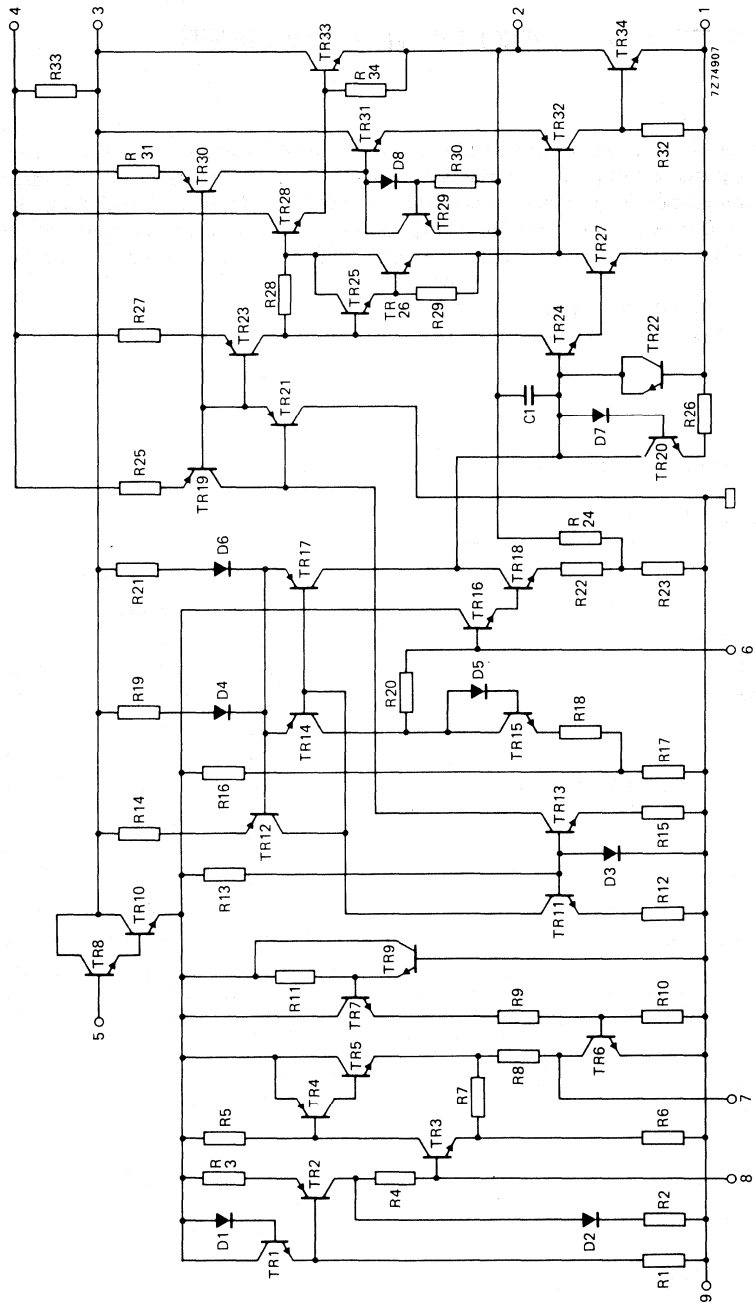


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24 V
Peak output current	I_{OM}	max.	3 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100 hours

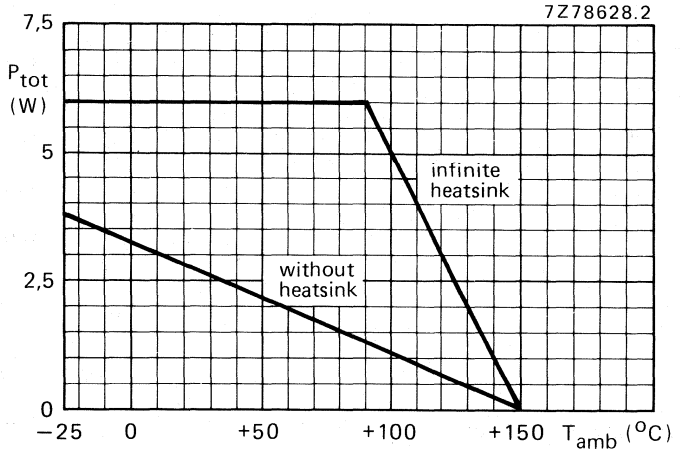


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 60 °C maximum; P_o = 3,8 W.

The maximum sine-wave dissipation is 1,8 W.

The derating of 10 K/W of the package requires the following external heatsink (for sine-wave drive):

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{1{,}8} = 50\ \text{K/W}.$$

Since $R_{th\ j\text{-}tab}$ = 10 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a} = 50 - (10 + 1) = 39$ K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P	3,6 to 20	V
Repetitive peak output current	I_{ORM}	< 2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ. 14 < 22	mA mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)			
with bootstrap:			
V_P = 16 V; R_L = 4 Ω	P_o	typ. 6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	> 3,6 typ. 4,2	W W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
without bootstrap:			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 3,0	W
Voltage gain:			
preamplifier (note 2)	G_{v1}	typ. 23 21 to 25	dB dB
power amplifier	G_{v2}	typ. 29 27 to 31	dB dB
total amplifier	$G_{v\,tot}$	typ. 52 50 to 54	dB dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ. 0,3 < 1	% %
Frequency response; −3 dB (note 3)	B	60 Hz to 15	kHz
Input impedance:			
preamplifier (note 4)	$\lvert Z_{i1} \rvert$	> 100 typ. 200	kΩ kΩ
power amplifier	$\lvert Z_{i2} \rvert$	typ. 20	kΩ
Output impedance preamplifier	$\lvert Z_{o1} \rvert$	typ. 1	kΩ
Output voltage preamplifier (r.m.s. value)			
d_{tot} < 1% (note 2)	$V_{o(rms)}$	> 0,7	V
Noise output voltage (r.m.s. value; note 5)			
R_S = 0 Ω	$V_{n(rms)}$	typ. 0,2	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ. 0,6 < 1,4	mV mV
Noise output voltage at f = 500 kHz (r.m.s. value)			
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ. 8	μV
Ripple rejection (note 6)			
f = 1 to 10 kHz	RR	typ. 42	dB
f = 100 Hz; C2 = 1 μF	RR	> 35	dB
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ. 35	mA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at P_o = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

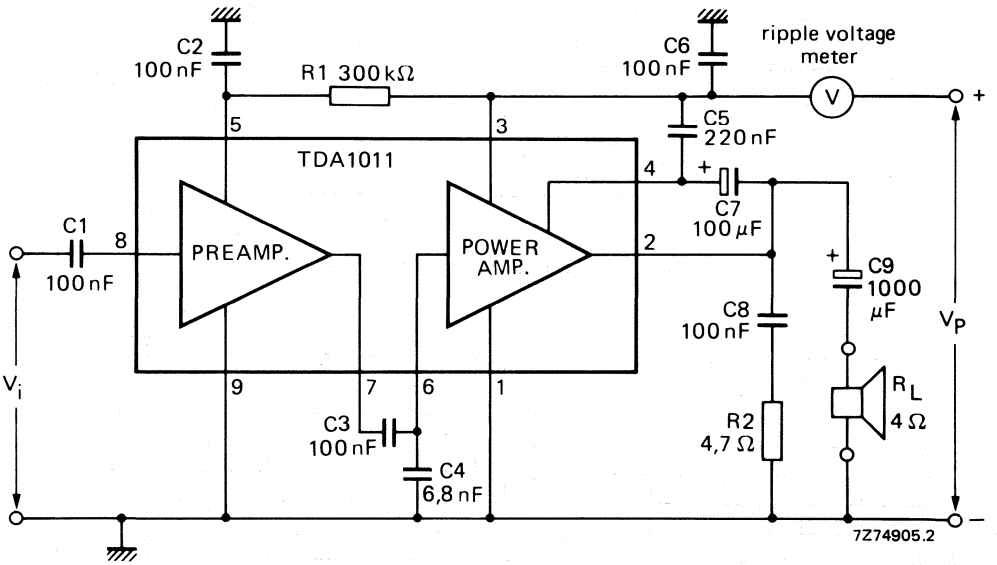


Fig. 3 Test circuit.

APPLICATION INFORMATION

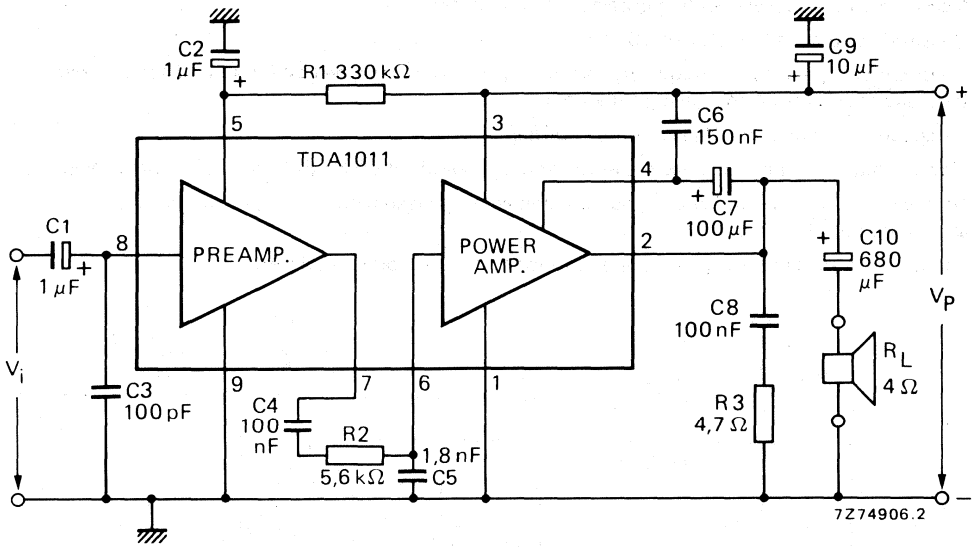


Fig. 4 Circuit diagram of a 4 W amplifier.

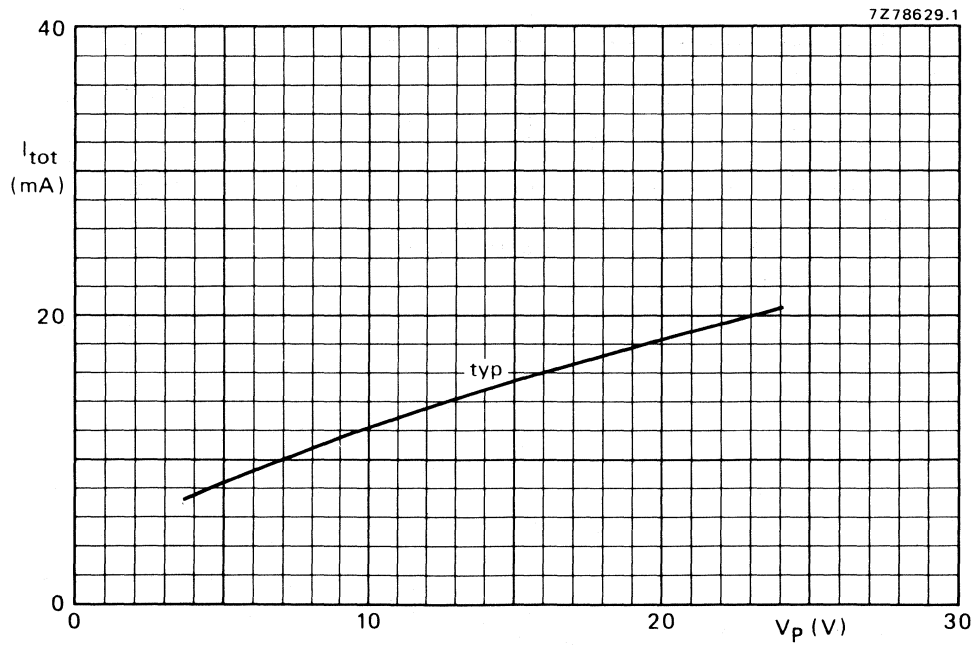


Fig. 5 Total quiescent current as a function of supply voltage.

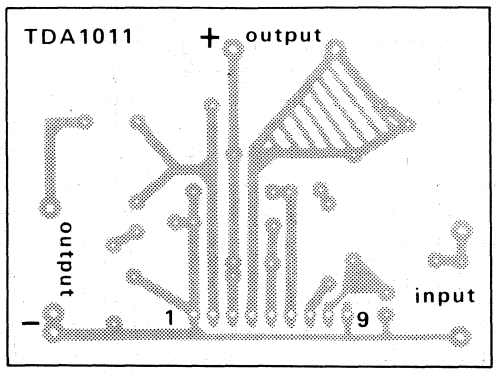


Fig. 6 Track side of printed-circuit board used for the circuit of Fig. 4; p.c. board dimensions 62 mm x 48 mm.

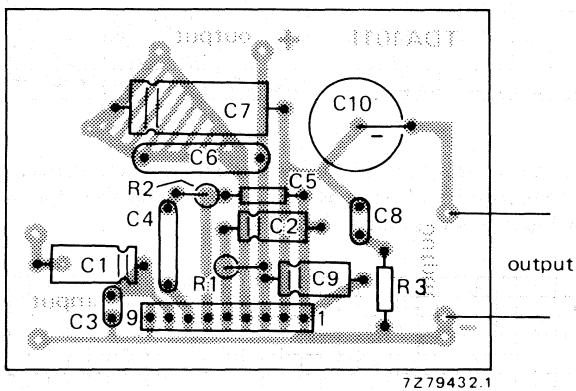


Fig. 7 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

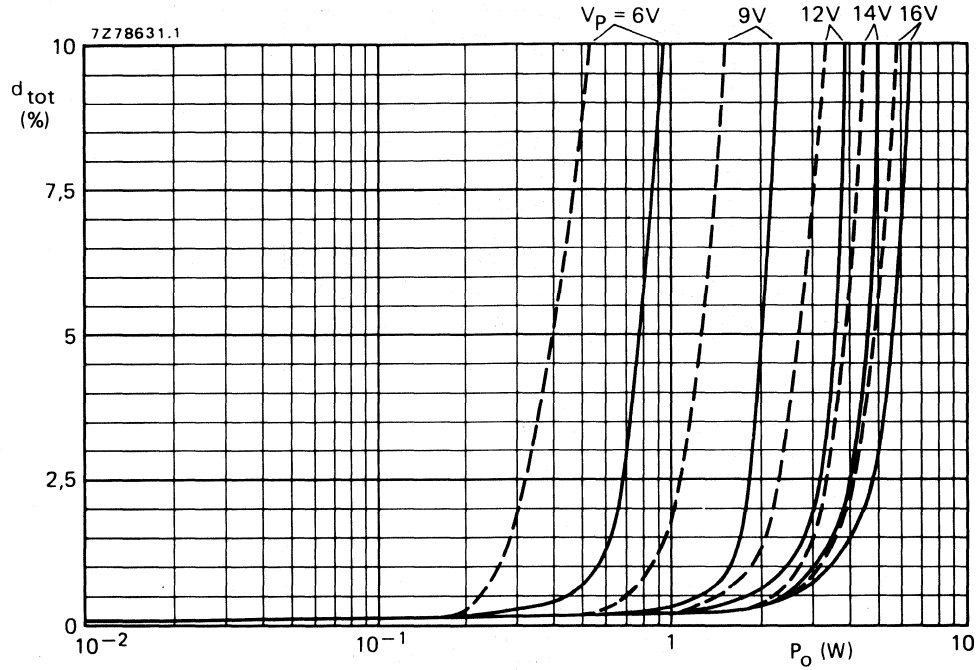


Fig. 8 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

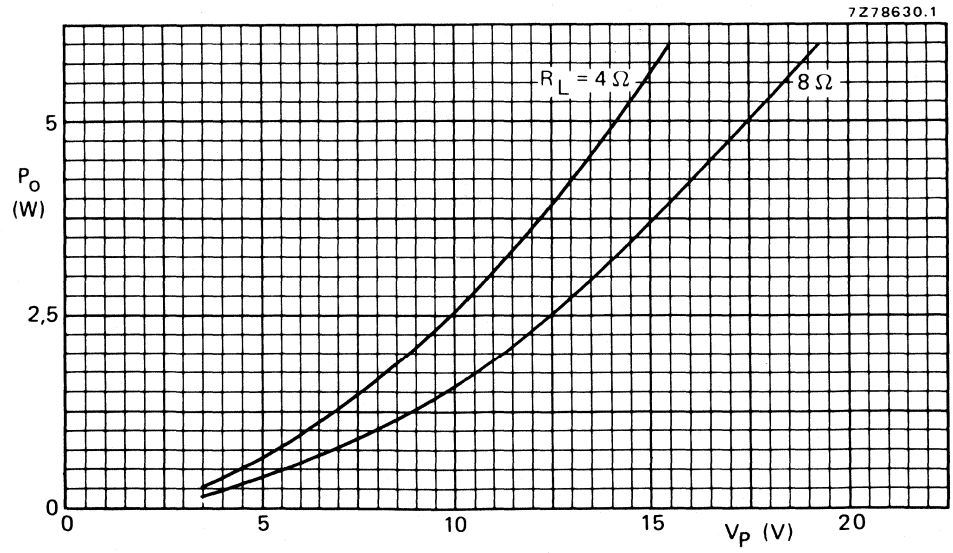


Fig. 9 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

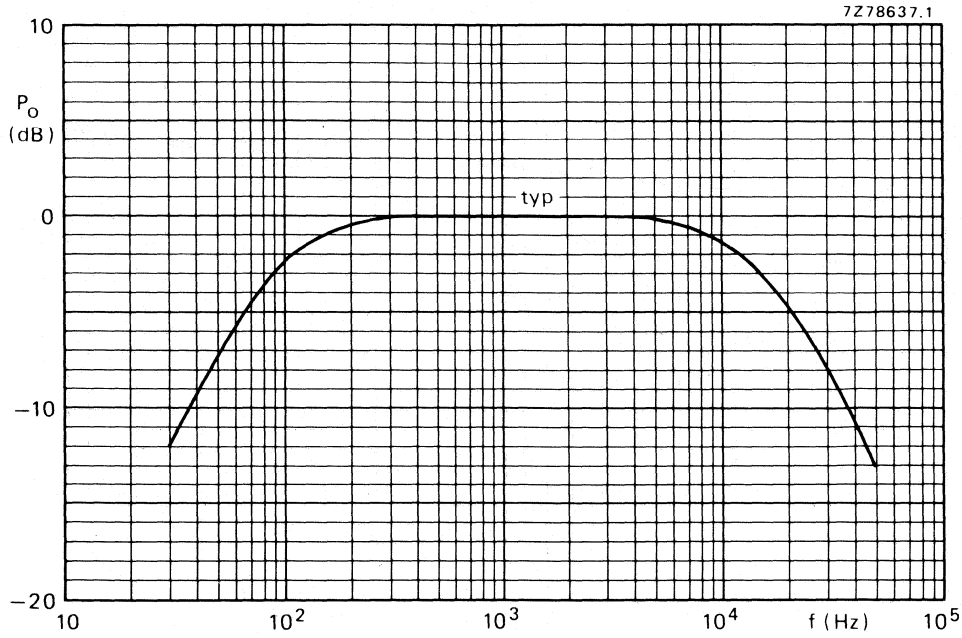


Fig. 10 Voltage gain as a function of frequency; P_o relative to 0 dB = 1 W; V_P = 12 V; R_L = 4 Ω.

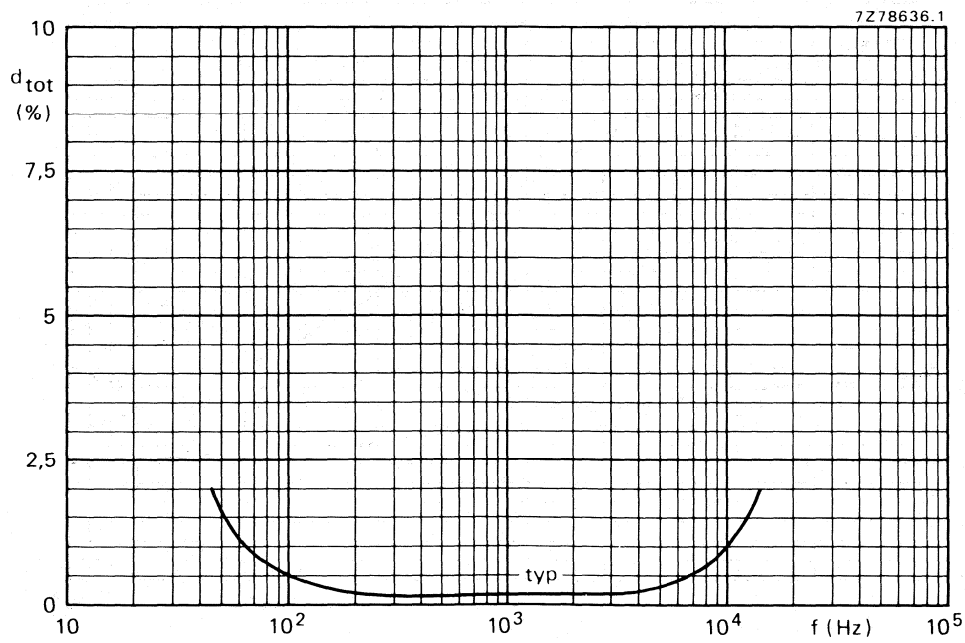


Fig. 11 Total harmonic distortion as a function of frequency; P_o = 1 W; V_P = 12 V; R_L = 4 Ω.

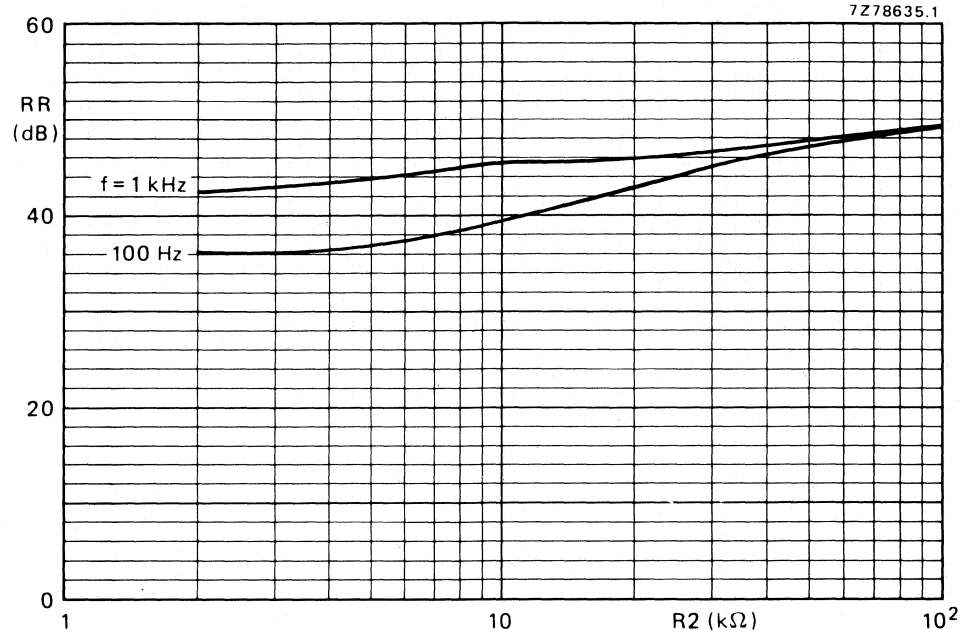


Fig. 12 Ripple rejection as a function of R2 (see Fig. 4); $R_S = 0$; typical values.

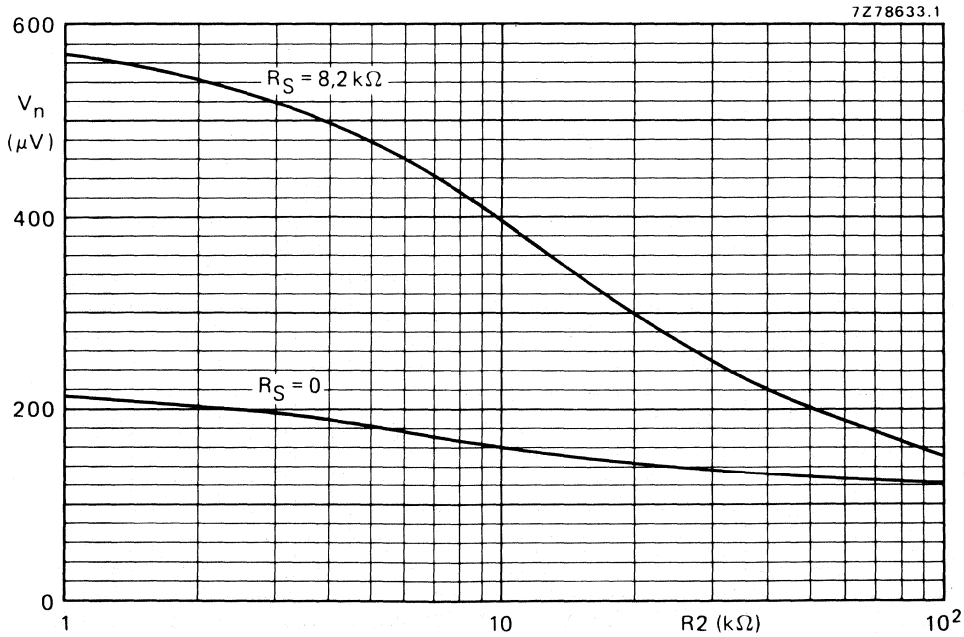


Fig. 13 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

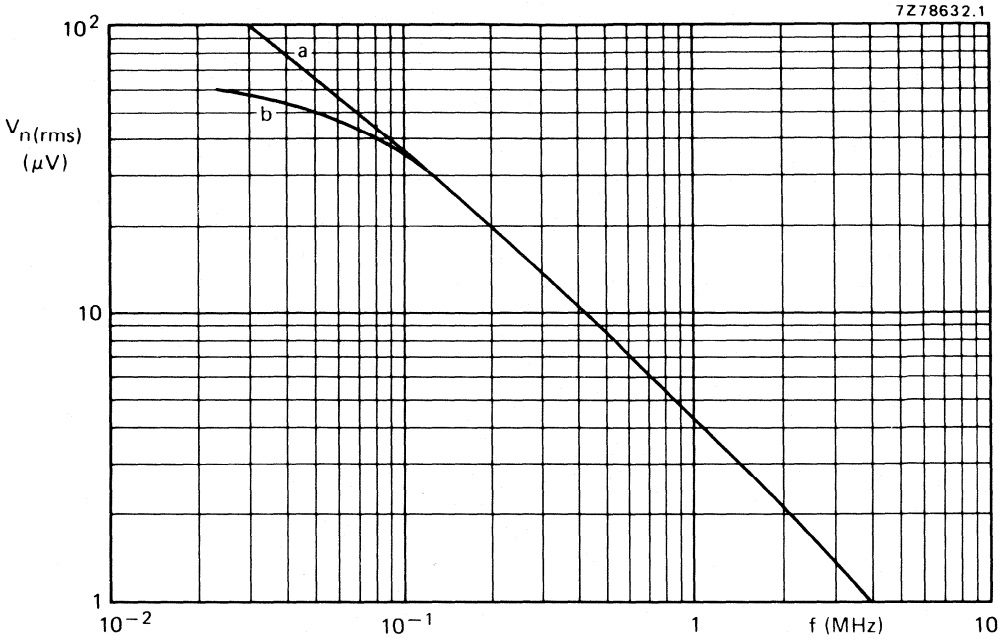


Fig. 14 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

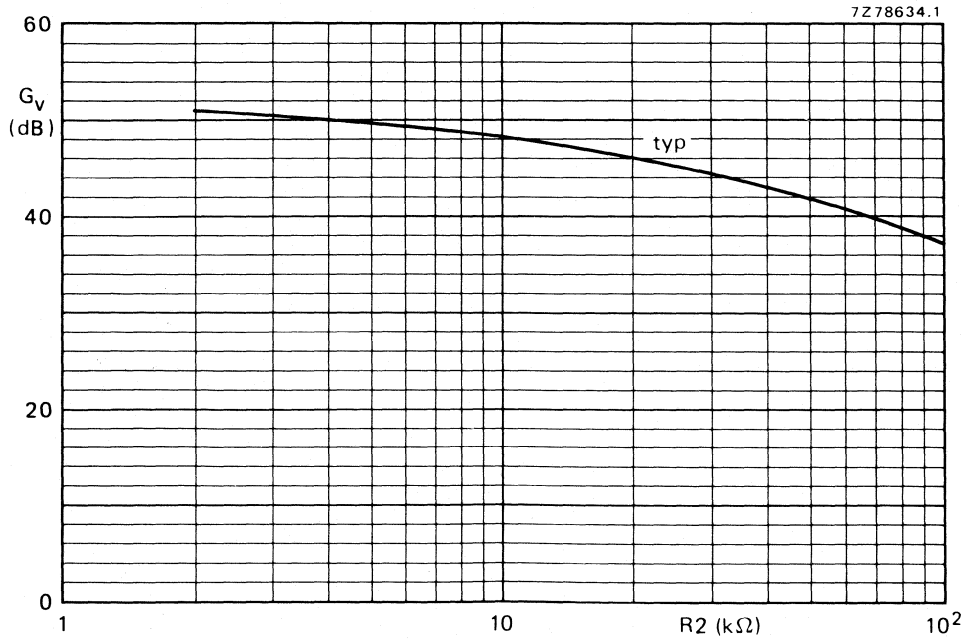


Fig. 15 Voltage gain as a function of R2 (see Fig. 4).

4 W AUDIO POWER AMPLIFIER WITH DC VOLUME CONTROL

GENERAL DESCRIPTION

The TDA1013B is an integrated audio amplifier circuit with DC volume control, encapsulated in a 9-lead single in-line (SIL) plastic package. The wide supply voltage range makes this circuit ideal for applications in mains and battery-fed apparatus such as television receivers and record players.

The DC volume control stage has a logarithmic control characteristic with a range of more than 80 dB; control is by means of a DC voltage variable between 2 and 6.5 V.

The audio amplifier has a well defined open loop gain and a fixed integrated closed loop. This device requires only a few external components and offers stability and performance.

Features

- Few external components
- Wide supply voltage range
- Wide control range
- Pin compatible with TDA1013A
- Fixed gain
- High signal-to-noise ratio
- Thermal protection

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10	18	40	V
Repetitive peak output current		I_{ORM}	–	–	1.5	A
Total sensitivity	P_o = 2.5 W; DC control at max. gain	V_i	44	55	69	mV
Audio amplifier						
Output power	THD = 10%; R_L = 8 Ω	P_o	4.0	4.2	–	W
Total harmonic distortion	P_o = 2.5 W; R_L = 8 Ω	THD	–	0.15	0.1	%
Sensitivity	P_o = 2.5 W	V_i	100	125	160	mV
DC volume control unit						
Gain control range		$\|\Delta G_v\|$	80	–	–	dB
Signal handling	THD < 1%; DC control = 0 dB	V_i	1.2	1.7	–	V
Sensitivity (pin 6)	V_o = 125 mV; max. voltage gain	V_i	39	45	55	mV
Input impedance (pin 8)		$\|Z_i\|$	23	29	35	kΩ

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

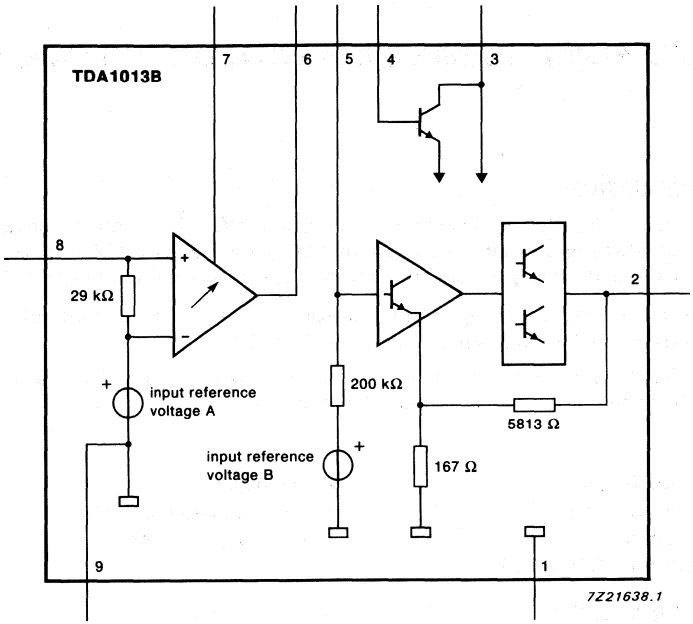


Fig.1 Block diagram.

PINNING

1 power ground
2 amplifier output
3 supply voltage
4 electronic filter
5 amplifier input
6 control unit output
7 control voltage
8 control unit input
9 signal ground (substrate)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	40	V
Non-repetitive peak output current	I_{OSM}	–	3	A
Repetitive peak output current	I_{ORM}	–	1.5	A
Storage temperature range	T_{stg}	–55	+ 150	°C
Crystal temperature	T_c	–	+ 150	°C
Total power dissipation	P_{tot}	see Fig. 2		

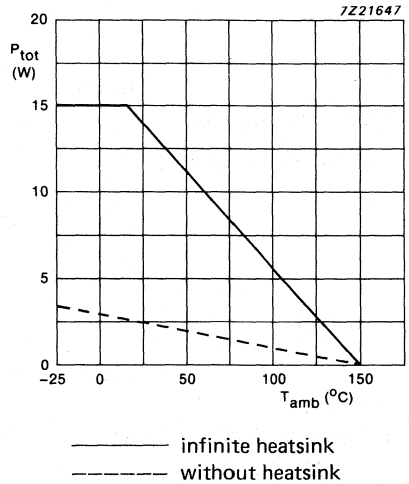


Fig.2 Power derating curve.

HEATSINK DESIGN EXAMPLE

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C; T_c = 150 °C (max.); for a 4 W application, the maximum dissipation is approximately 2.5 W. The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} =$$

$$\frac{T_{j\ max} - T_{amb\ max}}{P_{max}} = \frac{150 - 60}{2.5} = 36\ K/W$$

Since $R_{th\ j\text{-}tab}$ = 9 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 36 – (9 + 1) = 26 K/W.

CHARACTERISTICS

V_P = 18 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; see Fig.10; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	10	18	40	V
Total quiescent current		I_{tot}	–	25	60	mA
Noise output voltage	note 1					
at maximum gain	R_S = 0 Ω	V_n	–	0.5	–	mV
at maximum gain	R_S = 5 kΩ	V_n	–	0.6	1.4	mV
at minimum gain	R_S = 0 Ω	V_n	–	0.25	–	mV
Total sensitivity	P_o = 2.5 W; DC control at max. gain	V_i	44	55	69	mV
Audio amplifier						
Repetitive peak output current		I_{ORM}	–	–	1.5	A
Output power	THD = 10%; R_L = 8 Ω	P_o	4.0	4.2	–	W
Total harmonic distortion	P_o = 2.5 W; R_L = 8 Ω	THD	–	0.15	1.0	%
Sensitivity	P_o = 2.5 W	V_i	100	125	160	mV
Input impedance (pin 5)		$\|Z_i\|$	100	200	500	kΩ
Power bandwidth		B_P	–	30 to 40 000	–	Hz
DC volume control unit						
Gain control range		$\|\Delta G_v\|$	80	90	–	dB
Signal handling	THD < 1%; DC control = 0 dB	V_i	1.2	1.7	–	V
Sensitivity (pin 6)	V_o = 125 mV; max. voltage gain	V_i	39	44	55	mV
Input impedance (pin 8)		$\|Z_i\|$	23	29	35	kΩ
Output impedance (pin 6)		$\|Z_o\|$	45	60	75	Ω

Note to the characteristics

1. Measured in a bandwidth in accordance with IEC 179, curve 'A'.

APPLICATION INFORMATION

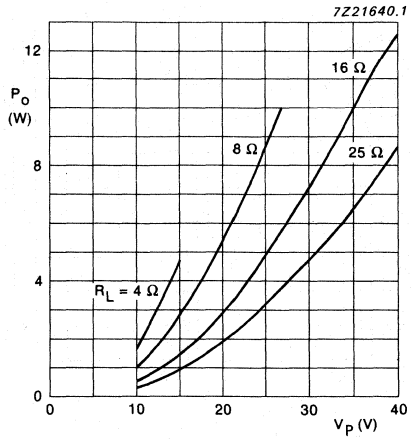


Fig.3 Output power as a function of supply voltage; f = 1 kHz; THD = 10% and control voltage (V_7) = 6.5 V.

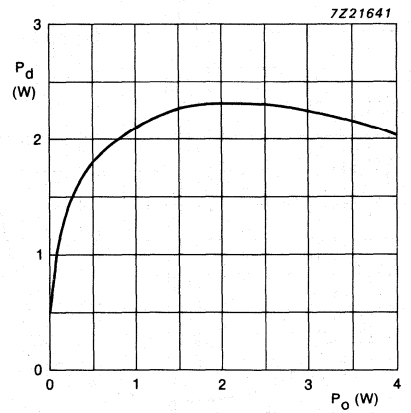


Fig.4 Power dissipation as a function of output power; V_P = 18 V; f = 1 kHz; R_L = 8 Ω and control voltage (V_7) = 6.5 V.

APPLICATION INFORMATION (continued)

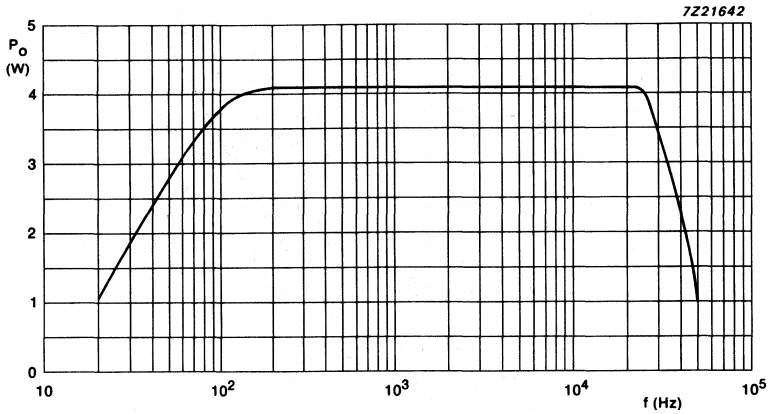


Fig.5 Power bandwidth; V_P = 18 V; R_L = 8 Ω; THD = 10% and control voltage (V_7) = 6.5 V.

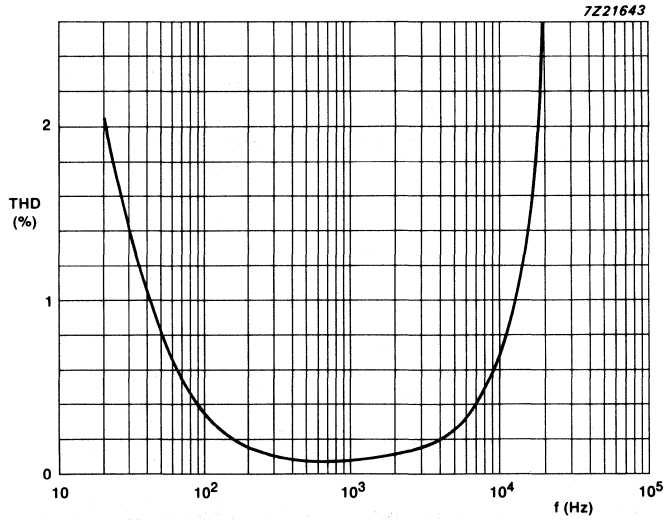


Fig.6 Total harmonic distortion as a function of frequency; V_P = 18 V; R_L = 8 Ω; P_o = 2.5 W and control voltage = 6.5 V.

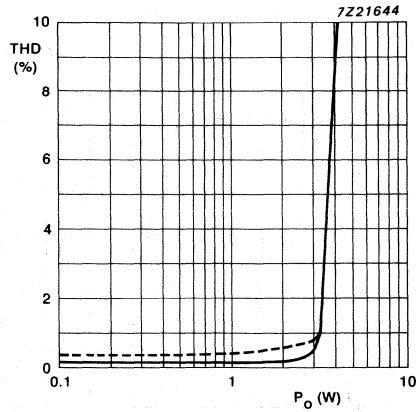


Fig.7 Total harmonic distortion as a function of output power; V_P = 18 V; R_L = 8 Ω and control voltage = 6.5 V.

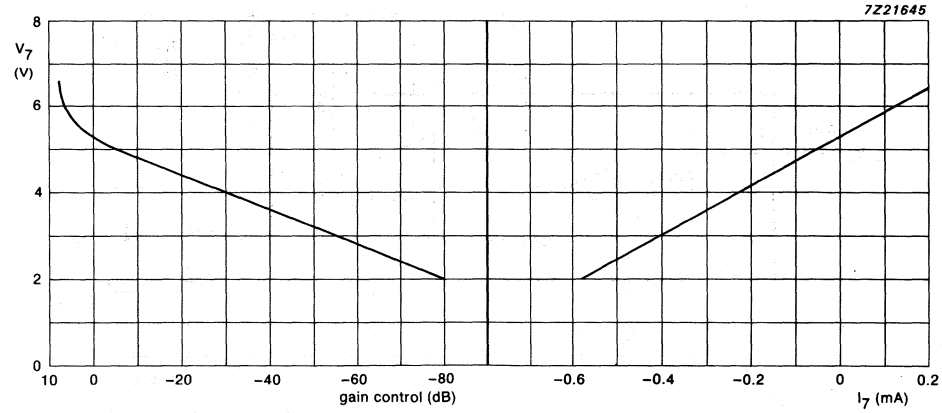


Fig.8 Typical control curve.

APPLICATION INFORMATION (continued)

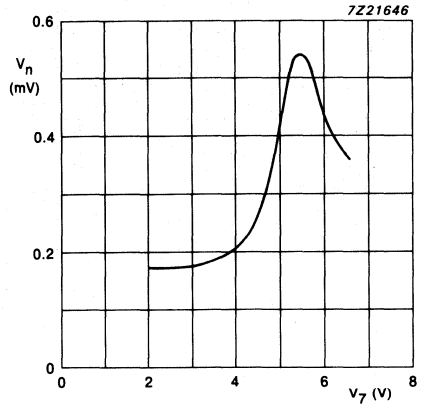
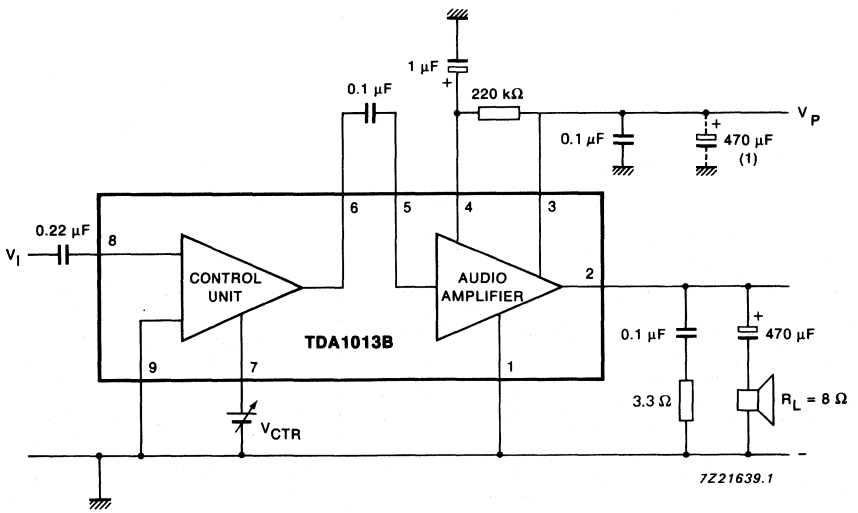


Fig.9 Noise output voltage as a function of the control voltage; V_P = 18 V; R_L = 8 Ω (in accordance with IEC 179, curve 'A').



(1) Belongs to power supply circuitry.

Fig.10 Application diagram.

1 TO 4 W AUDIO POWER AMPLIFIER

The TDA1015 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The very low applicable supply voltage of 3,6 V permits 6 V applications.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P	3,6 to 18	V
Peak output current	I_{OM}	max. 2,5	A
Output power at d_{tot} = 10%			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ. 0,3	%
Input impedance			
preamplifier (pin 8)	$\|Z_i\|$	> 100	kΩ
power amplifier (pin 6)	$\|Z_i\|$	typ. 20	kΩ
Total quiescent current	I_{tot}	typ. 14	mA
Operating ambient temperature	T_{amb}	−25 to + 150	°C
Storage temperature	T_{stg}	−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

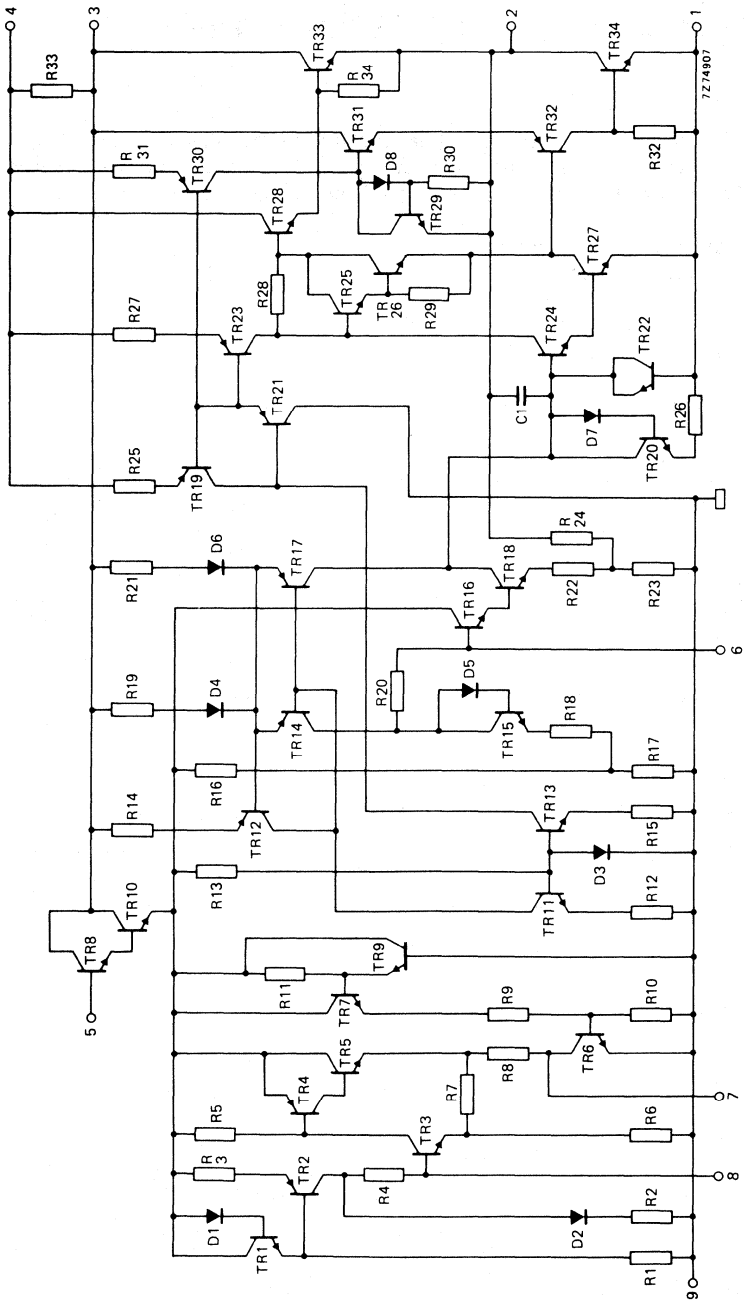


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Peak output current	I_{OM}	max.	2,5	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}	−55 to + 150		°C
Operating ambient temperature	T_{amb}	−25 to + 150		°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100	hours

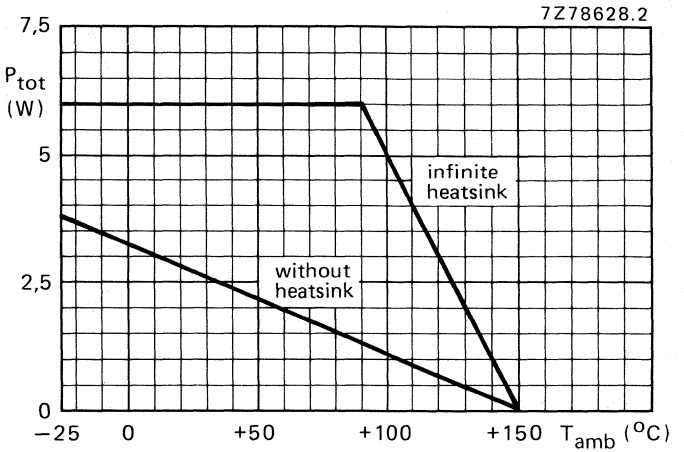


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 45 °C maximum.

The maximum sine-wave dissipation is 1,8 W.

$$R_{th\,j\text{-}a} = R_{th\,j\text{-}tab} + R_{th\,tab\text{-}h} + R_{th\,h\text{-}a} = \frac{150 - 45}{1,8} = 58 \text{ K/W}.$$

Where $R_{th\,j\text{-}a}$ of the package is 45 K/W, so no external heatsink is required.

D.C. CHARACTERISTICS

Supply voltage range	V_P	3,6 to 18	V
Repetitive peak output current	I_{ORM}	< 2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ. 14 < 25	mA mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)			
with bootstrap:			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
without bootstrap:			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 3,0	W
Voltage gain:			
preamplifier (note 2)	G_{v1}	typ. 23	dB
power amplifier	G_{v2}	typ. 29	dB
total amplifier	$G_{v\,tot}$	typ. 52 49 to 55	dB dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ. 0,3 < 1,0	% %
Frequency response; −3 dB (note 3)	B	60 Hz to 15	kHz
Input impedance:			
preamplifier (note 4)	$\lvert Z_{i1} \rvert$	> 100 typ. 200	kΩ kΩ
power amplifier	$\lvert Z_{i2} \rvert$	typ. 20	kΩ
Output impedance preamplifier	$\lvert Z_{o1} \rvert$	typ. 1	kΩ
Output voltage preamplifier (r.m.s. value)			
d_{tot} < 1% (note 2)	$V_{o(rms)}$	typ. 0,8	V
Noise output voltage (r.m.s. value; note 5)			
R_S = 0 Ω	$V_{n(rms)}$	typ. 0,2	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ. 0,5	mV
Noise output voltage at f = 500 kHz (r.m.s. value)			
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ. 8	μV
Ripple rejection (note 6)			
f = 100 Hz	RR	typ. 38	dB

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at P_o = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

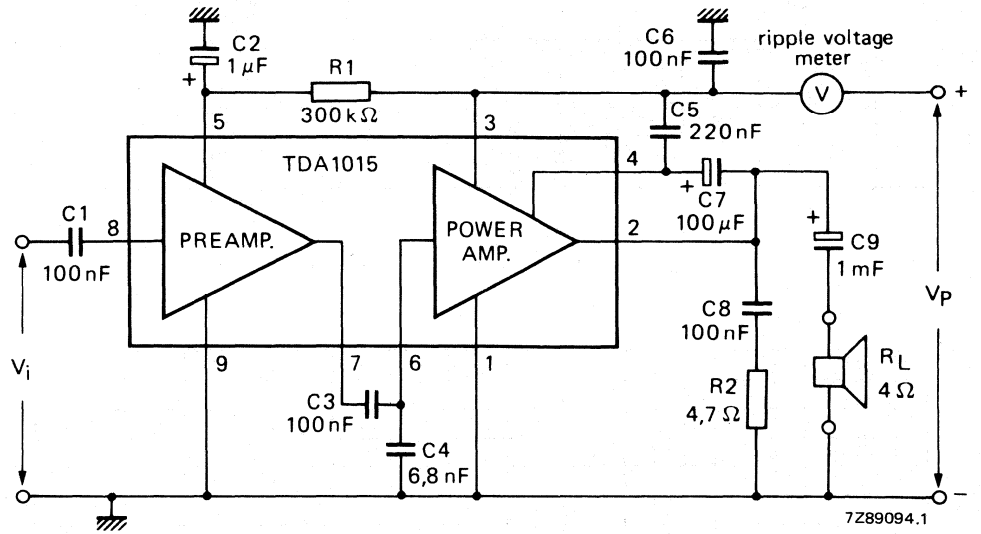


Fig. 3 Test circuit.

APPLICATION INFORMATION

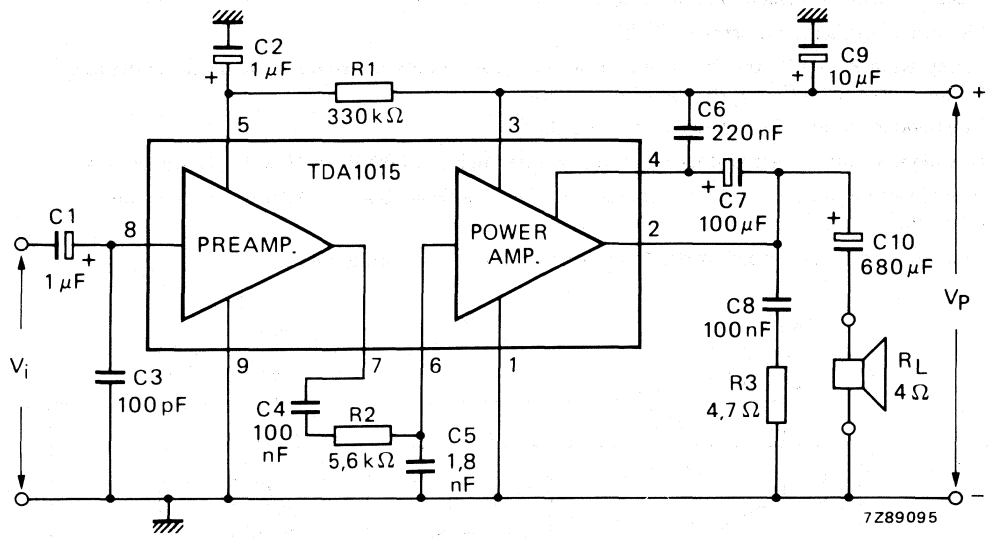


Fig. 4 Circuit diagram of a 1 to 4 W amplifier.

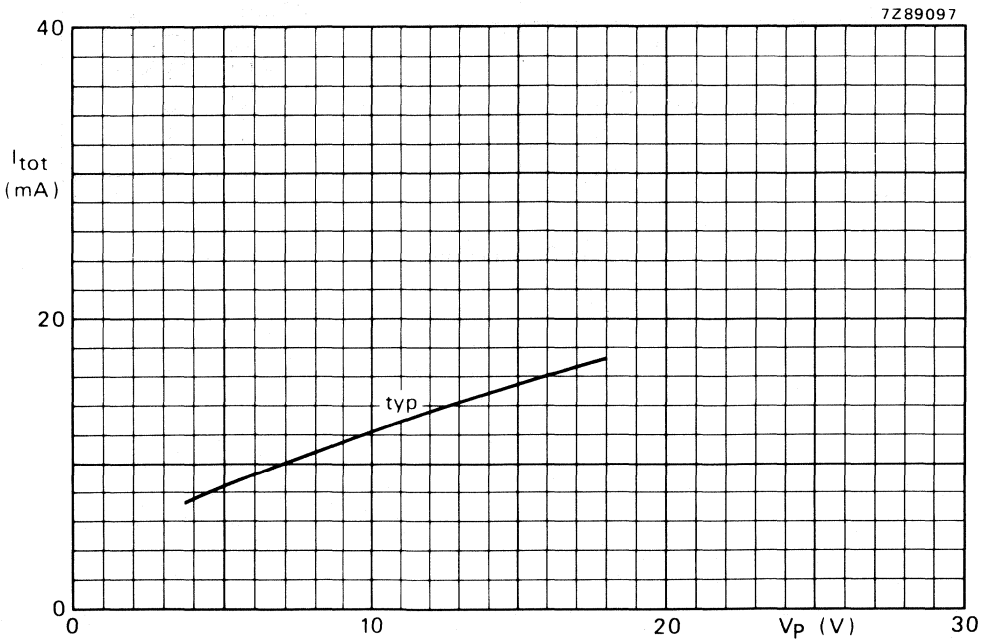


Fig. 5 Total quiescent current as a function of supply voltage.

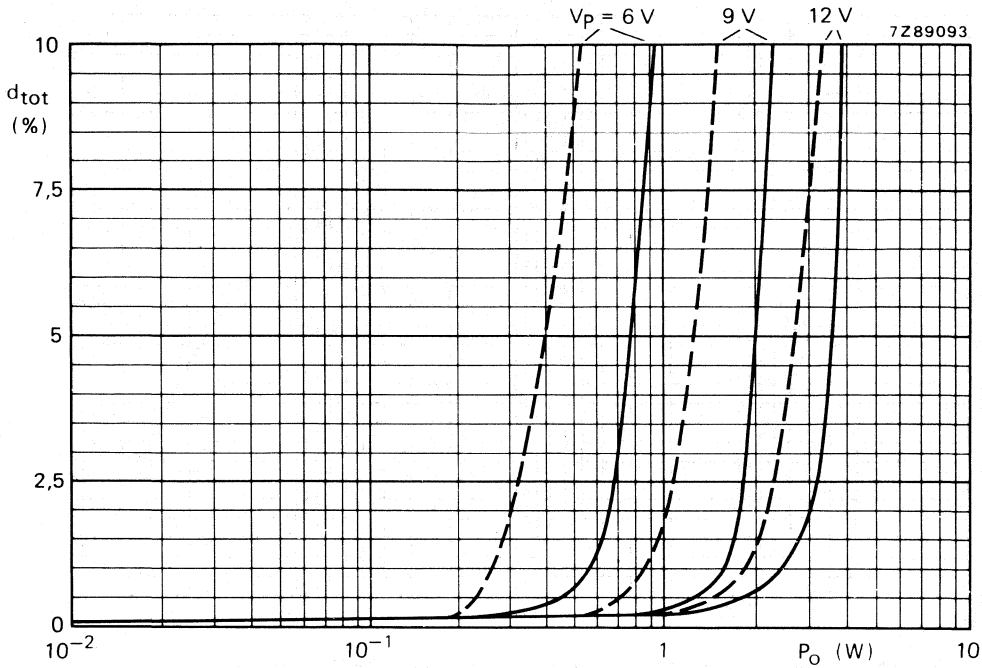


Fig. 6 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; — — — without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

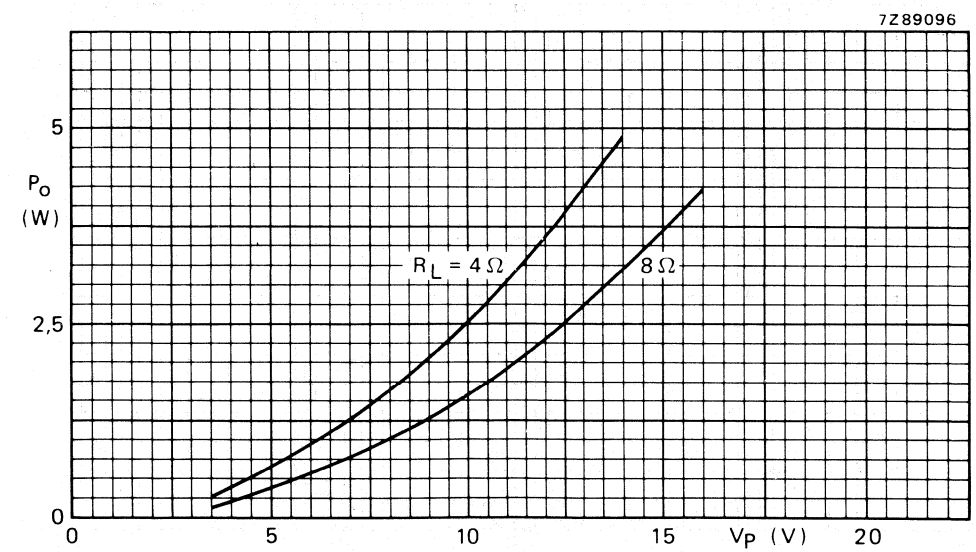


Fig. 7 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

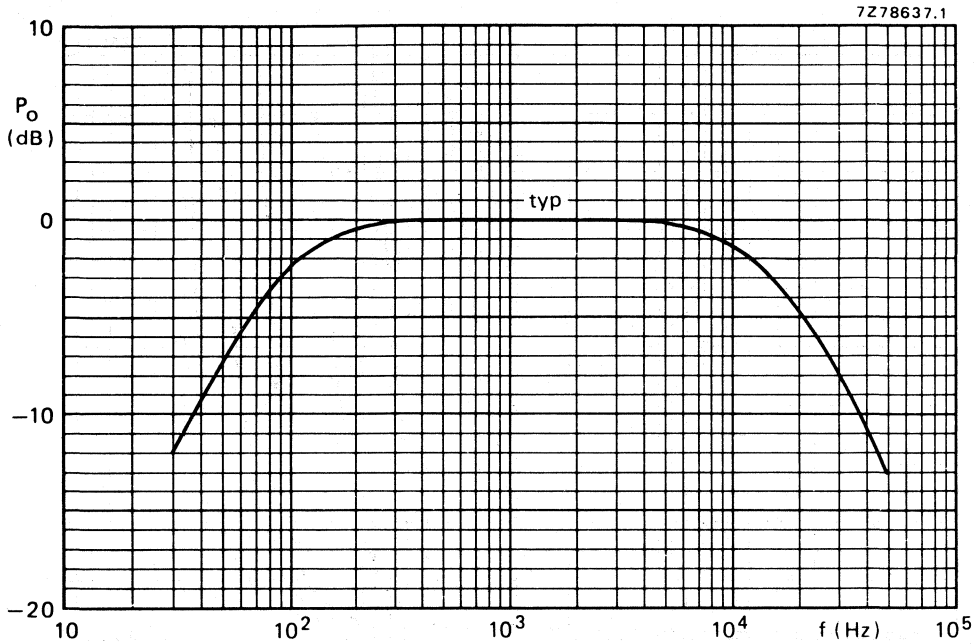


Fig. 8 Voltage gain as a function of frequency; P_o relative to 0 dB = 1 W; V_P = 12 V; R_L = 4 Ω.

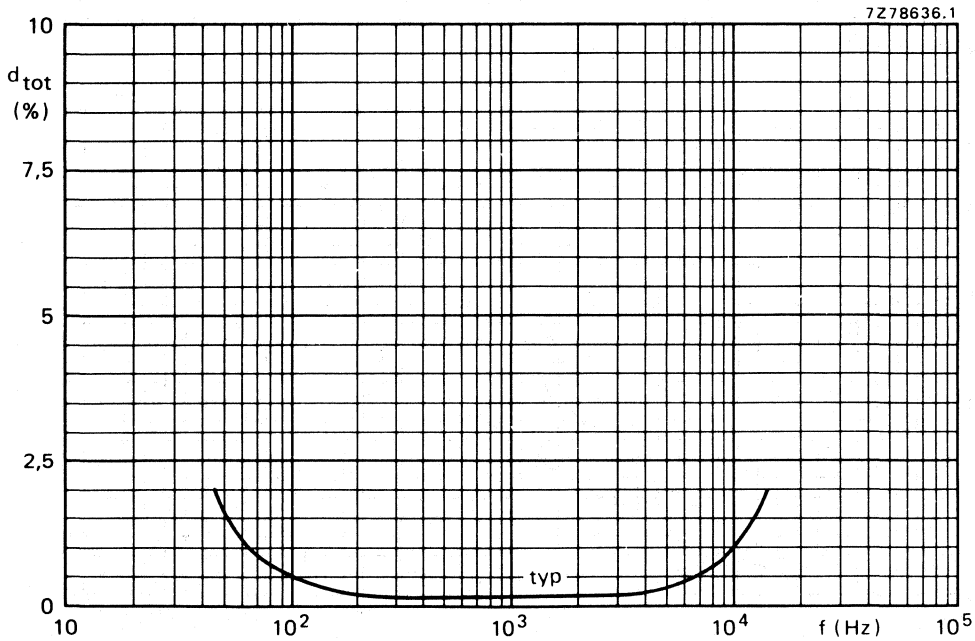


Fig. 9 Total harmonic distortion as a function of frequency; P_o = 1 W; V_P = 12 V; R_L = 4 Ω.

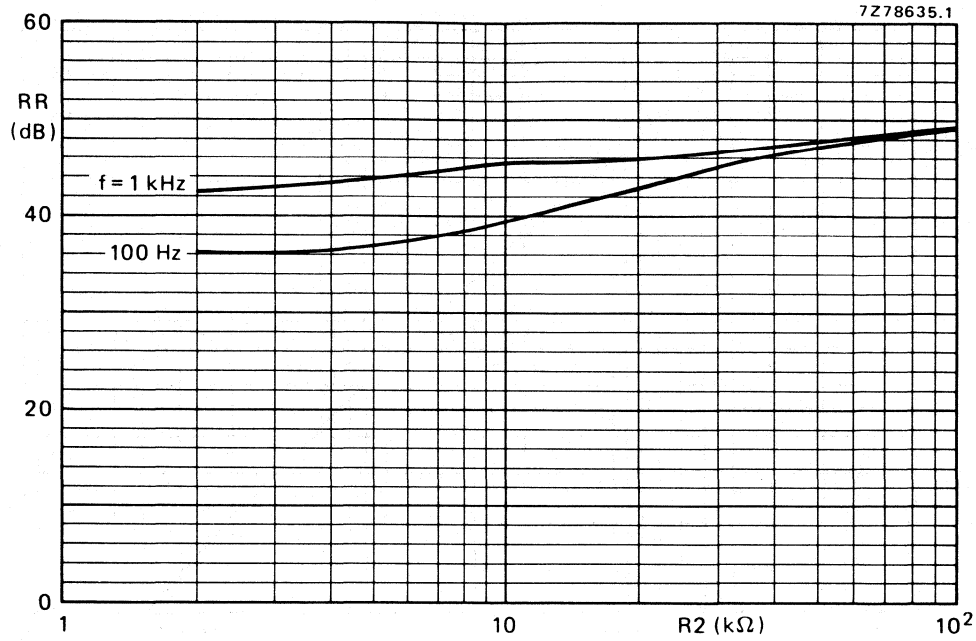


Fig. 10 Ripple rejection as a function of R2 (see Fig. 4); $R_S = 0$; typical values.

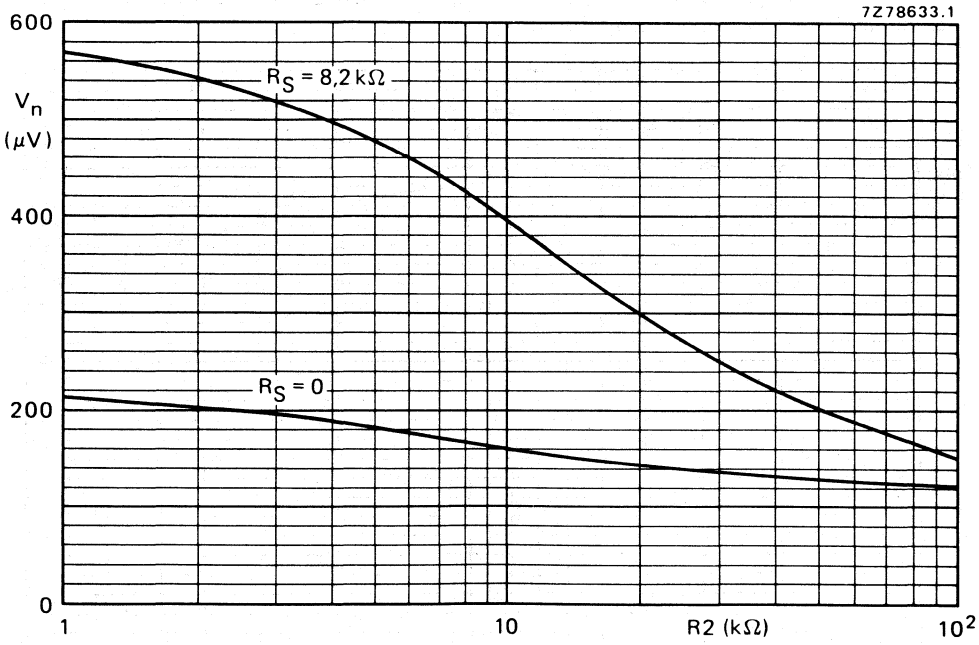


Fig. 11 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

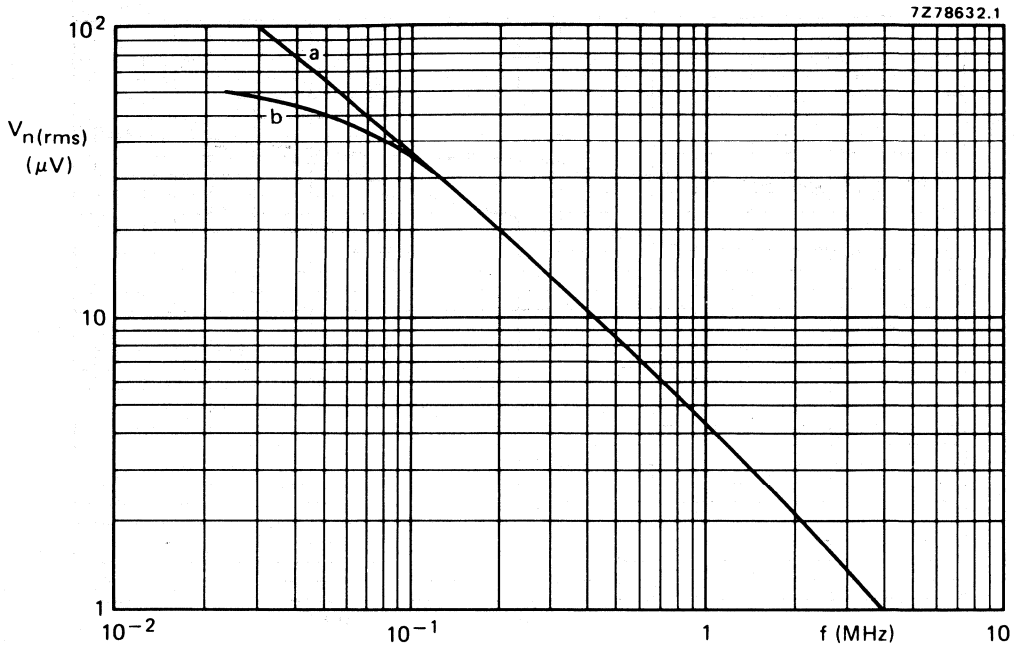


Fig. 12 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

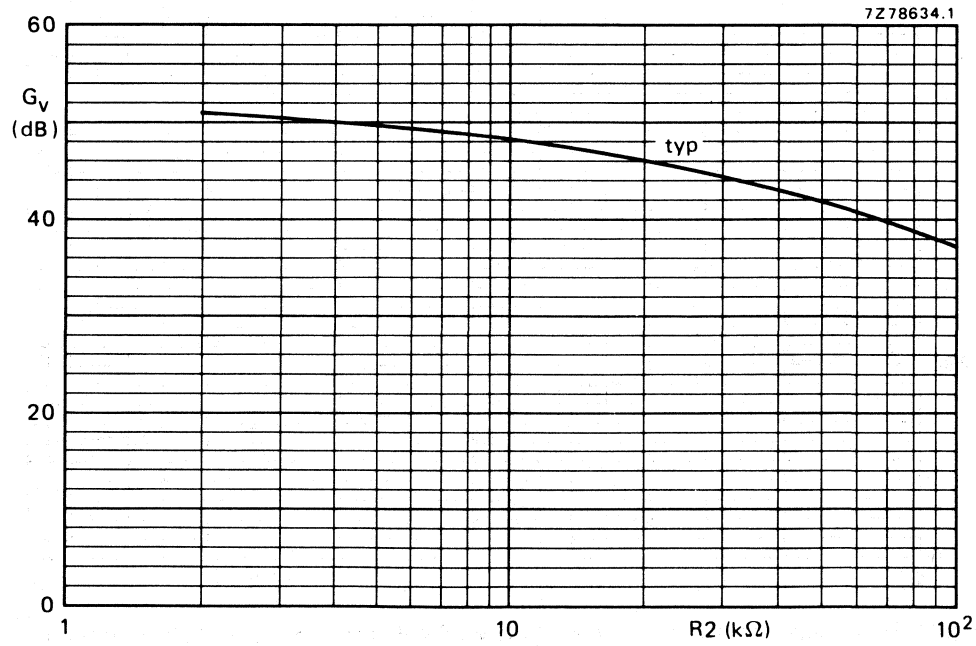


Fig. 13 Voltage gain as a function of R2 (see Fig. 4).

0,5 W AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1015T is a low-cost audio amplifier which can deliver up to 0,5 W output power into a 16 Ω load impedance at a supply voltage of 9 V. The amplifier is specially designed for portable applications such as radios and recorders. The IC has a very low supply voltage requirement (3,6 V min.).

Features

- High input impedance
- Separated preamplifier and power amplifier
- Limited noise behaviour at radio frequencies
- Short-circuit protected
- Miniature encapsulation

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 12	V
Peak output current	I_{OM}	max.	1	A
Output power	P_o	typ.	0,5	W
Voltage gain power amplifier	G_{v1}	typ.	29	dB
Voltage gain preamplifier	G_{v2}	typ.	23	dB
Total quiescent current	I_{tot}	max.	22	mA
Operating ambient temperature range	T_{amb}		−25 to +150	°C
Storage temperature range	T_{stg}		−55 to +150	°C

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

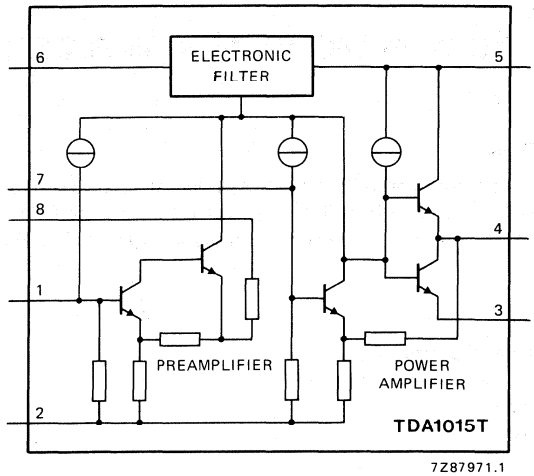


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	12 V
Peak output current	I_{OM}	max.	1 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range			−55 to +150 °C
A.C. short-circuit duration of load during sine-wave drive at V_P = 9 V	t_{sc}	max.	1 hour

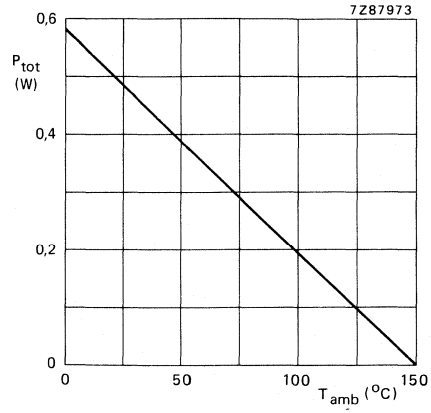


Fig. 2 Power derating curve.

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 9 V; R_L = 16 Ω; f = 1 kHz; see Fig. 3; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_P	3,6	9	12	V
Repetitive peak output current	I_{ORM}	–	–	1	A
Total quiescent current	I_{tot}	–	12	22	mA
A.F. output power at d_{tot} = 10% (note 1)					
V_P = 9 V; R_L = 16 Ω	P_o	–	0,5	–	W
V_P = 6 V; R_L = 8 Ω	P_o	–	0,3	–	W
Voltage gain power amplifier	G_{v1}	–	29	–	dB
Voltage gain preamplifier (note 2)	G_{v2}	–	23	–	dB
Total voltage gain	G_{tot}	49	52	55	dB
Frequency response at −3 dB (note 3)	B	–	60 to 15 000	–	Hz
Input impedance power amplifier	$\|Z_{i1}\|$	–	20	–	kΩ
Input impedance preamplifier (note 4)	$\|Z_{i2}\|$	100	200	–	kΩ
Output impedance preamplifier	$\|Z_{o2}\|$	0,5	1	1,5	kΩ
Output voltage preamplifier (r.m.s. value) d_{tot} < 1% (note 2)	$V_{o2(rms)}$	–	0,7	–	V
Noise output voltage (r.m.s. value) (note 5)					
R_S = 0 Ω	$V_{n(rms)}$	–	0,2	–	mV
R_S = 10 kΩ	$V_{n(rms)}$	–	0,5	–	mV
Noise output voltage (r.m.s. value) f = 500 kHz; B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	–	8	–	μV
Ripple rejection at f = 100 Hz; C2 = 1 μF (note 6)	RR	–	38	–	dB

Notes to the characteristics

1. Output power is measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistance of 20 kΩ.
3. The frequency response is mainly determined by the capacitors, C1, C3 (low frequency) and C4 (high frequency).
4. Independent of load impedance of preamplifier.
5. Effective unweighted r.m.s. noise voltage measured in a bandwidth from 60 Hz to 15 kHz (slopes 12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude of 2 V).

APPLICATION INFORMATION

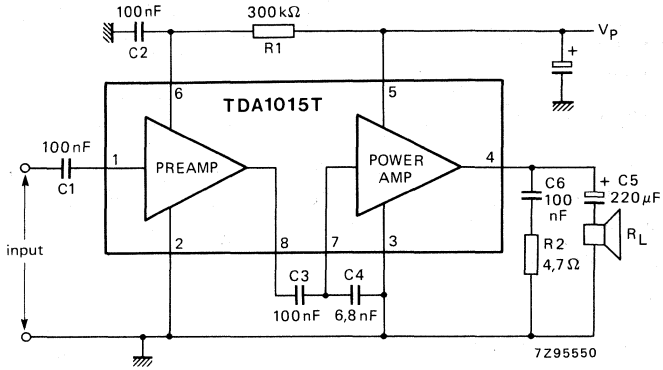


Fig. 3 Test circuit.

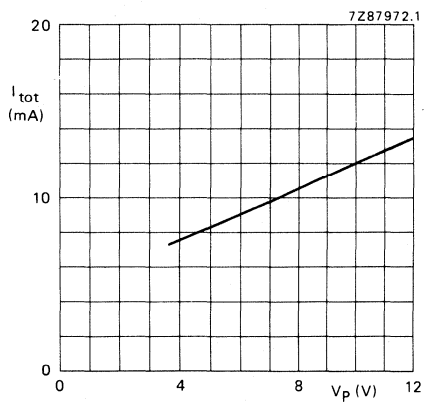


Fig. 4 Total quiescent current as a function of supply voltage.

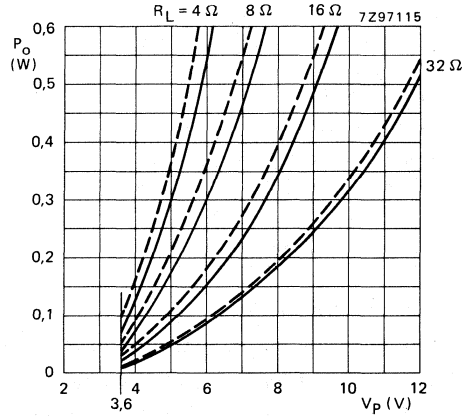


Fig. 5 Output power as a function of supply voltage; d_{tot} = 10%; f = 1 kHz.
——— measured in Fig. 3
– – – – measured with a 1,5 MΩ resistor connected between pins 7 and 2.

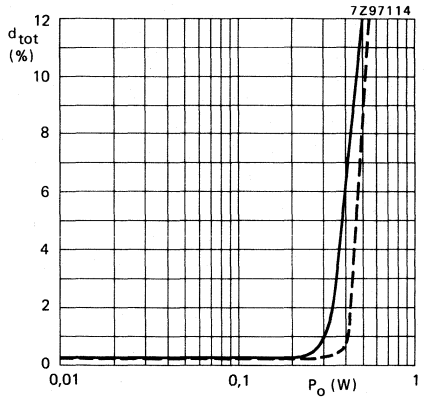


Fig. 6 Total distortion as a function of output power; V_P = 9 V; R_L = 16 Ω; f = 1 kHz.
——— measured in Fig. 3
– – – – – measured with a 1,5 MΩ resistor connected between pins 7 and 2.

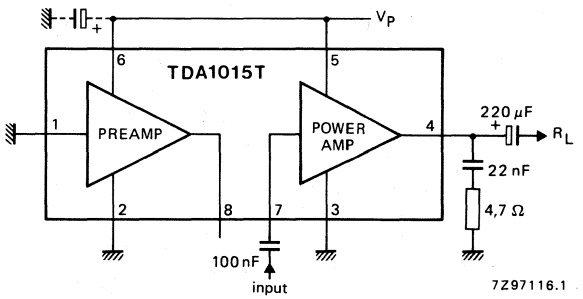


Fig. 7 Application circuit for power stage only and battery power supply; G_{v1} = 29 dB; $|Z_{i1}|$ = 20 kΩ.

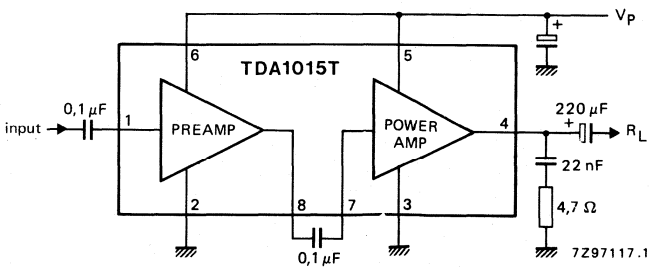


Fig. 8 Application circuit for preamplifier and power amplifier stages and battery power supply; $G_{v\,tot}$ = 52 dB; $|Z_{i2}|$ = 200 kΩ.

RECORDING/PLAYBACK AND 2 W AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1016 is a monolithic integrated audio power amplifier, preamplifier and A.L.C. circuit designed for applications in radio-recorders and recorders. The wide supply voltage range makes this circuit very suitable for d.c. and a.c. apparatus. The circuit incorporates the following features:

Features

- Power amplifier/monitor amplifier
- Preamplifier/record and playback amplifier
- Automatic Level Control (A.L.C.) circuit
- Voltage stabilizer
- Short-circuit (up to 12 V a.c.) and thermal protection.

QUICK REFERENCE DATA

Supply voltage range	V_P	3,6 to 15	V
Supply current; total quiescent at V_P = 6 V	I_{tot}	typ. 10	mA
Operating ambient temperature range	T_{amb}	−25 to 150	°C
Power amplifier			
Output power at d_{tot} = 10%			
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2	W
Closed loop gain	G_c	typ. 36	dB
Preamplifier			
Open loop gain	G_o	min. 70	dB
Minimum closed loop voltage gain	$G_{c\,min}$	min. 35	dB
Output voltage at d_{tot} = 1%	V_o	min. 1	V
Automatic Level Control (A.L.C.)			
Gain variation for ΔV_i = 40 dB	ΔG_v	typ. 2	dB
Stabilized supply voltage			
Output voltage	$V_{5\text{-}16}$	typ. 2,6	V

PACKAGE OUTLINE

16-lead DIL; plastic, with internal heat spreader (SOT38).

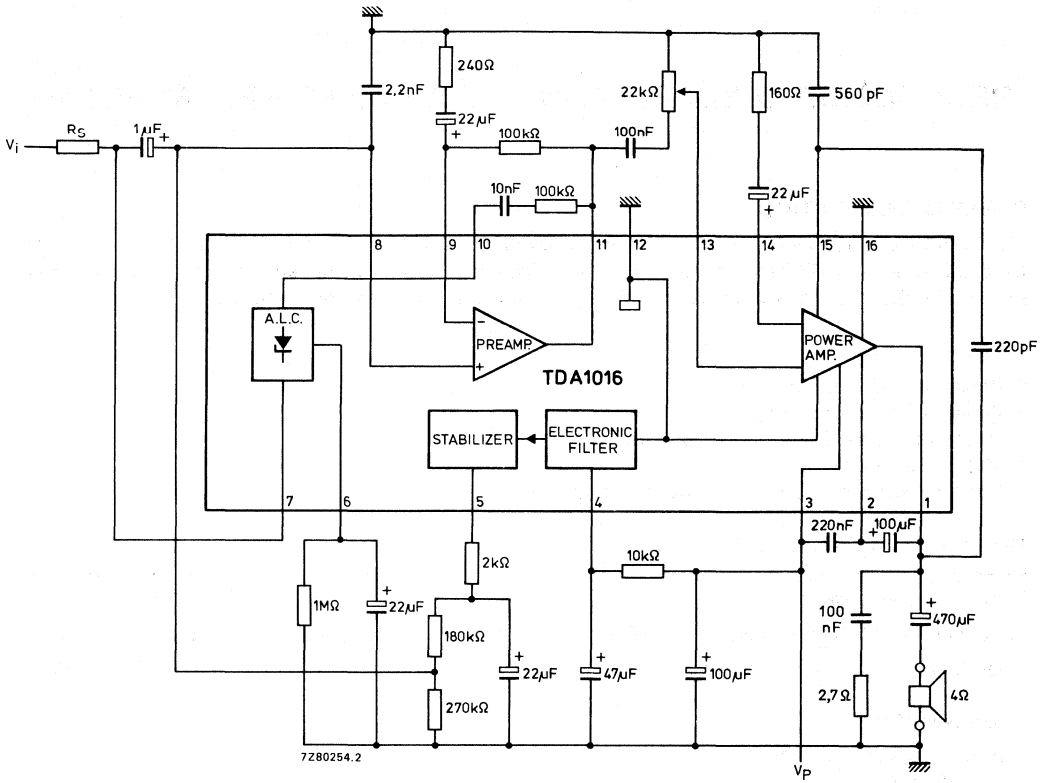


Fig. 1 Block diagram with external components; also used as test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 3)	V_P	max.	18	V
Repetitive peak output current	I_{ORM}	max.	1	A
Non-repetitive peak output current (pin 1)	I_{OSM}	max.	2	A
Total power dissipation	see derating curve Fig. 2			
A.C. short-circuit duration of load during sinewave drive; V_P = 12 V	t_{sc}	max.	100	hours
Crystal temperature	T_c	max.	150	°C
Storage temperature range	T_{stg}	−55 to +	150	°C
Operating ambient temperature range	T_{amb}	−25 to +	150	°C

THERMAL RESISTANCE

The power derating curve (Fig. 2) is based on the following data

From junction to ambient	$R_{th\ j\text{-}a}$	=	55	K/W

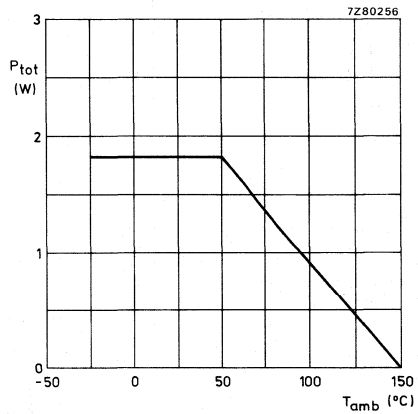


Fig. 2 Power derating curve.

CHARACTERISTICS

V_P = 6 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	V_P	3,6	6	15	V
Supply current; total quiescent at V_P = 6 V	I_{tot}	–	10	–	mA
Power amplifier					
Output power at d_{tot} = 10%*					
V_P = 6 V	P_o	–	1	–	W
V_P = 9 V	P_o	–	2	–	W
Closed loop voltage gain	G_c	–	36	–	dB
Total harmonic distortion at P_o = 0,5 W	d_{tot}	–	–	1	%
Input impedance	$\|Z_i\|$	0,5	–	–	MΩ
Ripple rejection at f = 100 Hz (R_S = 0 Ω)	RR	40	50	–	dB
Noise output voltage (r.m.s. value) R_S = 0 Ω; B = 60 Hz to 15 kHz	$V_{n(rms)}$	–	90	200	μV
Noise output voltage at 500 kHz R_S = 0 Ω; B = 5 kHz	V_n	–	8	–	μV
Preamplifier					
Open loop voltage gain at f = 10 kHz	G_o	70	78	–	dB
Closed loop voltage gain	G_c	–	52	–	dB
Minimum closed loop voltage gain (when changing R_f)	$G_{c\,min}$	35	–	–	dB
Output voltage at d_{tot} = 1%	V_o	1	–	–	V
Output voltage with A.L.C. V_i = 2 mV	V_o	0,45	0,5	0,55	V
Total harmonic distortion with A.L.C.					
V_i = 2 mV	d_{tot}	–	–	1	%
V_i = 360 mV	d_{tot}	–	–	3	%
Signal-to-noise ratio related to V_i = 1,2 mV; R_S = 1 kΩ; B = 60 Hz to 15 kHz	S/N	–	60	–	dB
Input impedance	$\|Z_i\|$	100	–	–	kΩ
Ripple rejection at f = 100 Hz; R_S = 0 Ω	RR	50	54	–	dB
Output impedance **	$\|Z_o\|$	–	–	50	Ω

* Measured with an ideal coupling capacitor connected to the speaker load.

** I_P (effective value) must not exceed 1 mA.

parameter	symbol	min.	typ.	max.	unit
Automatic Level Control (A.L.C.) (see Fig. 3)**					
Gain variation for ΔV_i = 45 dB	ΔG_v	–	2	3	dB
Limiting time*	t_l	–	–	50	ms
Level setting time*	t_s	–	–	50	ms
Recovery time* ▲	t_r	–	100	–	s
Voltage stabilizer					
Output voltage	$V_{11\text{-}15}$	–	2,6	–	V
Load current	I_{11}	–	–	1,5	mA
Ripple rejection at f = 100 Hz	RR	40	–	–	dB

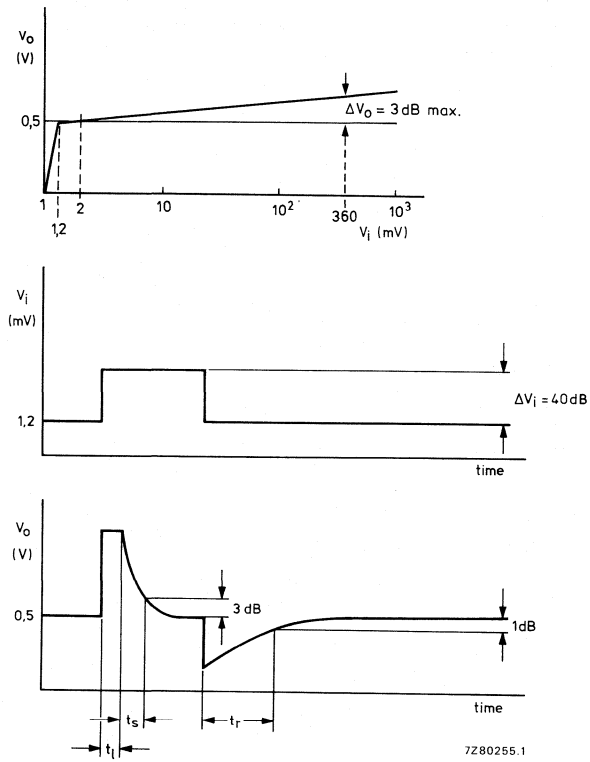


Fig. 3 Typical A.L.C. curve with R_S = 10 kΩ.

* At ΔV_i = 40 dB with respect to V_i = 1,2 mV.

** The A.L.C. tracking in stereo has a typical spread of 1 dB if pins 6 of both ICs are connected to the same RC network.

▲ Without a shunt resistor across A.L.C.
With 1 MΩ or 2,2 MΩ across A.L.C. recovery time becomes 22 or 50 seconds.

12 W CAR RADIO POWER AMPLIFIER

The TDA1020 is a monolithic integrated 12 W audio amplifier in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a car radio amplifier. At a supply voltage of V_P = 14,4 V, an output power of 7 W can be delivered into a 4 Ω load and 12 W into 2 Ω.

To avoid interferences and car ignition signals coming from the supply lines into the IC, frequency limiting is used beyond the audio spectrum in the preamplifier and the power amplifier.

The maximum supply voltage of 18 V makes the IC also suitable for mains-fed radio receivers, tape recorders or record players. However, if the supply voltage is increased above 18 V (< 45 V), the device will not be damaged (load dump protected). Also a short-circuiting of the output to ground (a.c.) will not destroy the device. Thermal protection is built-in. As a special feature, the circuit has a low stand-by current possibility.

The TDA1020 is pin-to-pin compatible with the TDA1010.

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 18	V
Repetitive peak output current	I_{ORM}	<	4	A
Output power at d_{tot} = 10% (with bootstrap)				
V_P = 14,4 V; R_L = 2 Ω	P_o	>	10	W
		typ.	12	W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	7	W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,5	W
Output power at d_{tot} = 10% (without bootstrap)				
V_P = 14,4 V; R_L = 4 Ω	P_o	>	4,5	W
Input impedance				
preamplifier (pin 8)	$\|Z_i\|$	typ.	40	kΩ
power amplifier (pin 6)	$\|Z_i\|$	typ.	40	kΩ
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	30	mA
Stand-by current	I_{sb}	<	1	mA
Storage temperature range	T_{stg}	−55 to + 150		°C
Crystal temperature	T_c	max.	150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

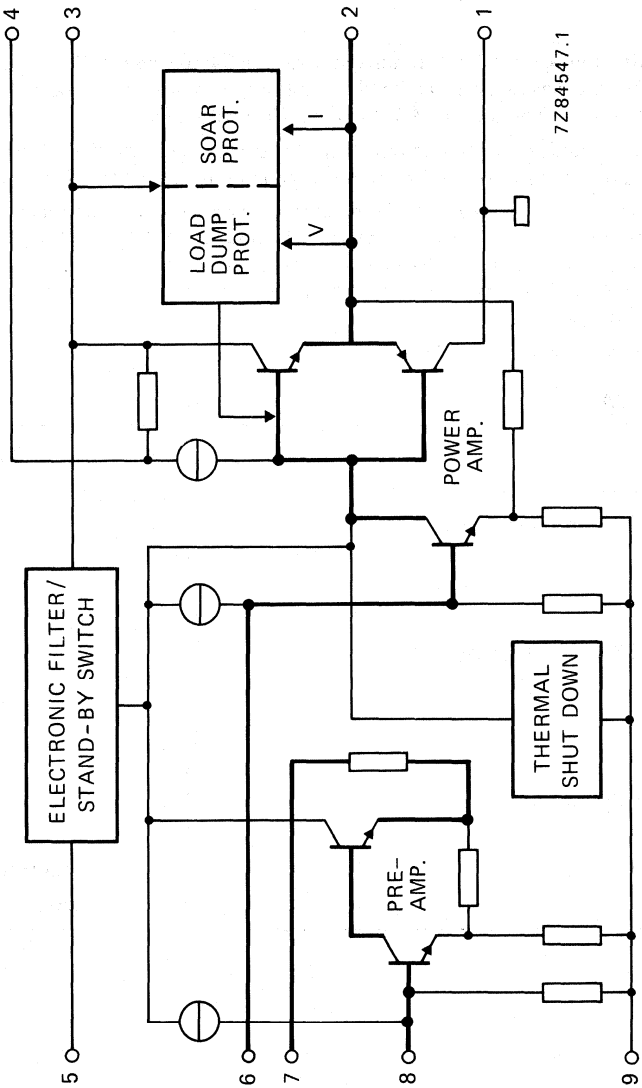


Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.

PINNING

1. Negative supply (substrate)
2. Output power stage
3. Positive supply (V_P)
4. Bootstrap
5. Ripple rejection filter
6. Input power stage
7. Output preamplifier
8. Input preamplifier
9. Negative supply

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; operating (pin 3)	V_P	max.	18 V
Supply voltage; non-operating	V_P	max.	28 V
Supply voltage; load dump	V_P	max.	45 V
Non-repetitive peak output current	I_{OSM}	max.	6 A
Total power dissipation	see derating curves Fig. 2		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	150 °C
Short-circuit duration of load behind output electrolytic capacitor at 1 kHz sine-wave overdrive (10 dB); V_P = 14,4 V	t_{sc}	max.	100 hours

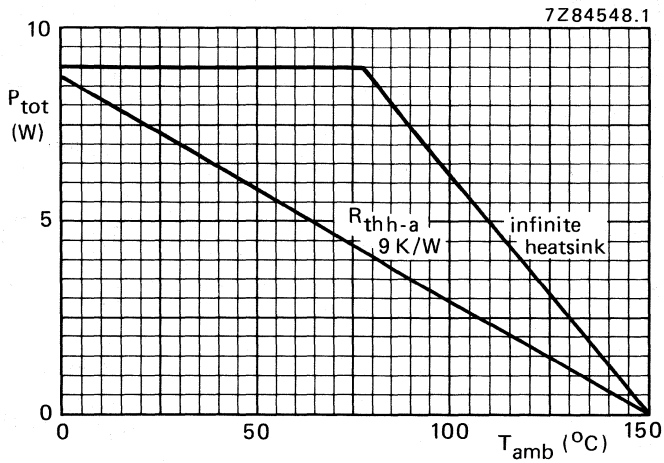


Fig. 2 Power derating curves.

HEATSINK DESIGN EXAMPLE

The derating of 8 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

10 W in 2 Ω at V_P = 14,4 V
maximum sine-wave dissipation: 5,2 W
T_{amb} = 60 °C maximum

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{5{,}2} = 17{,}3\ \text{K/W}$$

Since $R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} = 8$ K/W, $R_{th\ h\text{-}a} = 17{,}3 - 8 \approx 9$ K/W.

D.C. CHARACTERISTICS

Supply voltage range (pin 3)	V_P	6 to 18	V
Repetitive peak output current	I_{ORM}	< 4	A
Total quiescent current			
at V_P = 14,4 V	I_{tot}	typ. 30	mA
at V_P = 18 V	I_{tot}	typ. 40	mA

A.C. CHARACTERISTICS

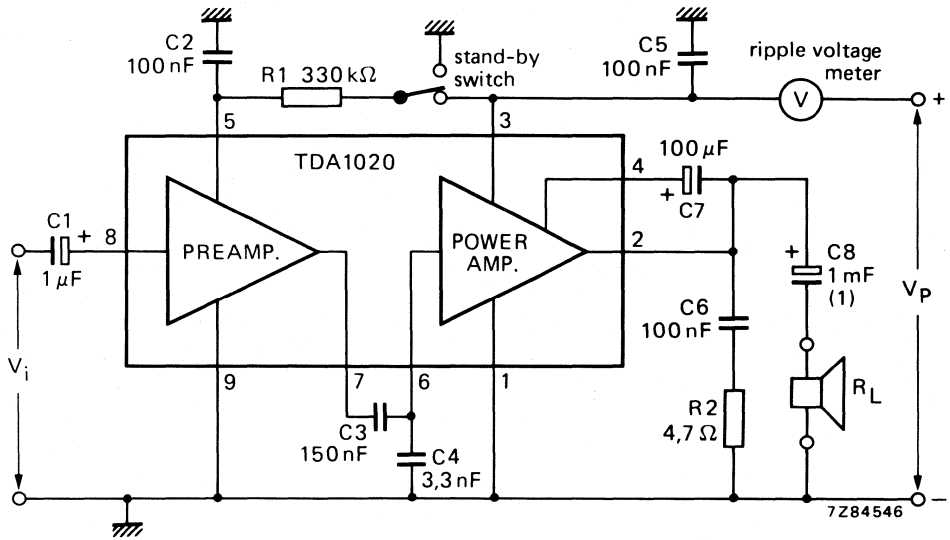
T_{amb} = 25 °C; V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; unless otherwise specified; see also Fig. 3

Output power at d_{tot} = 10%; with bootstrap (note 1)			
V_P = 14,4 V; R_L = 2 Ω	P_o	> 10 typ. 12	W W
V_P = 14,4 V; R_L = 4 Ω	P_o	> 6 typ. 7	W W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ. 3,5	W
Output power at d_{tot} = 1%; with bootstrap (note 1)			
V_P = 14,4 V; R_L = 2 Ω	P_o	typ. 9,5	W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ. 6	W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ. 3	W
Output voltage (r.m.s. value)			
R_L = 1 kΩ; d_{tot} = 0,5%	$V_{o(rms)}$	typ. 5	V
Output power at d_{tot} = 10%; without bootstrap	P_o	> 4,5	W
Voltage gain			
preamplifier (note 2)	G_{v1}	typ. 17,7 16,7 to 18,7	dB dB
power amplifier	G_{v2}	typ. 29,5 28,5 to 30,5	dB dB
total amplifier	$G_{v\,tot}$	typ. 47 46,2 to 48,2	dB dB
Input impedance			
preamplifier	$\lvert Z_i \rvert$	typ. 40 28 to 52	kΩ kΩ
power amplifier	$\lvert Z_i \rvert$	typ. 40 28 to 52	kΩ kΩ
Output impedance			
preamplifier	$\lvert Z_o \rvert$	typ. 2,0 1,4 to 2,6	kΩ kΩ
power amplifier	$\lvert Z_o \rvert$	typ. 50	mΩ
Output voltage (r.m.s. value) at d_{tot} = 1%			
preamplifier (note 2)	$V_{o(rms)}$	> 1 typ. 1,5	V V
Frequency response	B	50 Hz to 25	kHz
Noise output voltage (r.m.s. value; note 3)			
R_S = 0 Ω	$V_{n(rms)}$	typ. 0,3 < 0,5	mV mV
R_S = 8,2 kΩ	$V_{n(rms)}$	typ. 0,5 < 1,0	mV mV

Ripple rejection (note 4)			
at f = 100 Hz; C2 = 1 μF	RR	typ.	44 dB
at f = 1 kHz to 10 kHz	RR	>	48 dB
		typ.	54 dB
Bootstrap current at onset of clipping (pin 4)			
R_L = 4 Ω and 2 Ω	I_4	typ.	40 mA
Stand-by current (note 5)	I_{sb}	<	1 mA
Crystal temperature for −3 dB gain	T_c	>	150 °C

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 40 kΩ.
3. Measured according to IEC curve-A.
4. Maximum ripple amplitude is 2 V; input is short-circuited.
5. Total current when disconnecting pin 5 or short-circuited to ground (pin 9).
6. The tab must be electrically floating or connected to the substrate (pin 9).



(1) With R_L = 2 Ω, preferred value of C8 = 2200 μF.

Fig. 3 Test circuit.

SIGNAL-SOURCES SWITCH

The TDA1029 is a dual operational amplifier (connected as an impedance converter) each amplifier having 4 mutually switchable inputs which are protected by clamping diodes. The input currents are independent of switch position and the outputs are short-circuit protected.

The device is intended as an electronic two-channel signal-source switch in a.f. amplifiers.

QUICK REFERENCE DATA

Supply voltage range (pin 14)	V_P		6 to 23	V
Operating ambient temperature	T_{amb}		−30 to + 80	°C
Supply voltage (pin 14)	V_P	typ.	20	V
Current consumption	I_{14}	typ.	3,5	mA
Maximum input signal handling (r.m.s. value)	$V_{i(rms)}$	typ.	6	V
Voltage gain	G_v	typ.	1	
Total harmonic distortion	d_{tot}	typ.	0,01	%
Crosstalk	α	typ.	70	dB
Signal-to-noise ratio	S/N	typ.	120	dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

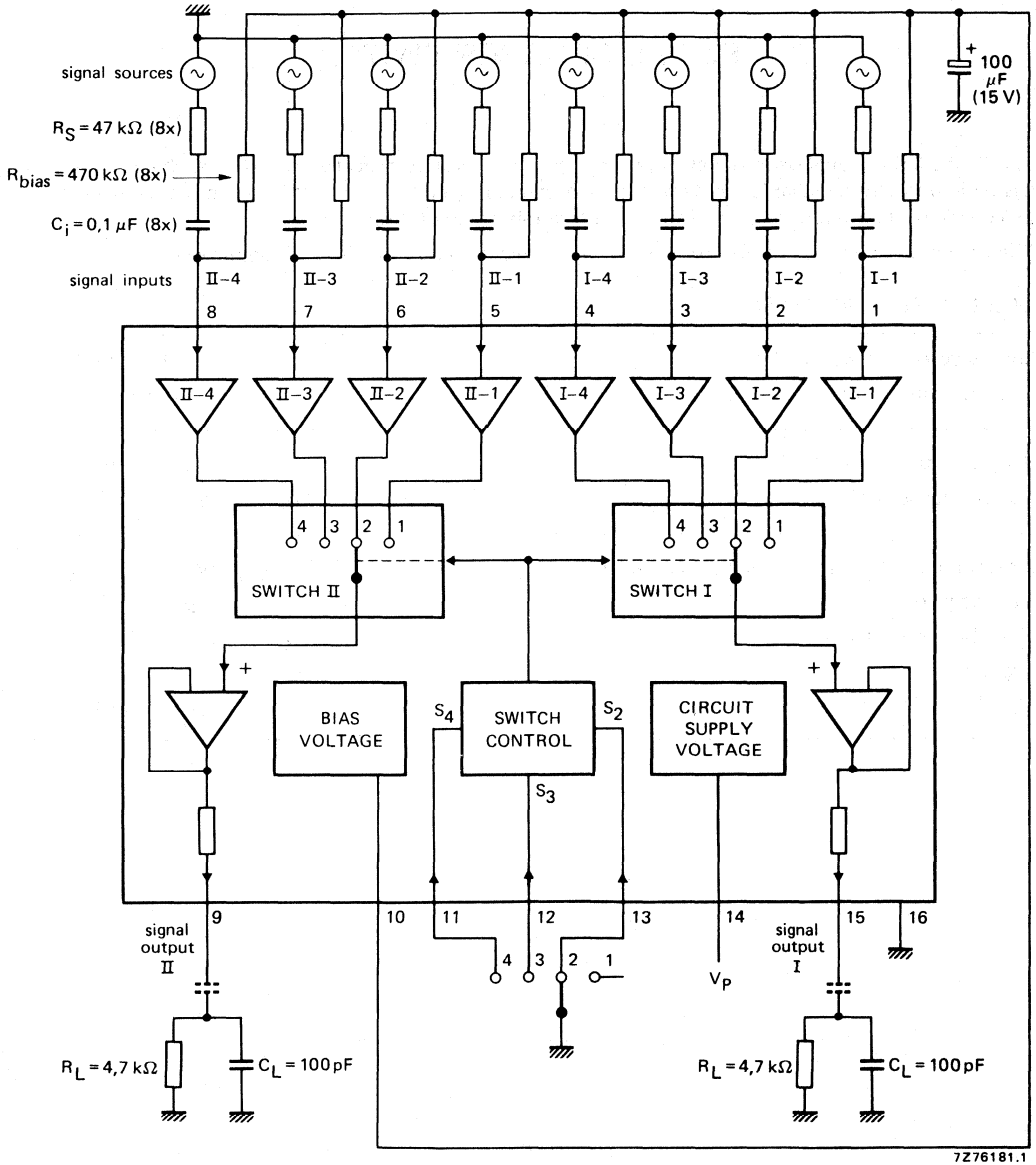


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 14)	V_P	max.	23	V
Input voltage (pins 1 to 8)	V_I	max.	V_P	
	$-V_I$	max.	0,5	V
Switch control voltage (pins 11, 12 and 13)	V_S		0 to 23	V
Input current	$\pm I_I$	max.	20	mA
Switch control current	$-I_S$	max.	50	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to + 80	°C

CHARACTERISTICS

V_P = 20 V; T_{amb} = 25 °C; unless otherwise specified

Current consumption				
without load; $I_g = I_{15} = 0$	I_{14}	typ.	3,5	mA
			2 to 5	mA
Supply voltage range (pin 14)	V_P		6 to 23	V
Signal inputs				
Input offset voltage of switched-on inputs $R_S \leqslant 1$ kΩ	V_{io}	typ.	2	mV
		<	10	mV
Input offset current of switched-on inputs	I_{io}	typ.	20	nA
		<	200	nA
Input offset current of a switched-on input with respect to a non-switched-on input of a channel	I_{io}	typ.	20	nA
		<	200	nA
Input bias current independent of switch position	I_i	typ.	250	nA
		<	950	nA
Capacitance between adjacent inputs	C	typ.	0,5	pF
D.C. input voltage range	V_I		3 to 19	V
Supply voltage rejection ratio; $R_S \leqslant 10$ kΩ	SVRR	typ.	100	μV/V
Equivalent input noise voltage $R_S = 0$; f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	3,5	μV
Equivalent input noise current f = 20 Hz to 20 kHz (r.m.s. value)	$I_{n(rms)}$	typ.	0,05	nA
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at R_S = 1 kΩ; f = 1 kHz	α	typ.	100	dB

CHARACTERISTICS (continued)

Signal amplifier

Voltage gain of a switched-on input at $I_9 = I_{15} = 0$; $R_L = \infty$	G_v	typ.	1
Current gain of a switched-on amplifier	G_i	typ.	10^5

Signal outputs

Output resistance (pins 9 and 15)	R_o	typ.	400 Ω
Output current capability at V_P = 6 to 23 V	$\pm I_9$; $\pm I_{15}$	typ.	5 mA
Frequency limit of the output voltage $V_{i(p-p)}$ = 1 V; R_S = 1 kΩ; R_L = 10 MΩ; C_L = 10 pF	f	typ.	1,3 MHz
Slew rate (unity gain); $\Delta V_{9\text{-}16}/\Delta t$; $\Delta V_{15\text{-}16}/\Delta t$ R_L = 10 MΩ; C_L = 10 pF	S	typ.	2 V/μs

Bias voltage

D.C. output voltage	$V_{10\text{-}16}$	typ. 10,2 to 11,8	11 V * V
Output resistance	$R_{10\text{-}16}$	typ.	8,2 kΩ

Switch control

switched-on inputs	interconnected pins	control voltages		
		$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
I-1, II-1	1-15, 5-9	H	H	H
I-2, II-2	2-15, 6-9	H	H	L
I-3, II-3	3-15, 7-9	H	L	H
I-4, II-4	4-15, 8-9	L	H	H
I-4, II-4	4-15, 8-9	L	L	H
I-4, II-4	4-15, 8-9	L	H	L
I-4, II-4	4-15, 8-9	L	L	L
I-3, II-3	3-15, 7-9	H	L	L

In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time. In that case safe switching-through is obtained at $V_{SL} \leqslant 1{,}5$ V.

Control inputs (pins 11, 12 and 13)

Required voltage			
HIGH	V_{SH}	>	3,3 V **
LOW	V_{SL}	<	2,1 V
Input current			
HIGH (leakage current)	I_{SH}	<	1 μA
LOW (control current)	$-I_{SL}$	<	250 μA

* $V_{10\text{-}16}$ is typically $0{,}5 \cdot V_{14\text{-}16} + 1{,}5 \cdot V_{BE}$.

** Or control inputs open ($R_{11,12,13-16} > 33$ MΩ).

APPLICATION INFORMATION

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 1; R_S = 47 kΩ; C_i = 0,1 μF; R_{bias} = 470 kΩ; R_L = 4,7 kΩ; C_L = 100 pF (unless otherwise specified)

Voltage gain	G_v	typ.	−1,5	dB
Output voltage variation when switching the inputs	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	typ. <	10 100	mV mV
Total harmonic distortion				
over most of signal range (see Fig. 4)	d_{tot}	typ.	0,01	%
V_i = 5 V; f = 1 kHz	d_{tot}	typ.	0,02	%
V_i = 5 V; f = 20 Hz to 20 kHz	d_{tot}	typ.	0,03	%
Output signal handling				
d_{tot} = 0,1%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	> typ.	5,0 5,3	V V
Noise output voltage (unweighted)				
f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	5	μV
Noise output voltage (weighted)				
f = 20 Hz to 20 kHz (in accordance with DIN 45405)	V_n	typ.	12	μV
Amplitude response				
V_i = 5 V; f = 20 Hz to 20 kHz; C_i = 0,22 μF	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	<	0,1	dB *
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz	α	typ.	75	dB **
Crosstalk between switched-on inputs and the outputs of the other channels	α	typ.	90	dB **

* The lower cut-off frequency depends on values of R_{bias} and C_i.

** Depends on external circuitry and R_S. The value will be fixed mostly by capacitive crosstalk of the external components.

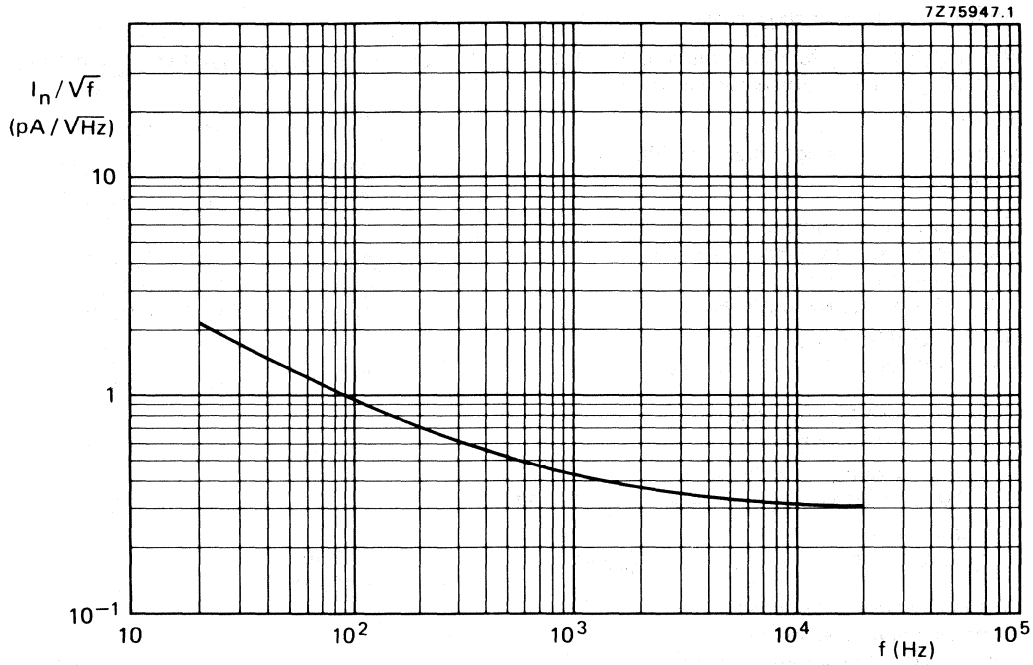


Fig. 2 Equivalent input noise current.

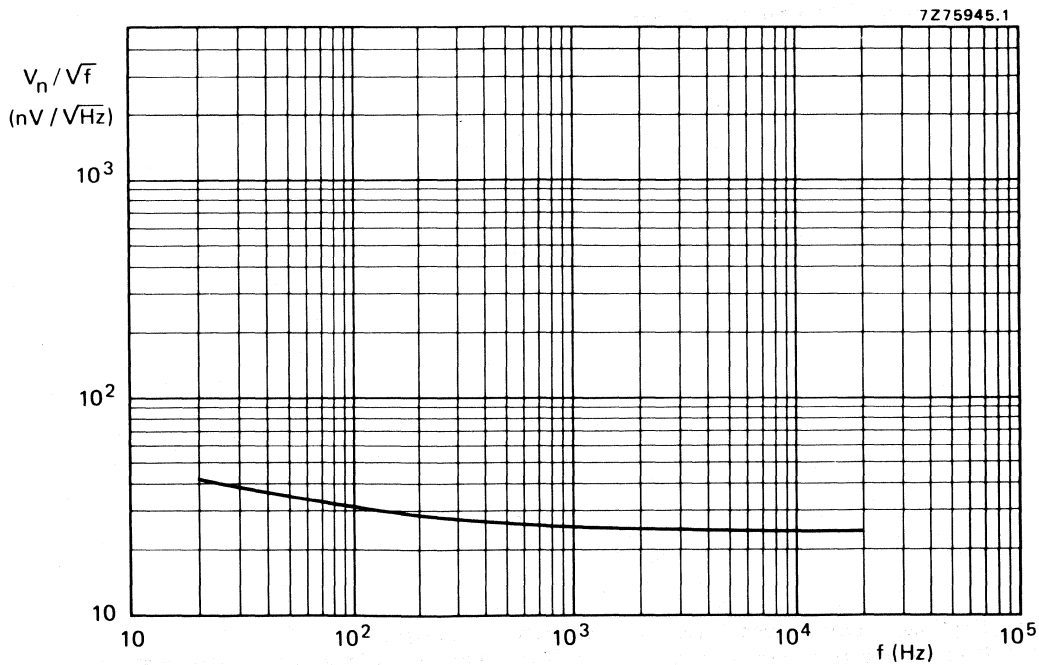


Fig. 3 Equivalent input noise voltage.

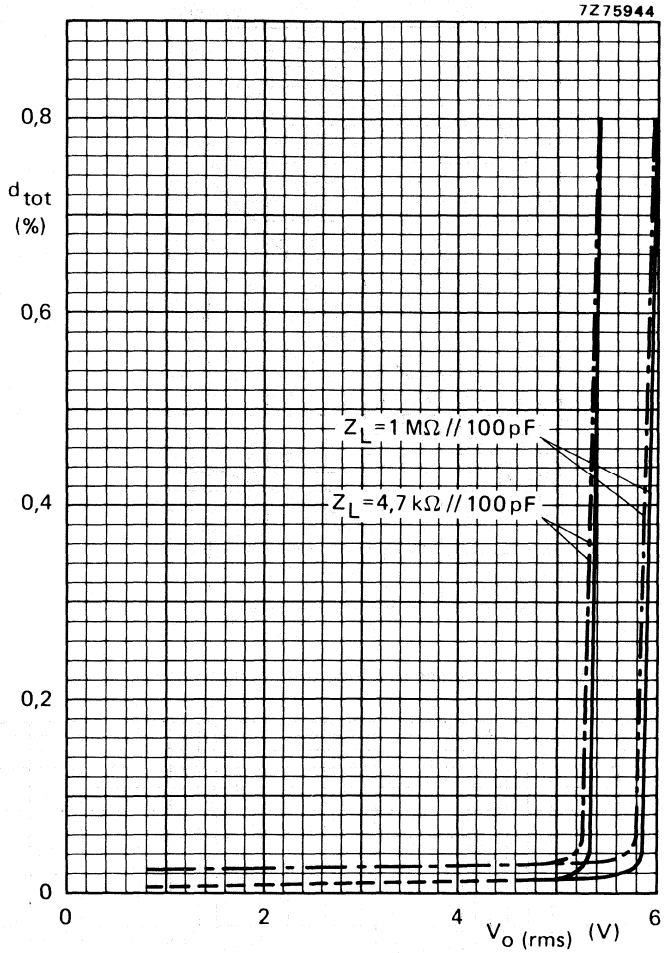


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; — - — - f = 20 kHz.

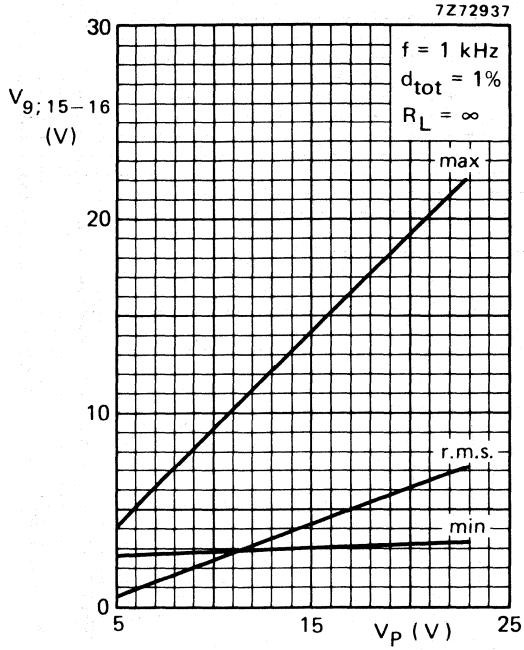


Fig. 5 Output voltage as a function of supply voltage.

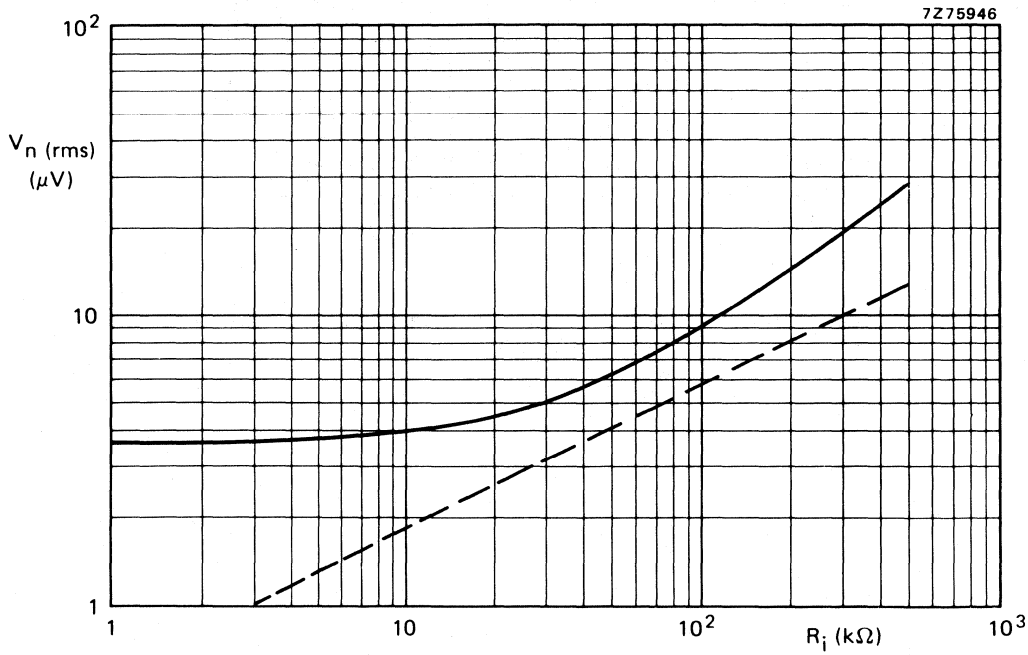


Fig. 6 Noise output voltage as a function of input resistance; G_v = 1; f = 20 Hz to 20 kHz.
—— V_n (output); – – – V_n (R_S).

APPLICATION NOTES

Input protection circuit and indication

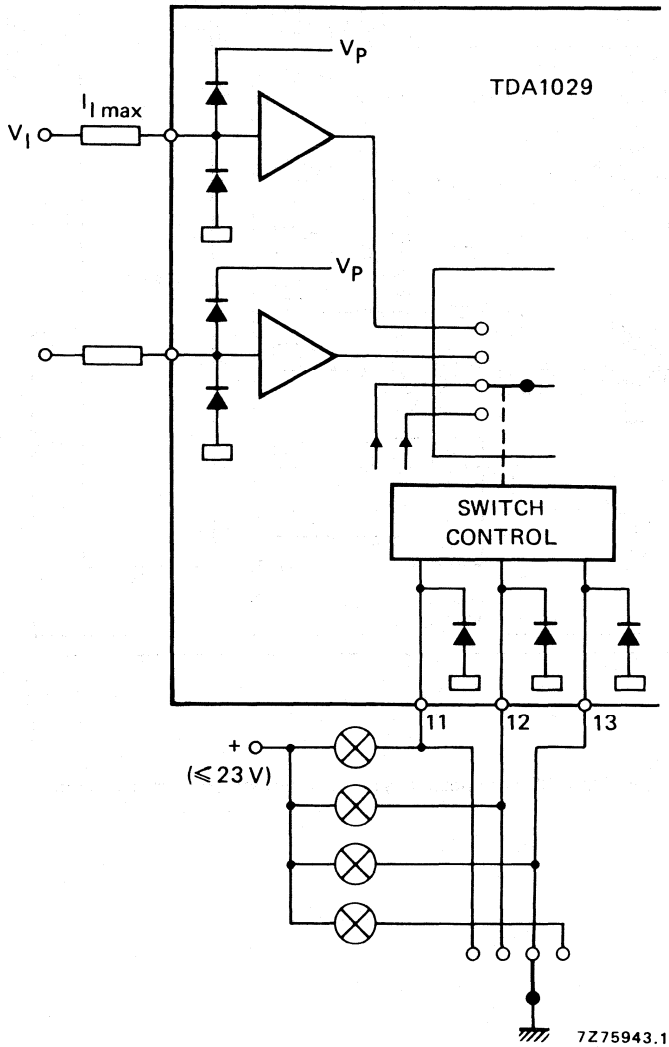


Fig. 7 Circuit diagram showing input protection and indication.

Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range; e.g. unused inputs can be connected directly to pin 10.

Circuits with standby operation

The control inputs (pins 11, 12 and 13) are high-ohmic at $V_{SH} \leqslant 20$ V ($I_{SH} \leqslant 1\ \mu A$), as well as, when the supply voltage (pin 14) is switched off.

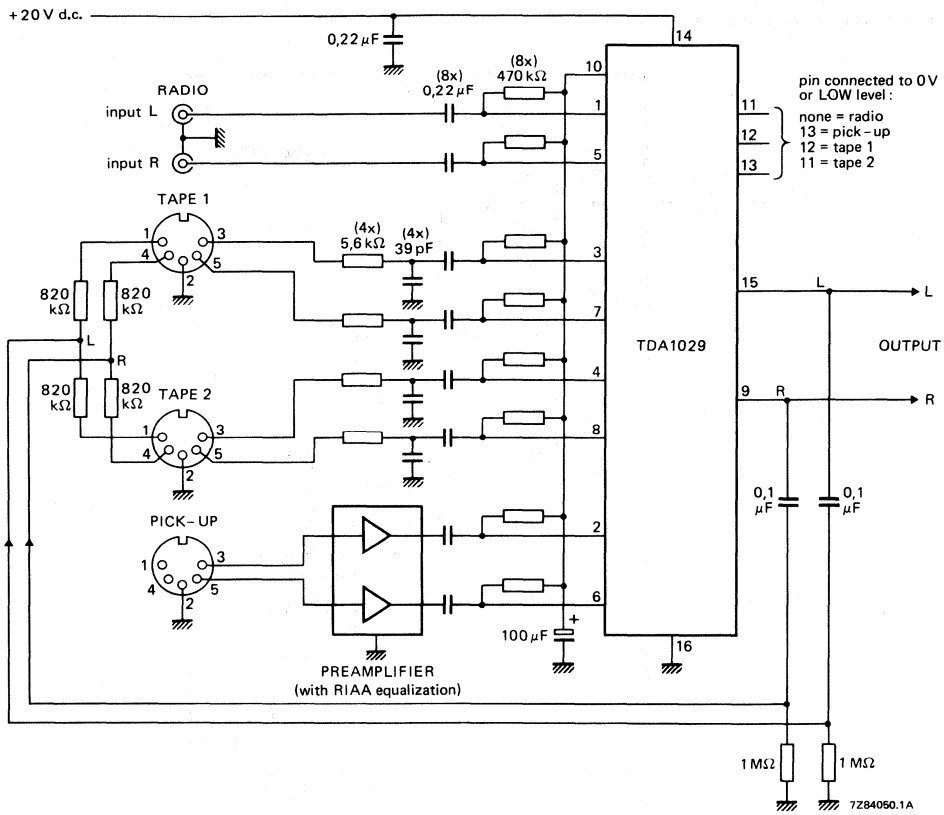


Fig. 8 TDA1029 connected as a four input stereo source selector.

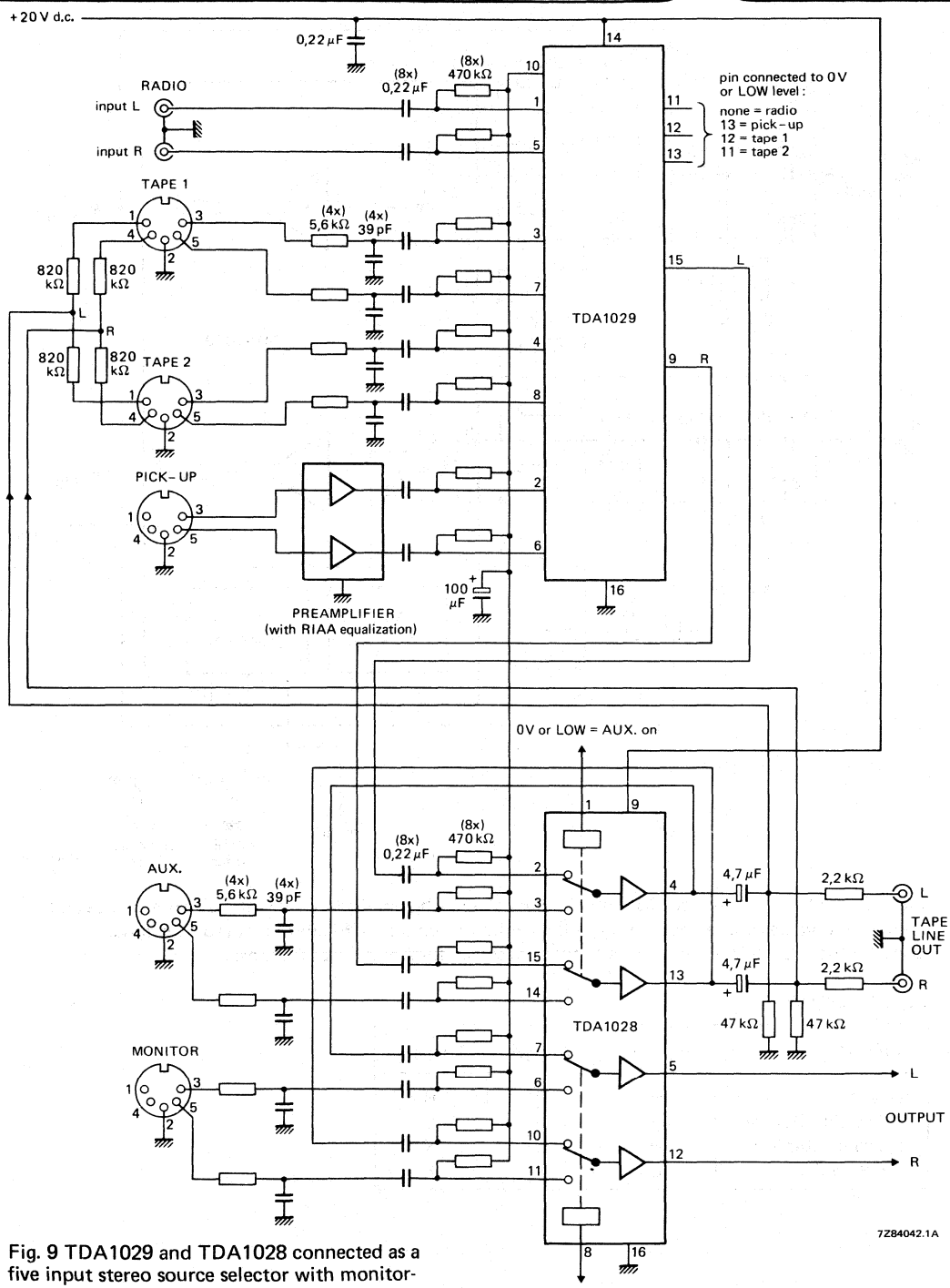


Fig. 9 TDA1029 and TDA1028 connected as a five input stereo source selector with monitoring facilities.

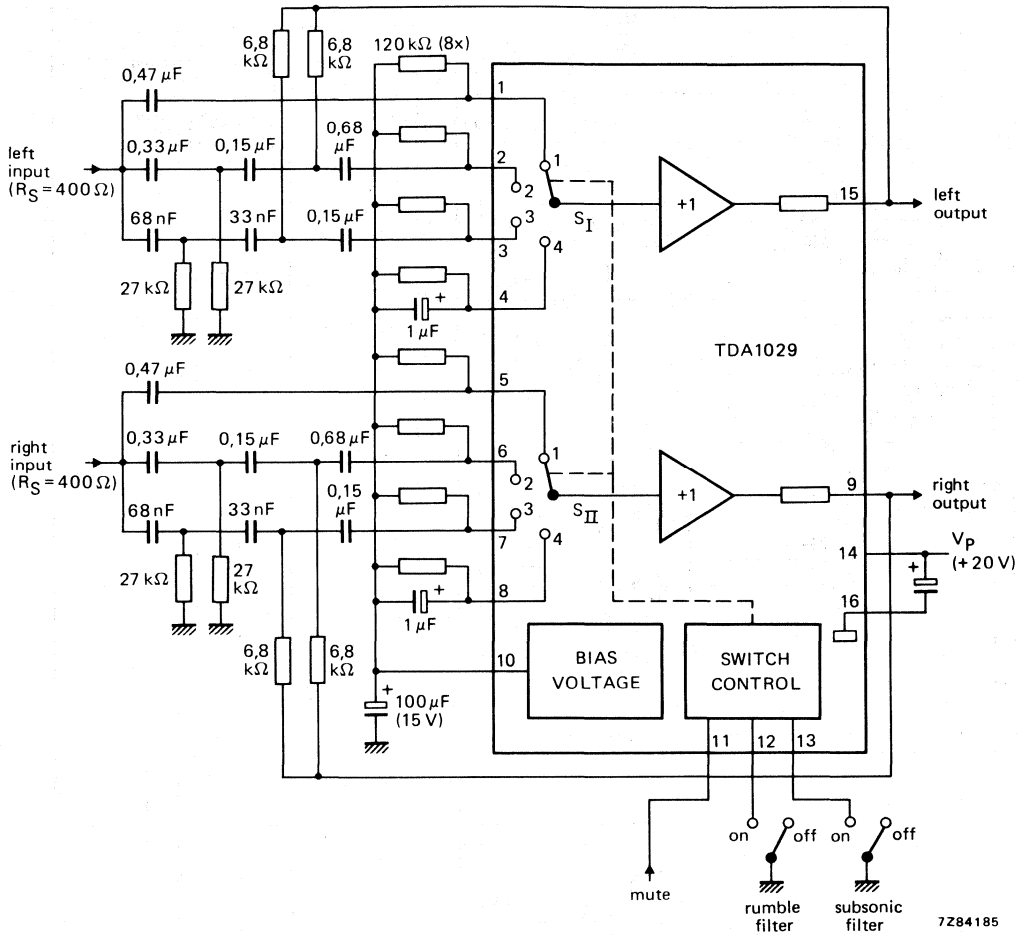


Fig. 10 TDA1029 connected as a third-order active high-pass filter with Butterworth response and component values chosen according to the method proposed by Fjällbrant. It is a four-function circuit which can select mute, rumble filter, subsonic filter and linear response.

Switch control

function	$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
linear	H	H	H
subsonic filter 'on'	H	H	L
rumble filter 'on'	H	L	X
mute 'on'	L	X	X

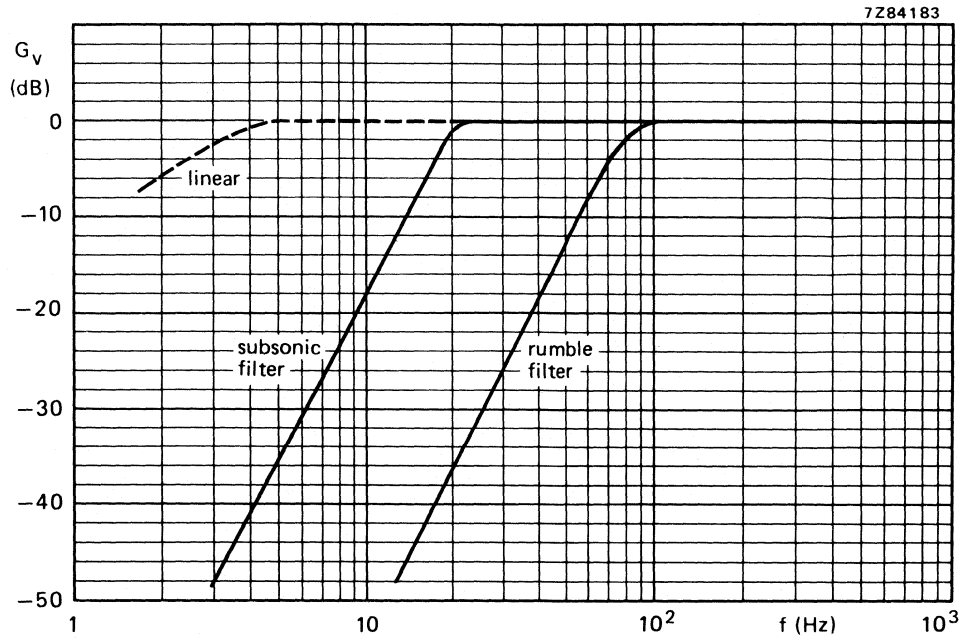


Fig. 11 Frequency response curves for the circuit of Fig. 10.

AM RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TDA1072A integrated AM receiver circuit performs the active and part of the filtering functions of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50 MHz and can handle r.f. signals up to 500 mV. R.F. radiation and sensitivity to interference are minimized by an almost symmetrical design. The voltage-controlled oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the i.f. amplifier.

Features

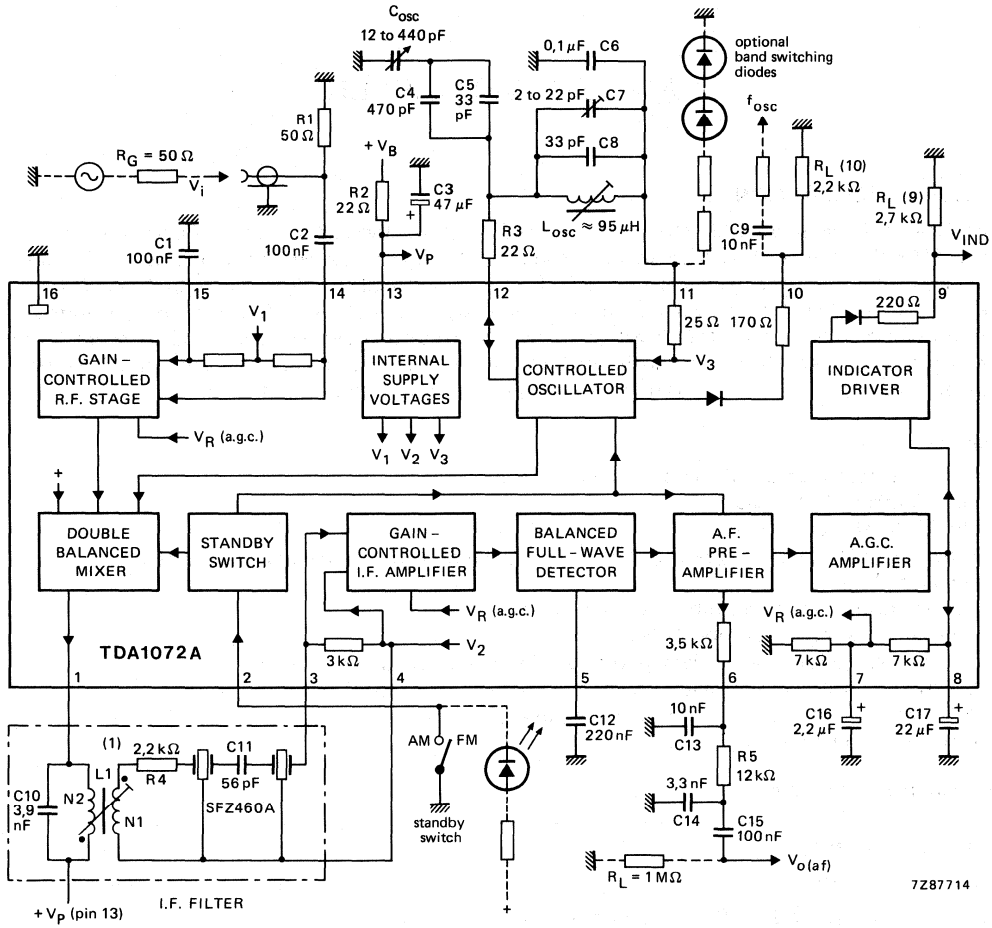
- Inputs protected against damage by static discharge
- Gain-controlled r.f. stage
- Double balanced mixer
- Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils
- Gain-controlled i.f. stage with wide a.g.c. range
- Full-wave, balanced envelope detector
- Internal generation of a.g.c. voltage with possibility of second-order filtering
- Buffered field strength indicator driver with short-circuit protection
- A.F. preamplifier with possibilities for simple a.f. filtering
- Electronic standby switch

QUICK REFERENCE DATA

Supply voltage range	V_P	7,5 to 18	V
Supply current range	I_P	15 to 30	mA
R.F. input voltage for S + N/N = 6 dB at m = 30%	V_i	typ. 1,5	μV
R.F. input voltage for 3% total harmonic distortion (THD) at m = 80%	V_i	typ. 500	mV
A.F. output voltage with V_i = 2 mV; f_i = 1 MHz; m = 30% and f_m = 400 Hz	$V_{o(af)}$	typ. 310	mV
A.G.C. range: change of V_i for 1 dB change of $V_{o(af)}$		typ. 86	dB
Field strength indicator voltage at V_i = 500 mV; $R_{L(9)}$ = 2,7 kΩ	V_{IND}	typ. 2,8	V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).



(1) Coil data: TOKO sample no. 7XNS-A7523DY; L1 : N1/N2 = 12/32; $Q_o = 65$; $Q_B = 57$.
Filter data: $Z_F = 700\ \Omega$ at $R_{3\text{-}4} = 3\ k\Omega$; $Z_I = 4{,}8\ k\Omega$.

Fig. 1 Block diagram and test circuit (connections shown in broken lines are not part of the test circuit).

FUNCTIONAL DESCRIPTION

Gain-controlled r.f. stage and mixer

The differential amplifier in the r.f. stage employs an a.g.c. negative feedback network to provide a wide dynamic range. Very good cross-modulation behaviour is achieved by a.g.c. delays at the various signal stages. Large signals are handled with low distortion and the S/N ratio of small signals is improved. Low noise working is achieved in the differential amplifier by using transistors with low base resistance.

A double balanced mixer provides the i.f. output signal to pin 1.

Oscillator

The differential amplifier oscillator is temperature compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage $V_{11\text{-}16}$. An extra buffered oscillator output (pin 10) is available for driving a synthesizer. If this is not needed, resistor $R_{L(10)}$ can be omitted.

Gain-controlled i.f. amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the a.g.c. negative feedback network.

Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. Residual i.f. carrier is blocked from the signal path by an internal low-pass filter.

A.F. preamplifier

This stage preamplifies the audio frequency output signal. The amplifier output has an emitter follower with a series resistor which, together with an external capacitor, yields the required low-pass for a.f. filtering.

A.G.C. amplifier

The a.g.c. amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the a.g.c. voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives fast a.g.c. settling time which is advantageous for electronic search tuning. The a.g.c. settling time can be further reduced by using capacitors of smaller value in the external filter (C16 and C17). The a.g.c. voltage is fed to the r.f. and i.f. stages via suitable a.g.c. delays. The capacitor at pin 7 can be omitted for low-cost applications.

Field strength indicator output

A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If the field strength information is not needed, $R_{L(9)}$ can be omitted.

Standby switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer and a.f. preamplifier are switched off.

Short-circuit protection

All pins have short-circuit protection to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Supply voltage	$V_P = V_{13-16}$	max.	20	V
Total power dissipation	P_{tot}	max.	875	mW
Input voltage	$\|V_{14-15}\|$	max.	12	V
	$-V_{14-16}$, $-V_{15-16}$	max.	0,6	V
	V_{14-16}, V_{15-16}	max.	V_P	V
Input current	$\|I_{14}\|$, $\|I_{15}\|$	max.	200	mA
Operating ambient temperature range	T_{amb}	−40 to	+80	°C
Storage temperature range	T_{stg}	−55 to	+150	°C
Junction temperature	T_j	max.	+125	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	80	K/W

DEVICE CHARACTERISTICS

$V_P = V_{13-16} = 8{,}5$ V; $T_{amb} = 25$ °C; $f_i = 1$ MHz; $f_m = 400$ Hz; m = 30%; $f_{if} = 460$ kHz; measured in test circuit of Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	$V_P = V_{13-16}$	7,5	8,5	18	V
Supply current	$I_P = I_{13}$	15	23	30	mA
R.F. stage and mixer					
Input voltage (d.c. value)	V_{14-16}, V_{15-16}	–	$V_P/2$	–	V
R.F. input impedance at $V_i < 300\ \mu V$	R_{14-16}, R_{15-16}	–	5,5	–	kΩ
	C_{14-16}, C_{15-16}	–	25	–	pF
R.F. input impedance at $V_i > 10$ mV	R_{14-16}, R_{15-16}	–	8	–	kΩ
	C_{14-16}, C_{15-16}	–	22	–	pF
I.F. output impedance	R_{1-16}	500	–	–	kΩ
	C_{1-16}	–	6	–	pF
Conversion transconductance before start of a.g.c.	I_1/V_i	–	6,5	–	mA/V
Maximum i.f. output voltage, inductive coupling to pin 1	$V_{1-13(p-p)}$	–	5	–	V
D.C. value of output current (pin 1) at $V_i = 0$ V	I_1	–	1,2	–	mA
A.G.C. range of input stage		–	30	–	dB
R.F. signal handling capability: input voltage for THD = 3% at m = 80%	$V_{i(rms)}$	–	500	–	mV

parameter	symbol	min.	typ.	max.	unit
Oscillator					
Frequency range	f_{osc}	0,6	–	60	MHz
Oscillator amplitude (pins 11 to 12)	$V_{11\text{-}12}$	–	130	150	mV
External load impedance	$R_{12\text{-}11(ext)}$	0,5	–	200	kΩ
External load impedance for no oscillation	$R_{12\text{-}11(ext)}$	–	–	60	Ω
Ripple rejection at $V_{P(rms)}$ = 100 mV; f_P = 100 Hz ($RR = 20 \log [V_{13\text{-}16}/V_{11\text{-}16}]$)	RR	–	55	–	dB
Source voltage for switching diodes (6 x V_{BE})	$V_{11\text{-}16}$	–	4,2	–	V
D.C. output current (for switching diodes)	$-I_{11}$	0	–	20	mA
Change of output voltage at ΔI_{11} = 20 mA (switch to maximum load)	$\Delta V_{11\text{-}16}$	–	0,5	–	V
Buffered oscillator output					
D.C. output voltage	$V_{10\text{-}16}$	–	0,7	–	V
Output signal amplitude	$V_{10\text{-}16(p\text{-}p)}$	–	320	–	mV
Output impedance	R_{10}	–	170	–	Ω
Output current	$-I_{10(peak)}$	–	–	3	mA
I.F., a.g.c. and a.f. stages					
D.C. input voltage	$V_{3\text{-}16}$, $V_{4\text{-}16}$	–	2,0	–	V
I.F. input impedance	$R_{3\text{-}4}$	2,4	3	3,9	kΩ
	$C_{3\text{-}4}$	–	7	–	pF
I.F. input voltage for THD = 3% at m = 80%	$V_{3\text{-}4}$	–	90	–	mV
Voltage gain before start of a.g.c.	$V_{3\text{-}4}/V_{6\text{-}16}$	–	68	–	dB
A.G.C. range of i.f. stages: change of $V_{3\text{-}4}$ for 1 dB change of $V_{o(af)}$; $V_{3\text{-}4(ref)}$ = 75 mV	$\Delta V_{3\text{-}4}$	–	55	–	dB
A.F. output voltage at $V_{3\text{-}4(if)}$ = 50 μV	$V_{o(af)}$	–	130	–	mV
A.F. output voltage at $V_{3\text{-}4(if)}$ = 1 mV	$V_{o(af)}$	–	310	–	mV
A.F. output impedance (pin 6)	$\lvert Z_o \rvert$	–	3,5	–	kΩ
Indicator driver					
Output voltage at V_i = 0 mV; $R_{L(9)}$ = 2,7 kΩ	$V_{9\text{-}16}$	–	20	150	mV
Output voltage at V_i = 500 mV; $R_{L(9)}$ = 2,7 kΩ	$V_{9\text{-}16}$	2,5	2,8	3,1	V
Load resistance	$R_{L(9)}$	1,5	–	–	kΩ

DEVICE CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Standby switch					
Switching threshold at V_P = 7,5 to 18 V; T_{amb} = −40 to + 80 °C					
on-voltage	$V_{2\text{-}16}$	0	–	2,0	V
off-voltage	$V_{2\text{-}16}$	3,5	–	20	V
on-current at $V_{2\text{-}16}$ = 0 V	$-I_2$	–	–	200	μA
off-current at $V_{2\text{-}16}$ = 20 V	$\|I_2\|$	–	–	10	μA

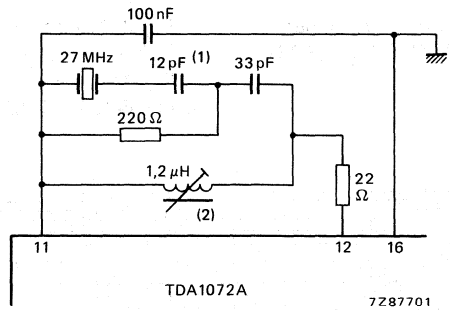
OPERATING CHARACTERISTICS

V_P = 8,5 V; f_i = 1 MHz; m = 30%; f_m = 400 Hz; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
R.F. sensitivity					
R.F. input required for S + N/N = 6 dB	V_i	–	1,5	–	μV
R.F. input required for S + N/N = 26 dB	V_i	–	15	–	μV
R.F. input required for S + N/N = 46 dB	V_i	–	150	–	μV
R.F. input at start of a.g.c.	V_i	–	30	–	μV
R.F. large signal handling					
R.F. input at THD = 3%; m = 80%	V_i	–	500	–	mV
R.F. input at THD = 3%; m = 30%	V_i	–	700	–	mV
R.F. input at THD = 10%; m = 30%	V_i	–	900	–	mV
A.G.C. range					
Change of V_i for 1 dB change of $V_{o(af)}$; $V_{i(ref)}$ = 500 mV	ΔV_i	–	86	–	dB
Change of V_i for 6 dB change of $V_{o(af)}$; $V_{i(ref)}$ = 500 mV	ΔV_i	–	91	–	dB
Output signal					
A.F. output voltage at V_i = 4 μV; m = 80%	$V_{o(af)}$	–	130	–	mV
A.F. output voltage at V_i = 1 mV	$V_{o(af)}$	240	310	390	mV
THD at V_i = 1 mV; m = 80%	d_{tot}	–	0,5	–	%
THD at V_i = 500 mV; m = 30%	d_{tot}	–	1	–	%
Signal-to-noise ratio at V_i = 100 mV	(S + N)/N	–	58	–	dB
Ripple rejection at V_i = 2 mV; $V_{P(rms)}$ = 100 mV; f_P = 100 Hz ($RR = 20 \log [V_P/V_{o(af)}]$)	RR	–	38	–	dB

parameter	symbol	min.	typ.	max.	unit
Unwanted signals					
Suppression of i.f. whistles at V_i = 15 μV; m = 0% related to a.f. signal of m = 30%					
at $f_i \approx 2 \times f_{if}$	α_{2if}	–	37	–	dB
at $f_i \approx 3 \times f_{if}$	α_{3if}	–	44	–	dB
I.F. suppression at r.f. input					
for symmetrical input	α_{if}	–	40	–	dB
for asymmetrical input	α_{if}	–	40	–	dB
Residual oscillator signal at mixer output					
at f_{osc}	$I_{1(osc)}$	–	1	–	μA
at 2 x f_{osc}	$I_{1(2osc)}$	–	1,1	–	μA

APPLICATION INFORMATION



(1) Capacitor values depend on crystal type.
(2) Coil data: 9 windings of 0,1 mm dia laminated Cu wire on TOKO coil set 7K 199CN; Q_o = 80.

Fig. 2 Oscillator circuit using quartz crystal; centre frequency = 27 MHz.

APPLICATION INFORMATION (continued)

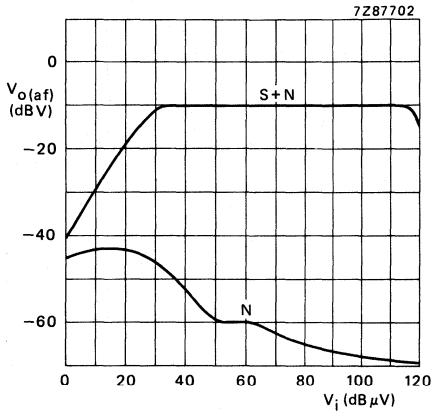


Fig. 3 A.F. output as a function of r.f. input in the circuit of Fig. 1; f_i = 1 MHz; f_m = 400 Hz; m = 30%.

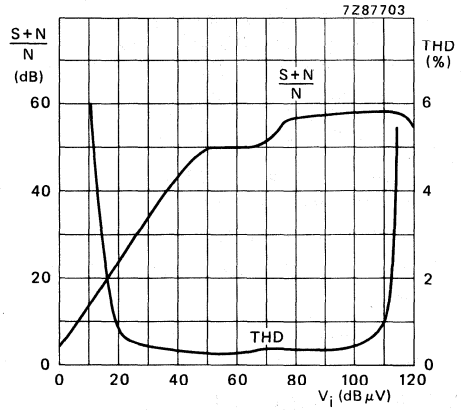


Fig. 4 Total harmonic distortion and (S + N)/N as functions of r.f. input in the circuit of Fig. 1; m = 30% for (S + N)/N curve and m = 80% for THD curve.

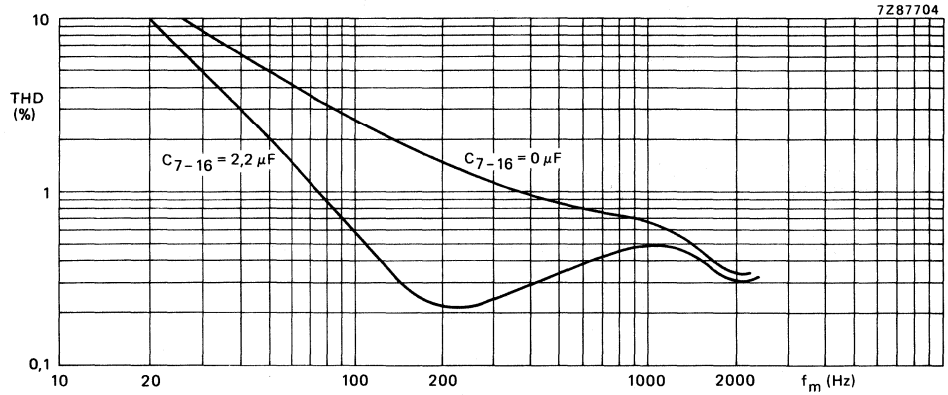


Fig. 5 Total harmonic distortion as a function of modulation frequency at V_i = 5 mV; m = 80%; measured in the circuit of Fig. 1 with $C_{7-16(ext)}$ = 0 μF and 2,2 μF.

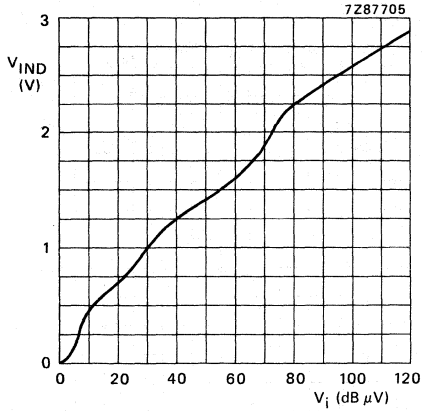


Fig. 6 Indicator driver voltage as a function of r.f. input in the circuit of Fig. 1.

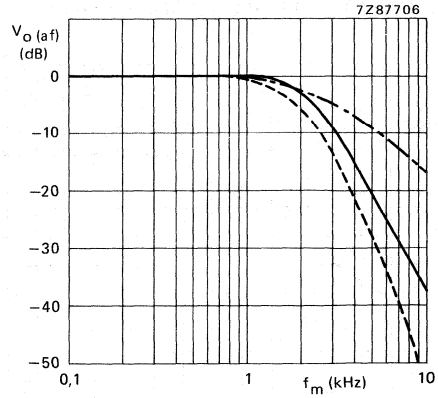


Fig. 7 Typical frequency response curves from Fig. 1 showing the effect of filtering as follows:
———— with i.f. filter;
— · — · — · — · with a.f. filter;
— — — — — with i.f. and a.f. filters.

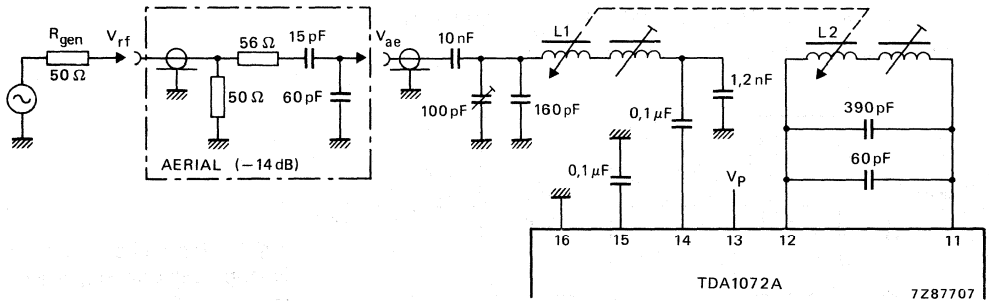


Fig. 8 Car radio application with inductive tuning.

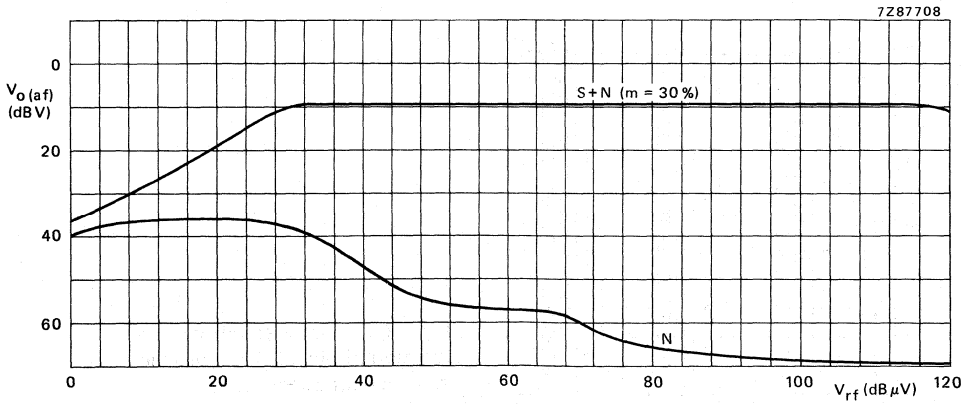


Fig. 9 A.F. output as a function of r.f. input using the circuit of Fig. 8 with that of Fig. 1.

APPLICATION INFORMATION (continued)

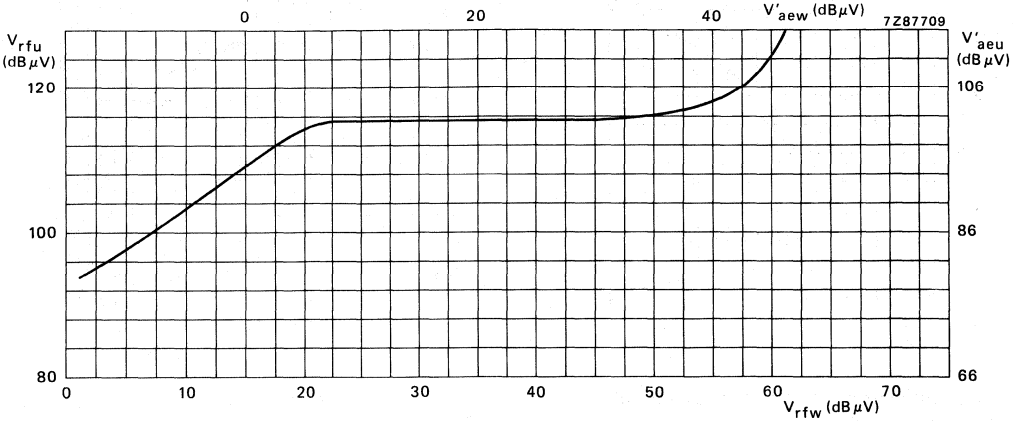


Fig. 10 Suppression of cross-modulation as a function of input signal, measured in the circuit of Fig. 8 with the input circuit as shown in Fig. 11. Curve is for Wanted $V_{o(af)}$/Unwanted $V_{o(af)}$ = 20 dB; V_{rfw}, V_{rfu} are signals at the aerial input, V'_{aew}, V'_{aeu} are signals at the unloaded output of the aerial.

Wanted signal (V'_{aew}, V_{rfw}): f_i = 1 MHz; f_m = 400 Hz; m = 30%.

Unwanted signal (V'_{aeu}, V_{rfu}): f_i = 900 kHz; f_m = 400 Hz; m = 30%.

Effective selectivity of input tuned circuit = 21 dB.

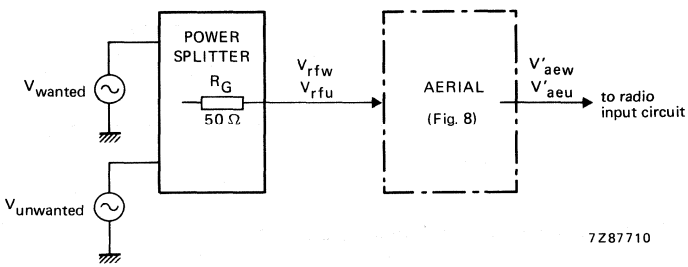


Fig. 11 Input circuit to show cross-modulation suppression (see Fig. 10).

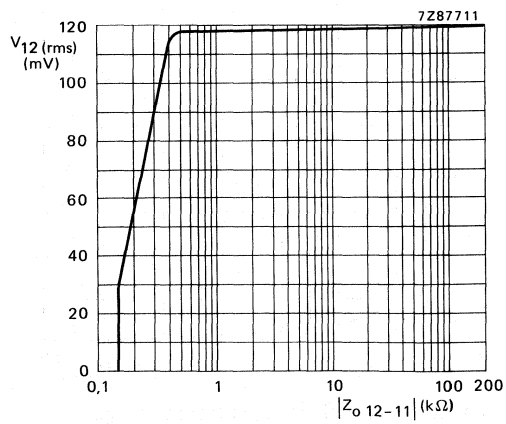


Fig. 12 Oscillator amplitude as a function of pin 11, 12 impedance in the circuit of Fig. 8.

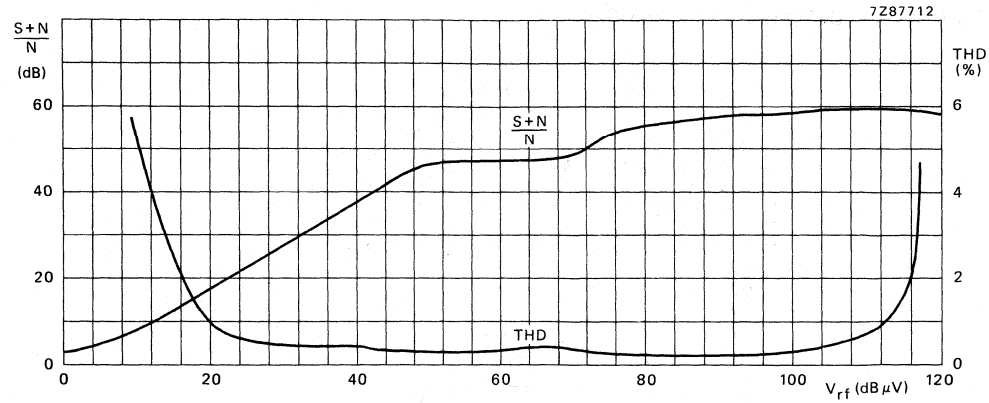


Fig. 13 Total harmonic distortion and (S + N)/N as functions of r.f. input using the circuit of Fig. 8 with that of Fig. 1.

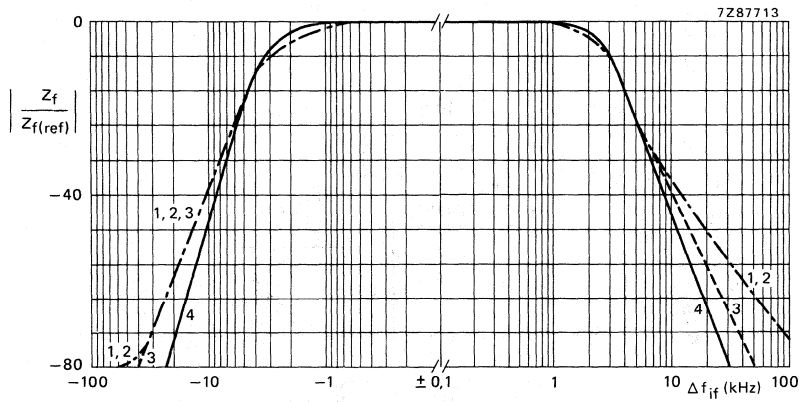


Fig. 14 Forward transfer impedance as a function of intermediate frequency for filters 1 to 4 shown in Fig. 15; centre frequency = 455 kHz.

APPLICATION INFORMATION (continued)

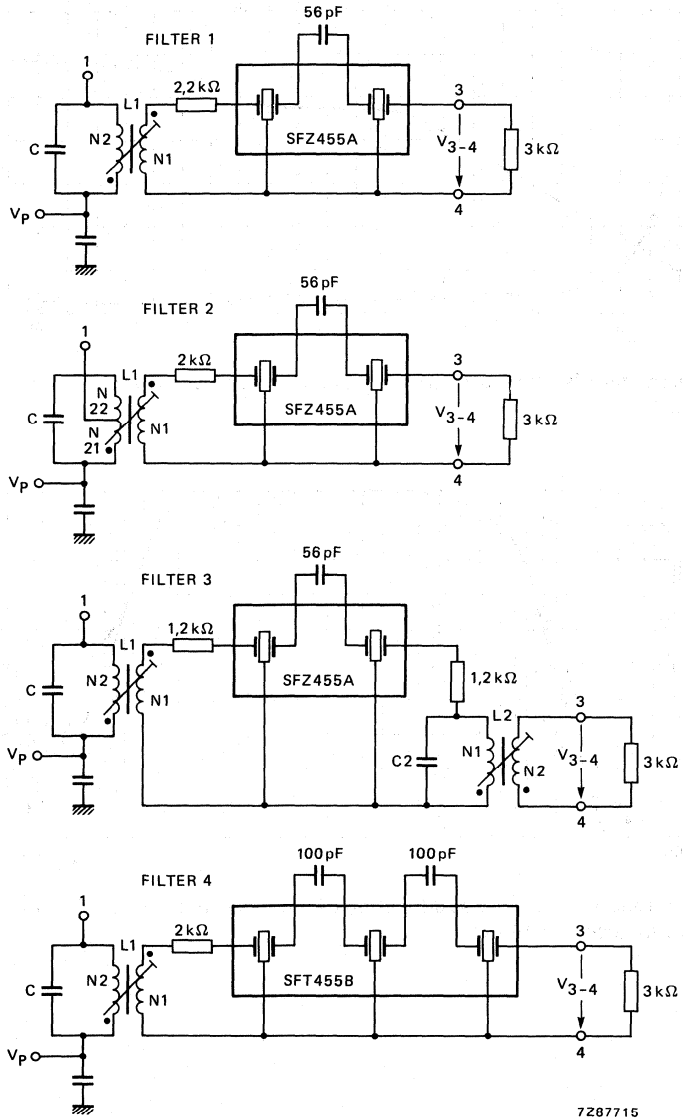
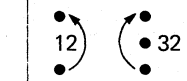
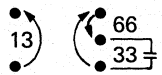
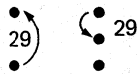


Fig. 15 I.F. filter variants applied to the circuit of Fig. 1. For filter data, refer to Table 1.

Table 1 Data for I.F. filters shown in Fig. 15. Criterium for adjustment is Z_F = maximum (optimum selectivity curve at centre frequency f_0 = 455 kHz). See also Fig. 14.

filter no.	1	2	3		4	unit
Coil data	L1	L1	L1	L2	L1	
Value of C	3900	430	3900	4700	3900	pF
N1: N2	12 : 32	13 : (33 + 66)	15 : 31	29 : 29	13 : 31	
Diameter of Cu laminated wire	0,09	0,08	0,09	0,08	0,09	mm
Q_o	65 (typ.)	50	75	60	75	
Schematic* of windings				 (N1) (N2)		
Toko order no.	7XNS-A7523DY	L7PES-A0060BTG	7XNS-A7518DY	7XNS-A7521AIH	7XNS-A7519DY	
Resonators						
Murata type	SFZ455A	SFZ455A	SFZ455A		SFT455B	
D (typical value)	4	4	4		6	dB
R_G, R_L	3	3	3		3	kΩ
Bandwidth (−3 dB)	4,2	4,2	4,2		4,5	kHz
S_{9kHz}	24	24	24		38	dB
Filter data						
Z_I	4,8	3,8	4,2		4,8	kΩ
Q_B	57	40	52 (L1)	18 (L2)	55	
Z_F	0,70	0,67	0,68		0,68	kΩ
Bandwidth (−3 dB)	3,6	3,8	3,6		4,0	kHz
S_{9kHz}	35	31	36		42	dB
S_{18kHz}	52	49	54		64	dB
S_{27kHz}	63	58	66		74	dB

* The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding, N2 the outer winding.

APPLICATION INFORMATION (continued)

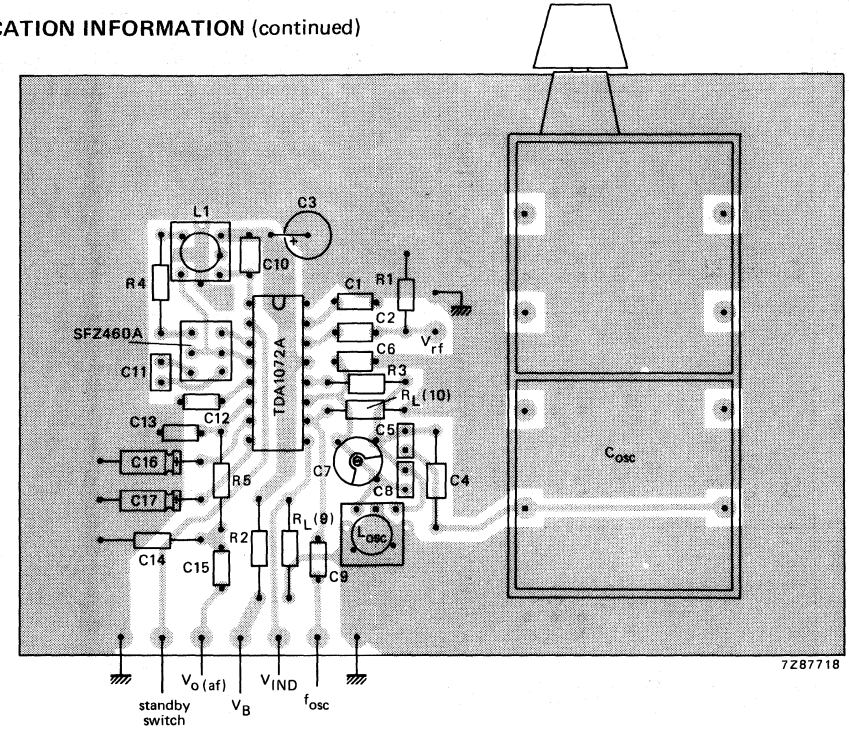


Fig. 16 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 1.

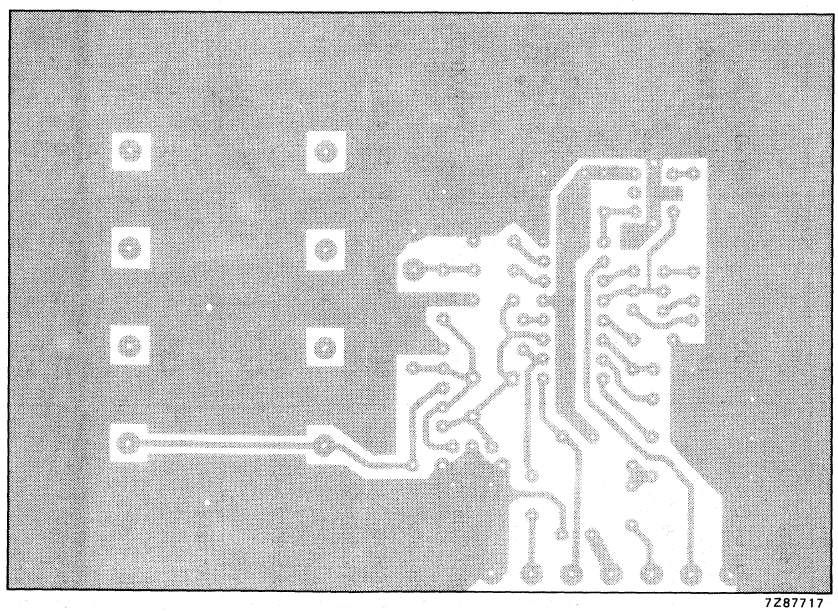
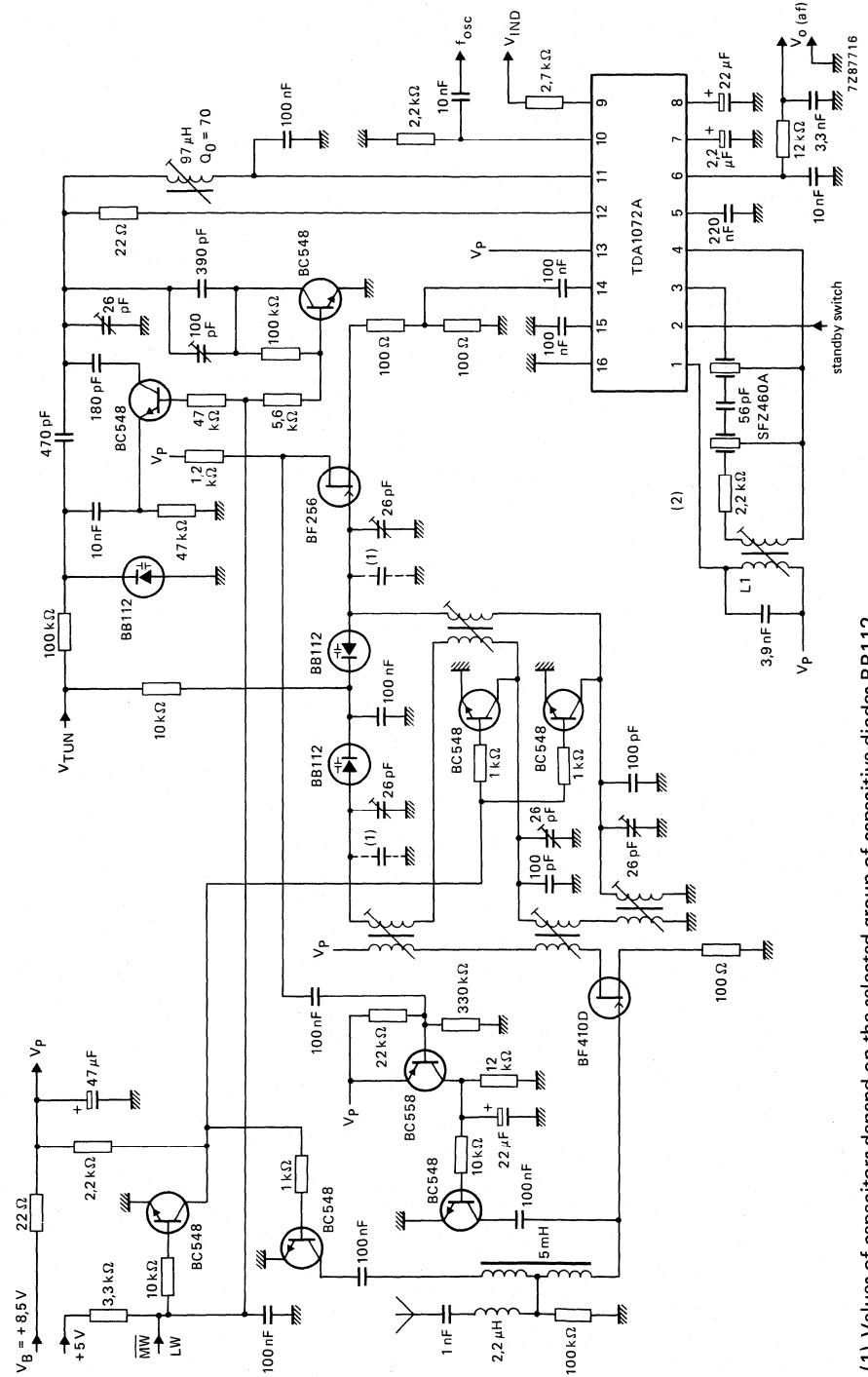


Fig. 17 Printed-circuit board showing track side.



(1) Values of capacitors depend on the selected group of capacitive diodes BB112.
(2) For i.f. filter and coil data refer to Fig. 1.

Fig. 18 Car radio application with capacitive diode tuning and electronic MW/LW switching. The circuit includes pre-stage a.g.c. optimised for good large-signal handling.

AM RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TDA1072AT integrated AM receiver circuit performs the active and part of the filtering functions of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50 MHz and can handle RF signals up to 500 mV. RF radiation and sensitivity to interference are minimized by an almost symmetrical design. The voltage-controlled oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the IF amplifier.

Features

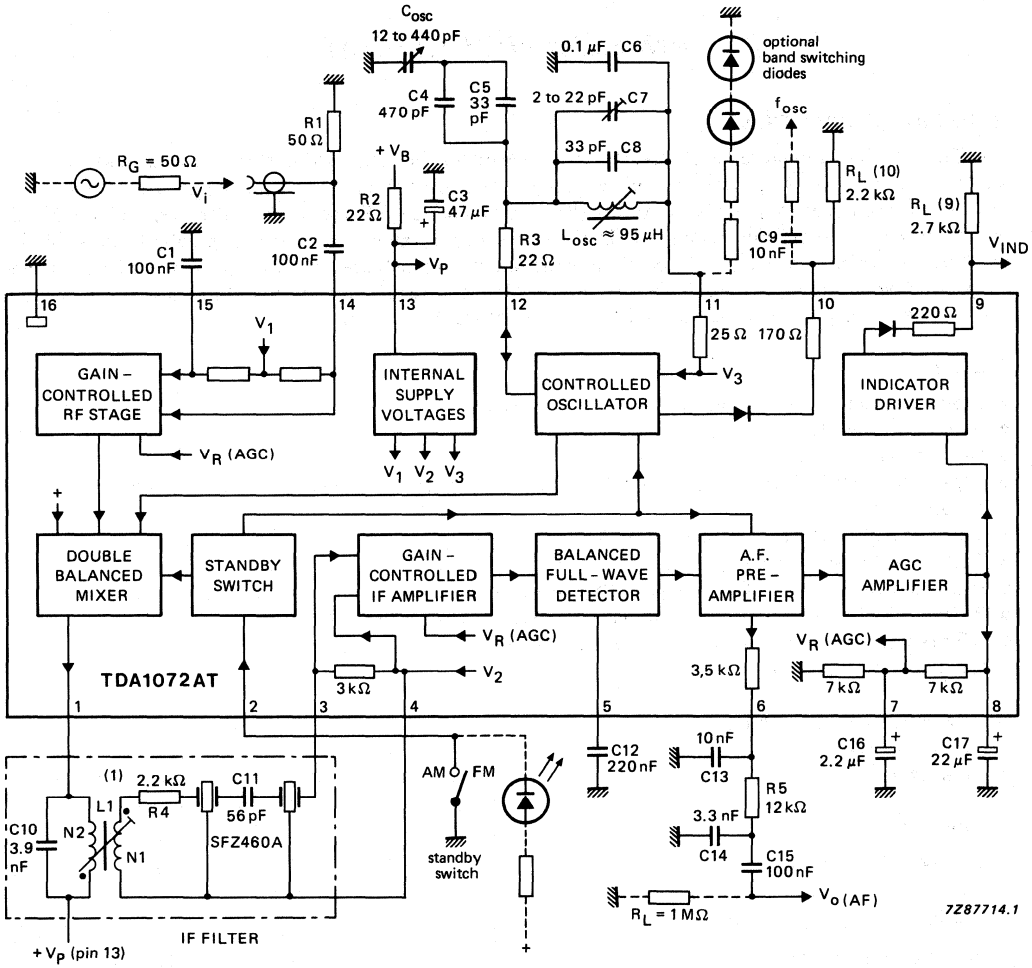
- Inputs protected against damage by static discharge
- Gain-controlled RF stage
- Double balanced mixer
- Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils
- Gain-controlled IF stage with wide AGC range
- Full-wave, balanced envelope detector
- Internal generation of AGC voltage with possibility of second-order filtering
- Buffered field strength indicator driver with short-circuit protection
- AF preamplifier with possibilities for simple AF filtering
- Electronic standby switch

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	7.5	–	10	V
Supply current range		I_P	15	–	26	mA
RF input voltage for S+N/N = 6 dB at m = 30%		V_I	–	1.5	–	μV
RF input voltage for 3% total harmonic distortion (THD) at m = 80%		V_I	–	500	–	mV
AF output voltage with V_I = 2 mV; f_I = 1 MHz; m = 30% and f_m = 400 Hz		$V_{O(AF)}$	–	310	–	mV
AGC range: change of V_I for 1 dB change of $V_{O(AF)}$			–	86	–	dB
Field strength indicator voltage at V_I = 500 mV; $R_{L(9)}$ = 2.7 kΩ		V_{IND}	–	2.8	–	V

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO16; SOT109A).



(1) Coil data: TOKO sample no. 7XNS-A7523DY; L1: N1/N2 = 12/32; Q_o = 65; Q_B = 57.
Filter data: Z_F = 700 Ω at R_{3-4} = 3 kΩ; Z_1 = 4.8 kΩ.

Fig.1 Block diagram and test circuit (connections shown in broken lines are not part of the test circuit).

FUNCTIONAL DESCRIPTION

Gain-controlled RF stage and mixer

The differential amplifier in the RF stage employs an AGC negative feedback network to provide a wide dynamic range. Very good cross-modulation behaviour is achieved by AGC delays at the various signal stages. Large signals are handled with low distortion and the S/N ratio of small signals is also improved. Low noise working is achieved in the differential amplifier by using transistors with a low base resistance.

A double balanced mixer provides the IF output to pin 1.

Oscillator

The differential amplifier oscillator is temperature compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage $V_{11\text{-}16}$. An extra buffered oscillator output is available for driving a synthesizer. If this is not needed, resistor $R_{L(10)}$ can be omitted.

Gain-controlled IF amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the AGC negative feedback network.

Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. The residual IF carrier is blocked from the signal path by an internal low-pass filter.

AF preamplifier

This stage preamplifies the audio frequency output. The amplifier output stage uses an emitter follower with a series resistor which, together with an external capacitor, provides the required low-pass filtering for AF signals.

AGC amplifier

The AGC amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the AGC voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives a fast AGC settling time which is advantageous for electronic search tuning. The AGC settling time can be further reduced by using capacitors of smaller value in the external filter. The AGC voltage is fed to the RF and IF stages via suitable AGC delays. The capacitor at pin 7 can be omitted for low-cost applications.

Field strength indicator output

A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If field strength information is not needed, $R_{L(9)}$ can be omitted.

FUNCTIONAL DESCRIPTION (continued)

Standby switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer and demodulator are switched off.

Short-circuit protection

All pins have short-circuit protection to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	$V_P = V_{13-16}$	V_{13}	–	12	V
Input voltage					
pins 14-15		V_{14-15}	–	10	V
pins 14-16		V_{14-16}	–	V_P	V
pins 15-16		V_{15-16}	–	V_P	V
pins 14-16		V_{14-16}	–	–0.6	V
pins 15-16		V_{15-16}	–	–0.6	V
Input current (pins 14 and 15)		I_{14-15}	–	200	mA
Total power dissipation*		P_{tot}	–	300	mW
Operating ambient temperature range		T_{amb}	–40	+ 80	°C
Storage temperature range		T_{stg}	–55	+ 150	°C
Junction temperature		T_j	–	+ 125	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	300	K/W
		160	K/W*

* Mounted on epoxiprint

CHARACTERISTICS

$V_P = V_{13-16} = 8.5$ V; $T_{amb} = 25$ °C; $f_i = 1$ MHz; $f_m = 400$ Hz; m = 30%; $f_{IF} = 460$ kHz; measured in test circuit of Fig.1; all measurements are with respect to ground (pin 16); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 13)		V_{13}	7.5	8.5	10	V
Supply current (pin 13)		I_{13}	15	23	27	mA
RF stage and mixer						
Input voltage (DC value)		V_{14-15}	–	$V_P/2$	–	V
RF input impedance at $V_I < 300\ \mu V$		R_{14-15}	–	5.5	–	kΩ
		C_{14-15}	–	25	–	pF
RF input impedance at $V_I > 10$ mV		R_{14-15}	–	8	–	kΩ
		C_{14-15}	–	22	–	pF
IF output impedance		R_1	500	0	0	kΩ
		C_1	–	6	–	pF
Conversion transconductance before start of AGC		I_1/V_I	–	6.5	–	mA/V
Maximum IF output voltage, inductive coupling to pin 1, (peak-to-peak value)		$V_{1(p-p)}$	–	5	–	V
DC value of output current (pin 1) at $V_I = 0$ V		I_1	–	1.2	–	mA
AGC range of input stage			–	30	–	dB
RF signal handling capability: input voltage for THD = 3% at m = 80% (RMS value)		$V_{I(rms)}$	–	500	–	mV
Oscillator						
Frequency range		Δf	0.6	–	60	MHz
Oscillator amplitude (pins 11 to 12) (peak-to-peak value)		$V_{11-12(p-p)}$	–	130	150	mV
External load impedance		$R_{11-12(ext)}$	0.5	–	200	kΩ
External load impedance for no oscillation		$R_{11-12(ext)}$	–	–	60	Ω

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Ripple rejection at V_P = 100 mV (RMS value); f_p = 100 Hz ($RR = 20 \log [V_{13}/V_{11}]$)						
Source voltage for switching diodes (6 x V_{BE})		V_{11}	–	4.2	–	V
DC output current (for switching diodes)	$V_P = V_{13} \leqslant 9$ V	I_{11}	0	–	5	mA
Change of output voltage at ΔI_{11} = 20 mA (switch to maximum load)		ΔV_{11}	–	0.5	–	V
Buffered oscillator output						
DC output voltage		V_{10}	–	0.7	–	V
Output signal amplitude (peak-to-peak value)		$V_{10(p\text{-}p)}$	–	320	–	mV
Output impedance		R_{10}	–	170	–	Ω
Output current		$I_{10(peak)}$	–	–	–3	mA
IF, AGC and AF stages						
DC input voltage		$V_{3\text{-}4}$	–	2	–	V
IF input impedance		$R_{3\text{-}4}$	2.4	3.0	3.9	kΩ
		$C_{3\text{-}4}$	–	7	–	pF
IF input voltage for THD = 3% at m = 80%		$V_{3\text{-}4}$	–	90	–	mV
Voltage gain before start of AGC		$V_{3\text{-}4}/V_6$	–	68	–	dB
AGC range of IF stages: change of $V_{3\text{-}4}$ for 1 dB change of $V_{O(AF)}$; $V_{3\text{-}4(ref)}$ = 75 mV		$\Delta V_{3\text{-}4}$	–	55	–	dB
AF output voltage at $V_{3\text{-}4(IF)}$ = 50 μV		$V_{O(AF)}$	–	130	–	mV
AF output voltage at $V_{3\text{-}4(IF)}$ = 1 mV		$V_{O(AF)}$	–	310	–	mV
AF output impedance (pin 6)		$\lvert Z_O \rvert$	–	3.5	–	kΩ

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Indicator driver						
Output voltage at V_I = 0 mV	$R_{L(9)}$ = 2.7 kΩ	V_9	–	20	150	mV
Output voltage at V_I = 500 mV	$R_{L(9)}$ = 2.7 kΩ	V_9	2.5	2.8	3.1	V
Load resistance		$R_{L(9)}$	2.7	–	–	kΩ
Standby switch						
Switching threshold at V_P = 7.5 to 18 V; T_{amb} = −40 to + 80 °C						
ON-voltage		V_2	0	–	2	V
OFF-voltage		V_2	3.5	–	20	V
ON-current	V_2 = 0 V	I_2	–	–	−200	μA
OFF-current	V_2 = 20 V	I_2	–	–	10	μA

OPERATING CHARACTERISTICS

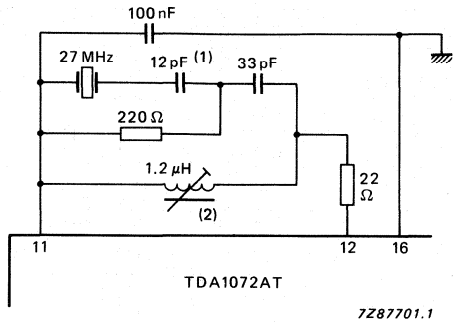
V_P = 8.5 V; f_I = 1 MHz; m = 30%; f_m = 400 Hz; T_{amb} = 25 °C; measured in Fig.1; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
RF sensitivity						
RF input required for S+N/N = 6 dB		V_I	–	1.5	–	μV
S+N/N = 26 dB		V_I	–	15	–	μV
S+N/N = 46 dB		V_I	–	150	–	μV
RF input at start of AGC		V_I	–	30	–	μV
RF large signal handling						
RF input at THD = 3%; m = 80%		V_I	–	500	–	mV
THD = 3%; m = 30%		V_I	–	700	–	mV
THD = 10%; m = 30%		V_I	–	900	–	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
AGC range						
Change of V_I for						
1 dB change of $V_{O(AF)}$	$V_{I(ref)}$ = 500 mV	ΔV_I	–	86	–	dB
6 dB change of $V_{O(AF)}$	$V_{I(ref)}$ = 500 mV	ΔV_I	–	91	–	dB
Output signal						
AF output voltage at						
V_I = 4 μV	m = 80%	$V_{O(AF)}$	–	130	–	mV
V_I = 1 mV		$V_{O(AF)}$	240	310	390	mV
Total harmonic distortion at						
V_I = 1 mV	m = 80%	d_{tot}	–	0.5	–	%
V_I = 500 mV	m = 30%	d_{tot}	–	1	–	%
Signal-to-noise ratio	V_I = 100 mV	S+N/N	–	58	–	dB
Ripple rejection at V_I = 2 mV V_P = 100 mV (RMS value) f_p = 100 Hz ($RR = 20 \log [V_P/V_{O(AF)}]$)		RR	–	38	–	dB
Unwanted signals						
Suppression of IF whistles at V_I = 15 μV; m = 0% related to AF signal of m = 30%						
at $f_I \approx 2 \times f_{IF}$		α_{2IF}	–	37	–	dB
at $f_I \approx 3 \times f_{IF}$		α_{3IF}	–	44	–	dB
IF suppression at RF input						
for symmetrical input		α_{IF}	–	40	–	dB
for asymmetrical input		α_{IF}	–	40	–	dB
Residual oscillator signal at mixer output						
at f_{osc}		$I_{(osc)}$	–	1	–	μA
at 2 x f_{osc}		$I_{(2osc)}$	–	1.1	–	μA

APPLICATION INFORMATION



(1) Capacitor values depend on crystal type.
(2) Coil data: 9 windings of 0.1 mm dia laminated Cu wire on TOKO coil set 7K 199CN; $Q_o = 80$.

Fig.2 Oscillator circuit using quartz crystal; centre frequency = 27 MHz.

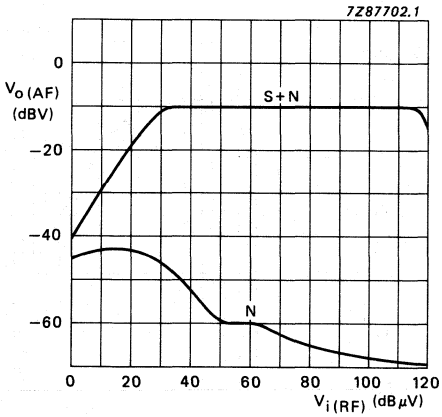


Fig.3 AF output as a function of RF input in the circuit of Fig.1; f_I = 1 MHz; f_m = 400 Hz; m = 30%.

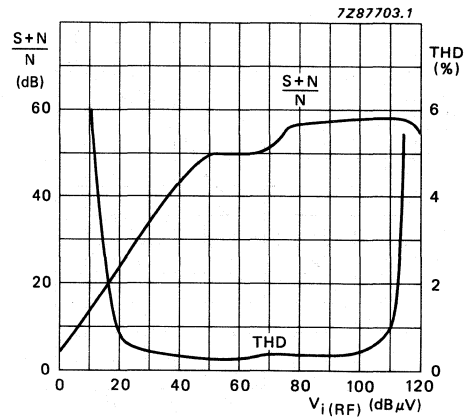


Fig.4 Total harmonic distortion and S+N/N as functions of RF input in the circuit of Fig.1; m = 30% for (S+N)/N curve and m = 80% for THD curve.

APPLICATION INFORMATION (continued)

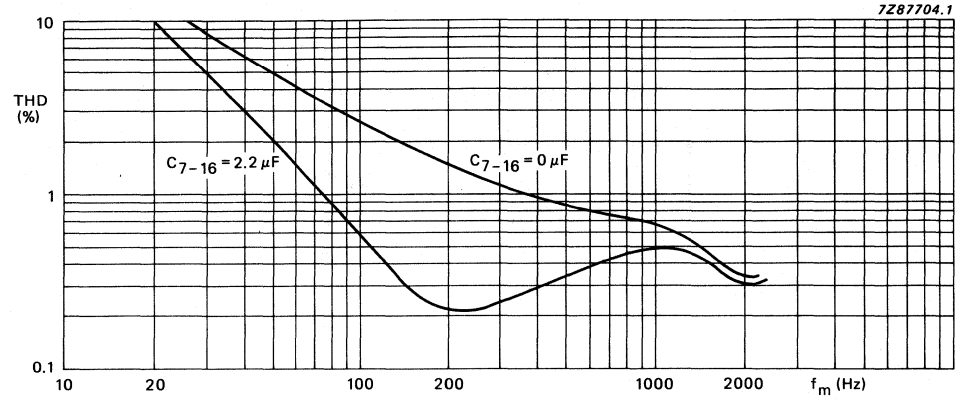


Fig.5 Total harmonic distortion as a function of modulation frequency at V_I = 5 mV; m = 80%; measured in the circuit of Fig.1 with $C_{7-16(ext)}$ = 0 μF and 2.2 μF.

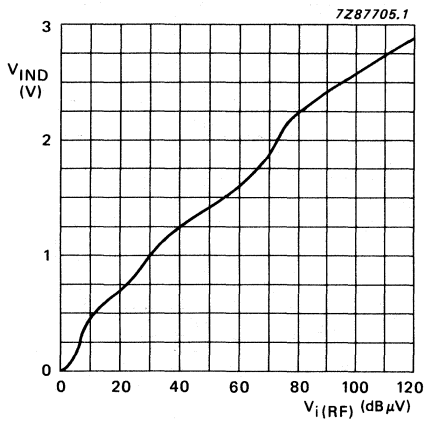
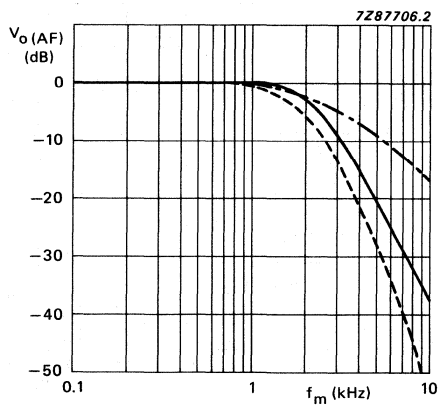


Fig.6 Indicator driver voltage as a function of RF input in the circuit of Fig.1.



—— with IF filter
—·— with AF filter
------ with IF and AF filter

Fig.7 Typical frequency response curves from Fig.1 showing the effects of filtering.

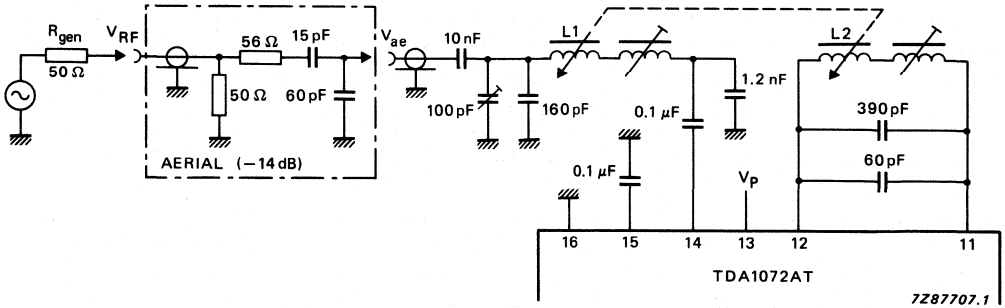


Fig.8 Car radio application with inductive tuning.

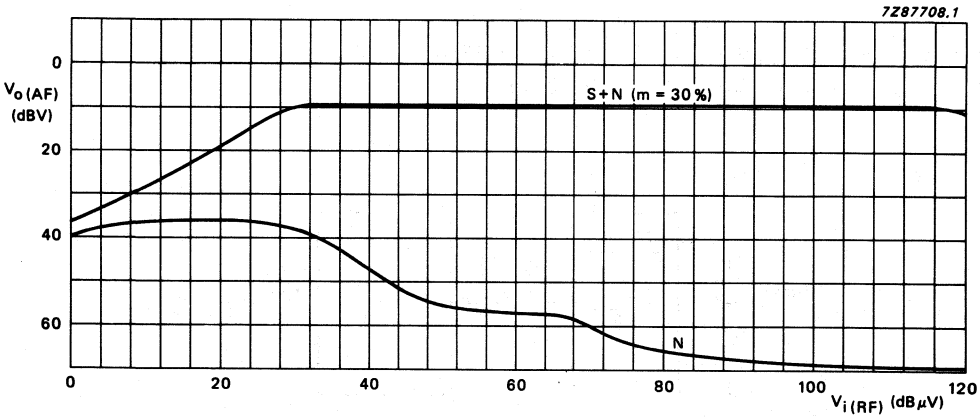


Fig.9 AF output as a function of RF input using the circuit of Fig.8 with that of Fig.1.

APPLICATION INFORMATION (continued)

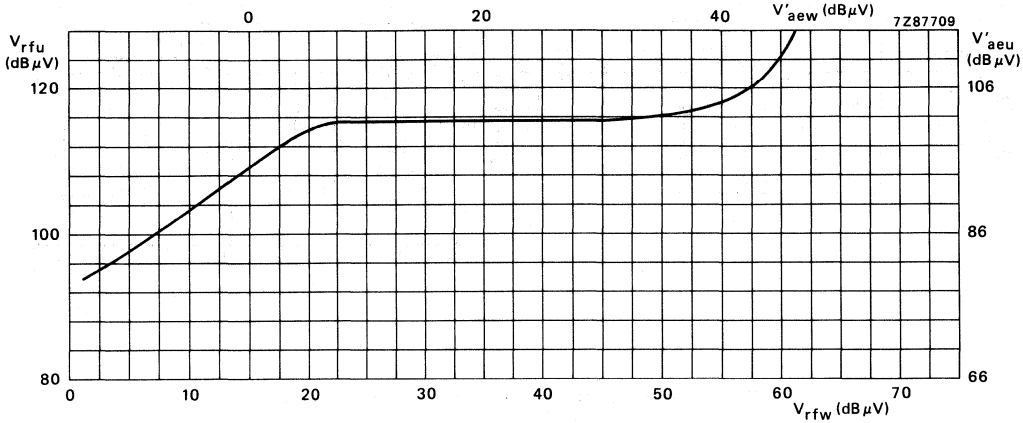


Fig.10 Suppression of cross-modulation as a function of input signal, measured in the circuit of Fig.8 with the input circuit as shown in Fig.11. Curve is for wanted $V_{O(AF)}$/unwanted $V_{O(AF)}$ = 20 dB; V_{rfw}, V_{rfu} are signals at the aerial input, V'_{aew}, V'_{aeu} are signals at the unloaded output of the aerial.

Wanted signal (V'_{aew}, V_{rfw}): f_i = 1 MHz; f_m = 400 Hz; m = 30%.

Unwanted signal (V'_{aeu}, V_{rfu}): f_i = 900 kHz; f_m = 400 Hz; m = 30%.

Effective selectivity of input tuned circuit = 21 dB.

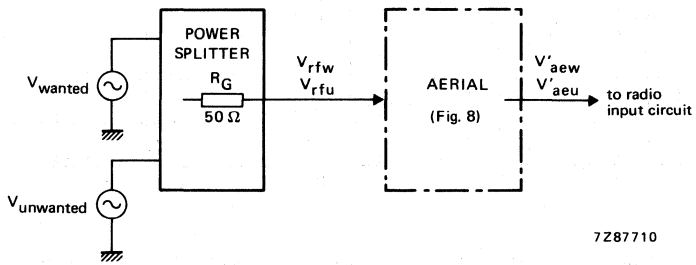


Fig.11 Input circuit to show cross-modulation suppression (see Fig.10).

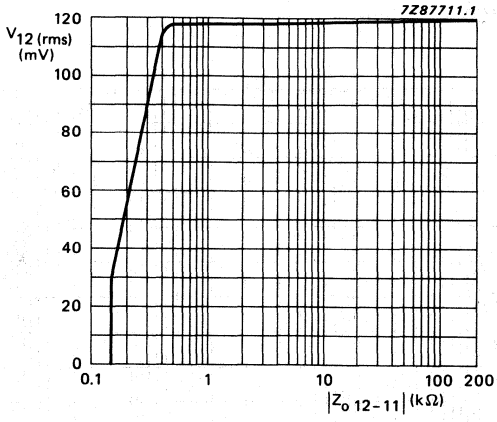


Fig.12 Oscillator amplitude as a function of the impedance at pins 11 and 12 in the circuit of Fig.8.

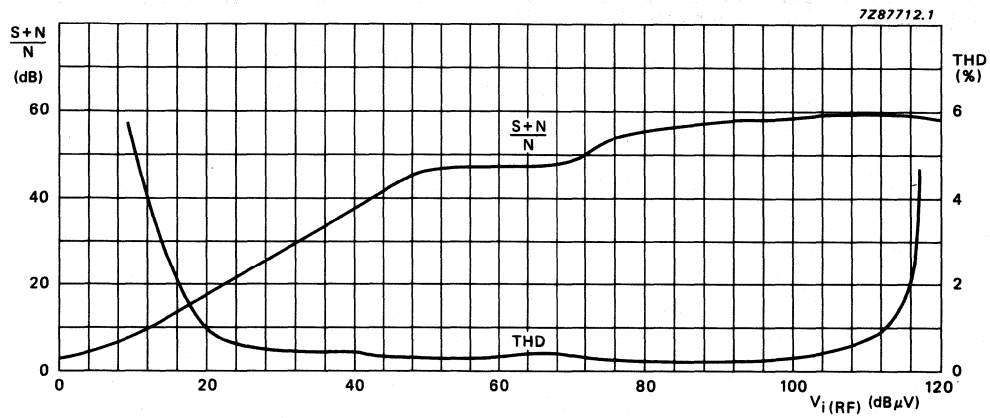


Fig.13 Total harmonic distortion and (S+N)/N as functions of RF input using the circuit of Fig.8 with that of Fig.1.

APPLICATION INFORMATION (continued)

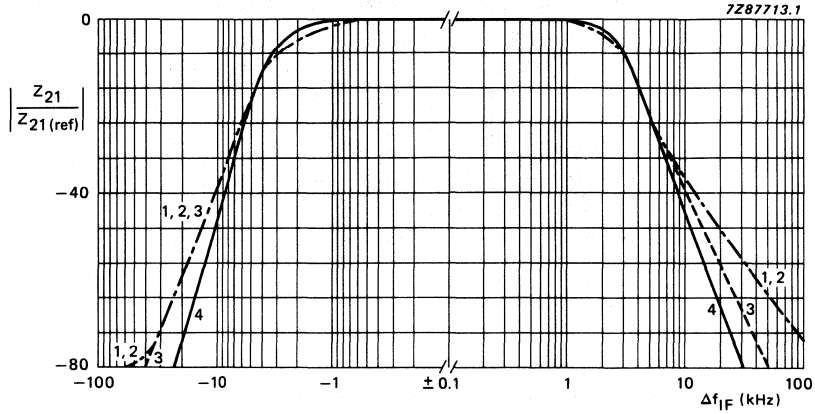


Fig.14 Forward transfer impedance as a function of intermediate frequency for filters 1 to 4 shown in Fig.14; centre frequency = 455 kHz.

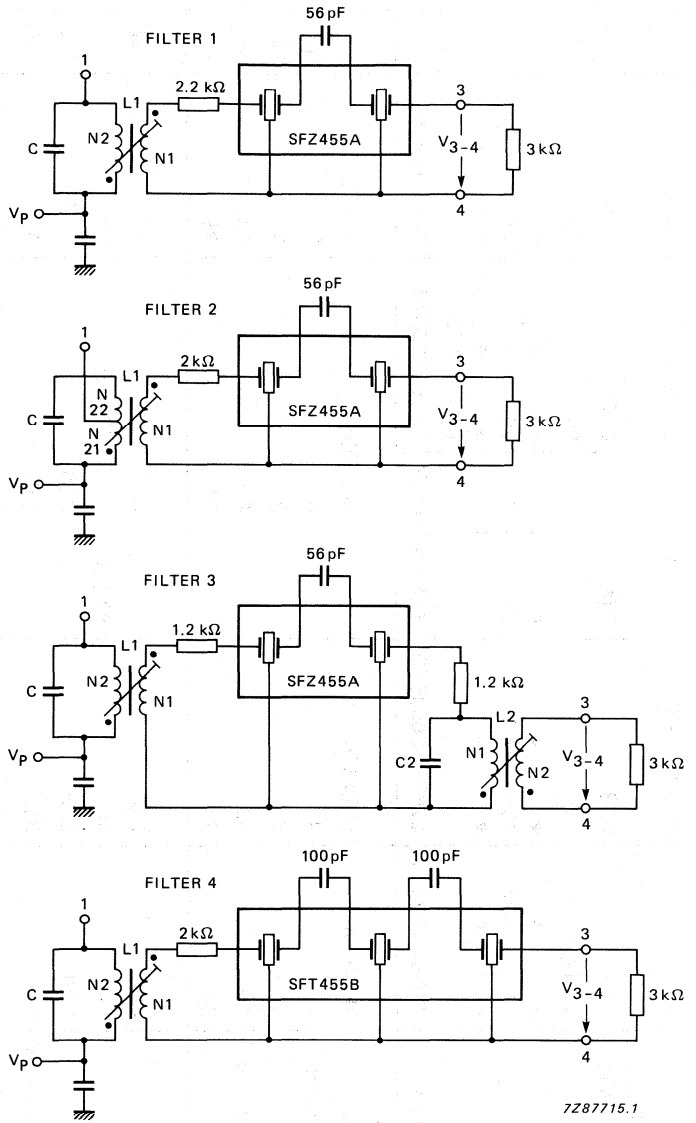
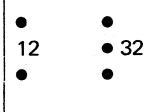
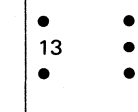
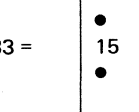
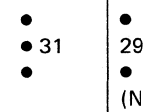
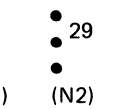
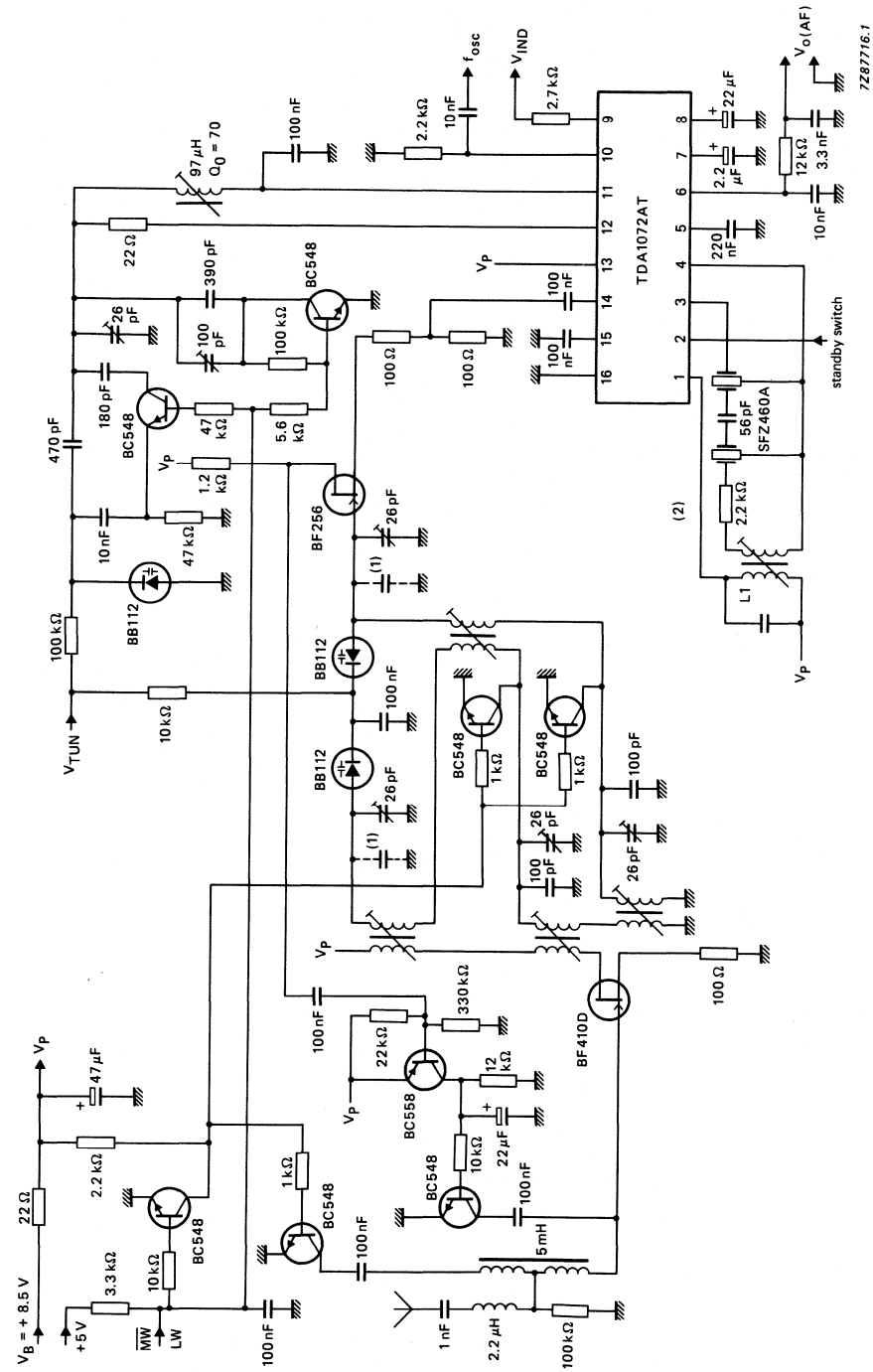


Fig.15 IF filter variants applied to the circuit of Fig.1; for filter data refer to Table 1.

filter no.	1	2	3		4	unit
Coil data	L1	L1	L1	L2	L1	
Value of C	3900	430	3900	4700	3900	pF
N1: N2	12 : 32	13 : (33 + 66)	15 : 31	29 : 29	13 : 31	
Diameter of Cu laminated wire	0.09	0.08	0.09	0.08	0.09	mm
Q_o	65 (typ.)	50	75	60	75	
Schematic* of windings						
Toko order no.	7XNS-A7523DY	L7PES-A0060BTG	7XNS-A7518DY	7XNS-A7521AIH	7XNS-A7519DY	
Resonators						
Murata type	SFZ455A	SFZ455A	SFZ455A		SFT455B	
D (typical value)	4	4	4		6	dB
R_G, R_L	3	3	3		3	kΩ
Bandwidth (−3 dB)	4.2	4.2	4.2		4.5	kHz
S_{9kHz}	24	24	24		38	dB
Filter data						
Z_I	4.8	3.8	4.2		4.8	kΩ
Q_B	57	40	52 (L1)	18 (L2)	55	
Z_F	0.70	0.67	0.68		0.68	kΩ
Bandwidth (−3 dB)	3.6	3.8	3.6		4.0	kHz
S_{9kHz}	35	31	36		42	dB
S_{18kHz}	52	49	54		64	dB
S_{27kHz}	63	58	66		74	dB

* The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding. N2 the outer winding.

Table 1 Data for IF filters shown in Fig.15. Criterium for adjustment is Z_F = maximum (optional selectivity curve at centre frequency f_o = 455 kHz). See also Fig.14.



(1) Values of capacitors depend on the selected group of capacitive diodes BB112.

(2) For IF filter and coil data refer to Fig.1.

Fig.18 Car radio application with capacitive diode tuning and electronic MW/LW switching. The circuit includes pre-stage AGC optimised for good large-signal handling.

DUAL TANDEM ELECTRONIC POTENTIOMETER CIRCUIT

GENERAL DESCRIPTION

The TDA1074A is a monolithic integrated circuit designed for use as volume and tone control circuit in stereo amplifiers. This dual tandem potentiometer IC consists of two ganged pairs of electronic potentiometers with the eight inputs connected via impedance converters, and the four outputs driving individual operational amplifiers. The setting of each electronic potentiometer pair is controlled by an individual d.c. control voltage. The potentiometers operate by current division between the arms of cross-coupled long-tailed pairs. The current division factor is determined by the level and polarity of the d.c. control voltage with respect to an externally available reference level of half the supply voltage. Since the electronic potentiometers are adjusted by a d.c. control voltage, each pair can be controlled by single linear potentiometers which can be located in any position dictated by the equipment styling. Since the input and feedback impedances around the operational amplifier gain blocks are external, the TDA1074A can performs bass/treble and volume/loudness control. It also can be used as a low-level fader to control the sound distribution between the front and rear loudspeakers in car radio installations.

Features

- High impedance inputs to both 'ends' of each electronic potentiometer
- Ganged potentiometers track within 0,5 dB
- Electronic rejection of supply ripple
- Internally generated reference level available externally so that the control voltage can be made to swing positively and negatively around a well-defined 0 V level
- The operational amplifiers have push-pull outputs for wide voltage swing and low current consumption
- The operational amplifier outputs are current limited to provide output short-circuit protection
- Although designed to operate from a 20 V supply (giving a maximum input and output signal level of 6 V), the TDA1074A can work from a supply as low as 7,5 V with reduced input and output signal levels

QUICK REFERENCE DATA

Supply voltage (pin 11)	V_P	typ.	20 V
Supply current (pin 11)	I_P	typ.	22 mA
Input signal voltage (r.m.s. value)	$V_{i(rms)}$	max.	6 V
Output signal voltage (r.m.s. value)	$V_{o(rms)}$	max.	6 V
Total harmonic distortion	THD	typ.	0,05 %
Output noise voltage (r.m.s. value)	$V_{no(rms)}$	typ.	50 μV
Control range	$\Delta\alpha$	typ.	110 dB
Cross-talk attenuation (L/R)	α_{ct}	typ.	80 dB
Ripple rejection (100 Hz)	α_{100}	typ.	46 dB
Tracking of ganged potentiometers	ΔG_v	typ.	0,5 dB
Supply voltage range	V_P		7,5 to 23 V
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

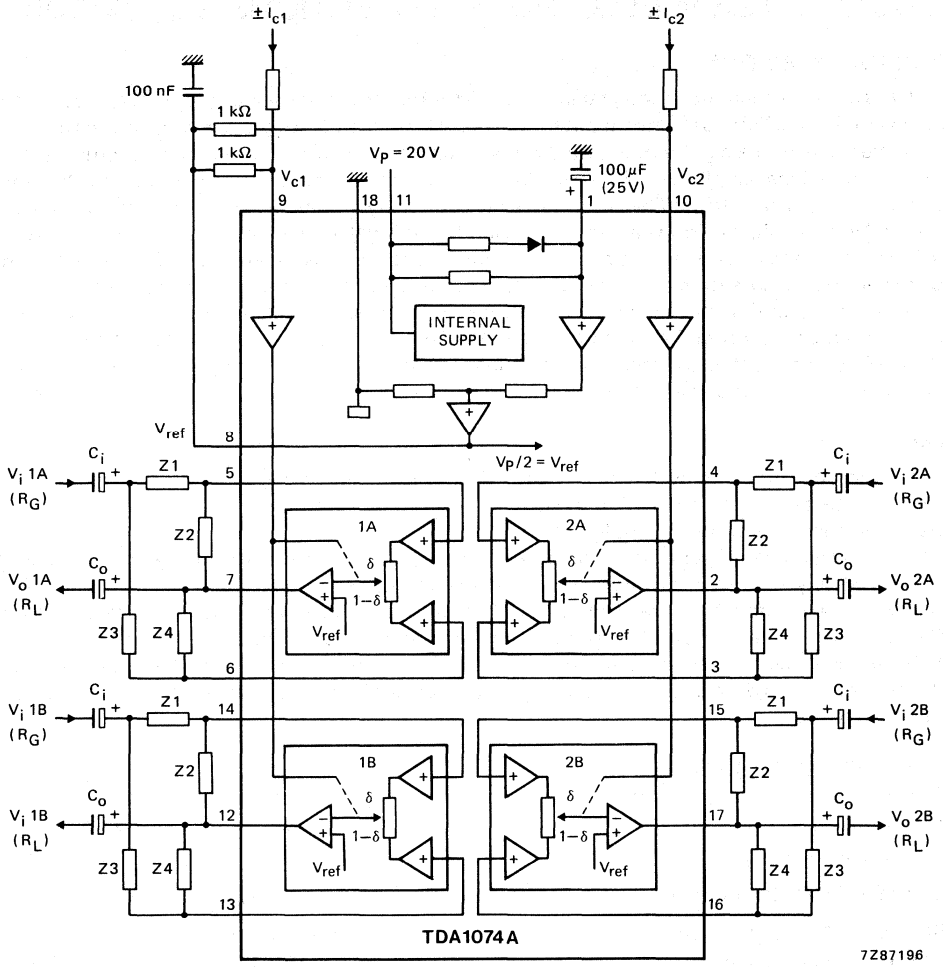


Fig. 1 Block diagram and basic external components; I_{c1} (at pin 9) and I_{c2} (at pin 10) are control input currents; V_{c1} (at pin 9) and V_{c2} (at pin 10) are control input voltages with respect to $V_{ref} = V_P/2$ at pin 8; Z1 = Z2 = Z3 = Z4 = 22 kΩ; the input generator resistance R_G = 60 Ω; the output load resistance R_L = 4,7 kΩ; the coupling capacitors at the inputs and outputs are C_i = 2,2 µF and C_o = 10 µF respectively.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	V_P	max.	23 V
Control voltages (pins 9 and 10)	$\pm V_{c1}; \pm V_{c2}$	max.	1 V
Input voltage ranges (with respect to pin 18) at pins 3, 4, 5, 6, 13, 14, 15, 16	V_i		0 to V_P V
Total power dissipation	P_{tot}	max.	800 mW
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80 K/W

REMARK

The difference between the TDA1074 and its successor the TDA1074A is shown in Fig. 2 as the different component configuration at pin 8.

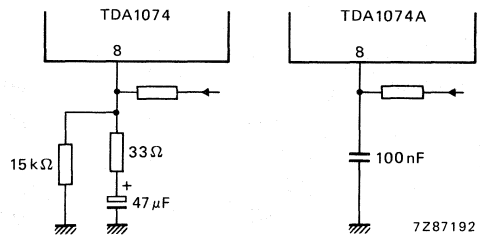


Fig. 2 Component configuration at pin 8 showing the difference between the TDA1074 and the TDA1074A.

APPLICATION INFORMATION

Treble and bass control circuit

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 3; R_G = 60 Ω; $R_L > 4{,}7$ kΩ; $C_L < 30$ pF; f = 1 kHz; with a linear frequency response ($V_{c1} = V_{c2} = 0$ V); unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply current (without load)	I_P	14	22	30	mA
Frequency response (−1 dB) $V_{c1} = V_{c2} = 0$ V	f	10	–	20 000	Hz
Voltage gain at linear frequency response ($V_{c1} = V_{c2} = 0$ V)	G_v*	–	0	–	dB
Gain variation at f = 1 kHz at maximum bass/treble boost or cut at $\pm V_{c1} = \pm V_{c2} = 120$ mV	ΔG_v*	–	± 1	–	dB
Bass boost at 40 Hz (ref. 1 kHz) $V_{c2} = 120$ mV		–	17,5	–	dB
Bass cut at 40 Hz (ref. 1 kHz) $-V_{c2} = 120$ mV		–	17,5	–	dB
Treble boost at 16 kHz (ref. 1 kHz) $V_{c1} = 120$ mV		–	16	–	dB
Treble cut at 16 kHz (ref. 1 kHz) $-V_{c1} = 120$ mV		–	16	–	dB
Total harmonic distortion at $V_{o(rms)} = 300$ mV f = 1 kHz (measured selectively)	THD	–	0,002	–	%
f = 20 Hz to 20 kHz	THD	–	0,005	–	%
at $V_{o(rms)} = 5$ V f = 1 kHz	THD	–	0,015	0,1	%
f = 20 Hz to 20 kHz	THD	–	0,05	0,1	%
Signal level at THD = 0,7% (input and output)	$V_{i;\,o(rms)}$	5,5	6,2	–	V
Power bandwidth at reference level $V_{o(rms)} = 5$ V (−3 dB); THD = 0,1%	B	–	40	–	kHz
Output noise voltages signal plus noise (r.m.s. value); f = 20 Hz to 20 kHz	$V_{no(rms)}$	–	75	–	μV
noise (peak value); weighted to DIN 45 405; CCITT filter	$V_{no(m)}$	–	160	230	μV

* $G_v = V_o/V_i$.

Treble and bass control circuit

parameter	symbol	min.	typ.	max.	unit
Cross-talk attenuation (stereo)					
f = 1 kHz	α_{ct}	–	86	–	dB
f = 20 Hz to 20 kHz	α_{ct}	–	80	–	dB
Control voltage cross-talk to the outputs at f = 1 kHz; $V_{c1(rms)} = V_{c2(rms)} = 1$ mV	$-\alpha_{ct}$	–	20	–	dB
Ripple rejection at f = 100 Hz; $V_{P(rms)} < 200$ mV	α_{100}	–	46	–	dB

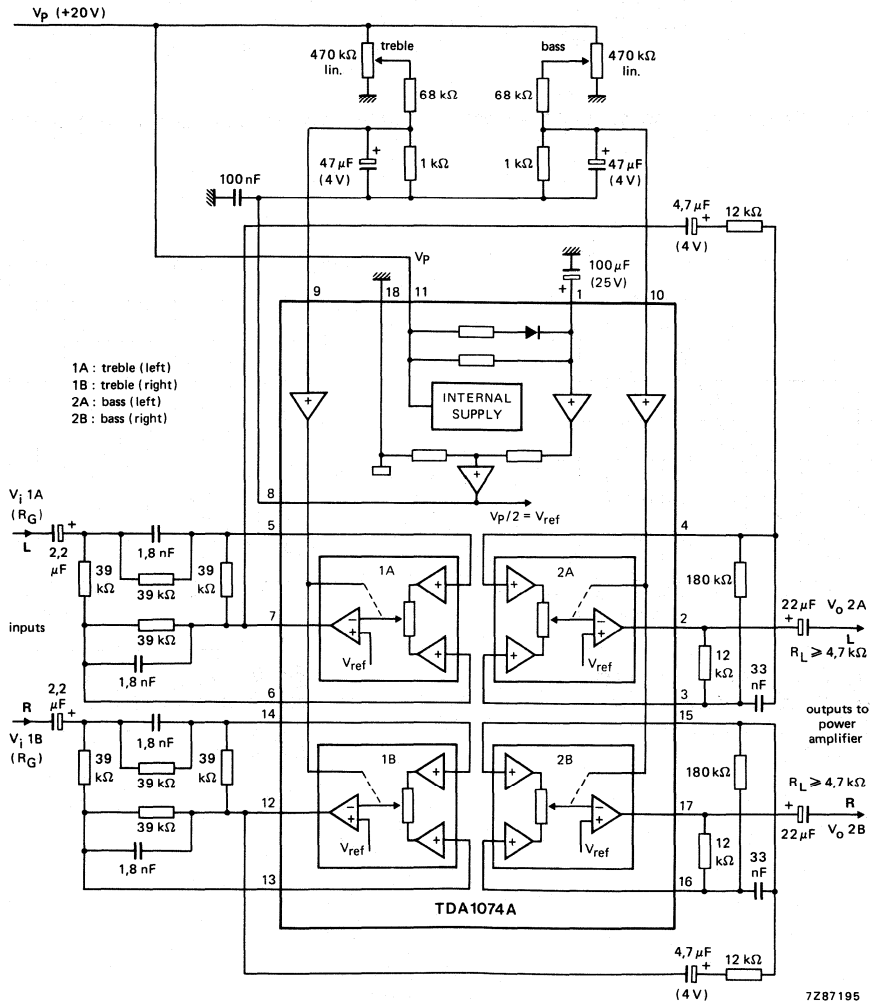


Fig. 3 Application diagram for treble and bass control.

APPLICATION INFORMATION (continued)

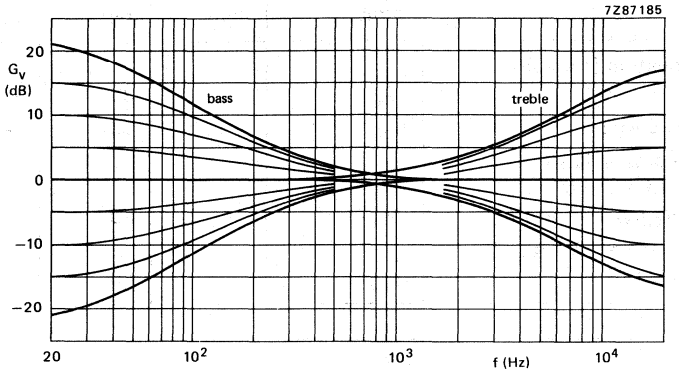


Fig. 4 Frequency response curves; voltage gain (treble and bass) as a function of frequency.

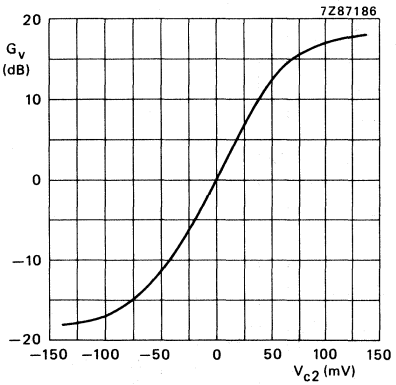


Fig. 5 Control curve; voltage gain (bass) as a function of the control voltage (V_{c2}); f = 40 Hz.

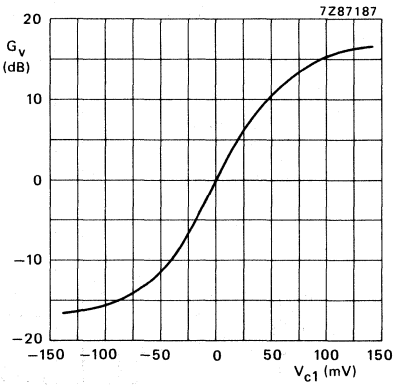
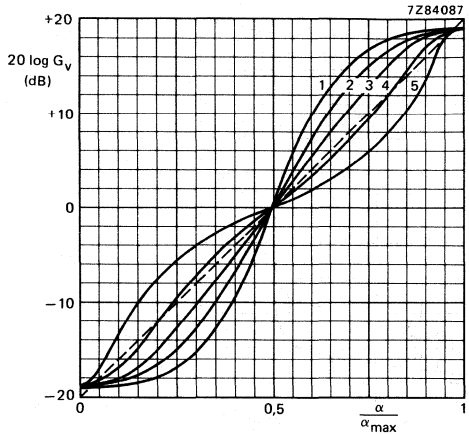


Fig. 6 Control curve; voltage gain (treble) as a function of the control voltage (V_{c1}); f = 16 kHz.



curve no.	value of R
1	10 kΩ
2	100 kΩ
3	220 kΩ
4	470 kΩ
5	1 MΩ

Fig. 7 Voltage gain ($G_V = V_o/V_i$) control curves as a function of the angle of rotation (α) of a linear potentiometer (R); for curve numbers see table above; f = 40 Hz to 16 kHz.

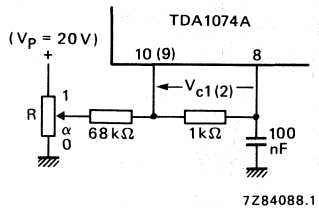


Fig. 8 Circuit diagram for measuring curves in Fig. 7.

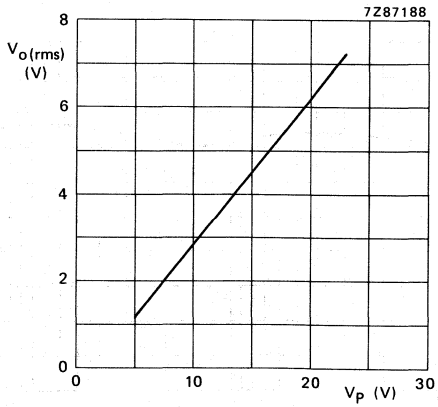


Fig. 9 Output signal level as a function of V_P; THD = 0,7%; f = 1 kHz; $V_{c1} = V_{c2} = 0$ V.

APPLICATION INFORMATION (continued)

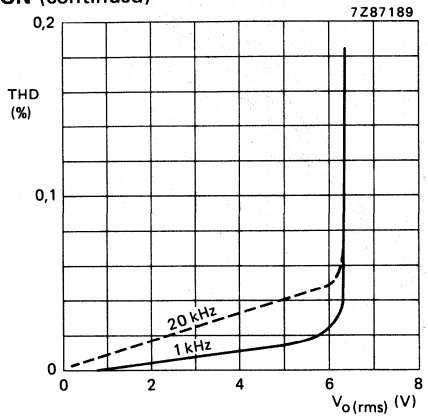


Fig. 10 Total harmonic distortion as a function of the output level; V_P = 20 V; R_L = 4,7 kΩ; $V_{c1} = V_{c2}$ = 0 V (linear, $G_{v\,tot}$ = 1). ——— f = 1 kHz; – – – – f = 20 kHz.

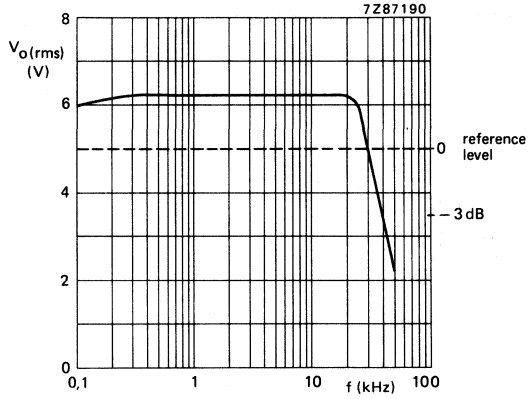


Fig. 11 Power bandwidth at THD = 0,1%; reference level is 5 V (r.m.s.).

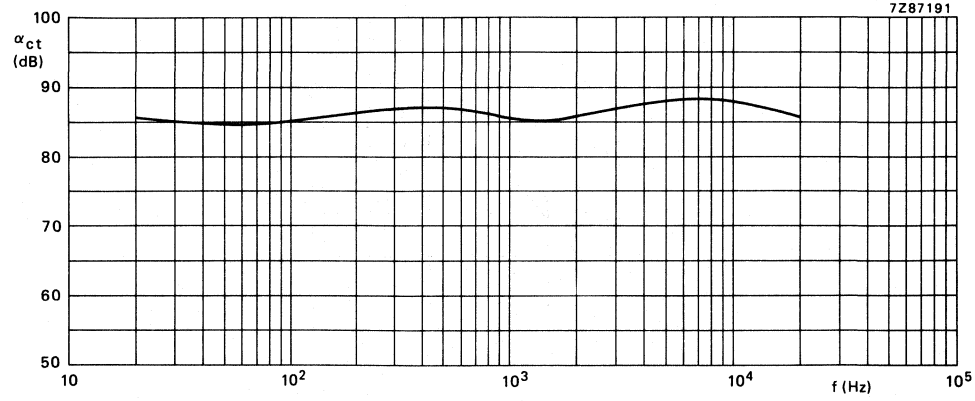
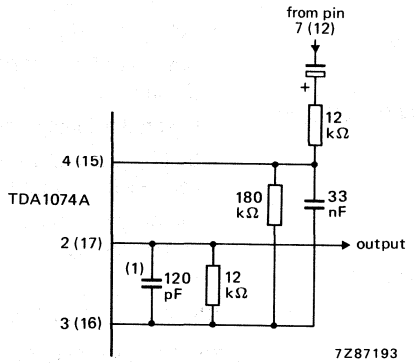


Fig. 12 Cross-talk as a function of frequency; linear treble/bass setting ($V_{c1} = V_{c2}$ = 0 V); V_i = 5 V; R_G = 60 Ω; R_L = 4,7 kΩ.

Application recommendations

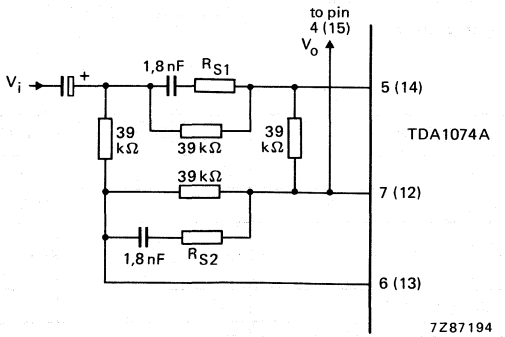
1. If one or more electronic potentiometers in an IC are not used, the following is recommended:
   a. Unused signal inputs of an electronic potentiometer should be connected to the associated output, e.g. pins 3 and 4 to pin 2.
   b. Unused control voltage inputs should be connected directly to pin 8 (V_{ref}).
2. Where more than one TDA1074A IC are used in an application, pins 1 can be connected together; however, pins 8(V_{ref}) may not be connected together directly.
3. Additional circuitry for limiting the frequency response in the ultrasonic range.



(1) $f_{-3\,dB}$ = 110 kHz at linear setting

Fig. 13 Circuit diagram for frequency response limiting.

4. Alternative circuitry for limiting the gain of the treble control circuit in the ultrasonic range.



For $R_{S1} = R_{S2}$ = 3,3 kΩ; $f_{-3\,dB} \cong$ 1 MHz at linear setting
For $R_{S1} = R_{S2}$ = 0 Ω; $f_{-3\,dB} \cong$ 100 kHz at linear setting

Fig. 14 Circuit diagram for limiting gain of treble control circuit.

Digital servo processor (DSIC2) TDA1301T

FEATURES

The DSIC2 realizes the following servo functions:

- Diode signal preprocessing
- Focus servo loop
- Radial servo loop
- Sledge motor servo loop
- Three-line serial interface via the microcontroller

The other features include:

- Full digital signal processing
- Low power consumption, down to 30 mW
- Low voltage supply 3 to 5.5 V
- Integrated analog-to-digital converters and digital servo loop filters
- Double speed possible
- Easy application
  - Single supply voltage
  - Small number of external components; only 6 decoupling capacitors
  - Flexible system oscillator circuitry
  - Usable for single/double Foucault and astigmatic focus
  - Full automatic radial error signal initialization offset control and level initialization for track position indicator
  - No external adjustments required; no component ageing
  - Wide range of adjustable servo characteristics
  - Simple 3-line serial command interface
  - 28-pin SO package
  - Great flexibility towards different CD mechanisms
  - Full and transparent application information
- High robustness/shock insensitivity
  - Sophisticated track-loss (TL) detection mechanism
  - Fast focus restart procedure
  - Extended radial error signal
  - Adjustable radial shock detector
  - Defect drop-out detector
- Fully automatic jump procedure for radial servo
- Automatic focus start-up procedure and built-in FOK (Focus OK)
- Fast radial jump or access procedure
- Self-operational servo-control without continuous communication via the microcontroller
- Direct communication to photodiode optics; no external preprocessing.

GENERAL DESCRIPTION

The TDA1301T is a fully digital servo processor which has been designed to provide all servo functions, except the spindle motor control, in two-stage three-spot compact disc systems. The device offers a high degree of integration, combined with the low additional cost of external components. The servo characteristics have a wide range of adjustment via a three-line serial interface. This offers an enormous flexibility with respect to applications for different CD mechanisms. The circuit is optimized for low-power low-voltage applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		3.0	–	5.5	V
V_{DDA}	analog supply voltage		3.0	–	5.5	V
I_{DDD}	digital supply current		–	5	–	mA
I_{DDA}	analog supply current		–	5	–	mA
$I_{DDD(q)}$	digital quiescent supply current		–	–	10	µA
$I_{i(cd)}$	central diode input currents (D1 to D4)	note 1	–	–	15.8	µA
$I_{i(sd)}$	satellite diode input currents (R1 and R2)	note 1	–	–	7.9	µA
P_{tot}	total power dissipation		–	50	–	mW
T_{amb}	operating ambient temperature		–40	–	+85	°C

Note

1. f_{sys} = 4.2336 MHz; V_{RL} = 0 V; V_{RH} = 2.5 V (externally applied).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1301T	28	SO28L	plastic	SOT136A

BLOCK DIAGRAM

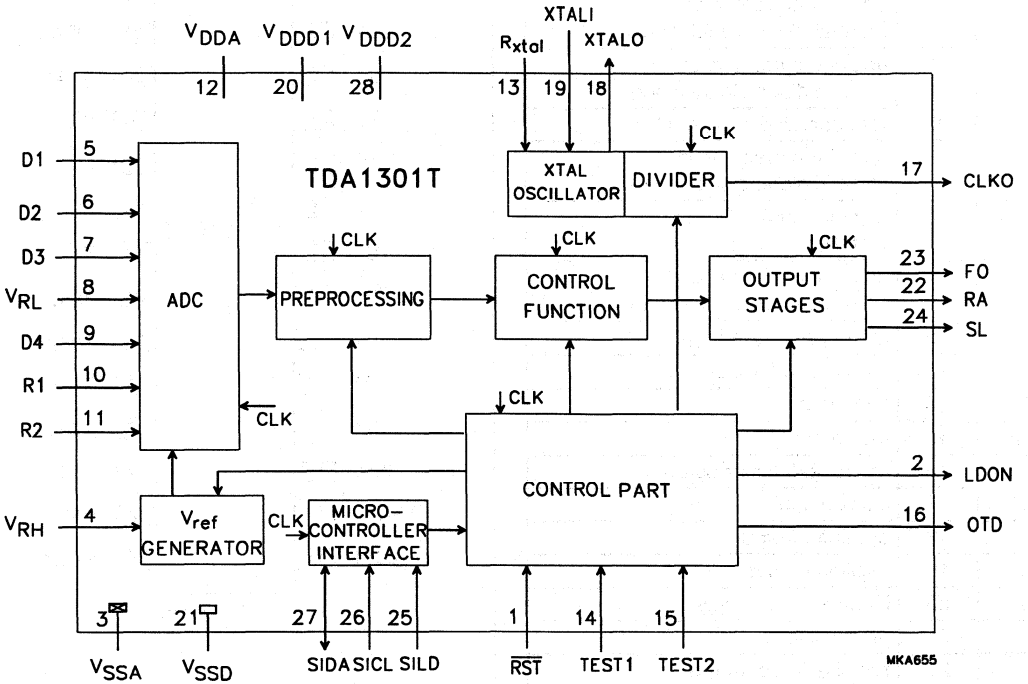


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{RST}$	1	reset input (active LOW)
LDON	2	laser drive on output
V_{SSA}	3	analog ground
V_{RH}	4	reference input for reference voltage generator
D1	5	unipolar current input (central diode signal input)
D2	6	unipolar current input (central diode signal input)
D3	7	unipolar current input (central diode signal input)
V_{RL}	8	reference input for ADC
D4	9	unipolar current input (central diode signal input)
R1	10	unipolar current input (satellite diode signal input)
R2	11	unipolar current input (satellite diode signal input)
V_{DDA}	12	analog supply voltage
$XTAL_{ref}$	13	oscillator reference input
TEST1	14	test input 1
TEST2	15	test input 2
OTD	16	off-track detector output
CLKO	17	clock output
XTALO	18	oscillator output
XTALI	19	oscillator input
V_{DDD1}	20	digital power supply 1
V_{SSD}	21	digital ground
RA	22	radial actuator output
FO	23	focus actuator output
SL	24	sledge output
SILD	25	serial interface load input
SICL	26	serial interface clock input
SIDA	27	serial interface data input/output
V_{DDD2}	28	digital power supply 2

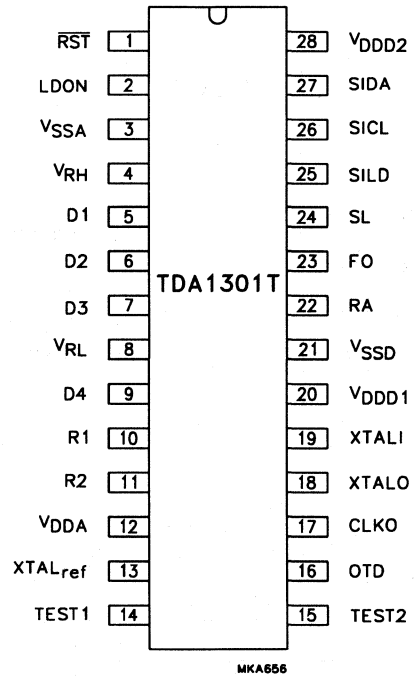


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Three spots front-end

The photo detector in a two-stage three-spots compact disc system normally contains six discrete elements. Four of these elements (in the event of single Foucault: three elements) carry the central aperture (CA) signal while the other two elements (satellite signals) carry the radial tracking information. Besides the HF signal, which is finally applied to both of the audio channels, the central aperture also contains information for the focus servo loop. To enable the HF signal to be processed, the frequency contents of the central aperture signal must be divided into an HF data part and an LF servo part. The HF signal is processed outside the DSIC2 by the TDA1302 or a discrete amplifier-equalizer. The necessary crossover point, to extract the LF servo part, is compensated for in the amplifier.

Diode signal processing

The analog signals from the photo detectors are converted into a digital representation using analog-to-digital converters. The ADCs are designed to convert unipolar currents into a digital code. The dynamic range of the input currents is adjustable within a given range and is dependent on the ADC input reference voltages V_{RL} and V_{RH}. The maximum current for the central diodes signals is given in equation (1).

$$I_{i(max)} = f_{sys} \times (V_{RH} - V_{RL}) \times 1.5 \times 10^{-6} \text{ [}\mu\text{A]} \quad (1)$$

The maximum current for the satellite signals is given in equation (2).

$$I_{i(max)} = f_{sys} \times (V_{RH} - V_{RL}) \times 0.75 \times 10^{-6} \text{ [}\mu\text{A]} \quad (2)$$

V_{RH} is generated internally. There are four different levels (1.0, 1.5, 2.0 and 2.5 V) which can be selected under software control. In the application V_{RL} is connected to V_{SSA}. It is also possible to drive V_{RH} with an external voltage source but in this situation the internal voltage source has to be switched off (software controlled).

Signal conditioning

The digital codes retrieved from the ADCs are applied to logic circuitry to obtain the various control signals. The signals from the central aperture detectors are processed so that the normalized focus error signal (FE) given in equation (3) is realized:

$$FE_n = \frac{D1 - D2}{D1 + D2} - \frac{D3 - D4}{D3 + D4} \quad (3)$$

Where the detector set-up is assumed to be as illustrated in Fig.3.

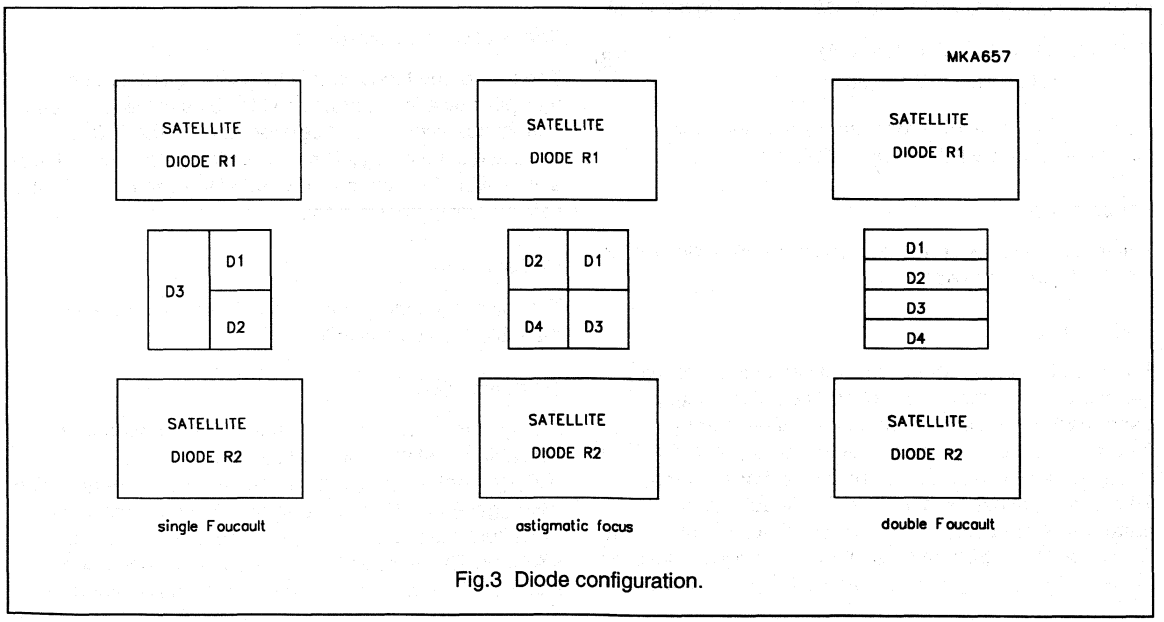


Fig.3 Diode configuration.

In the event of single Foucault focusing method, the DSIC2 signal conditioning can be switched under software control so that the signal processing conforms to that given in equation (4).

$$FE_n = 2 \times \frac{D1 - D2}{D1 + D2} \quad (4)$$

The FE_n thus obtained is further processed by a proportional integral and differential filter section (PID). A focus OK flag (FOK) is generated by means of the central aperture signal and an adjustable reference level. This signal is used to provide extra protection for the Track-Loss (TL) generation, the focus start-up procedure and the drop-out detection. The radial or tracking error signal is generated by the satellite detector signals R1 and R2. The radial error signal (RE) can be formulated as per equation (5).

$$RE_s = (R1 - R2) \times RE\_gain + (R1 + R2) \times RE\_offset \quad (5)$$

Where the index 's' indicates the automatic scaling operation which is performed on the radial error signal.

This scaling is necessary to avoid non-optimum dynamic range usage in the digital representation and, also, to reduce radial bandwidth spread. The radial error signal will also be released from offset during disc start-up. The four signals from the central aperture detectors, together with the satellite detector signals, generate a track position signal (TPI) which can be formulated as per equation (6).

$$TPI = \sin [(D1 + D2 + D3 + D4) - (R1 + R2) \times Sum\_gain] \quad (6)$$

Where the weighting factor Sum_gain is generated internally in the DSIC2 during initialization.

Focus control

The following focus servo functions are incorporated in the DSIC2 digital controller.

Focus start-up

Five initially loaded coefficients influence the start-up behaviour of the focus controller. The automatically generated triangular voltage can be influenced by 3 parameters, for the height (ramp_heigth) and DC-offset (ramp_offset) of the triangle and its steepness (ramp_inc). To protect against false focus point detections two parameters are available. One is an absolute level on the CA signal (CA_start) and the other is an absolute level on the FE_n signal (FE_start). When the CA_start level is reached, the FOK signal becomes true. If the FOK signal is true when the level on the FE_n signal is reached the focus PID is enabled and switches on when the next zero crossing is detected in the FE_n signal.

Focus position control loop

The focus control loop contains a digital PID controller which has 5 parameters available to the user. These coefficients influence the integrating (foc_int), proportional (foc_prop) and differentiating (foc_pole_lead) action of this PID and the digital low-pass filter (foc_pole_noise) which follows the PID. The fifth coefficient (foc_gain) influences the loop gain.

Drop-out detection

This detector can be influenced by one parameter (CA_drop). The FOK signal will become false and the integrator of the PID will hold if the CA signal drops below the programmed absolute CA level. When the FOK signal becomes false it is assumed, initially, to be caused by a black dot.

Focus loss detection and fast restart

Whenever FOK is false for longer than approximately 3 ms, it is assumed that the focus point is lost. A fast restart procedure is initiated which is capable of restarting the focus loop within 200 to 300 ms depending on the programmed coefficients set by the microcontroller.

Focus loop gain switching

The gain of the focus control loop (foc_gain) can be multiplied by a factor of 2 or divided by a factor of 2 during normal operation. The integrator value of the PID is corrected accordingly. The differentiating (foc_pole_lead) action of the PID can be switched at the same time as the gain switching is performed.

Radial control

The following radial servo functions are incorporated in the DSIC2 digital controller.

Level initialization

During start-up an automatic adjustment procedure is activated to set the values of the radial error gain (RE_gain), offset (RE_offset) and satellite sum signal gain (Sum_gain) for TPI level generation. The initialization procedure runs in a radial open-loop situation and is $\leq$300 ms. This start-up time period may coincide with the last part of the turn table motor start-up time period.

Automatic gain adjustment: as a result of this initialization the amplitude of the RE signal is adjusted within 10% around the nominal RE amplitude.

Offset adjustment: the additional offset in RE due to the limited accuracy of the start-up procedure is less than 50 nm.

TPI level generation: the accuracy of the initialization procedure is such that the duty cycle range of TPI becomes $0.4 < \delta < 0.6$ {δ = TPI(HIGH)/TPI(period)}.

SLEDGE HOME

Sledge moves to reference position (end_stop_switch) at the inner side of the disc with user defined voltage.

TRACKING CONTROL

The actuator is controlled using a PID loop-filter with user defined coefficients and gain. For stable operation between the tracks, the S-curve is extended over ¾ track. Upon request from the microcontroller S-curve extension over 2 tracks is used, automatically changing to access control when these two tracks are exceeded.
Both modes of S-curve extension make use of a track-count mechanism as described in Section "Off-track counting" . In this mode track counting results in automatic 'return-to-zero track', to avoid major music rhythm disturbances in the audio output to provide improved shock resistance. The sledge is continuously controlled using the filtered value of the integrator contents of the actuator, or upon request by the microcontroller. The microcontroller can read out this integrator value and provides the sledge with step pulses to reduce power consumption. Filter coefficients of the continuous sledge control can be preset by the user.

ACCESS

The access procedure is divided into 2 different modes, depending on the requested jump size.

The access procedure makes use of a track counting mechanism (see Section "Off-track counting"), a velocity signal based upon the number of tracks passed within a fixed time interval, a velocity setpoint calculated from the number of tracks to go and a user programmable parameter indicating the maximum sledge performance. If the number of tracks to go is greater than break_dist the sledge jump mode will be activated (otherwise the actuator jump will be performed). The requested jump size together with the required sledge braking distance at maximum access speed defines the value break_dist.
During the actuator jump mode, velocity control with a PI controller is used for the actuator.

The sledge is then continuously controlled using the filtered value of the integrator contents of the actuator. All filter parameters (for actuator and sledge) are user programmable.
In the sledge jump mode, maximum power (user programmable) is applied to the sledge in the correct direction, while the actuator becomes Idle (the contents of the actuator integrator leaks to zero just after the sledge jump mode is initiated).

Table 1 Access procedure.

ACCESS TYPE	JUMP SIZE	ACCESS SPEED
Actuator jump	1 – break distance (1)	decreasing velocity
Sledge jump	break (1) – 32768	minimum power to sledge (1)

Note

1. Can be preset by the microcontroller.

Defect detector

A built-in defect detector prevents the light spot from going out-of-focus and going off-track due to disc drop-out excitations. The defect detector can be switched ON or OFF under software control and can be applied to the focus control only, or to both the focus and radial control. The detected defect signal holds the focus and radial loop filter outputs. The hold signal is generated whenever the reflected light intensity drops rapidly (<1.5 ms) down to 75% of the actual intensity level.

Shock detector

The shock detector can be switched ON during normal track following. The shock detector detects, within an adjustable frequency band, whether the disturbances in the radial spot position relative to the track exceeds an adjustable level. Every time the radial tracking error (RE) exceeds this level the radial control bandwidth is switched directly to twice the original bandwidth.
The shock detection level is adjustable in 64 steps from 0 to 100% of the nominal radial amplitude. The bandpass filter (BPF) lower frequency (–3 dB) can be fixed at 0 or 20 Hz. Independently, the BPF upper frequency (–3 dB) can be fixed at 750 or 1850 Hz.

Off-track counting

TPI is a flag which is used to indicate whether the spot is positioned on the track (with a margin of ¼ of the track-pitch).

In combination with the radial polarity flag (RP) the relative spot-position over the tracks can be determined. These signals are, however, affected with some uncertainties caused by:

- Disc defects such as scratches and fingerprints.
- The HF information on the disc, which is considered as noise by the detector signals.

In order to determine the spot position with sufficient accuracy, extra conditions are necessary to generate a TL signal as well as an off-track counter value. These extra conditions influence the maximum speed and this implies that, internally, one of the three following counting states is selected. These states are:

1. Protected state: used in normal play situations.
   A good detection caused by disc defects is important in this state.
2. Slow counting state: used in low velocity track jump situations.
   In this state a fast response is important rather than the protection against disc defects (if the phase relationship between TL and RP of a $\frac{1}{2\pi}$ rad is affected too much, the direction cannot be determined accurately any more).
3. Fast counting state: used in high velocity track jump situations.
   Highest obtainable velocity is the most important feature in this state.

Off-track detection

During active radial tracking, off-track detection is realized by continuously monitoring the off-track counter value. The off-track flag (OTD) becomes valid whenever the off-track counter value is not equal to zero. Depending on the type of extended S-curve the off-track counter will be reset after $\frac{3}{4}$ extend or at the original track in the $2\frac{1}{4}$ track extend mode.

Output stages

The control signals for the different actuators are 1-bit noise shaped digital outputs at 1.0584 MHz. An analog representation of the output signals can be achieved by connecting a first-order low-pass filter to the outputs. When the $\overline{\text{RST}}$ pin is held LOW, the focus, radial and sledge output stages are 3-state.

Serial interface

To control the DSIC2 operation, a serial interface is implemented which allows communication with a microcontroller via a 3-line serial bus consisting of:

- Serial clock line (SICL
- Serial data line (SIDA)
- Serial control line (SILD).

The SICL line is controlled by a microcontroller and can be completely asynchronous from the oscillator frequency of the DSIC2. The SILD line is used for read/write control and end-of-byte signalling.
The communication is bi-directional and processes 8-bit words (1 byte, MSB first). The data present on the SIDA line is clocked on the positive edge of SICL. One information exchange consists of one command byte and up to 7 data bytes.

The first byte defines the command, and is always input to the DSIC2. This byte defines if data has to be written to or read from the DSIC2. If data has to be written to the DSIC2 this byte also specifies the number of data bytes. The number of bytes read from the DSIC2 can vary from 0 up to 5 and only depends on how many the microprocessor requires to read. Further information concerning the serial protocol is available upon request.

Clock generation

The DSIC2 operates with an internal clock frequency of approximately 4 MHz. The circuit that generates the clock has three modes: the oscillator frequency divided by 2, 3 or 4 (software controlled). It is therefore possible to connect a crystal or a resonator with a frequency of 8.4672, 11.2896 or 16.9344 MHz. These frequencies are derived from today's frequently used decoder IC frequencies. It is also possible to drive the clock circuit with an external clock signal. The clock buffer output (CLKO) can supply the system clock or twice the system clock (also switchable under software control via the serial bus) to be used as a clock generator for other ICs. The oscillator circuit is optimized for low power dissipation. To guarantee optimum performance with a quartz crystal or a resonator the gain of the oscillator can be adjusted by an external resistor connected to the $XTAL_{ref}$ input.

Reset

The reset is controlled by means of the $\overline{\text{RST}}$ pin (active LOW). This circuit ensures proper initialization of the digital circuit and the output stages.

Laser drive on

The LDON pin is used to switch the laser drive OFF and ON. It is an open-drain output. When the laser is ON, the output has a high impedance.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	0	6.5	V
V_{DDA}	analog supply voltage	0	6.5	V
ΔV_{SS}	difference in ground supply voltage between V_{SSA} and V_{SSD}	−5.0	+5.0	mV
P_{max}	maximum power dissipation	−	100	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−40	+85	°C

HANDLING

Classification A: human body model; C = 100 pF; R = 1500 Ω; V ≥ 2000 V.
Charge device model: C = 200 pF; R = 0 Ω; V ≥ 250 V.
Pulse widths in accordance with *"UZW-BO/FQ-A302 and B302"* are applicable and can be found in the *"Quality reference pocket-book"* (ordering number 9398 510 34011).

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	80 K/W

CHARACTERISTICS

$V_{DDD} = V_{DDA} = 5$ V; $V_{SSA} = V_{SSD} = 0$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage		3.0	–	5.5	V
V_{DDA}	analog supply voltage		3.0	–	5.5	V
I_{DDD}	digital supply current		–	5	–	mA
I_{DDA}	analog supply current		–	5	–	mA
$I_{DDD(q)}$	quiescent current		–	–	60	µA
P_{tot}	total power dissipation		–40	–	+85	°C
Analog part						
$I_{i(cd)max}$	maximum input current for central diode input signal	note 1	–	15.8	–	µA
$I_{i(sd)max}$	maximum input current for satellite diode input signal	note 1	–	7.9	–	µA
V_{RH}	HIGH level reference voltage	note 2				
	output stage 1		0.9	1.0	1.1	V
	output stage 2		1.35	1.5	1.65	V
	output stage 3		1.8	2.0	2.2	V
	output stage 4		2.25	2.5	2.75	V
PSRR	power supply ripple rejection at pin 4	note 3	45	55	–	dB
V_{RH}	HIGH level reference voltage	input state; note 4	0.5	–	$V_{DDA} - 0.5$	V
V_{RL}	LOW level reference voltage		0	$V_{DDA} - 1.5$	–	V
(THD+N)/S	total harmonic distortion plus signal-to-noise ratio	at 0 dB; note 5	–	–50	–45	dB
S/N	signal-to-noise ratio		–	55	–	dB
PSRR	power supply ripple rejection at pin 12	note 3	–	45	–	dB
G_{tol}	gain tolerance	note 6	–10	–	+15	%
ΔG	variation of gain between channels		–	–	2	%
α_{cs}	channel separation		–	60	–	dB
Digital part						
INPUTS: TEST1, TEST2, SICL AND SILD						
V_{IL}	LOW level input voltage	$T_{amb} = -40$ to +85 °C	–	–	$0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage	$T_{amb} = -40$ to +85 °C	$0.75V_{DDD}$	–	–	V
I_{LI}	input leakage current		–	–	10	µA
INPUT: NRST						
V_{IL}	LOW level input voltage	$T_{amb} = -40$ to +85 °C	–	–	$0.2V_{DDD}$	V
V_{IH}	HIGH level input voltage	$T_{amb} = -40$ to +85 °C	$0.8V_{DDD}$	–	–	V
I_{LI}	input leakage current		–	–	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OUTPUTS: CLKO AND OTD						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	1.6	–	–	mA
I_{OH}	HIGH level output current	$V_{OH} = V_{DDD} - 0.4$ V	1.3	–	–	mA
t_r	rise time	note 7	–	–	44	ns
t_f	fall time	note 7	–	–	40	ns
OUTPUT: LDON						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3.3	–	–	mA
I_{OZ}	3-state output leakage current	T_{amb} = –40 to +85 °C; $V_O = V_{SSD}/V_{DDD}$	–	–	1.5	µA
t_r	rise time, LOW to 3-state	C_L = 50 pF	–	–	37	ns
t_f	fall time, 3-state to LOW	C_L = 50 pF	–	–	20	ns
OUTPUTS; RA, FO AND SL						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3.3	–	–	mA
I_{OH}	HIGH level output current	$V_{OH} = V_{DDD} - 0.4$ V	1.8	–	–	mA
I_{OZ}	3-state output leakage current	T_{amb} = –40 to +85 °C; $V_O = V_{SSD}/V_{DDD}$	–	–	1.5	µA
t_r	rise time	note 7	–	–	37	ns
t_f	fall time	note 7	–	–	20	ns
INPUT/OUTPUT: SIDA						
V_{IL}	LOW level input voltage	T_{amb} = –40 to +85 °C	–	–	$0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage	T_{amb} = –40 to +85 °C	$0.75V_{DDD}$	–	–	V
I_{OL}	LOW level output sink current	V_{OL} = 0.4 V	3.3	–	–	mA
I_{OH}	HIGH level output source current	$V_{OH} = V_{DDD} - 0.4$ V	1.8	–	–	mA
I_{OZ}	3-state output leakage current	T_{amb} = –40 to +85 °C; $V_O = V_{SSD}$ or V_{DDD}	–	–	1.5	µA
t_r	rise time	note 7	–	–	37	ns
t_f	fall time	note 7	–	–	20	ns
OSCILLATOR						
f_{osc}	oscillator frequency		8	–	17	MHz
C_i	input capacitance		–	–	4	pF
C_o	output capacitance		–	–	4	pF
C_{fb}	feedback capacitance		–	–	3	pF
R_{xtal}	external oscillator reference resistor	note 8	25	–	100	kΩ
R_{ext}	external reference resistor	note 9	–	10	–	kΩ
$V_{19(p-p)}$	minimum input clock voltage level from external oscillator (peak-to-peak value)	AC-coupled; R_{ext} = 10 kΩ; R_{bias} = 1 MΩ connected between pins 18 and 19	–	500	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Slave clock mode: XTALI						
V_{IL}	LOW level input voltage		–	–	0.5	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
t_H	HIGH level input time	relative to the clock period	45	–	55	%

Notes

1. f_{sys} = 4.2336 MHz; V_{RL} = 0 V; V_{RH} = 2.5 V (externally applied).
2. Internal reference source with 4 different output voltages. Selection is achieved via the serial interface. The given values are for an unloaded reference voltage.
3. f_{ripple} = 1 kHz; V_{ripple} = 0.5 V (p-p).
4. Internal reference is switched OFF by serial interface. V_{RH} is the reference input.
5. Externally applied V_{RH} = 2.5 V and V_{RL} = 0 V, measuring bandwidth: 200 Hz to 20 kHz, $f_{i(ADC)}$ = 1 kHz.
6. The gain of the ADC is defined as: $G_{ADC} = f_{sys}/I_{max}$ (counts/mA). Thus the digital output is $I_I \times G_{ADC}$ where: digital output is the number of pulses at the digital output in counts per second and I_I is the DC input current in mA.
   The maximum input current depends on the system frequency (f_{sys}) and on $V_{ref} = V_{RH} - V_{RL}$
   For D1 to D4: $I_{i(max)} = 1.5 \times f_{sys} \times V_{ref} \times 10^{-6}/R_i \times f_{sys}$ [μA].
   For R1 and R2: $I_{i(max)} = 0.75 \times f_{sys} \times V_{ref} \times 10^{-6}/R_i \times f_{sys}$ [μA].
   The gain tolerance is the deviation from the calculated gain regarding note 1.
7. At 10 to 90% levels with C_L = 50 pF.
8. A resistor must be connected to set the gain of the oscillator circuit. The value of the resistor depends on the crystal or resonator connected to the oscillator circuit (see also Chapter "Application information").
9. When the TDA1301T is supplied by an external oscillator frequency, no crystal or resonator is required while the external reference resistor has different limits.

APPLICATION INFORMATION

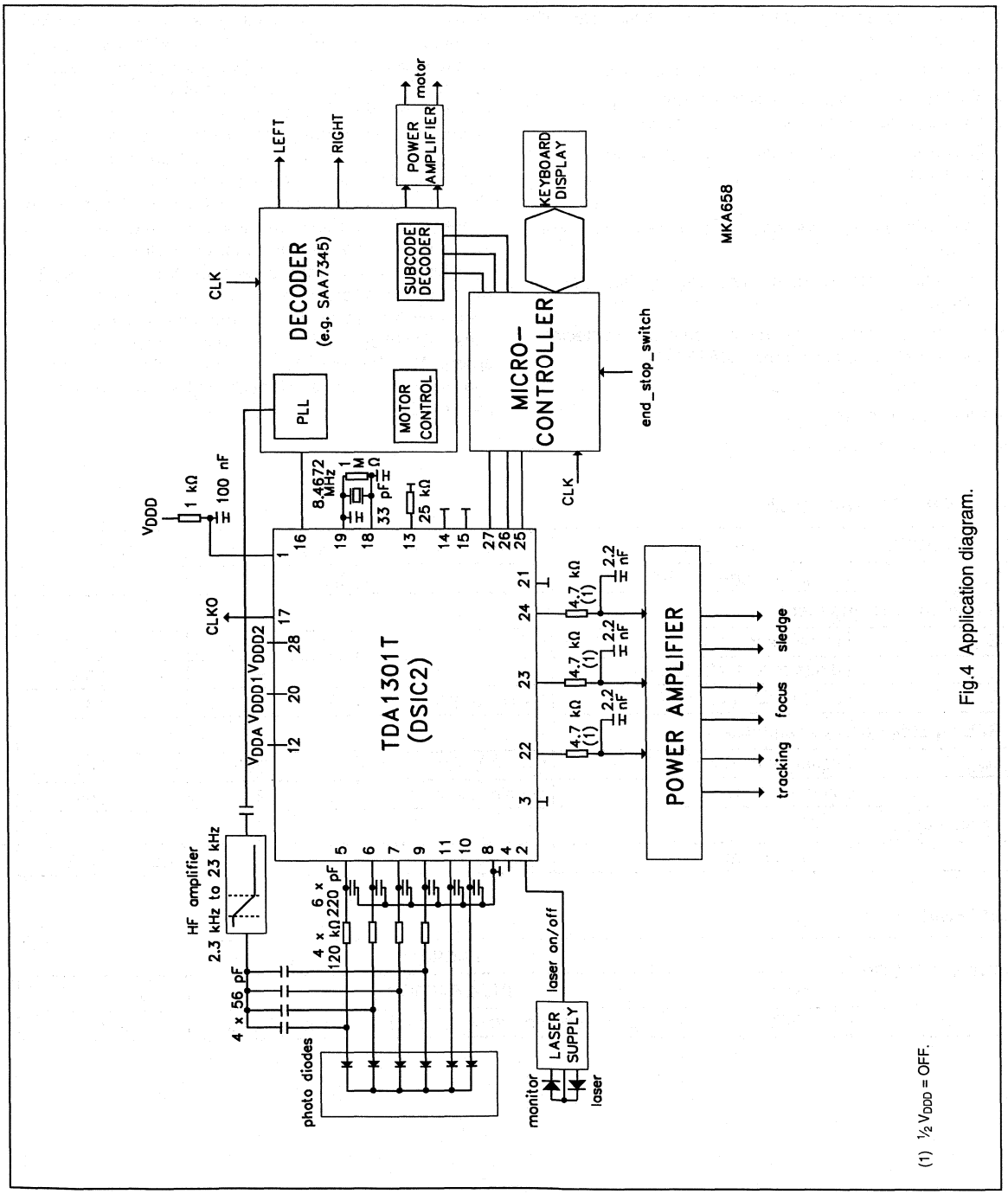


Fig.4 Application diagram.

Data amplifier and laser supply circuit for CD player and read only optical systems

TDA1302T

FEATURES

- Six input buffer amplifiers with low-pass filtering and with virtually no offset
- HF data amplifier with a high or low gain mode
- Two built-in equalizers for single or double-speed mode ensuring high performance in both modes
- Fully automatic laser control including stabilization and an ON/OFF switch, plus a separate supply (V_{DDL}) for power reduction
- Adjustable laser bandwidth and laser switch-on current slope
- Protection circuit to prevent laser damage due to supply voltage dip
- Optimized interconnectiion between pick-up detector and digital servo processor (TDA1301T)
- Wide supply voltage range
- Wide temperature range
- Low power consumption.

GENERAL DESCRIPTION

The TDA1302T is a data amplifier and laser supply circuit for three-beam pick-up detectors applied in a wide range of mechanisms for Compact Disc and read only optical systems. The device contains 6 amplifiers which amplify and filter the focus and radial diode signals and provides an equalized RF signal suitable for single or double speed mode; the mode can be switched by means of the speed control pin. The device can accommodate astigmatic, single foucault and double foucault detectors and can be applied to all N-sub laser/monitor diode units even though the circuit has been optimized for the Philips CDM12 mechanisms and the digital servo controller TDA1301T. After a single initial adjustment the circuit will maintain control over the laser diode current thus resulting in a constant light output power which is independent of ageing. The IC is mounted in a small-outline package to enable it to be mounted close to the laser pick-up unit on the sledge.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (pin 18)		3.4	–	5.5	V
Diode current amplifiers						
G_{dn}	amplification		–	1.55	–	dB
$I_{os(d)}$	diode output offset current		–	–	100	nA
B	3 dB bandwidth	$I_{i(d)}$ = 1.67 μA	50	–	–	kHz
RFE amplifier (built-in equalizer)						
$t_{d(eq)}$	equalization delay	f_i = 0.3 MHz	–	320	–	ns
$t_{d(f)}$	flatness delay	double-speed	–	5	–	ns
Laser supply						
$I_{o(l)}$	output current	V_{DDL} = 3 V	–	–	–100	mA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1302T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

Data amplifier and laser supply circuit for CD player and read only optical systems

TDA1302T

SCHEMATIC DIAGRAM

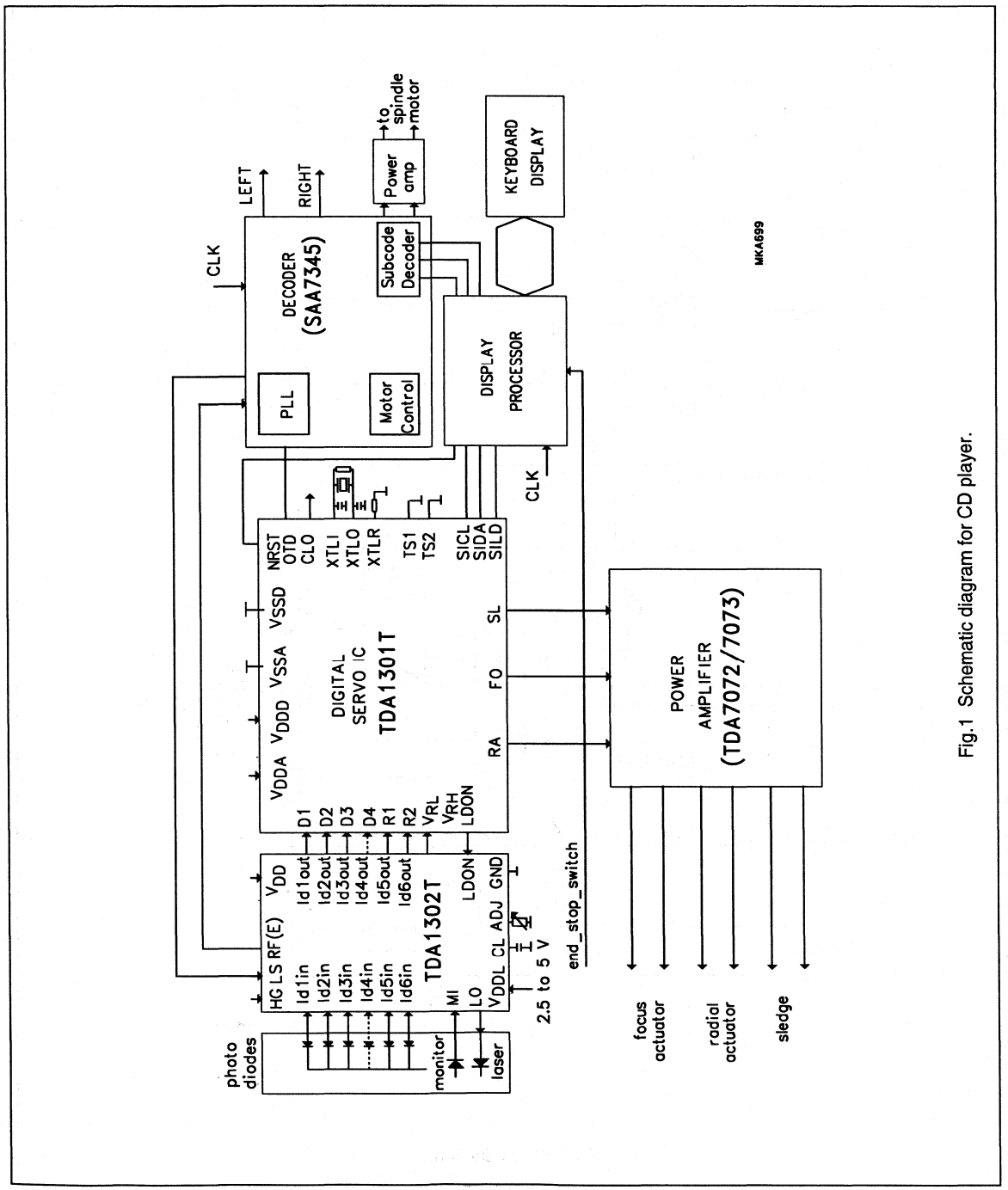


Fig.1 Schematic diagram for CD player.

BLOCK DIAGRAM

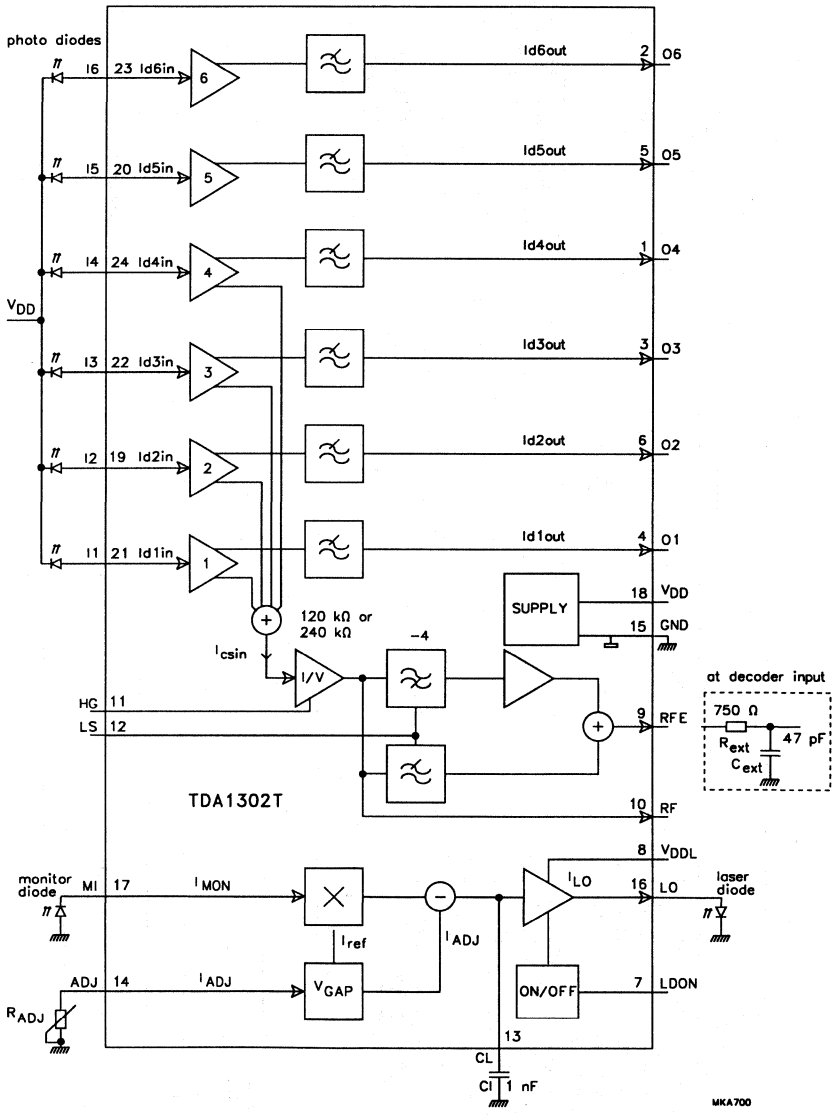


Fig.2 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
O4	1	output of diode current amplifier 4
O6	2	output of diode current amplifier 6
O3	3	output of diode current amplifier 3
O1	4	output of diode current amplifier 1
O5	5	output of diode current amplifier 5
O2	6	output of diode current amplifier 2
LDON	7	control pin for switching the laser ON and OFF
V_{DDL}	8	laser supply voltage
RFE	9	equalized output voltage of sum signal of amplifiers 1 to 4
RF	10	unequalized output
HG	11	control pin for gain switch
LS	12	control pin for speed switch
CL	13	external capacitor
ADJ	14	reference input normally connected to ground via a resistor
GND	15	0 V supply; substrate connection (ground)
LO	16	current output to the laser diode
MI	17	laser monitor diode input
V_{DD}	18	amplifier supply voltage
I2	19	photo detector input 2 (central)
I5	20	photo detector input 5 (satellite)
I1	21	photo detector input 1 (central)
I3	22	photo detector input 3 (central)
I6	23	photo detector input 6 (satellite)
I4	24	photo detector input 4 (central)

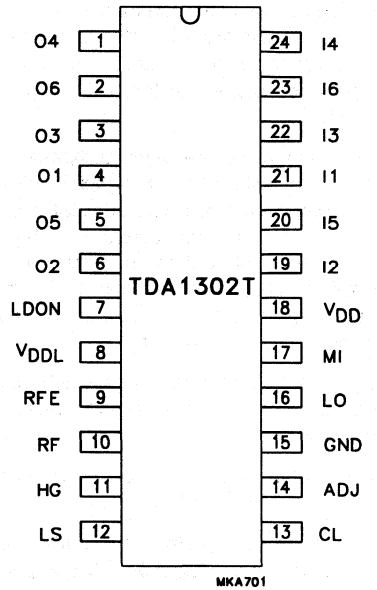


Fig.3 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1302T can be divided into two main sections, the laser control circuit and the photo diode signal filter and amplification section.

Laser control circuit

The main function of the laser control circuit is to control the laser diode current in order to achieve a constant light output power which is based on the current of the monitor diode which is continuously monitored. The circuit is built up into three parts.

The first part is the input stage which compares the monitor diode current with a current which is 10 times the value of the adjustable current. The adjustable current is derived from a bandgap reference source, to be temperature independent, and can be further adjusted by the external resistor R_{ADJ} in order to adapt the circuit to the parameters of the laser/monitor diode unit to be used. The difference is fed to the second part.

The second part is the integrator stage which makes use of an external capacitor CL. This capacitor has two different functions.

During switch-on of the laser current, it provides a current slope of typically: $dI_{LO}/dt \cong 10^{-6}/CL$ (A/s).

After switch-on it ensures that the bandwidth conforms to the typical formula: $f_B \cong K \times A_{ext} \times 90^{-9}/(CL \times I_{MON})$ (Hz).

where A_{ext} represents the AC gain of an extra loop amplifier, if applied, and $K = dI_{monitor}/dI_{laser}$ which is determined by the laser/monitor unit.

I_{MON} is the average current (pin 17) at typical light emission power of the laser diode.

The third part is the power output stage, its input being the integrator output signal. This stage has a separate supply voltage (V_{DDL}) thereby offering the possibility of reduced power consumption by supplying this pin with the minimum voltage necessary.

It also has a laser diode protection circuit which is enabled prior to the output drive transistor becoming saturated due to a large voltage dip on V_{DDL}. Saturation will result in a lower current from the laser diode, which is normally followed immediately by an increment of the voltage from the external capacitor CL, which could cause damage to the laser diode at the end of the voltage dip. The protection circuit prevents an increment of the capacitor voltage and thus offers full protection to the laser diode under these circumstances.

Photo diode signal filter and amplification section

This section has 6 identical current amplifiers. Amplifiers 1 to 4 are designed to amplify the focus photo diode signals. Each amplifier has two outputs, an LF output and an internal RF output. Amplifiers 5 and 6 are used for the radial photo diode currents and have only an LF output. All 6 output signals are low-pass filtered with a corner frequency at 65 kHz. The internal RF output signals are summed together and converted into a voltage by means of a selectable transresistance of 120 kΩ or 240 kΩ. This signal is available directly at pin 10, however, there is also an unfiltered signal available at pin 9. The equalization filter used has 2 different filter curves, one for single-speed mode and one for double-speed mode.

Table 1 Operational modes.

SWITCH	PIN	IF NOT CONNECTED DEFAULT	MODE(1)					
			GAIN		SPEED		LASER	
			HIGH	LOW	SINGLE	DOUBLE	ON	OFF
Control pin	HG	1	1	0	X	X	X	X
	LS	1	X	X	1	0	X	X
	LDON	1	X	X	X	X	1	0

Note

1. Where X = don't care.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–	8.0	V
P_{tot}	total power dissipation	–	300	mW
T_{stg}	storage temperature	–65	+150	°C
T_{amb}	operating ambient temperature	–40	+85	°C

HANDLING

Classification A: human body model; C = 100 pF; R = 1500 Ω; V = ± 2000 V.
Charge device model: C = 200 pF; L = 2.5 μH; R = 0 Ω; V = 250 V.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	60 K/W

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611 part E"*. The numbers of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9398 510 63011.

CHARACTERISTICS

V_{DD} = 3.4 V; V_{DDL} = 2.5 V; T_{amb} = 25 °C; R_{ADJ} = 48 kΩ; HG = logic 1; LS = logic 1; with an external LP filter (R_{ext} = 750 Ω, C_{ext} = 47 pF) at pin 9; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{DD}	amplifier supply current	laser OFF	–	8	–	mA
V_{DD}	amplifier supply voltage		3.4	–	5.5	V
V_{DDL}	laser control supply voltage		2.5	–	5.5	V
P_{diss}	power dissipation	laser OFF; V_{DD} = 3.4 V	–	27	–	mW
Diode current amplifiers (1 to 6)						
$I_{i(d)}$	diode input current	note 1	–	–	10	μA
N_{eq}	equivalent noise input		–	1	–	pA/√Hz
$V_{i(d)}$	diode input voltage	$I_{i(d)}$ = 1.67 μA	–	0.9	–	V
$V_{o(d)}$	diode output voltage		–0.2	–	V_{DD} – 1	V
G_{dn}	amplification	$I_{i(d)}$ = 1.67 μA; $V_{o(dn)}$ = 0 V; note 2	1.43	1.55	1.67	dB
$I_{os(d)}$	diode output offset current	I_{csin} = I_{tsin} = 0; note 3	–	–	100	nA
$Z_{o(d)}$	output impedance	I_{di} = 1.67 μA; $V_{o(dn)}$ = 0 V	500	–	–	kΩ
B	3 dB bandwidth	$I_{i(d)}$ = 1.67 μA	50	68	–	kHz
G_{mm}	mismatch in amplification	I_{di} = 1.67 μA; $V_{o(dn)}$ = $V_{o(dm)}$	–	–	3	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data amplifier; equalized single and double speed						
V_{RFO}	DC output voltage	$I_{csin} = 0$	–	0.3	–	V
R_{RF}	transresistance	$f_i = 100$ kHz; note 4	100	120	143	kΩ
		$f_i = 100$ kHz; note 5	200	240	285	kΩ
V_{RFMO}	output voltage	note 6	–	–	$V_{DD} - 1.2$	V
SR_{RF}	slew rate	$V_{SR} = 1$ V (p-p)	–	6	–	V/μs
Z_{oRF}	output impedance	$f_i = 1$ MHz	–	100	–	Ω
$t_{d(eq)}$	equalization delay	note 7	–	320	–	ns
$t_{d(f)}$	flatness delay (Φ/ω)	LS = 1 or 0; notes 7 and 8	–	10.5	–	ns
G_R	gain ratio	note 8	4.5	6	–	dB
B_{RF}	unequalized output bandwidth	$I_{i(d)} = 1.67$ μA	3	5	–	MHz
Control pins LDON, LS and HG (with 47 kΩ internal pull-up resistor)						
V_{IL}	LOW level input voltage		–0.2	–	+0.5	V
V_{IH}	HIGH level input voltage		$V_{DD} - 1$	–	$V_{DD} + 0.2$	V
I_{IL}	LOW level input current		–	–	100	μA
Laser output						
$V_{o(l)}$	output voltage	$I_{o(l)} = 100$ mA	–0.2	–	$V_{DD} - 0.7$	V
$I_{o(l)}$	output current		–	–	–100	mA
Monitor diode input						
$V_{i(mon)}$	monitor input voltage	$I_{i(mon)} = -1$ mA	–	$V_{DD} - 0.7$	–	V
$I_{i(mon)}$	monitor input current		–	–	2	mA
Reference source V_{GAP} and laser adjustment current I_{ADJ}						
V_{ref}	reference voltage	$R_{ADJ} = 48$ kΩ	1.15	1.24	1.31	V
ΔT	reference temperature drift	$R_{ADJ} = 48$ kΩ	–	40×10^{-6}	–	
SR_{ref}	reference supply rejection		–	–	1	%
I_{ADJ}	adjustment current	$R_{ADJ} = 5.6$ kΩ	–	–	200	μA
Z_i	input impedance	$R_{ADJ} = 48$ kΩ	–	1	–	kΩ
$d_{Io(l)}/dt$	slew rate output current	$C_L = 1$ nF	–	1	–	mA/μs
M	multiplying factor ($I_{i(mon)}/I_{ADJ}$)		–	10	–	

Notes to the characteristics

1. The maximum input current is defined as the current in which the gain reaches its minimum. Increasing the supply voltage to $V_{DD} = 5$ V increases the maximum input current (see also Figs 4 and 5).
2. The gain increases if a larger supply voltage is used (see also Fig.6).
3. I_{csin} is the sum of the diode input currents 1 to 4; I_{tsin} is the sum of the diode input currents 5 and 6.
4. Transresistance 120 kΩ means LOW gain, selected if HG = logic 0 (see Table 1).
5. Transresistance 240 kΩ means HIGH gain, selected if HG = logic 1 (see Table 1).
6. Output voltage swing will be: $V_{SRRF} = V_{RFMO} = V_{RFO(p-p)}$.
7. Refers to equalized output only.
8. For single speed the gain ratio is defined as gain difference between 1 MHz and 100 kHz, while the flatness delay is defined up to 1 MHz (see also Fig.7). For double speed the gain ratio is defined as gain difference between 2 MHz and 200 kHz, while the flatness delay is defined up to 2 MHz.

Transfer function

The equalized amplifier including C_{ext} and R_{ext} has the following transfer functions, where 'rfe' refers to equalized output only and 'rf' refers to equalized and not equalized outputs.

FOR SINGLE SPEED (SP = LOGIC 1)

$$\frac{V_{rfe}}{I_{csin}} = R_{rf} \times \frac{\left(1 - ks^2\right)/\omega^2_{os}}{1 + 1/Q \times s/\omega_{os} + s^2/\omega^2_{os}} \times \frac{1}{1 + s/\omega_1} \times \frac{1}{1 + sR_{ext} \times C_{ext}} \quad (1)$$

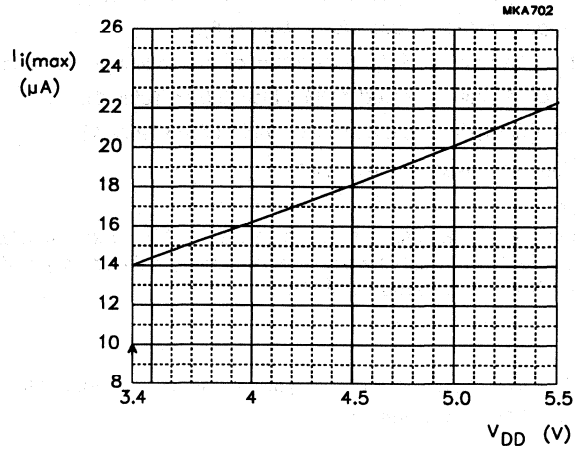
FOR DOUBLE SPEED (SP = LOGIC 0)

$$\frac{V_{rfe}}{I_{csin}} = R_{rf} \times \frac{\left(1 - ks^2\right)/\omega^2_{os}}{1 + 1/Q \times s/\omega_{od} + s^2/\omega^2_{od}} \times \frac{1}{1 + sR_{ext} \times C_{ext}} \quad (2)$$

The denominator forms the denominator of a Bessel low-pass filter.

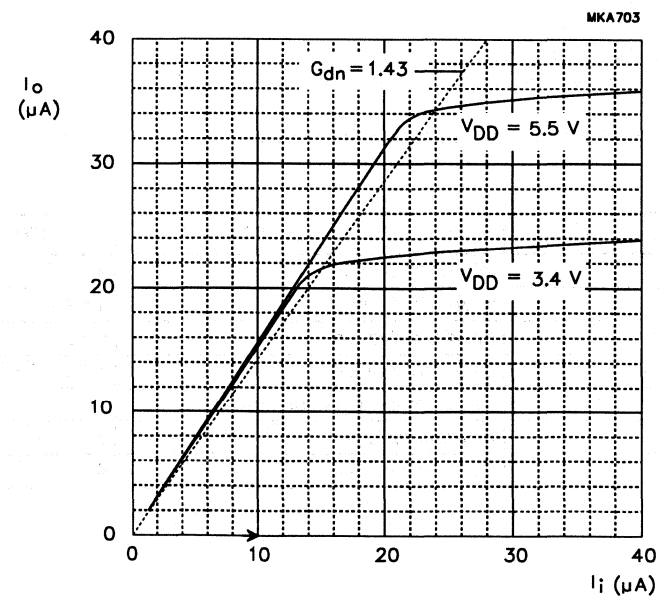
Table 2 Transresistance.

SYMBOL	DESCRIPTION	TYP.	UNIT
k	internally defined	4	
$\omega_{os}/\omega_1 = \omega_{od}/\omega_2$	internally defined	1.094	
Q	internally defined	0.691	
$\omega_{od} = 2 \times \omega_{os}$	internally defined	17.6×10^{-6}	rad/s
R_{RF}	see Chapter "Characteristics"	–	
R_{ext}	external resistor	750	Ω
C_{ext}	external capacitor	47	pF



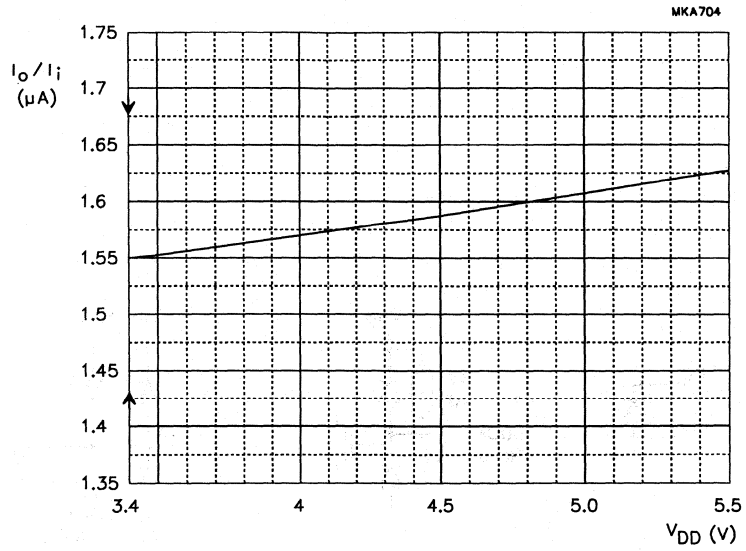
↑ = test limit.

Fig.4 Maximum input current as a function of V_{DD}.



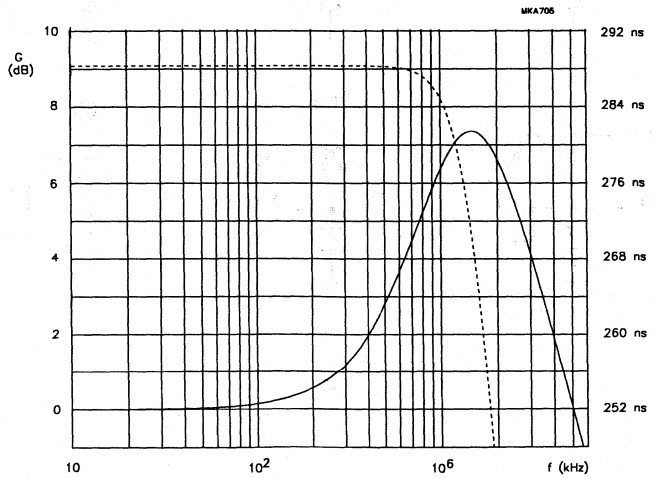
→ = test limit.

Fig.5 Output current as a function of input current.



↓ = test limit.

Fig.6 Gain as a function of V_{DD}.



The dashed line = delay (ns); the solid line = gain (dB).

Fig.7 Transfer for single speed.

INTERNAL PIN CONFIGURATION

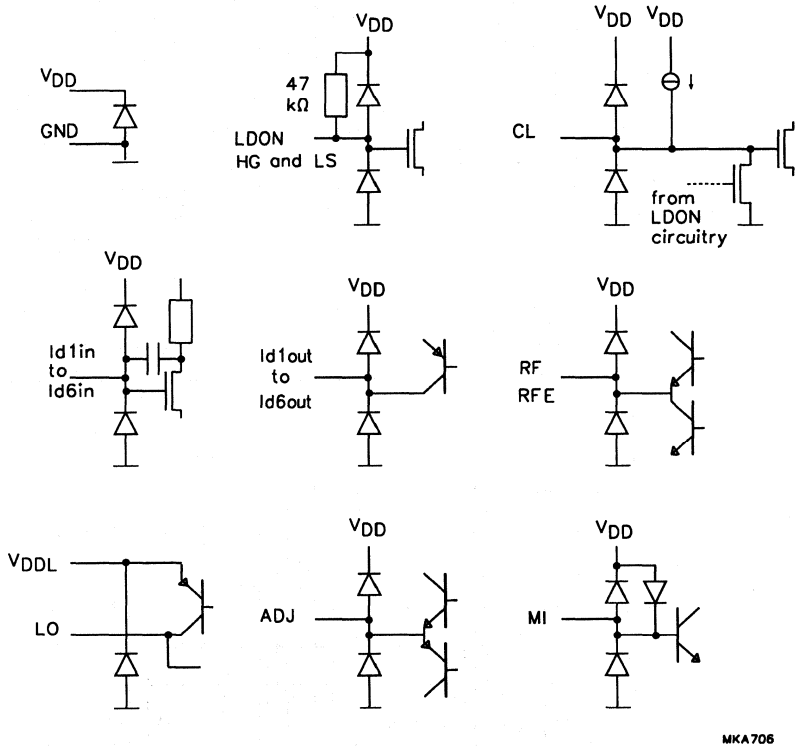


Fig.8 Equivalent internal pin diagrams.

APPLICATION INFORMATION

The TDA 1302T is optimized for Philips CDM12 mechanisms and, subsequently, this application is preferred.

Application with Philips CDM12

The CDM12 mechanism uses an N sub-laser diode together with a P sub-monitor diode and, since TDA1302T is optimized for this type, besides the standard components CL and R_{ADJ}, no other external components are required as illustrated in Fig.9.

As two central spot diodes are summed together inside the pick-up unit, one input pin remains unused as shown in Fig.10. Unused central spot inputs should be connected to ground in order to eliminate noise contribution to the RF and RFE signals.

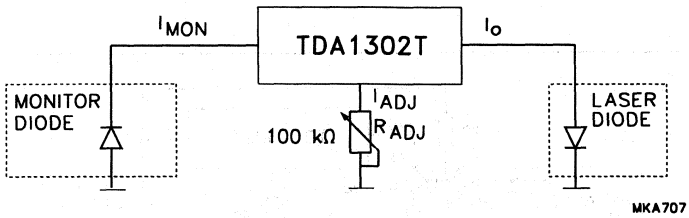


Fig.9 Application of the CDM12 laser/monitor diode unit.

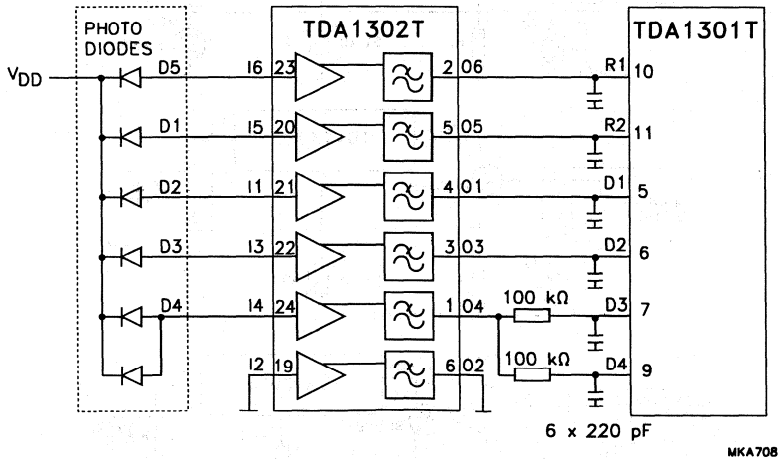


Fig.10 Application of the CDM12 pick-up unit.

Application of other mechanisms

The TDA1302T can accommodate all laser/monitor configurations with an N sub-laser diode. When an N sub-monitor diode is used, external circuitry is required as illustrated in Figs 11(a) to 11(d). Most of these laser/monitor diode units have a variable resistor (R_m) in parallel with the monitor diode which has been pre-adjusted so that the voltage drop across this resistor has a specific value at nominal laser diode output power. The four circuits given each detail specific values for some frequently used pick-up units as given in Table 3. Each circuit has its own advantages. All circuits illustrated make use of the fixed voltage (<200 mV) across the built-in monitor resistor.

Table 3 Pick-up units.

PICK-UP UNIT	MANUFACTURER	APPLICATION
SLD104U	Sony corporation	KSM210 (Sony)
LT022MS	Sharp corporation	KSM210 (Sony)
RLD-78MA	Rohm corporation	KSM210 (Sony)
		HOP-M3TR (Hitachi)
SF91	Sony corporation	CDV90V1 (Sanyo)

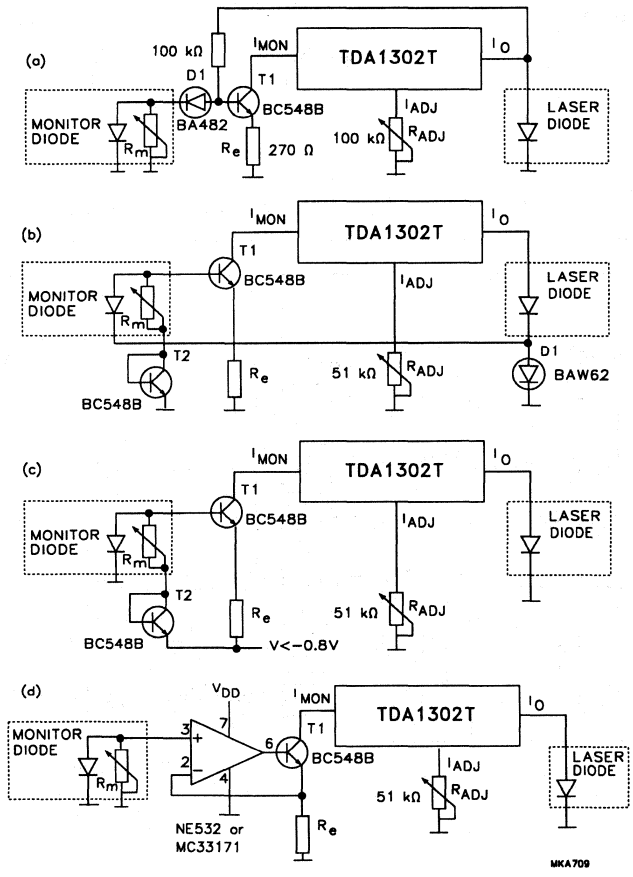


Fig.11 Applications of the laser/monitor units.

PROPERTIES OF CIRCUIT FIG.11(a)

It is important that the V_d(D1) approaches V_{be}(T1) at approximately 150 μA, that is why a small diode has been applied such as the BA482. Additional adjustment may be necessary. this depends on the matching of V_d(D1) and V_{be}(T1) and the permitted tolerance on the laser current. The advised adjustment procedure is as follows:

1. Ensure that R_{ADJ} has the highest impedance at the beginning of the adjustment.
2. Adjust R_{ADJ} until the voltage across R_m has the value as indicated in Table 4.

Table 4 Variable resistor (R_m) voltage adjustment.

PICK-UP UNIT	MANUFACTURER	V_{Rm} (mV)
SLD104U	Sony corporation	150
LT022MS	Sharp corporation	150
RLD-78MA	Rohm corporation	150
SF90	Sanyo corporation	180
SF91	Sanyo corporation	180

Table 5 Further circuit properties of Fig.11.

FIGURE	PROPERTIES
(a)	single supply voltage
	only a few components are required; 2R, 1T and 1D
	supply voltage independent
(b)	single supply voltage
	only a few components are required; 1R, 2T and 1D
	supply voltage independent
	no extra adjustment necessary if T1 and T2 match
(c)	only a few components are required; 1R and 2T
	supply voltage independent
	no extra adjustment necessary
	better power efficiency than (b)
(d)	single supply voltage
	supply voltage independent
	no extra adjustment necessary
	no matching components required

In Figs 11(b) to 11(d) solutions have been given requiring no adjustment. R_{ADJ} and R_e can be calculated as follows: $R_{ADJ} = 12.4R_e/V_{Rm}$ at $P_{o(nom)}$.

Examples of advised values applicable to Fig.11(b), (c) and (d) are given in Table 6.

Table 6 Advised circuit values.

PICK-UP UNIT	MANUFACTURER	R_e (Ω)	R_{ADJ} (kΩ)
SLD104U	Sony corporation	620	51
LT022MS	Sharp corporation	620	51
RLD-78MA	Rohm corporation	620	51
SF90	Sanyo corporation	750	51
SF91[1]	Sanyo corporation	750	51

Note

1. Notwithstanding that the SF91 specification details an astigmatic detection system, TDA1301T requires a single Foucault parameter setting.

Figures 12 and 13 give the application diagrams of the pick-up unit of the mechanisms as previously indicated.

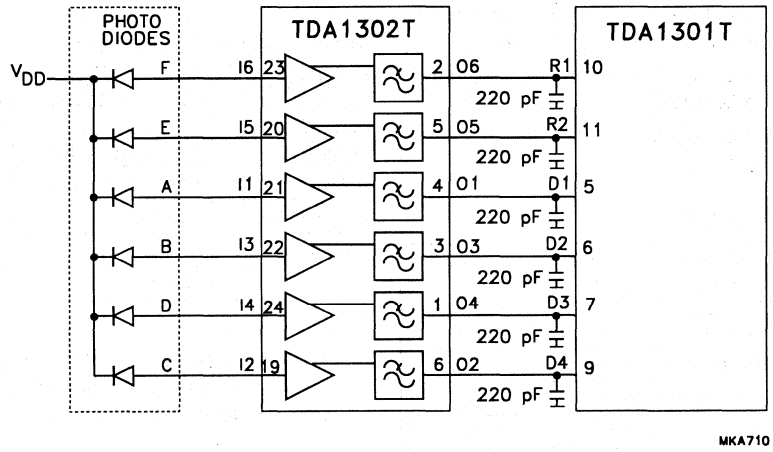


Fig.12 Application of pick-up units SLD104U, LT022MS and RLD-78MA.

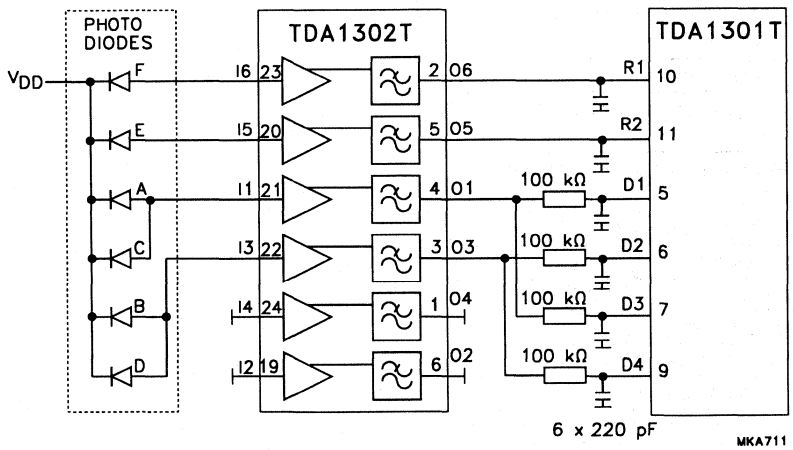


Fig.13 Application of pick-up unit SF91.

Circuit recommendations

PRINTED-CIRCUIT BOARD LAY-OUT ITEMS

It is advised to keep the output wires of the diode current amplifiers separated from the input as much as possible to prevent oscillations.

EXTERNAL MONITOR DIODE CIRCUITRY

TDA1302T protects the laser diode against damage due to supply voltage transients. When any external circuitry is used in the 'laser diode-monitor diode' chain, the safety of the laser diode completely relies on the quality of this external circuitry. Therefore, it should be noted that:

1. If such a circuit requires a supply voltage, make sure that this voltage is present at least at the same moment as V_{DDL} or earlier.
2. It is advised not to implement integrating actions in this external circuitry as this may conflict with the internal integrator, especially during possible supply voltage drops.

MEASUREMENT OF THE LASER DIODE CURRENT

It is advised not to connect any current meter directly in series with the laser diode. A safe method is the inclusion of a 1 Ω resistor, connected in series with the laser diode, and measuring the voltage across this resistor.

Digital servo driver (DSD1) TDA1303T

FEATURES

- Optimized for:
  - low voltage
  - low power
- Suppression of idle switching
- Optimized for generally used CD mechanisms
- Total output resistance less than 4 Ω
- Continuous adjustment of the gain for fluctuating battery voltage
- Battery voltage indication
- Switched-mode power supply for DC/DC down-conversion for laser supply voltage
- Single supply voltage rail
- Full digital signal processing.

GENERAL DESCRIPTION

The Digital Servo Driver (DSD1) provides 3 identical output driver functions for the motor/actuator for focus, radial and sledge control, a Switched-Mode Power Supply (SMPS) for the laser diode and a battery voltage indicator output, applied in a wide range of mechanisms for CD and read only optical systems.

The DSD1 contains 3 class D amplifiers for processing pulse duration modulation (PDM) signals for focus, radial and sledge control of a servo mechanism.

The gain of the class D amplifiers is continuously adapted for fluctuating battery voltage, resulting in a battery voltage independent output signal. The gain factor is determined using an analog-to-digital converter (ADC) which continuously measures the battery voltage.

As a result, the digital code can be read by the display processor by means of the 3-wire interface bus, which is compatible to TDA1301 and SAA7345. The laser supply voltage is produced by a switched-mode power supply in order to minimize the power loss in the DC/DC down-conversion.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD1}	digital stabilized supply voltage		3.4	5.0	5.5	V
V_{DDD2}	digital unstabilized supply voltage		3.0	5.0	6.5	V
V_{DDA}	analog supply voltage		3.4	5.0	5.5	V
I_{DDD1}	digital stabilized supply current		–	1	2	mA
I_{DDD2}	digital unstabilized supply current		–	0.75	1	mA
I_{DDA}	analog stabilized supply current		–	1	2	mA
I_o	output current per stage		–	–	300	mA
R_o	output resistance	V_{DDD2} = 3 V; T_{amb} = –40 to +85 °C	1	–	4	Ω
V_{ls}	laser switched-mode power supply sense input voltage		2.0	2.5	2.6	V
I_{ls}	laser switched-mode power supply sense input current		–	–	100	mA
f_{clk}	input clock frequency		–	4.2336	5	MHz
P_{tot}	total power dissipation	bridges off; laser off	–	12.5	–	mW
T_{amb}	operating ambient temperature		–40	–	+85	°C

Digital servo driver (DSD1) TDA1303T

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1303T	24	SO24L	plastic	SOT137-1

BLOCK DIAGRAM

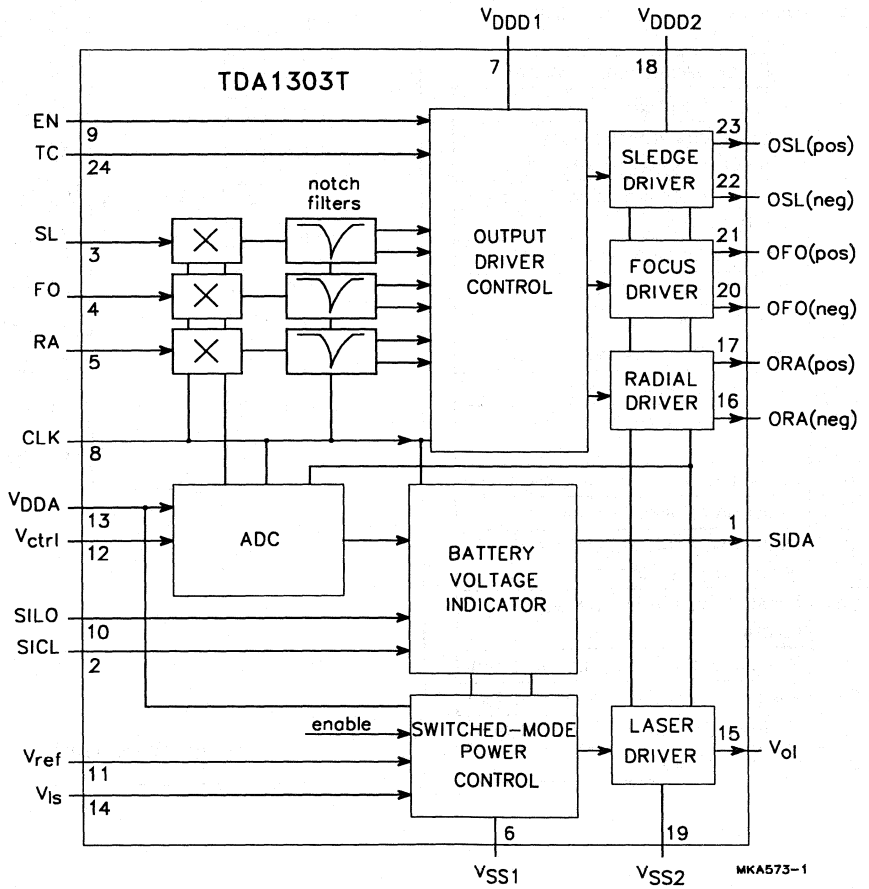


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SIDA	1	battery voltage indicator output
SICL	2	external clock input to synchronize read-out of battery indicator
SL	3	sledge control input signal
FO	4	focus control input signal
RA	5	radial control input signal
V_{SS1}	6	digital and analog ground supply voltage
V_{DDD1}	7	digital stabilized supply voltage
CLK	8	clock input signal
EN	9	enable focus, radial, sledge actuator/motor and SMPS input
SILO	10	serial interface load signal input for battery voltage
V_{ref}	11	reference voltage input for SMPS
V_{ctrl}	12	control voltage input for gain control
V_{DDA}	13	analog supply voltage
V_{ls}	14	laser supply sense input signal
V_{ol}	15	laser supply voltage output
ORA(neg)	16	radial actuator driver negative output
ORA(pos)	17	radial actuator driver positive output
V_{DDD2}	18	digital unstabilized supply voltage
V_{SS2}	19	digital and analog unstabilized ground supply voltage
OFO(neg)	20	focus actuator driver negative output
OFO(pos)	21	focus actuator driver positive output
OSL(neg)	22	sledge motor driver negative output
OSL(pos)	23	sledge motor driver positive output
TC	24	test control input

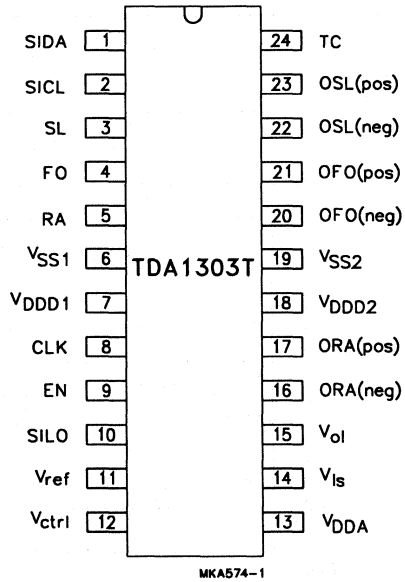


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Focus, radial and sledge amplifiers

The input signals FO, RA and SL are PDM signals with a sampling frequency $f_s = \frac{1}{4}f_{clk}$. These signals control the motor/actuator current by means of a class D amplifier (bridge). A notch filter is used to filter $\frac{1}{2}f_s$ to prevent idle switching.

There is also a circuit to perform 'break-before-make' switching of the large output transistors.
The maximum R_{on} (on-resistance) of the class D PMOS + NMOS transistor-pair is less than 4 Ω.

ADC for gain control

An ADC, as illustrated in Fig.3, measures the unstabilized supply voltage (V_{DDD2}). With V_{ctrl} the gain control range minimum starting value for V_{DDD2} is set, while the ratio of the $V_{DDD2(min)}$ and $V_{DDD2(max)}$ is determined by the ratio of R1 and R2. The resistors R1 and R2 are integrated and chosen so that $V_{DDD2(min)} = V_{ctrl} = 3.0$ V and $V_{DDD2(max)} = 6.5$ V. The ADC code can thus be determined:

$$ADCODE = 128 \times (V_{DDD2} - V_{ctrl}) \times \frac{R1 + R2}{R1 \times V_{ctrl}}$$

With a decoder the ADCODE is converted to a gain factor, so that the 3-input PDM codes are multiplied by a factor $\frac{V_{ctrl}}{V_{DDD2}}$; where:

$V_{DDD2(min)} = V_{ctrl}$

$V_{DDD2(max)} = k \times V_{ctrl}$

where:

$$k = \frac{3 \times R1 + R2}{R1 + R2}$$

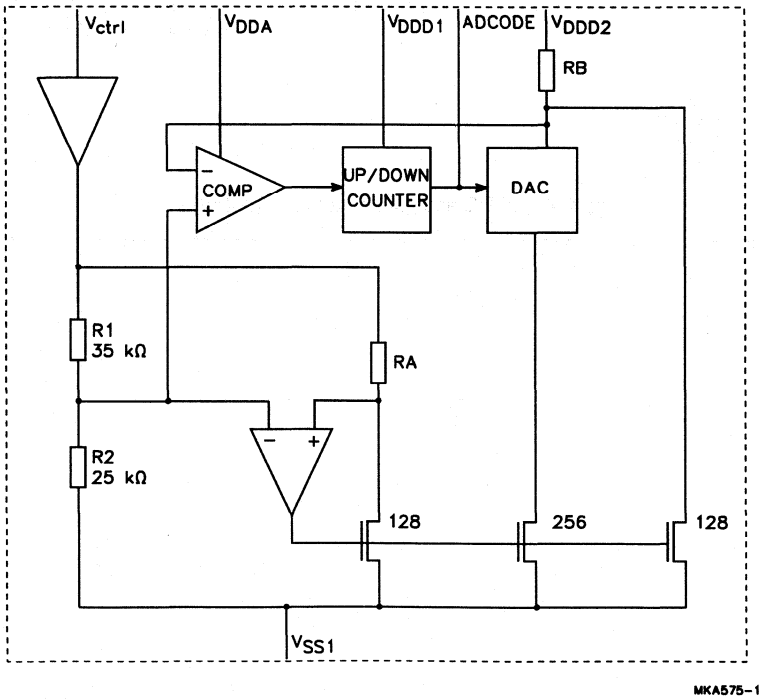
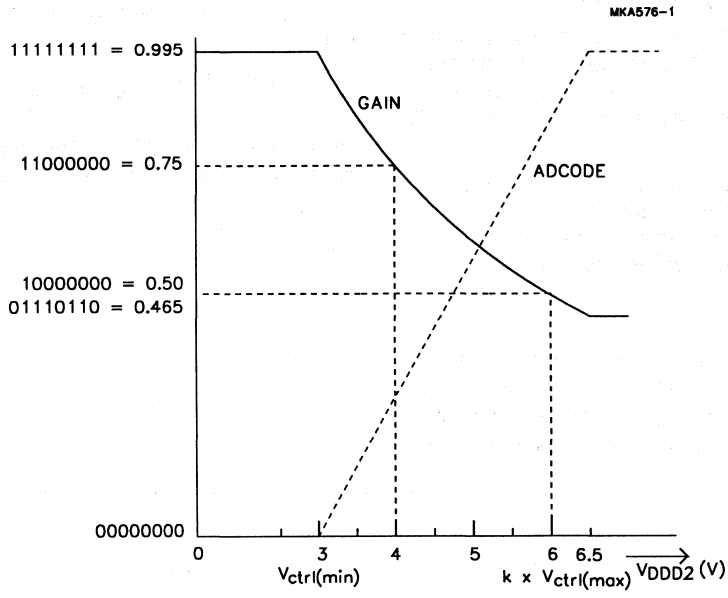


Fig.3 ADC with offset.



$$ADCODE = 1.7 \times 128 \times \frac{(V_{DDD2} - V_{ctrl})}{V_{ctrl}}$$

Fig.4 ADCODE and gain as a function of V_{DDD2}.

Battery voltage indicator

The battery voltage indicator is controlled by a handshake protocol, as illustrated in Fig.5. SIDA is a 3-state output.

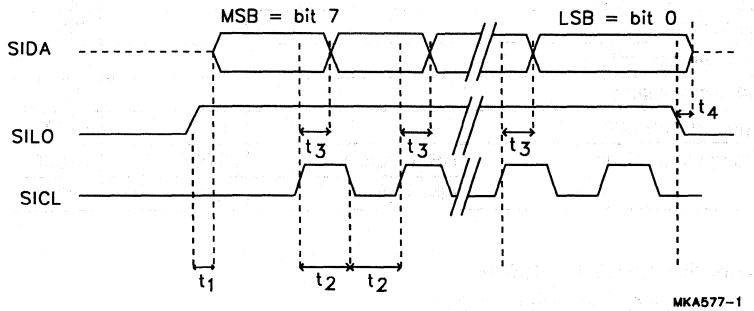


Fig.5 Handshake protocol for battery voltage indicator.

Laser switched-mode power supply

The laser switched-mode power supply consists of a comparator that compares the laser supply voltage to a reference voltage and determines the charging rate of the external capacitor.

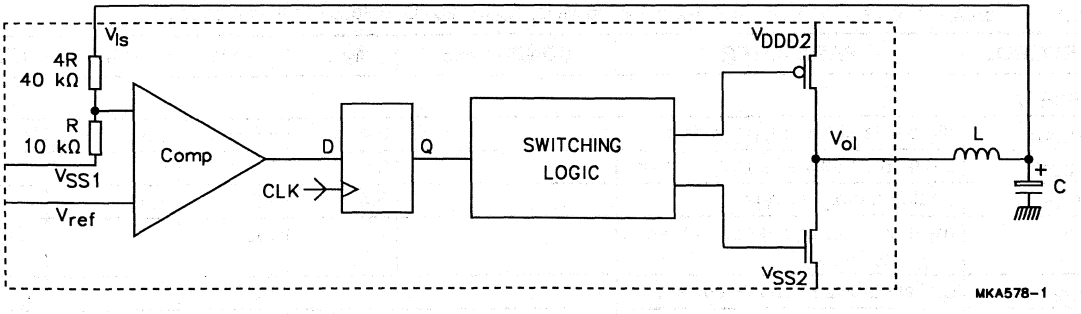


Fig.6 Schematic diagram of laser switched-mode power supply.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD1}	digital stabilized supply voltage		−0.5	+6.0	V
V_{DDD2}	digital unstabilized supply voltage		−0.5	+7.0	V
V_{DDA}	analog supply voltage		−0.5	+6.0	V
I_o	output current per stage		−	350	mA
P_{tot}	total power dissipation		−	840	mW
T_{xtal}	crystal temperature		−	150	°C
T_{stg}	storage temperature		−55	+150	°C
V_{es}	electrostatic handling	HBM; note 1	−2000	+2000	V
		MM; note 2	−200	+200	V

Notes

1. Human Body Model: R = 1.5 kΩ; C = 100 pF.
2. Machine Model: R = 10 Ω; C = 200 pF; L = 0.5 µH.

QUALITY SPECIFICATION

In accordance with *"UZW-BO/FQ-A302"* and *"UZW-BO/FQ-B302"*. The numbers of the quality specifications can be found in the *"Quality Reference Pocketbook"*. The pocketbook can be ordered using the code 9398 510 34011.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	65	K/W

CHARACTERISTICS

$V_{DDD1} = V_{DDD2} = V_{DDA} = 5$ V; $V_{ctrl} = 3$ V; $f_{clk} = 4.2336$ MHz; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD1}	digital stabilized supply voltage		3.4	5.0	5.5	V
V_{DDD2}	digital unstabilized supply voltage		3.0	5.0	6.5	V
V_{DDA}	analog supply voltage		3.4	5.0	5.5	V
ΔV	maximum voltage variation from V_{DDD1} to V_{DDA}		−	100	−	mV
I_{DDD1}	digital stabilized supply current		−	1.5	2	mA
I_{DDD2}	digital unstabilized supply current	no load	−	0.75	1	mA
I_{DDA}	analog supply current		−	1	2	mA
P_{tot}	total power dissipation	bridges off; laser off	10	12.5	22	mW
		loaded; note 1	−	220	−	mW

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital inputs; pins TC, EN, SL, FO, RA, CLK, SILO and SICL						
V_{IL}	LOW level input voltage	T_{amb} = −40 to +85 °C	–	–	$0.3V_{DDD1}$	V
V_{IH}	HIGH level input voltage	T_{amb} = −40 to +85 °C	$0.7V_{DDD1}$	–	–	V
I_{IL}	LOW level input current	T_{amb} = −40 to +85 °C	–	–	−1	µA
I_{IH}	HIGH level input current	T_{amb} = −40 to +85 °C	–	–	1	µA
Digital output; pin SIDA						
V_{OL}	LOW level output voltage	T_{amb} = −40 to +85 °C	–	–	0.5	V
V_{OH}	HIGH level output voltage	T_{amb} = −40 to +85 °C	4.5	–	–	V
I_{OL}	LOW level output current	T_{amb} = −40 to +85 °C; V_{OL} = 0.5 V	–	–	−2	mA
I_{OH}	HIGH level output current	T_{amb} = −40 to +85 °C; V_{OH} = 4.5 V	–	–	2	mA
Clock input; pin CLK						
f_{clk}	clock frequency		0.1	4.2336	5	MHz
Analog outputs; pins OSL(pos), OSL(neg), OFO(pos), OFO(neg), ORA(pos) and ORA(neg)						
R_o	output resistance	V_{DDD2} = 3 V; note 2	1	–	4	Ω
I_o	output current	V_{DDD2} = 3 V; note 2	–	–	300	mA
ΔG	total gain variation	V_{DDD2} = 3 to 6.5 V	–	4	–	%
ADC for gain control						
G_v	voltage gain		$\frac{0.9V_{ctrl}}{V_{DDD2}}$	$\frac{V_{ctrl}}{V_{DDD2}}$	$\frac{1.1V_{ctrl}}{V_{DDD2}}$	
ΔV/Δt	slew rate	f_{clk} = 4 MHz	12.3	13.7	15.1	mV/µs
S/N	signal-to-noise ratio	B = 0 to 1 kHz	40	48	–	dB
V_{ctrl}	control voltage		2.7	3.0	V_{DDA} − 0.3	V
Battery voltage indicator; handshake protocol with display processor; see Fig.5; note 3						
t_1	SILO bounce		0	–	700	ns
t_2	SICL pulse width		1420	–	–	ns
t_3	delay of SICL LOW-to-HIGH transition to SIDA		0	–	1420	ns
t_4	SILO HIGH-to-LOW transition to SIDA; 3-state	10 kΩ pull-up resistor	0	52	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Laser switched-mode power supply						
SVRR	unstabilized supply voltage rejection ratio	note 4	–	40	–	dB
V_{ol}	output voltage	note 5	$4.5V_{ref}$	$5.0V_{ref}$	$5.5V_{ref}$	V
$V_{ol(max)}$	maximum output voltage	I_L = 100 mA	–	–	$V_{DDD2} - 0.4$	V
I_{ol}	output current		–	–	100	mA
ΔV_{ls}	sensitivity of V_{ls} with respect to V_{ref}		–	–	10	mV
R_o	output resistance		1	–	4	Ω
V_{ref}	reference voltage		–	0.5	–	V
Z_i	input impedance		40	50	60	kΩ
f_{ripple}	SMPS ripple frequency	f_{clk} = 4.2336 MHz; I_L = 50 mA	–	–	0.5	MHz

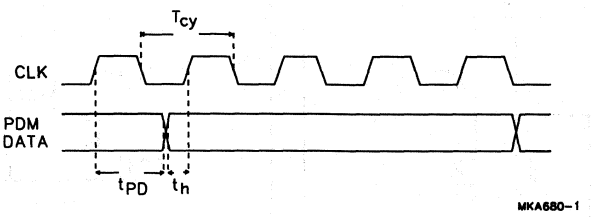
Notes

1. Total power dissipation at average load conditions: $R_{LFO} = R_{LRA}$ = 15.3 Ω, R_{LSL} = 10 Ω, I_{FO} = 126 mA, I_{RA} = 20 mA, I_{SL} = 150 mA and I_L = 100 mA; produces P_{tot} = 195 mW (+15 mW unloaded).
2. As can be seen in the equivalent circuit (Fig.8) the output resistances depend on each other (crosstalk); the contributions of the output resistance are determined by interconnect resistances (R_d, R_s and R_W), PMOS-resistances (R_p) and NMOS-resistances (R_n). R_p and R_n are both temperature and V_{DDD2} dependent. Global values are:

   $R_{VDDD2c} = R_{VSS2c} = R_W$ = 0.1 Ω.

   $R_d = R_s$ = 0.15 Ω.

   $R_p = R_n$ = 0.75 Ω.
3. Output code (8-bit binary coded); $ADCODE = 1.7 \times 128 \times \frac{(V_{DDD2} - V_{ctrl})}{V_{ctrl}}$
4. Rejection of V_{DDD2}: $V_{DDD2(ripple)}$ = 0.1 V; f = 1 kHz and I_L = 50 mA.
5. Ripple of laser output voltage (pin 15) is dependent on external components.



T_{cy} > 200 ns; t_{PD} = > 10 ns; t_h > 70 ns.

Fig.7 Format of driver PDM input signals.

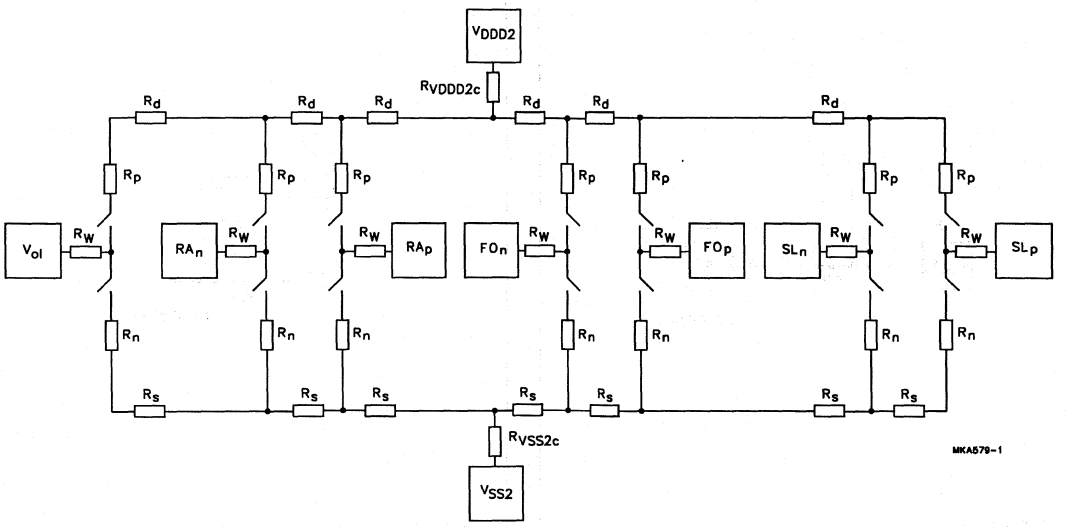
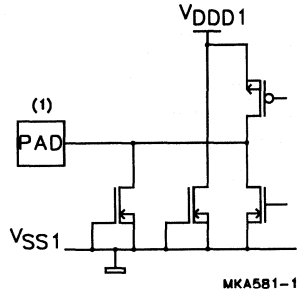


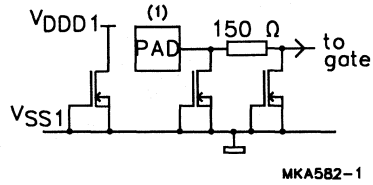
Fig.8 Equivalent circuit for output stages.

EQUIVALENT INTERNAL PIN CONNECTION DIAGRAMS



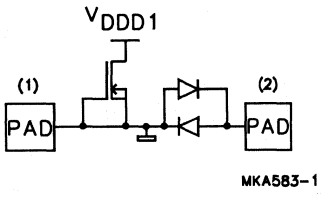
(1) Pin 1 = SIDA.

Fig.9 Pin 1.



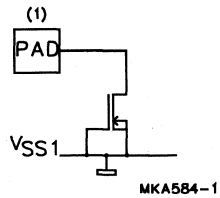
(1) Pin 2 = SICL; pin 3 = SL; pin 4 = FO; pin 5 = RA; pin 8 = CLK; pin 9 = EN; pin 10 = SILO; pin 24 = TC.

Fig.10 Pins 2 to 5, 8 to 10 and 24.



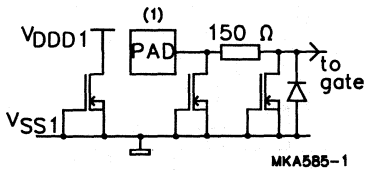
(1) Pin 6 = V_{SS1}.
(2) Pin 19 = V_{SS2}.

Fig.11 Pins 6 and 19.



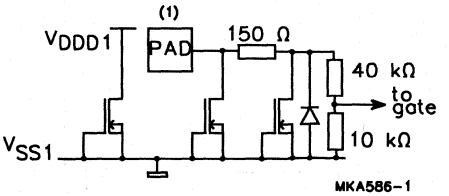
(1) Pin 7 = V_{DDD1}; pin 13 = V_{DDA}; pin 18 = V_{DDD2}.

Fig.12 Pins 7, 13 and 18.



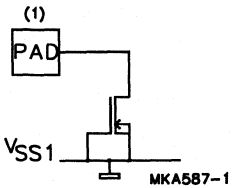
(1) Pin 11 = V_{ref}; pin 12 = V_{ctrl}.

Fig.13 Pins 11 and 12.



(1) Pin 14 = V_{ls}.

Fig.14 Pin 14.



(1) Pin 15 = V_{ol}; pin 16 = ORA(neg); pin 17 = ORA(pos); pin 20 = OFO(neg); pin 21 = OFO(pos); pin 22 = OSL(neg); pin 23 = OSL(pos).

Fig.15 Pins 15 to 17 and 20 to 23.

APPLICATION INFORMATION

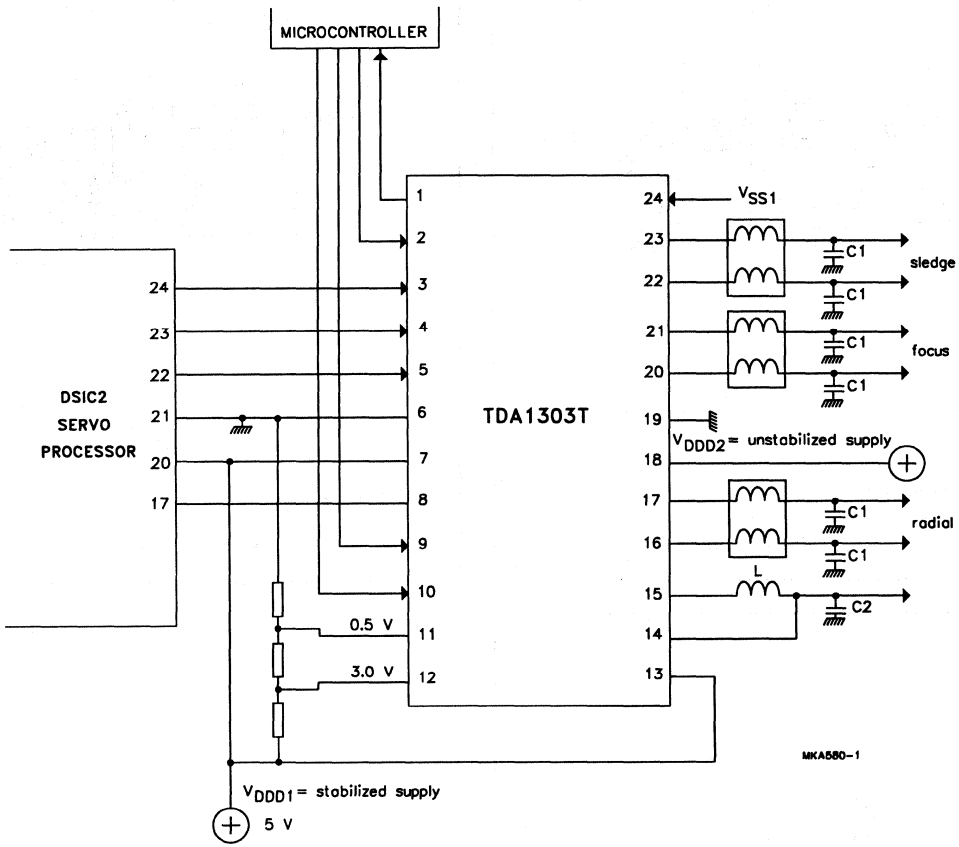


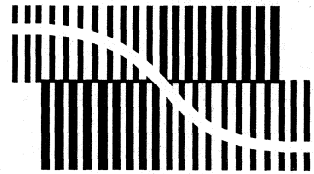
Fig.16 Application circuit for DSD1.

Stereo 1f_s data input up-sampling filter with bitstream continuous calibration dual DAC (BCC-DAC2)

TDA1305T

FEATURES

- Easy application
- 16f_s Finite-duration Impulse-Response (FIR) filter incorporated
- Selectable system clock (f_{sys}) 256f_s or 384f_s
- I²S-bus serial input format (at f_{sys} = 256f_s) or LSB fixed 16, 18 or 20 bits serial input mode (at f_{sys} = 384f_s)
- Slave-mode clock system
- Cascaded 4-stage digital filter incorporating 2-stage FIR filter, linear interpolator and sample-and-hold
- Smoothed transitions before and after muting (soft mute)
- Digital de-emphasis filter for three sampling rates of 32 kHz, 44.1 kHz and 48 kHz
- 12 dB attenuation via the attenuation input control
- Double speed mode
- 2nd order noise shaper
- 96 (f_{sys} = 384f_s) or 128 (f_{sys} = 256f_s) times oversampling in normal speed mode
- 48 (f_{sys} = 384f_s) or 64 (f_{sys} = 256f_s) times oversampling in double speed mode
- Bitstream continuous calibration concept
- Small outline SO28 package
- Voltage output 1.5 V (RMS) at line drive level
- Low total harmonic distortion
- No zero crossing distortion
- Inherently monotonic
- No analog post filtering required
- Superior signal-to-noise ratio
- Wide dynamic range (18-bit)
- Single rail supply (3.4 to 5.5 V).



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The TDA1305T is a new generation of filter-DAC which features a unique combination of bitstream and continuous calibration techniques. The converter functions as a bitstream converter for low signals while large signals are generated using the dynamic continuous calibration technique, thus resulting in low power consumption, small chip size and easy application.

The TDA1305T is a dual CMOS DAC with up-sampling filter and noise shaper. The combination of high oversampling up to 16f_s, 2nd order noise shaping and continuous calibration conversion ensures that only simple 1st order analog post filtering is required.

The TDA1305T supports the I²S-bus data input mode with word lengths of up to 20 bits (at f_{sys} = 256f_s) and the LSB fixed serial data input format with word lengths of 16, 18 and 20 bits (at f_{sys} = 384f_s). Four cascaded FIR filters increase the oversampling rate to 16 times. A sample-and-hold function increases the oversampling rate to 96 times (f_{sys} = 384f_s) or 128 times (f_{sys} = 256f_s). A 2nd order noise shaper converts this oversampled data to a bitstream for the 5-bit DACs.

The DACs are of the continuous calibration type and incorporate a special date coding. This ensures an extremely high signal-to-noise ratio, superior dynamic range and immunity to process variation and component ageing.

Two on-board operational amplifiers convert the digital-to-analog current to an output voltage. Externally connected capacitors perform the required 1st order filtering so that no further post filtering is required.

The unique combination of bitstream and continuous calibration techniques, together with a high degree of analog and digital integration, results in a single filter-DAC with 18-bit dynamic range, high linearity and simple low cost application.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1305T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

Stereo 1f_s data input up-sampling filter with bitstream continuous calibration dual DAC (BCC-DAC2)

TDA1305T

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	3.4	5.0	5.5	V
V_{DDA}	analog supply voltage	note 1	3.4	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage	note 1	3.4	5.0	5.5	V
I_{DDD}	digital supply current	V_{DDD} = 5 V; at code 00000H	–	30	–	mA
I_{DDA}	analog supply current	V_{DDA} = 5 V; at code 00000H	–	5.5	8	mA
I_{DDO}	operating amplifier supply current	V_{DDO} = 5 V; at code 00000H	–	6.5	9	mA
$V_{FS(rms)}$	full-scale output voltage (RMS value)	$V_{DDD} = V_{DDA} = V_{DDO}$ = 5 V	1.425	1.5	1.575	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level	–	–90	–81	dB
			–	0.003	0.009	%
		at –60 dB signal level	–	–44	–40	dB
			–	0.63	0.1	%
		at –60 dB signal level; A-weighted	–	–46	–	dB
			–	0.5	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighting; at code 00000H	100	108	–	dB
BR_{ns}	input bit rate at data input	f_s = 48 kHz; normal speed	–	–	3.072	Mbits
BR_{ds}	input bit rate at data input	f_s = 48 kHz; double speed	–	–	6.144	Mbits
f_{sys}	system clock frequency		6.4	–	18.432	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (VOL and VOR)		–	$\pm 100 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–30	–	+85	°C

Note

1. All V_{DD} and V_{SS} pins must be connected to the same supply.

Stereo $1f_s$ data input up-sampling filter with bitstream continuous calibration dual DAC (BCC-DAC2)

TDA1305T

BLOCK DIAGRAM

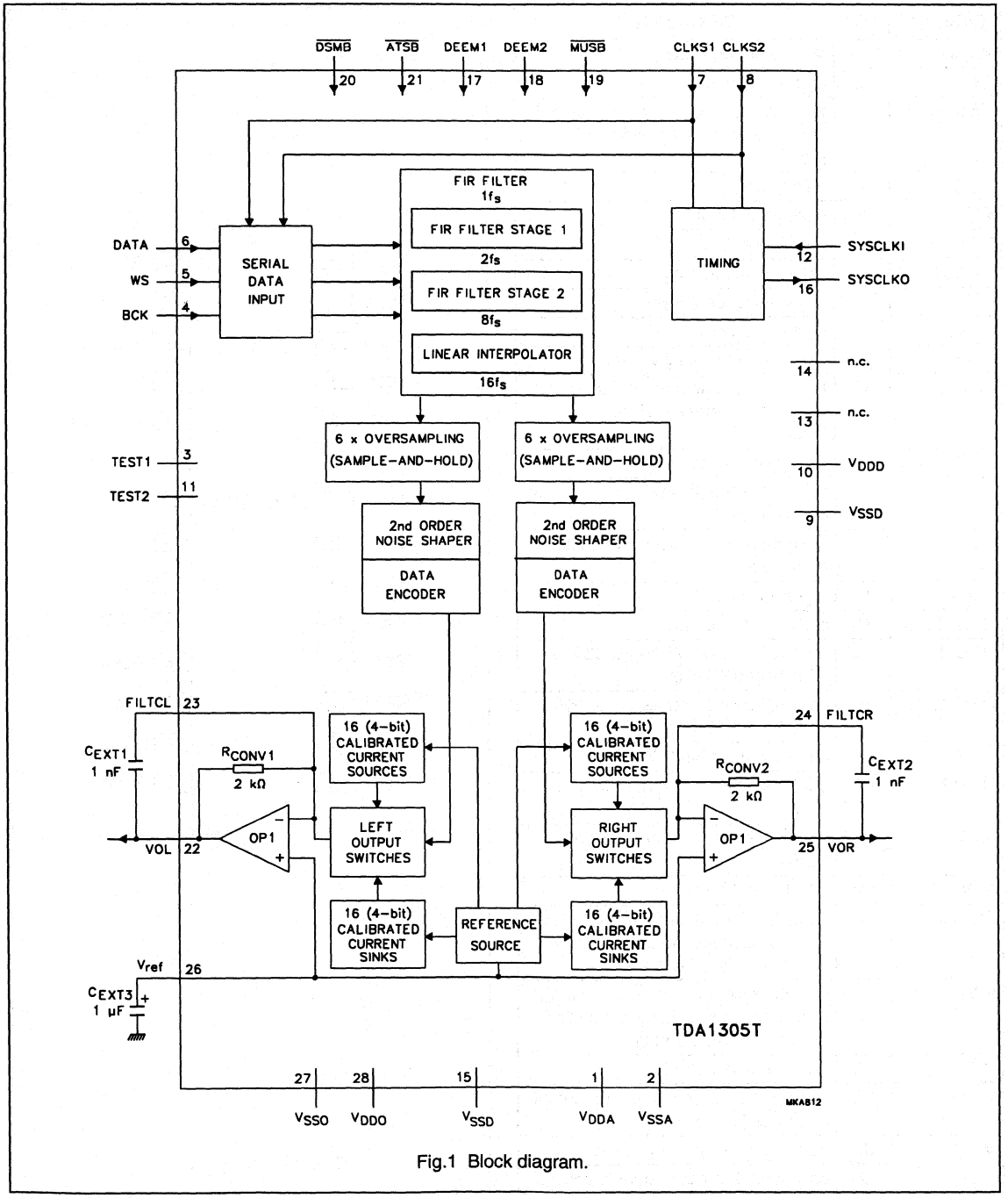


Fig.1 Block diagram.

Stereo 1f_s data input up-sampling filter with bitstream continuous calibration dual DAC (BCC-DAC2)

TDA1305T

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DDA}	1	analog supply voltage
V_{SSA}	2	analog ground
TEST1	3	test input; pin should be connected to ground (internal pull-down resistor)
BCK	4	bit clock input
WS	5	word select input
DATA	6	data input
CLKS1	7	clock selection 1 input
CLKS2	8	clock selection 2 input
V_{SSD}	9	digital ground
V_{DDD}	10	digital supply voltage
TEST2	11	test input; pin should be connected to ground (internal pull-down resistor)
SYSCLKI	12	system clock input
n.c.	13	not connected (this pin should be left open-circuit)
n.c.	14	not connected (this pin should be left open-circuit)
V_{SSD}	15	digital ground
SYSCLKO	16	system clock output
DEEM1	17	de-emphasis on/off; f_{DEEM} 32 kHz, 44 kHz and 48 kHz
DEEM2	18	de-emphasis on/off; f_{DEEM} 32 kHz, 44 kHz and 48 kHz
$\overline{MUSB}$	19	mute input (active LOW)
$\overline{DSMB}$	20	double-speed mode input (active LOW)
$\overline{ATSB}$	21	12 dB attenuation input (active LOW)
VOL	22	left channel output
FILTCL	23	capacitor for left channel 1st order filter function should be connected between pins 22 and 23
FILTCR	24	capacitor for right channel 1st order filter function should be connected between pins 25 and 24
VOR	25	right channel output
V_{ref}	26	internal reference voltage for output channels ($0.5V_{DD}$)
V_{SSO}	27	operational amplifier ground
V_{DDO}	28	operational amplifier supply voltage

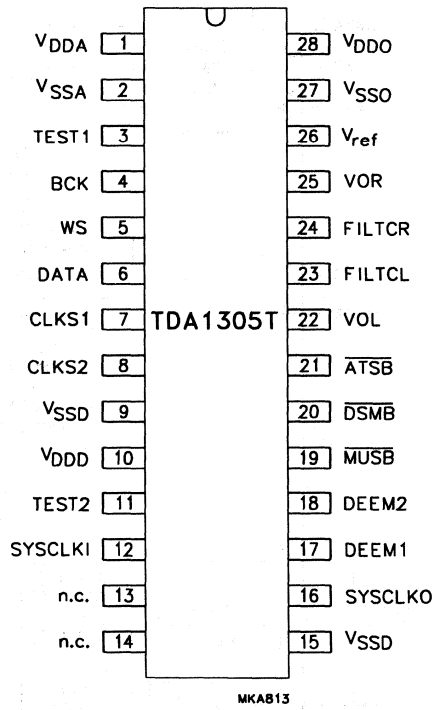


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1305T CMOS digital-to-analog bitstream converter incorporates an up-sampling filter and noise shaper which increase the oversampling rate of $1f_s$ input data to $96f_s$ ($f_{sys} = 192f_s$) or $128f_s$ ($f_{sys} = 256f_s$) in the normal speed mode. In the double speed mode the oversample rate of $1f_s$ input data is increased to $48f_s$ ($f_{sys} = 384f_s$) or $64f_s$ ($f_{sys} = 256f_s$). This oversampling, together with the 5-bit DAC, enables the filtering required for waveform smoothing and out-of-band noise reduction to be achieved by simple 1st order analog post filtering.

System clock and data input format

The TDA1305T accommodates slave mode only, this means that in all applications the system devices must provide a system clock of 256 or $384f_s$ (f_s = 32, 44.1 or 48 kHz). The system frequency is selectable by means of pin CLKS1 and pin CLKS2. The SYSCLKO output (pin 16) provides the system clock for external use.

The TDA1305T supports the following data input modes:

- I^2S-bus with data word lengths of up to 20 bits (at $f_{sys} = 256f_s$).
- LSB fixed serial format with data word lengths of 16, 18 and 20 bits (at $f_{sys} = 384f_s$). As this format idles on the MSB it is necessary to know how many bits are being transmitted.

The input format is shown in Fig.3. Left and right data-channel words are time-multiplexed.

Table 1 Data input format and system clock.

TEST1	CLKS1	CLKS2	DATA INPUT FORMAT	SYSTEM CLOCK	DATA CLOCK(1)	SYSCLKO
0	0	0	I^2S up to 20 bits	$256f_s$	>20	$256f_s$
0	0	1	LSB fixed 16 bits	$384f_s$	24	$384f_s$
0	1	0	LSB fixed 18 bits	$384f_s$	24	$384f_s$
0	1	1	LSB fixed 20 bits	$384f_s$	24	$384f_s$
1	0	0	reserved	–	–	–
1	0	1	LSB fixed 16 bits	$384f_s$	32	$384f_s$
1	1	0	LSB fixed 18 bits	$384f_s$	32	$384f_s$
1	1	1	LSB fixed 20 bits	$384f_s$	32	$384f_s$

Note

1. Number of clock pulses within half an audio sample.

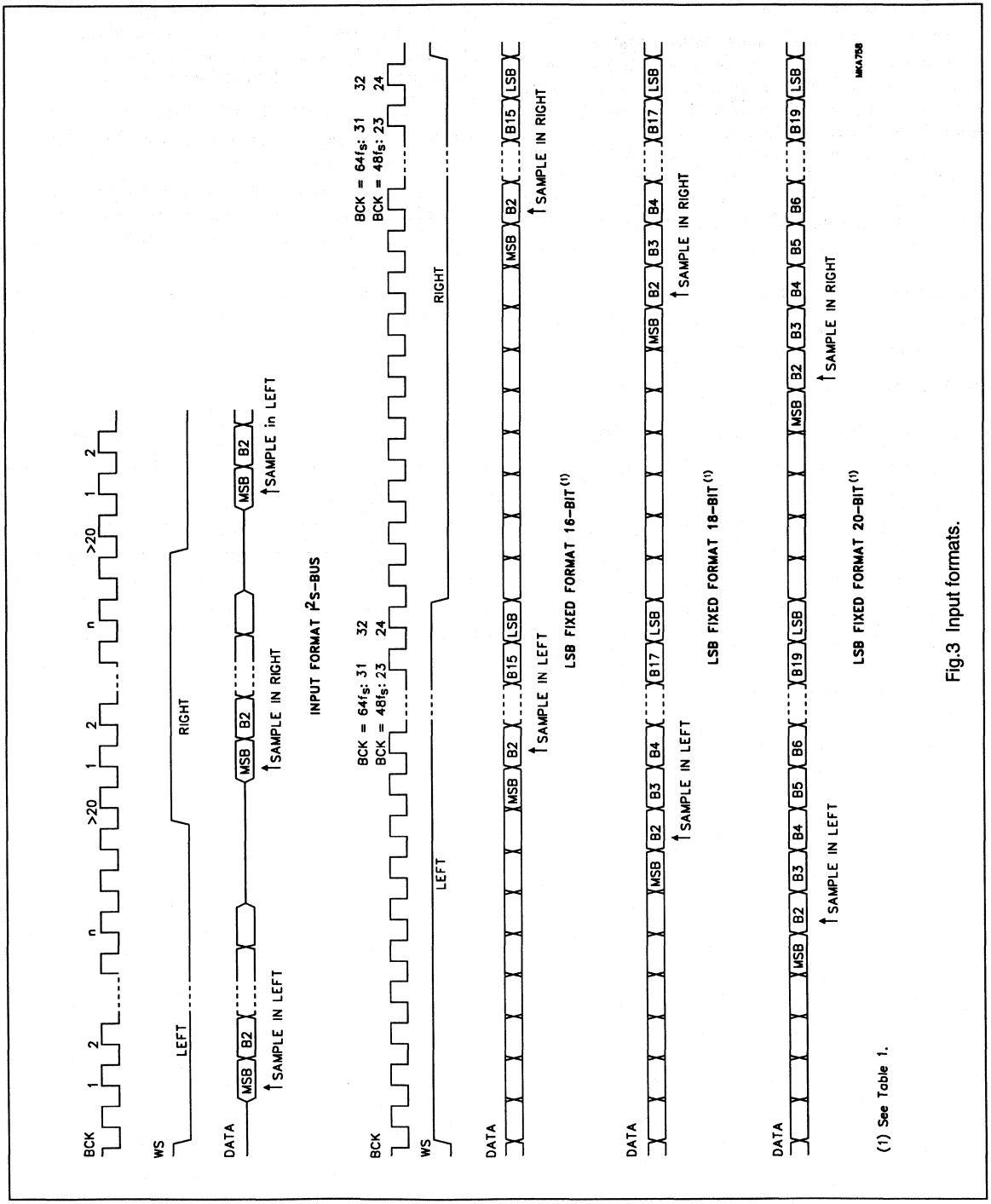


Fig.3 Input formats.

Mute

Soft mute is controlled by the $\overline{\text{MUSB}}$ at pin 9. When the input is active LOW the value of the samples is decreased smoothly to zero following a cosine curve. To step down the value of the data 32 coefficients are used, each one being used 31 times before stepping onto the next. When MUTE is released (pin 19 = HIGH), the samples are returned to the full level again following a cosine curve with the same coefficients being used in the reverse order. Mute is synchronized to prevent operation in the middle of a word.

De-emphasis

A digital de-emphasis is implemented for three sample rates (32, 44.1 and 48 kHz). By selecting DEEM1 and DEEM2 de-emphasis can be applied by means of a FIR filter. Time constants of the de-emphasis are 50 µs and 15 µs. De-emphasis is synchronized to prevent operation in the middle of a word. The de-emphasis deviation from ideal 50 µs and 15 µs de-emphasis is given in Table 4.

Table 2 De-emphasis.

DEEM1	DEEM2	CONDITION
0	0	de-emphasis disabled
0	1	de-emphasis for f_s = 32 kHz
1	0	de-emphasis for f_s = 4.1 kHz
1	1	de-emphasis for f_s = 48 kHz

Attenuation

Attenuation is controlled by the $\overline{\text{ATSB}}$ input (pin 21). When the input is active LOW the sample is multiplied by a coefficient that provides 12 dB attenuation. If the input is HIGH the multiplication factor is 1. Attenuation is synchronized to prevent operation in the middle of a word.

Double-speed mode

Double speed is controlled by the $\overline{\text{DSMB}}$ input (pin 20). When the input is active LOW the device operates in the double-speed mode.

Oversampling filter (normal-speed mode)

In the normal-speed mode the oversampling filter consists of:

- A 91st order half-band low-pass FIR filter which increases the oversampling rate from 1 time to 2 times.
- A 23rd order quarter band low-pass FIR filter which increases the oversampling rate from 2 times to 8 times.
- A linear interpolation section which increases the oversampling rate to 16 times. This removes the spectral components around $8f_s$.
- A sample-and-hold section which provides another 6 times oversampling to 96 times. The zero-order hold characteristic of this sample-and-hold section plus the 1st order analog filtering remove the spectral components around $16f_s$.

Pass-band ripple and stop-band attenuation for normal-speed are given in Table 3.

Oversampling filter (double-speed mode)

In the double-speed mode the oversampling filter consists of:

- A 51st order half-band low-pass FIR filter which increases the oversampling rate from 1 time to 2 times.
- A 7th order half-band low-pass FIR filter which increases the oversampling rate from 2 times to 4 times.
- A linear interpolation section which increases the oversampling rate to 8 times. This removes the spectral components around $4f_s$.
- A sample-and-hold section which provides another 6 times oversampling to 48 times. The zero-order hold characteristic of this sample-and-hold section plus the 1st order analog filtering remove the spectral components around $8f_s$.

Pass-band ripple and stop-band attenuation for double-speed are given in Table 3.

Noise shaper

In the normal speed mode the 2nd order digital noise shaper operates at $96f_s$ ($f_{sys} = 384f_s$) or $128f_s$ ($f_{sys} = 256f_s$). The digital noise shaper operates at $48f_s$ ($f_{sys} = 384f_s$) or $64f_s$ ($f_{sys} = 256f_s$) in double-speed mode. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique used in combination with a special data coding enables extremely high signal-to-noise ratios to be achieved. The noise shaper outputs a 5-bit pulse duration modulation (PDM) bitstream signal to the DAC.

Continuous calibration DAC

The dual 5-bit DAC uses the continuous calibration technique. This method, based on charge storage, involves exact duplication of a single reference current source. In the TDA1305T, 32 such current sources plus 1 spare source are continuously calibrated. The spare source is included to allow continuous converter operation.

The DAC receives a 5-bit data bitstream from the noise shaper. This data is then converted so that only small currents are switched to the output during digital silence (input 00000H). Using this technique extremely high signal-to-noise performance is achieved.

Operational amplifiers

High precision, low-noise amplifiers together with the internal conversion resistors R_{CONV1} and R_{CONV2} convert the converter output current to a voltage capable of driving a line output. This voltage is available at VOL and VOR (1.5 V RMS typical).

Connecting external capacitors CEXT1 and CEXT2 between FILTCL and VOL and between FILTCR and VOR respectively provides the required 1st order post filtering for the left and right channels (see Fig.1). The combinations of R_{CONV1} with CEXT1 and R_{CONV2} with CEXT2 determine the 1st order fall-off frequencies.

Internal reference circuitry

Internal reference circuitry ensures that the output voltage signal is proportional to the supply voltage, thereby maintaining maximum dynamic range for supply voltages from 3.4 to 5.5 V and making the circuit also suitable for battery-powered applications.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage		–	7.0	V
V_{DDA}	analog supply voltage		–	7.0	V
V_{DDO}	operational amplifier supply voltage		–	7.0	V
T_{xtal}	maximum crystal temperature		–	+150	°C
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient operating temperature		–30	+85	°C
V_{es}	electrostatic handling	note 1	–2000	+2000	V
		note 2	–200	+200	V

Notes

1. Human body model; C = 100 pF, R = 1500 Ω, V = 2000 V, 3 pulses positive and 3 pulses negative.
2. Machine model; C = 200 pF, R = 10 Ω, L = 0.5 μH.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	75	K/W

Stereo 1f_s data input up-sampling filter with bitstream continuous calibration dual DAC (BCC-DAC2) TDA1305T

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611E"*. The number of this quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9398 510 63011.

DIGITAL CHARACTERISTICS

V_{DD} = 3.4 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage	note 1	3.4	5.0	5.5	V
I_{DDD}	digital supply current	V_{DDD} = 5 V; at code 00000H	–	30	40	mA
V_{DDA}	analog supply voltage	note 1	3.4	5.0	5.5	V
I_{DDA}	analog supply current	V_{DDA} = 5 V; at code 00000H	–	5.5	8	mA
V_{DDO}	operational amplifier supply voltage	note 1	3.4	5.0	5.5	V
I_{DDO}	operational amplifier supply current	V_{DDO} = 5 V; at code 00000H	–	6.5	9	mA
RR	ripple rejection to V_{DDA}	note 2	–	25	–	dB
System clock input						
f_{sys}	system frequency	$f_{sys} = 384f_s$	9.6	16.93	18.4	MHz
		$f_{sys} = 256f_s$	6.4	11.29	12.28	MHz
V_{IL}	LOW level input voltage	note 3	−0.5	–	$0.2V_{DD}$	V
V_{IH}	HIGH level input voltage	note 3	$0.8V_{DD}$	–	V_{DD} + 0.5	V
$\|I_{LI}\|$	input leakage current	note 4	–	–	10	µA
C_i	input capacitance		–	–	10	pF
T_{cy}	clock cycle time	$f_{sys} = 384f_s$	104	59.1	54.2	ns
		$f_{sys} = 256f_s$	156	88.6	81.3	ns
Digital inputs; WS, BCK, DATA, $\overline{\text{DSMB}}$, $\overline{\text{MUSB}}$, DEEM1, DEEM2, $\overline{\text{ATSB}}$, CLKS1, CLKS2, TEST1 and TEST2						
V_{IL}	LOW level input voltage	note 3	−0.5	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	note 3	$0.7V_{DD}$	–	V_{DD} + 0.5	V
$\|I_{LI}\|$	input leakage current	note 4	–	–	10	µA
C_i	input capacitance		–	–	10	pF
Digital output; CDEC						
V_{OL}	LOW level output voltage	I_{OL} = 0.4 mA	0	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	V_{DD} − 0.5	–	V_{DD}	V
t_r	output rise time	note 5	–	–	20	ns
t_f	output fall time	note 5	–	–	20	ns
C_L	load capacitance		–	–	30	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial input data timing (Fig.4)						
f_{BCK}	bit-clock input (data input rate) frequency	$f_{sys} = 384f_s$	–	$48f_s$	–	MHz
		$f_{sys} = 256f_s$	–	$64f_s$	–	MHz
f_{WS}	word select input frequency	normal speed	25	44.1	48	kHz
		double speed	50	88.2	96	kHz
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
t_H	bit clock time HIGH		55	–	–	ns
t_L	bit clock time LOW		55	–	–	ns
t_{su}	data set-up time		40	–	–	ns
t_h	data hold time		10	–	–	ns
t_{suWS}	word select set-up time		40	–	–	ns
t_{hWS}	word select hold time		10	–	–	ns

Notes

1. All V_{DD} and V_{SS} pins must be connected externally to the same supply.
2. V_{ripple} = 1% of supply voltage; f_{ripple} = 100 Hz. Ripple rejection RR to V_{DDA} is dependent on the value of the external capacitor (C_{EXT3} in Fig.1) connected to V_{ref}. The value here assumes that C_{EXT3} = 1 µF.
3. Minimum V_{IL} and maximum V_{IH} are peak values to allow for transients.
4. I_{LImin} measured at V_I = 0 V; I_{LImax} measured at V_I = 5.5 V.
5. Reference levels = 10% and 90%.

ANALOG CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{DDO}$ = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference values						
V_{ref}	reference voltage level		2.45	2.5	2.55	V
R_{CONV}	current-to-voltage conversion resistor		1.6	2.2	2.8	kΩ
Analog outputs						
RES	resolution		–	–	18	bit
$V_{FS(rms)}$	full-scale output voltage (pins 23 and 25) (RMS value)		1.425	1.5	1.575	V
V_{OFF}	output voltage DC offset with respect to reference voltage level V_{ref}		–80	–65	–50	mV
TC_{FS}	full scale temperature coefficient		–	$\pm 100 \times 10^{-6}$	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB input level; note 1	–	–90	–81	dB
			–	0.003	0.009	%
		at –60 dB input level; note 2	–	–44	–40	dB
			–	0.63	1.0	%
		at –60 dB input level; A-weighted; note 3	–	–46	–	dB
			–	0.5	–	%
		at 0 dB input level; (20 Hz to 20 kHz); note 4	–	–90	–81	dB
			–	0.003	0.003	%
S/N	signal-to-noise ratio at bipolar zero	A weighted; at code (00000H)	100	108	–	dB
α_{cs}	channel separation		85	100	–	dB
$\lvert\delta V_O\rvert$	unbalance between outputs		–	0.2	0.3	dB
$\lvert Z_O\rvert$	dynamic output impedance		–	10	–	Ω
R_L	output load resistance		3	–	–	kΩ
C_L	output load capacitance		–	–	200	pF

Notes

1. Measured with a 1 kHz, 0 dB, 18-bit sine wave generated at a sampling rate of 48 kHz. The (THD + N)/S measured over a bandwidth of 20 Hz to 20 kHz.
2. Measured with a 1 kHz, -60 dB, 18-bit sine wave generated at a sampling rate of 48 kHz. The (THD + N)/S measured over a bandwidth of 20 Hz to 20 kHz. For 16-bit input signals, the performance is limited to the theoretical maximum.
3. Measured with a 1 kHz, -60 dB, 18-bit sine wave generated at a sampling rate of 48 kHz. The (THD + N)/S measured over a bandwidth of 20 Hz to 20 kHz and filtered with a A-weighted characteristic. For 16-bit input signals, the performance is limited to the theoretical maximum.
4. Measured with a sine wave from 20 Hz to 20 kHz generated at a sampling rate of 48 kHz. The (THD + N)/S measured over a bandwidth of 20 Hz to 20 kHz.

TEST AND APPLICATION INFORMATION

Filter characteristics (theoretical values)

Table 3 Normal speed filter characteristics.

ITEMS	SAMPLE FREQUENCY	RANGE	CONDITIONS	CHARACTERISTICS
Pass band	44.1 kHz	0 to 20 kHz		0 ±0.025 dB
	32 kHz	14.5 to 15 kHz		–0.15 dB (min.)
Stop band	44.1 kHz	24.1 to 150 kHz	typical	–60 dB (max.)
			worst case	–57 dB (max.)
		150 kHz to infinity	typical	–57 dB (max.)
			worst case	–47 dB (max.)
	32 kHz	17 to 17.5 kHz		–40 dB (max)

De-emphasis filter characteristics (theoretical values)

Table 4 De-emphasis deviation from ideal 50 µs to 15 µs de-emphasis network.

ITEM	SAMPLE FREQUENCY	RANGE	CHARACTERISTICS
Gain deviation	44.1 and 48 kHz	0 to 18 kHz	0 ±0.05 dB
		18 to 20 kHz	0.12 dB (max.)
	32 kHz	0 to 13 kHz	0 ±0.06 dB
		13 to 15 kHz	0.22 dB (max.)
Phase deviation	44.1 and 48 kHz	0 to 15 kHz	10 deg (max.)
		15 to 20 kHz	15 deg (max.)
	32 kHz	0 to 9 kHz	10 deg (max.)
		9 to 15 kHz	16 deg (max.)

Double-speed characteristics

Table 5 Double-speed filter characteristics.

ITEM	RANGE	CONDITIONS	CHARACTERISTICS
Pass band	0 to 17 kHz		0 ±0.075 dB
	17 to 20 kHz		−0.3 dB (min.)
Stop band	24.1 to 150 kHz	typical	−47 dB (max.)
		worst case	−45 dB (max.)
	150 kHz to infinite	typical	−33 dB (max.)
		worst case	−25 dB (max.)

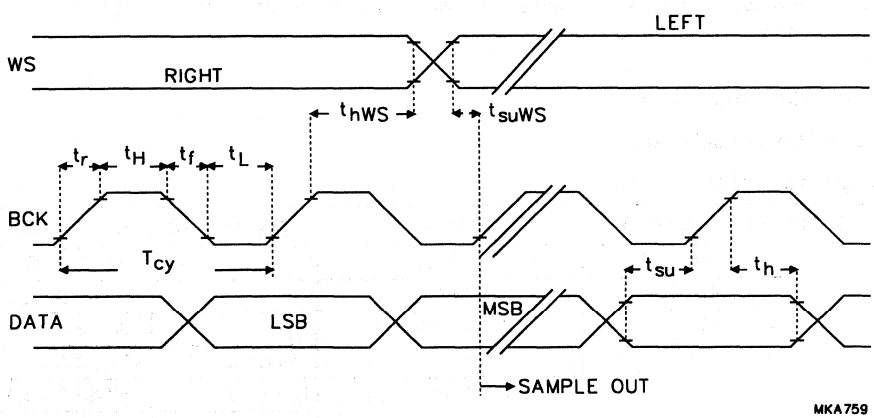


Fig.4 Timing of input signals.

APPLICATION INFORMATION

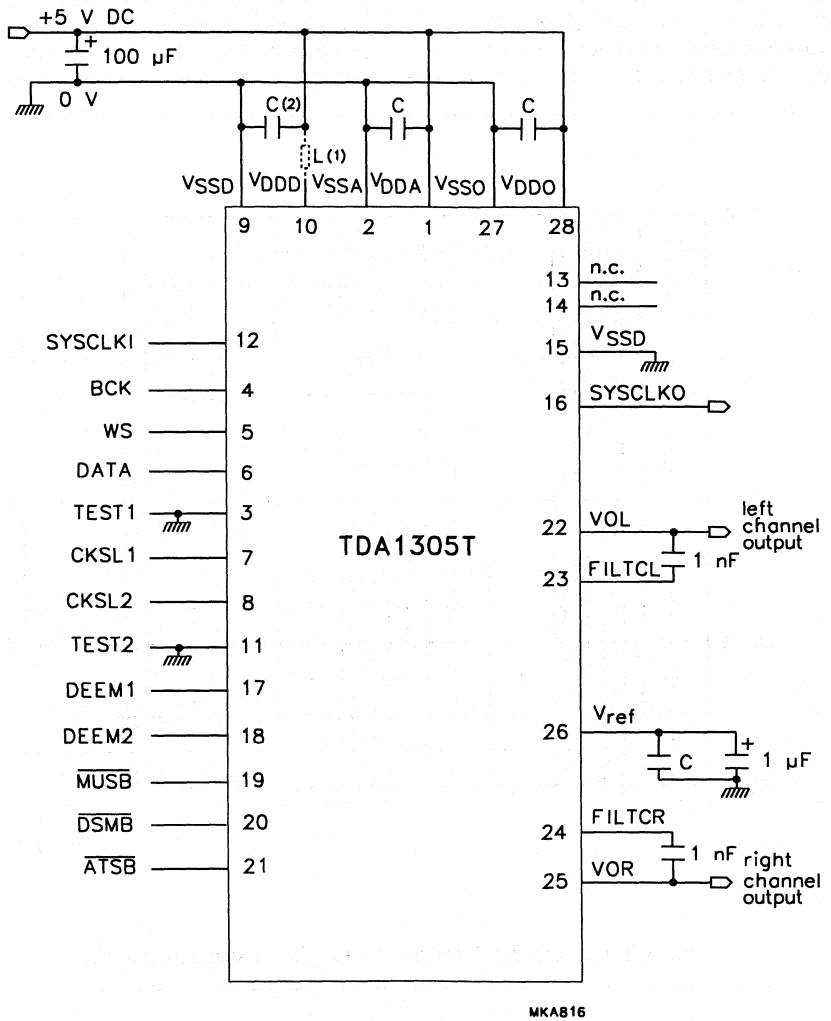
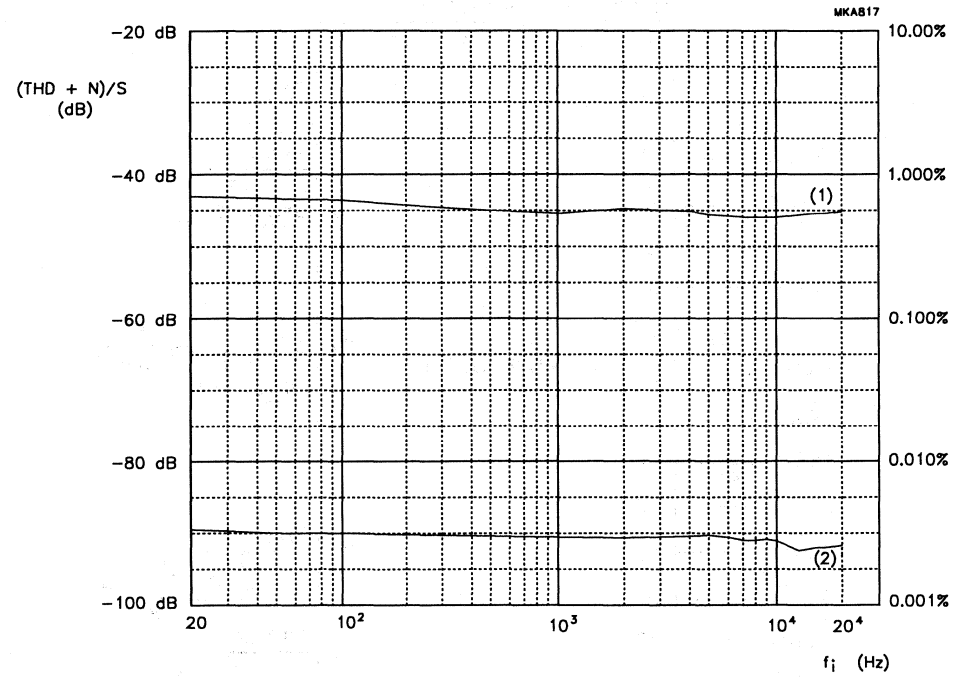


Fig.5 Application diagram.

A typical application diagram is illustrated in Fig.5. The left and right channel outputs can drive a line output directly. The series inductor (L) in the digital supply line, though not strictly necessary, helps to reduce crosstalk between the digital and analog circuits.

In Fig.6 measurements were taken with an 18-bit sine wave generated at a sampling rate of 48 kHz. The (THD + N)/S was measured over a bandwidth of 20 Hz to 20 kHz. The graph was constructed from average measurement values of a small amount of engineering samples. No guarantee for typical values is implied.

In Fig.6 measurements were taken with an 18-bit sine wave generated at a sampling rate of 48 kHz. The (THD + N)/S was measured over a bandwidth of 20 Hz to 20 kHz and filtered with A-weighted characteristics. The graph was constructed from average measurement values of a small amount of engineering samples. No guarantee for typical values is implied.



(1) Level = −60 dB.
(2) Level = 0 dB.

Fig.6 Total harmonic distortion as a function of signal frequency.

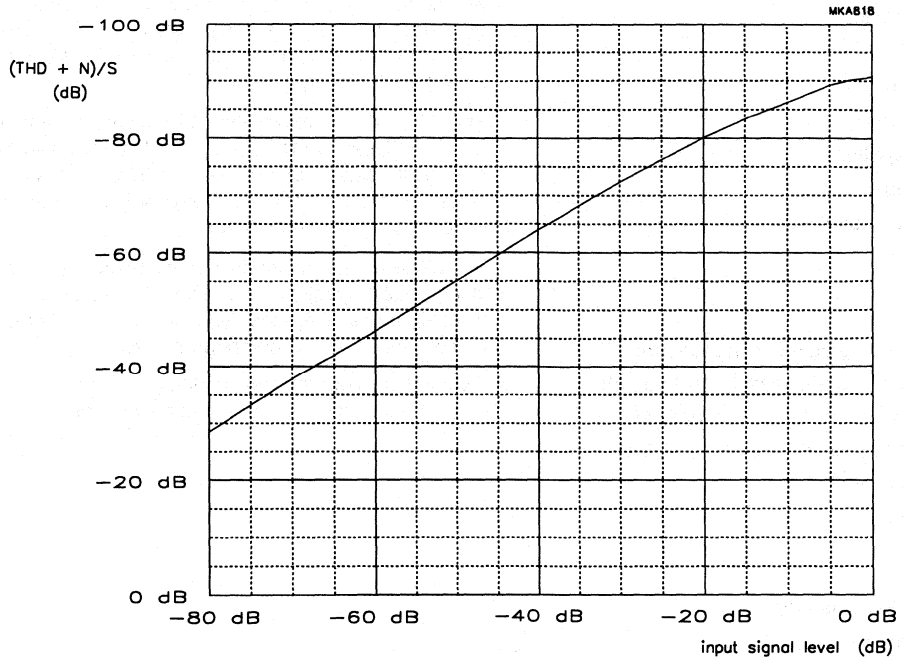


Fig.7 Total harmonic distortion as a function of signal level; (A-weighted).

Noise shaping filter DAC TDA1306T

FEATURES

General

- Double-speed mode
- Digital volume control
- Soft mute function
- 12 dB attenuation
- Low power dissipation
- Digital de-emphasis
- TDA1305T pin compatible.

Easy application

- Voltage output
- Only 1st-order analog post-filtering required
- Operational amplifiers and digital filter integrated
- Selectable system clock (f_{sys}) $256f_s$ or $384f_s$
- I^2S-bus ($f_{sys} = 256f_s$) or 16, 18 or 20 bits LSB fixed serial input format ($f_{sys} = 384f_s$).
- Single rail supply.

High performance

- Superior signal-to-noise ratio
- Wide dynamic range
- No zero crossing distortion
- Inherently monotonic
- Continuous calibration digital-to-analog conversion combined with noise shaping technique.

GENERAL DESCRIPTION

The TDA1306T is a dual CMOS digital-to-analog converter with up-sampling filter and noise shaper. The combination of oversampling up to $4f_s$, noise shaping and continuous calibration conversion ensures that only simple 1st-order analog post-filtering is required.

The TDA1306T supports the I^2S-bus data input mode ($f_{sys} = 256f_s$) with word lengths of up to 20 bits and the LSB fixed serial data input format ($f_{sys} = 384f_s$) with word lengths of 16, 18 or 20 bits. Two cascaded IIR filters increase the sampling rate 4 times.

The DACs are of the continuous calibration type and incorporate a special data coding. This ensures a high signal-to-noise ratio, wide dynamic range and immunity to process variation and component ageing.

Two on-board operational amplifiers convert the digital-to-analog current to an output voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1306T	SO24	plastic small outline package; 24 leads; body width 7.5 mm.	SOT137–1

QUICK REFERENCE DATA

All power supply pins V_{DD} and V_{SS} must be connected to the same external supply unit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage		4.5	5.0	5.5	V
I_{DDD}	digital supply current	V_{DDD} = 5 V; at code 00000H	–	5	8	mA
I_{DDA}	analog supply current	V_{DDA} = 5 V; at code 00000H	–	3	5	mA
I_{DDO}	operational amplifier supply current	V_{DDO} = 5 V; at code 00000H	–	2	4	mA
Analog signals						
$V_{FS(rms)}$	full-scale output voltage (RMS value)	$V_{DDD} = V_{DDA} = V_{DDO}$ = 5 V; R_L > 5 kΩ	0.935	1.1	1.265	V
R_L	output load resistance		5	–	–	kΩ
DAC performance						
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level; f_i = 1 kHz;	–	–70	–	dB
			–	0.032	–	%
		at –60 dB signal level; f_i = 1 kHz;	–	–42	–32	dB
			–	0.8	2.5	%
S/N_{ds}	signal-to-noise ratio at digital silence	no signal; A-weighted	–	–108	–96	dB
BR	input bit rate at data input	f_s = 44.1 kHz; normal speed	–	–	2.822	Mbits/s
		f_s = 44.1 kHz; double speed	–	–	5.645	Mbits/s
f_{sys}	system clock frequency (pin 12)		6.4	–	18.432	MHz
T_{amb}	operating ambient temperature		–40	–	+85	°C

BLOCK DIAGRAM

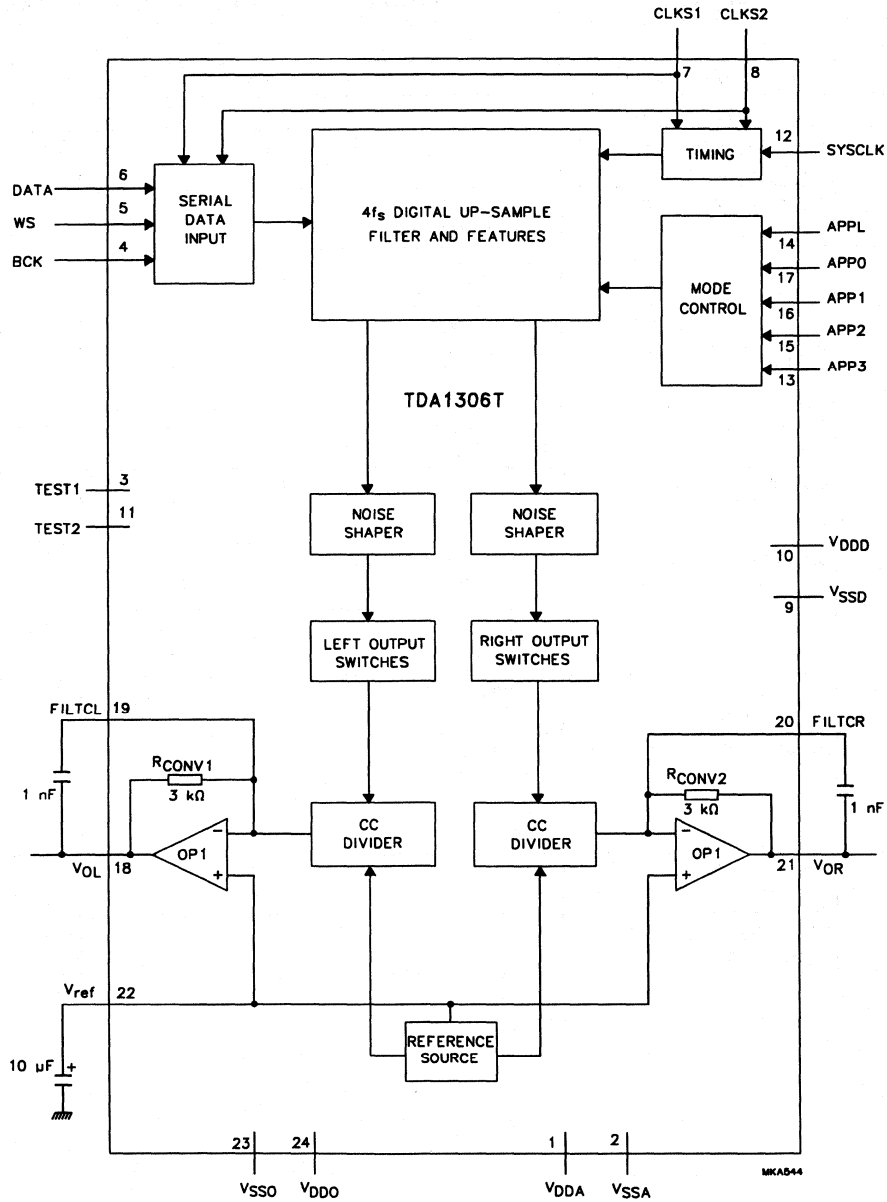


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DDA}	1	analog supply voltage (+5 V)
V_{SSA}	2	analog ground
TEST1	3	test input 1; pin should be connected to ground
BCK	4	bit clock input
WS	5	word select input
DATA	6	data input
CLKS1	7	clock and format selection 1 input
CLKS2	8	clock and format selection 2 input
V_{SSD}	9	digital ground
V_{DDD}	10	digital supply voltage (+5 V)
TEST2	11	test input 2; pin should be connected to ground
SYSCLK	12	system clock input $256f_s$ or $384f_s$
APP3	13	application mode 3 input
APPL	14	application mode selection input
APP2	15	application mode 2 input
APP1	16	application mode 1 input
APP0	17	application mode 0 input
V_{OL}	18	left channel output
FILTCL	19	capacitor for left channel 1st order filter function; should be connected between pins 19 and 18
FILTCR	20	capacitor for right channel 1st order filter function; should be connected between pins 20 and 21
V_{OR}	21	right channel output
V_{ref}	22	internal reference voltage for output channels; $0.5V_{DDO}$ (typ.)
V_{SSO}	23	operational amplifier ground
V_{DDO}	24	operational amplifier supply voltage

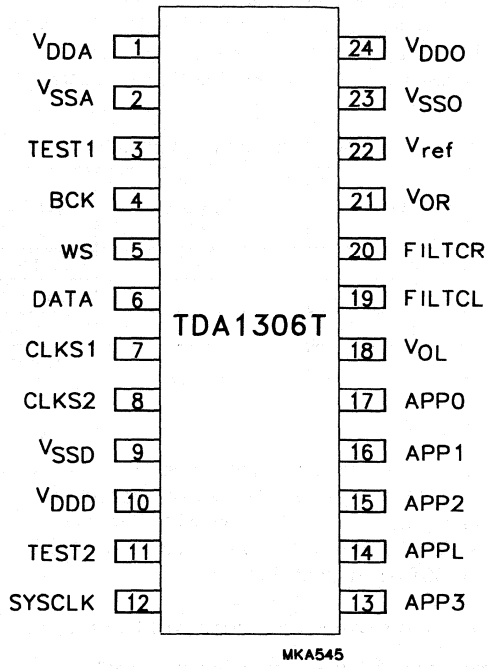


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1306T CMOS DAC incorporates an up-sampling filter, a noise shaper, continuous calibrated current sources and operational amplifiers.

System clock and data input format

The TDA1306T accommodates slave mode only. Consequently, in all applications, the system devices must provide the system clock. The system frequency is selectable at pins CLKS1 and CLKS2 (see Table 1).

The TDA1306T supports the following data input modes:

- I^2S-bus with data word length of up to 20 bits ($f_{sys} = 256f_s$)
- LSB fixed serial format with data word length of 16, 18 or 20 bits ($f_{sys} = 384f_s$). As this format idles on the MSB it is necessary to know how many bits are being transmitted.

The input formats are illustrated in Fig.9. Left and right data channel words are time multiplexed.

Table 1 Data input format and system clock.

CLKS1	CLKS2	DATA INPUT FORMAT	SYSTEM CLOCK	
			NORMAL SPEED	DOUBLE SPEED
0	0	I^2S-bus	$256f_s$	$128f_s$
0	1	LSB fixed 16 bits	$384f_s$	$192f_s$
1	0	LSB fixed 18 bits	$384f_s$	$192f_s$
1	1	LSB fixed 20 bits	$384f_s$	$192f_s$

Device operation

When the APPL pin is held HIGH and APP3 is held LOW, pins APP0, APP1 and APP2 form a microcontroller interface. When the APPL pin is held LOW, pins APP0, APP1, APP2 and APP3 form a pseudo-static application (TDA1305T pin compatible).

PSEUDO-STATIC APPLICATION MODE (APPL = LOGIC 0)

In this mode, the device operation is controlled by pseudo-static application pins where:

APP0 = attenuation mode control

APP1 = double-speed mode control

APP2 = mute mode control

APP3 = de-emphasis mode control.

In the pseudo-static application mode the TDA1306T is pin compatible with the TDA1305T slave mode. The correspondence between TDA1306T pin number, TDA1306T pin name, TDA1305T pin mnemonic and a description of the effects is given in Table 2.

Table 2 Pseudo-static application mode.

PIN MNEMONIC	PIN NUMBER	TDA1305T FUNCTION	VALUE	DESCRIPTION
APP0	17	ATSB	0	12 dB attenuation (from full scale) activated (only if MUSB = logic 1)
			1	full scale (only if MUSB = logic 1)
APP1	16	DSMB	0	double-speed mode
			1	normal-speed mode
APP2	15	MUSB	0	samples decrease to mute level
			1	level according to ATSB
APP3	13	DEEM1	0	de-emphasis OFF (44.1 kHz)
			1	de-emphasis ON (44.1 kHz)

MICROCONTROLLER APPLICATION MODE (APPL = LOGIC 1, APP3 = LOGIC 0).

In this mode, the device operation is controlled by a set of flags in an 8-bit mode control register. The 8-bit mode control register is written by a microcontroller interface where:

APPL = logic 1

APP0 = Data

APP1 = Clock

APP2 = RAB

APP3 = logic 0.

The correspondence between serial-to-parallel conversion, mode control flags and a summary of the effect of the control flags is given in Table 3. Figures 3 and 4 illustrate the mode set timing.

MICROCONTROLLER WRITE OPERATION SEQUENCE

The microcontroller write operation follows the following sequence:

- APP2 is held LOW by the microcontroller
- Microcontroller data is clocked into the internal shift register on the LOW-to-HIGH transition on pin APP1
- Data D7 to D0 is latched into the appropriate control register on the LOW-to-HIGH transition of pin APP2 (APP1 = HIGH)
- If more data is clocked into the TDA1306T before the LOW-to-HIGH transition on pin APP2 then only the last 8 bits are used
- If less data is clocked into the TDA1306T unpredictable operation will result
- If the LOW-to-HIGH transition of pin APP2 occurs when APP1 = LOW, the command will be disregarded.

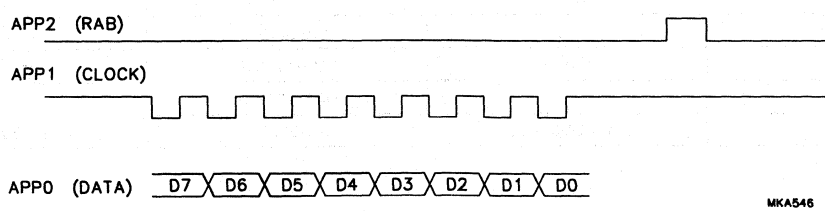


Fig.3 Microcontroller timing.

MICROCONTROLLER WRITE OPERATION SEQUENCE (REPEAT MODE)

The same command can be repeated several times (e.g. for fade function) by applying APP2 pulses as shown in Fig.4. It should be noted that APP1 must stay HIGH between APP2 pulses. A minimum pause of 22 ms is necessary between any two step-up or step-down commands.

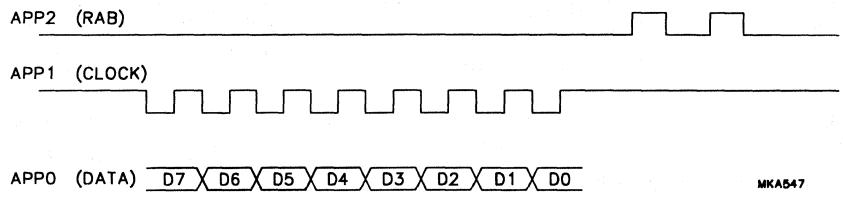


Fig.4 Microcontroller timing (repeat mode).

Table 3 Microcontroller mode control register.

BIT POSITION	FUNCTION	DESCRIPTION	ACTIVE LEVEL
D7	ATSB	12 dB attenuation (from full scale)	LOW
D6	DSMB	double speed	LOW
D5	MUSB	mute	LOW
D4	DEEM	de-emphasis	HIGH
D3	FS	full scale	HIGH
D2	INCR	increment	HIGH
D1	DECR	decrement	HIGH
D0	not applicable	reserved	not applicable

Volume control

A digital level control is incorporated in the TDA1306T which performs the function of soft mute and attenuation (pseudo-static application mode) or soft mute, attenuation, fade, increment and decrement (microcontroller application mode). The volume control of both channels can be varied in small step changes determined by the value of the internal fade counter where:

audio level = counter × maximum level/120,

where the counter is a 7-bit binary number between 0 and 120. The time taken for mute to vary from 120 to 0 is $1/120f_s$. For example, when f_s = 44.1 kHz, the time taken is approximately 3 ms.

VOLUME CONTROL (PSEUDO-STATIC APPLICATION MODE)

In the pseudo-static application mode (APPL = logic 0) the digital audio output level is controlled by APP0 (attenuation) and APP2 (mute) so only the final volume levels full scale, 12 dB (attenuate) and mute (–infinity dB) can be selected. The mute function has priority over the attenuation function. Accordingly, if MUSB is LOW, the state of ATSB has no effect. An example of volume control in this application mode is illustrated in Fig.5.

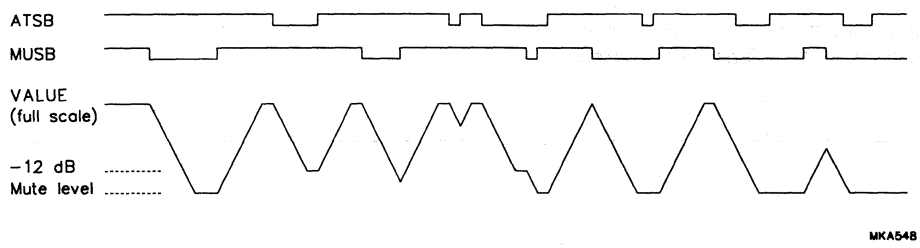


Fig.5 Volume control (pseudo-static application mode).

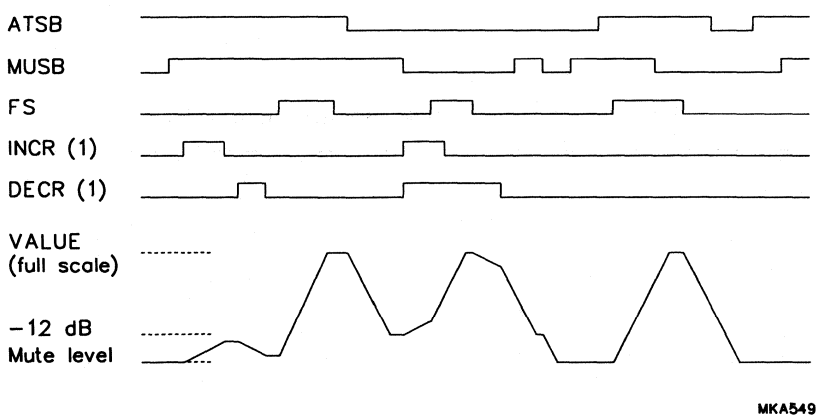
VOLUME CONTROL (MICROCONTROLLER APPLICATION MODE)

In the microcontroller application mode (APPL = logic 1, APP3 = logic 0) the audio output level is controlled by volume control bits ATSB, MUSB, FS, INCR and DECR.

Mute is activated by sending the MUSB command to the mode control register via the microcontroller interface. The audio output level will be reduced to zero in a maximum of 120 steps (depending on the current position of the fade counter) and taking a maximum of 3 ms. Mute, attenuation and full scale are synchronized to prevent operation in the middle of a word.

- The counter is preset to 120 by the full scale command.
- The counter is preset to 30 by the attenuate command when its value is more then 30. If the value of the counter is less than 30 dB the ATSB command has no effect.
- The counter is preset to logic 0 by the mute command MUSB.
- Attenuation (−12 dB) is activated by sending the ATSB command to the fade control register (D7).
- Attenuation and mute are cancelled by sending the full-scale command to the fade control register (Register D3).

To control the fade counter in a continuous way, the INCREMENT and DECREMENT commands are available (fade control Registers D1 and D2). They will increment and decrement the counter by 1 for each register write operation. When issuing more than 1 step-up or step-down command in sequence, the write repeat mode may be used (see microcontroller application mode). An example of volume control in this application mode is illustrated in Fig.6.



(1) INCR and DECR in repeat mode.

Fig.6 Volume control (microcontroller application mode).

There are two recommended application situations within the microcontroller mode:

- The customer wants to use the microcontroller interface without the volume setting facility. In this event the operation is as follows:
  - Mute ON; by sending the MUSB command
  - Mute OFF; by sending the FS command
  - Attenuation ON; by sending the ATSB command
  - Attenuation OFF; by sending the FS command.

  It is possible to switch from 'Attenuation ON' to 'Mute ON' but not vice-versa.
- Incorporating the volume control feature operates as follows:
  - Mute ON; by sending the MUSB command the microcontroller has to store the previous volume setting
  - Mute OFF; by sending succeeding INCR commands until the previous volume is reached
  - Attenuation ON; by sending succeeding DECR commands until a relative downstep of −12 dB is reached. The microcontroller has to store the previous volume
  - Attenuation OFF; by sending the succeeding INCR commands until the previous volume is reached
  - Volume UP; by sending succeeding INCR commands
  - Volume DOWN; by sending succeeding DECR commands.

De-emphasis

A digital de-emphasis is implemented in the TDA1306T. By selecting the DEEM bit at register D4 (microcontroller application mode) or activating the APP3 pin (pseudo-static application mode), de-emphasis can be applied by means of an IIR filter. De-emphasis is synchronized to prevent operation in the middle of a word.

Double-speed mode

The double-speed mode is controlled by the DSMB bit at register D6 (microcontroller application mode) or by activating the APP1 pin (pseudo-static application mode). When the control bit is active LOW the device operates in the double-speed mode.

Oversampling filter and noise shaper

The digital filter is a four times oversampling filter. It consists of two sections which each increase the sample rate by 2. The noise-shaper operates on $4f_s$ and reduces the in-band noise density.

DAC and operational amplifiers

In this noise shaping filter DAC a special data code and bidirectional current sources are used in order to achieve true low-noise performance. The special data code guarantees that only small values of current flow to the output during small signal passages while larger positive or negative values are generated using the bidirectional current sources. The noise shaping filter-DAC uses the continuous calibration conversion technique.

The operational amplifiers and the internal conversion resistors R_{CONV1} and R_{CONV2} convert the DAC current to an output voltage available at V_{OL} and V_{OR}. Connecting an external capacitor between FILTCL and V_{OL}, FILTCR and V_{OR} respectively provides the required 1st-order post filtering.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	–	7.0	V
T_{xtal}	maximum crystal temperature		–	+150	°C
T_{stg}	storage temperature		–65	+125	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic handling	note 2	–2000	+2000	V
		note 3	–200	+200	V

Notes

1. All V_{DD} and V_{SS} connections must be made to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 mH series inductor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	69	K/W

QUALITY SPECIFICATION

In accordance with *"UZW-BO/FQ-0601"*. The numbers of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9398 510 63011.

DC CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = 5$ V; $T_{amb} = 25$ °C; all voltages referenced to ground (pins 2, 9 and 23); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage (pin 10)	note 1	4.5	5.0	5.5	V
V_{DDA}	analog supply voltage (pin 1)	note 1	4.5	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage (pin 24)	note 1	4.5	5.0	5.5	V
I_{DDD}	digital supply current	$f_{sys} = 11.28$ MHz	–	5	8	mA
I_{DDA}	analog supply current	at digital silence	–	3	6	mA
I_{DDO}	operational amplifier supply current	no operational amplifier load resistor	–	2	4	mA
P_{tot}	total power dissipation	$f_{sys} = 11.28$ MHz; digital silence; no operational amplifier load resistor	–	50	90	mW
V_{IH}	HIGH level digital input voltage (pins 3 to 8 and 11 to 17)		$0.7V_{DDD}$	–	$V_{DDD} + 0.5$	V
V_{IL}	LOW level digital input voltage (pins 3 to 8 and 11 to 17)		–0.5	–	$0.3V_{DDD}$	V
R_{pd}	internal pull-down resistor to V_{SSD} (pins 3 and 11)		17	–	134	kΩ
$\|I_{LI}\|$	input leakage current		–	–	10	μA
C_i	input capacitance		–	–	10	pF
V_{ref}	reference voltage (pin 22)	with respect to V_{SSO}	$0.45V_{DDO}$	$0.5V_{DDO}$	$0.55V_{DDO}$	V
R_{CONV}	current-to-voltage conversion resistor		2.4	3.0	3.6	kΩ
$V_{FS(rms)}$	full-scale output voltage (RMS value)	$R_L > 5$ kΩ; note 2	0.935	1.1	1.265	V
R_L	output load resistance		5	–	–	kΩ

Notes

1. All power supply pins (V_{DD} and V_{SS}) must be connected to the same external power supply unit.
2. R_L is the AC resistance of the external circuitry connected to the audio outputs of the application circuit.

AC CHARACTERISTICS (ANALOG)

$V_{DDD} = V_{DDA} = V_{DDO} = 5$ V; $T_{amb} = 25$ °C; all voltages referenced to ground (pins 2, 9 and 23); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DACs						
SVRR	supply voltage ripple rejection V_{DDA} and V_{DDO}	f_{ripple} = 1 kHz; V_{ripple} = 100 mV (p-p); C22 = 10 µF	–	40	–	dB
ΔG_v	unbalance between the 2 DAC voltage outputs (pins 18 and 21)	maximum volume	–	–	0.5	dB
α_{ct}	crosstalk between the 2 DAC voltage outputs (pins 18 and 21)	one output digital silence the other maximum volume	–	–110	–85	dB
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level; f_i = 1 kHz	–	–70	–	dB
			–	0.032	–	%
		at –60 dB signal level; f_i = 1 kHz	–	–42	–32	dB
			–	0.8	2.5	%
S/N_{ds}	signal-to-noise ratio at digital silence	no signal; A-weighted	–	–108	–96	dB
Operational amplifiers						
G_v	open-loop voltage gain		–	85	–	dB
PSRR	power supply rejection ratio	f_{ripple} = 3 kHz; V_{ripple} = 100 mV (p-p); A-weighted	–	90	–	dB
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	$R_L > 5$ kΩ; f_i = 1 kHz; V_o = 2.8 V (p-p)	–	–100	–	dB
f_{UG}	unity gain frequency	open loop	–	4.5	–	MHz
$\|Z_o\|$	AC output impedance	$R_L > 5$ kΩ	–	1.5	150	Ω

AC CHARACTERISTICS (DIGITAL)

$V_{DDD} = V_{DDA} = V_{DDO}$ 4.5 to 5.5 V; all voltages referenced to ground (pins 2, 9 and 23); $T_{amb} = -40$ to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{WX}	clock cycle time	$f_{sys} = 384f_s$; normal speed	54.2	59.1	104	ns
		$f_{sys} = 192f_s$; double speed	54.2	59.1	104	ns
		$f_{sys} = 256f_s$; normal speed	81.3	88.6	156	ns
		$f_{sys} = 128f_s$; double speed	81.3	88.6	156	ns
t_{CWL}	f_{sys} LOW level pulse width		22	–	–	ns
t_{CWH}	f_{sys} HIGH level pulse width		22	–	–	ns
Serial input data timing (see Fig.8)						
f_s	word select input audio sample frequency	normal speed	25	44.1	48	kHz
		double speed	50	88.2	96	kHz
f_{BCK}	clock input frequency (data input rate)	$f_{sys} = 384f_s$; normal speed; note 1	–	–	$64f_s$	kHz
		$f_{sys} = 192f_s$; double speed; note 1	–	–	$64f_s$	kHz
		$f_{sys} = 256f_s$; normal speed	–	–	$64f_s$	kHz
		$f_{sys} = 128f_s$; double speed; note 2	–	–	$48f_s$	kHz
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
t_H	bit clock HIGH time		55	–	–	ns
t_L	bit clock LOW time		55	–	–	ns
t_{su}	data set-up time		20	–	–	ns
t_h	data hold time		10	–	–	ns
t_{suWS}	word select set-up time		20	–	–	ns
t_{hWS}	word select hold time		10	–	–	ns
Microcontroller interface timing (see Fig.9)						
t_L	input LOW time		2	–	–	µs
t_H	Input HIGH time		2	–	–	µs
t_{suDC}	set-up time DATA to CLOCK		1	–	–	µs
t_{hCD}	hold time CLOCK to DATA		1	–	–	µs
t_{suCR}	set-up time CLOCK to RAB		1	–	–	µs

Notes

1. A clock frequency of up to $96f_s$ is possible in the event of a rising edge of BCK occurring during SYSCLK = LOW.
2. A clock frequency of up to $64f_s$ is possible in the event of a rising edge of BCK occurring during SYSCLK = LOW.

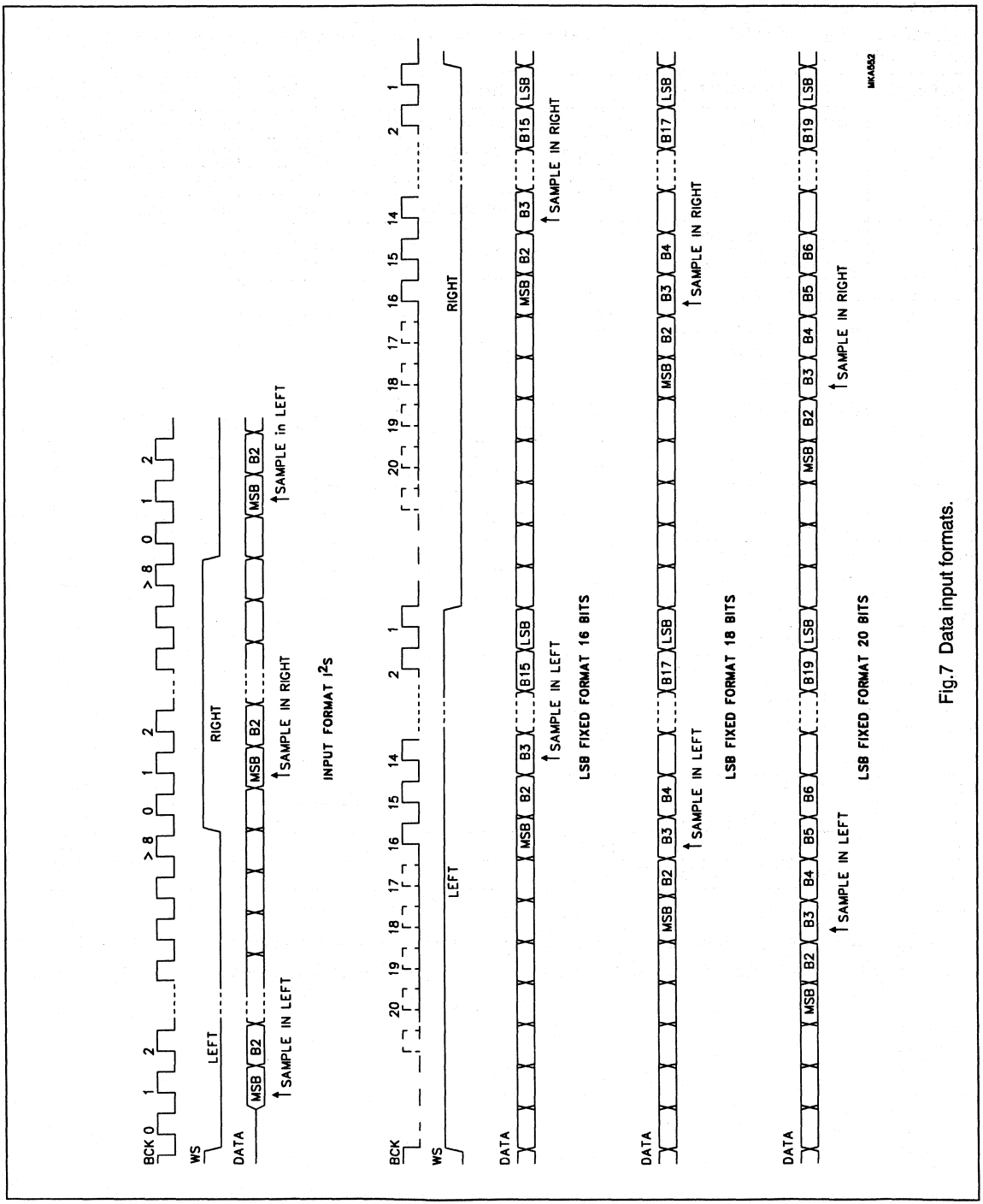


Fig.7 Data input formats.

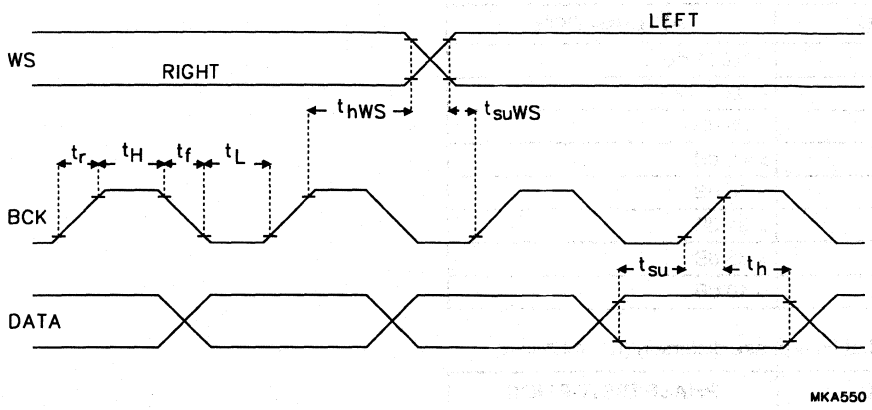


Fig.8 Timing of input signals.

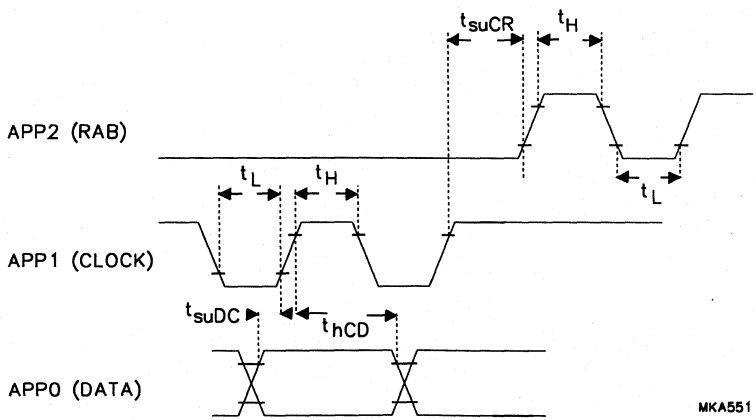


Fig.9 Microcontroller timing.

TEST AND APPLICATION INFORMATION

Filter characteristics

Table 4 Digital filter specification (f_s = 44.1 kHz).

BAND	ATTENUATION
0 to 19 kHz	< 0.001 dB
19 to 20 kHz	< 0.03 dB
24 kHz	> 25 dB
25 to 35 kHz	> 40 dB
35 to 64 kHz	> 50 dB
64 to 68 kHz	> 31 dB
68 kHz	> 35 dB
69 to 88 kHz	> 40 dB

Table 5 Digital filter phase distortion (f_s = 44.1 kHz).

BAND	PHASE DISTORTION
0 to 16 kHz	< ±1°

High-performance bitstream digital filter TDA1307

FEATURES

- Multiple format input: I²S, Sony 16, 18 and 20-bit
- 8-sample interpolation error concealment
- Digital mute, attenuation −12 dB
- Digital audio output function (biphase-mark encoded) according to IEC958
- Digital silence detection (output)
- Digital de-emphasis (selectable, FS-programmable)
- 8 x oversampling finite impulse response (FIR) filter
- DC-canceling filter (selectable)
- Peak detection (continuous) and readout to microprocessor
- Fade function: sophisticated volume control
- Selectable 3rd/4th order noise shaping
- Selectable dither generation and automatic scaling
- Dedicated TDA1547 1-bit output
- Differential mode bitstream: complementary data outputs available
- Simple 3-line serial microprocessor command interface
- Flexible system clock oscillator circuitry
- Power-on reset
- Standby function
- SDIL 42-pin package.

QUICK REFERENCE DATA

Voltages are referenced to V_{SS} (ground = 0 V); All V_{SS} and all V_{DD} connections should be connected externally to the same supply.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DDC1,2,3}$	supply voltage (pins 21, 41 and 8)		4.5	5.0	5.5	V
V_{DDOSC}	supply voltage (pin 24)		4.5	5.0	5.5	V
V_{DDAR}	supply voltage (pin 32)		4.5	5.0	5.5	V
V_{DDAL}	supply voltage (pin 29)		4.5	5.0	5.5	V
$I_{DDC1,2,3}$	supply current (pins 21, 41 and 8)	V_{DD} = 5 V	–	tbf	–	mA
I_{DDOSC}	supply current (pin 24)	V_{DD} = 5 V	–	tbf	–	mA
I_{DDAR}	supply current (pin 32)	V_{DD} = 5 V	–	tbf	–	mA
I_{DDAL}	supply current (pin 29)	V_{DD} = 5 V	–	tbf	–	mA
f_{XTAL}	oscillator clock frequency		–	33.8688	–	MHz
T_{amb}	operating ambient temperature		−20	–	+70	°C
P_{tot}	total power consumption		–	400	–	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1307	42	SDIL	plastic	SOT270AG

High-performance bitstream digital filter TDA1307

GENERAL DESCRIPTION

The TDA1307 is an advanced oversampling digital filter employing bitstream conversion technology, which has been designed for use in premium performance digital audio applications. Audio data is input to the TDA1307 through its multiple-format interface. Any of the four formats (I^2S, Sony 16, 18 or 20-bit) are acceptable. By using a highly accurate audio data processing structure, including 8 times oversampling digital filtering and up to 4th order noise shaping, a high quality bitstream is produced which, when used in the recommended combination with the TDA1547 bitstream DAC, provides the optimum in dynamic range and signal-to-noise performance. With the TDA1307, a high degree of versatility is achieved by a multitude of functional features and their easy accessibility; error concealment functions, audio peak data information and an advanced patented digital fade function are accessible through a simple microprocessor command interface, which also provides access to various integrated system settings and functions.

TDA1307 plus TDA1547 high-performance bitstream digital filter plus DAC combination:
For many features:

- Highly accessible structure
- Intelligent audio data processing

For optimum performance:

- 4th order noise shaping
- Improvement dynamic range (113 dB)
- Improvement signal-to-noise (115 dB)

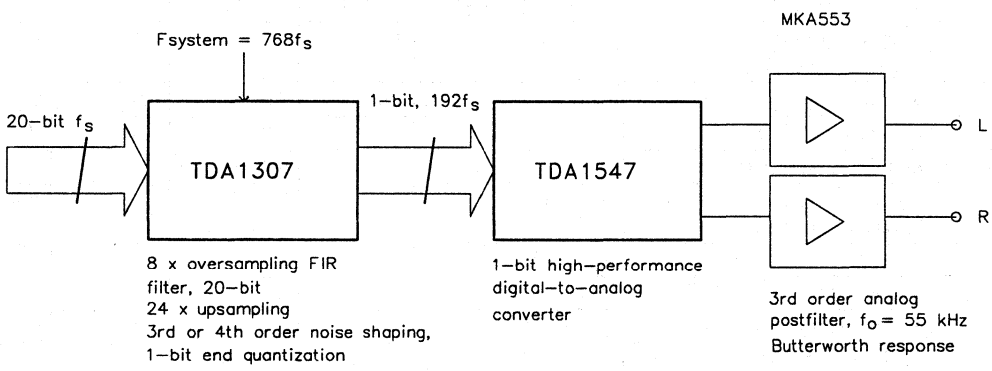


Fig.1 High performance bitstream reconstruction system.

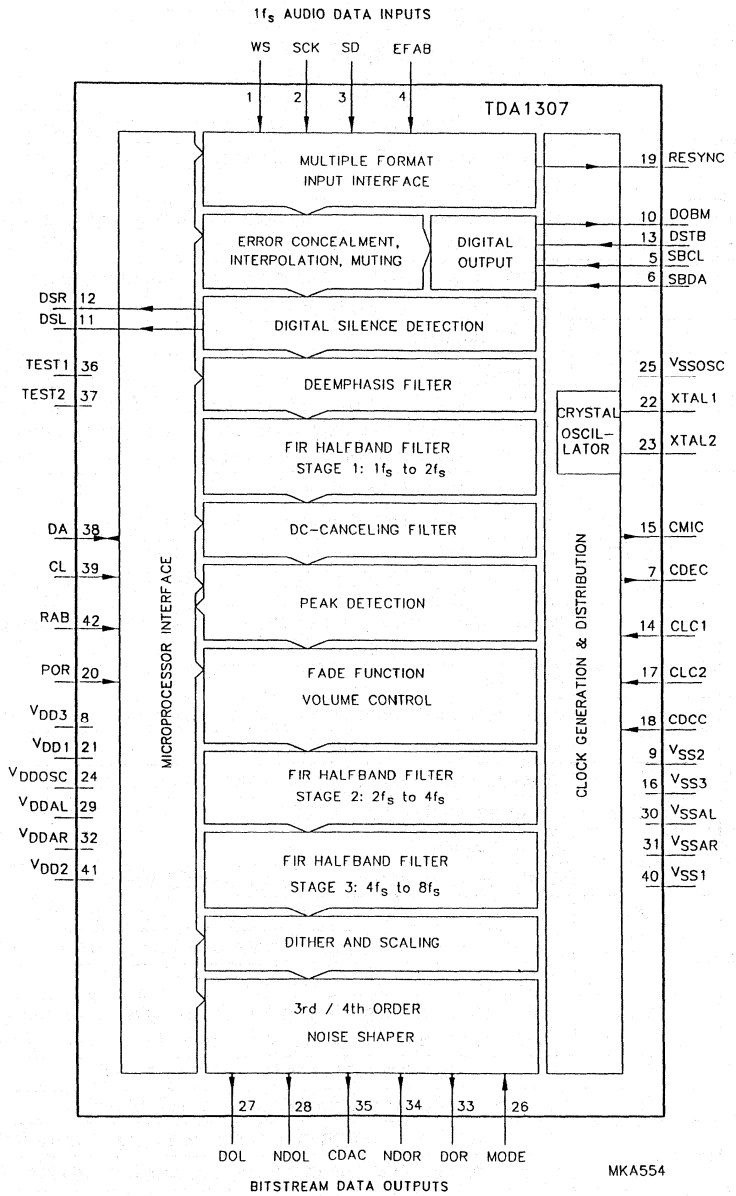


Fig.2 Block diagram.

PINNING

SYMBOL	PIN	TYPE, I/O	DESCRIPTION
WS	1	I	word select input to data interface
SCK	2	I	clock input to data interface
SD	3	I	data input to interface
EFAB	4	I; note 1	error flag: (active HIGH) input from decoder chip indicating unreliable data
SBCL	5	I	subcode clock: a 10-bit burst clock (typ. 2.8224 MHz) input which synchronizes the subcode data
SBDA	6	I	subcode data: a 10-bit burst of data, including flags and sync bits, serially input once per frame, clocked by burst clock input SBCL
CDEC	7	O	decoder clock output: frequency division programmable by means of pins 14 (CLC1) and 17 (CLC2) to output 192, 256, 384 or 768 times f_s
V_{DD3}	8		positive supply 3
V_{SS2}	9		ground 2
DOBM	10	O	digital audio output: this output contains digital audio samples which have received interpolation, attenuation and muting plus subcode data. Transmission is in biphase-mark code.
DSL	11	O	digital silence detected (active LOW) on left channel
DSR	12	O	digital silence detected (active LOW) on right channel
DSTB	13	I, note 2	DOBM standby mode enforce pin (active HIGH)
CLC1	14	I	application mode programming pin for CDEC (pin 7) frequency division
CMIC	15	O	clock output, provided to be used as running clock by microprocessor (in master mode only), output $96f_s$
V_{SS3}	16		ground 3
CLC2	17	I	application mode programming pin for CDEC (pin 7) frequency division
CDCC	18	I	master / slave mode selection pin
RESYNC	19	O	resynchronization: out-of-lock indication from data input section (active HIGH)
POR	20	I, note 2	power-on reset (active LOW)
V_{DD1}	21		supply voltage 1
XTAL1	22	I	crystal oscillator terminal: local crystal oscillator sense
XTAL2	23	O	crystal oscillator output: drive output to crystal or forced input in slave mode
V_{DDOSC}	24		positive supply connection to crystal oscillator circuitry
V_{SSOSC}	25		ground connection to crystal oscillator circuitry
MODE	26	I, note 2	evaluation mode programming pin (active LOW); in normal operation, this pin should be left open-circuit or connected to the positive supply
DOL	27	O	data output left channel to bitstream DAC TDA1547
NDOL	28	O	complementary data output left channel to TDA1547
V_{DDAL}	29		positive supply connection to output data driving circuitry, left channel
V_{SSAL}	30		ground connection to output data driving circuitry, left channel
V_{SSAR}	31		ground connection to output data driving circuitry, right channel
V_{DDAR}	32		positive supply connection to output data driving circuitry, right channel
DOR	33	O	data output right channel to TDA1547

SYMBOL	PIN	TYPE, I/O	DESCRIPTION
NDOR	34	O	complementary data output right channel to TDA1547
CDAC	35	O	clock output to bitstream DAC TDA1547
TEST1	36	I, note 1	test mode input. In normal operation this pin should be connected to ground
TEST2	37	I, note 1	test mode input. In normal operation this pin should be connected to ground
DA	38	I/O, note 2	bidirectional data line intended for control data from the microprocessor and peak data from the TDA1307
CL	39	I, note 2	clock input, to be generated by the microprocessor
V_{SS1}	40		ground 1
V_{DD2}	41		supply voltage 2
RAB	42	I, note 2	command / peak data request line

Notes

1. These pins are configured as internal pull-down.
2. These pins are configured as internal pull-up.

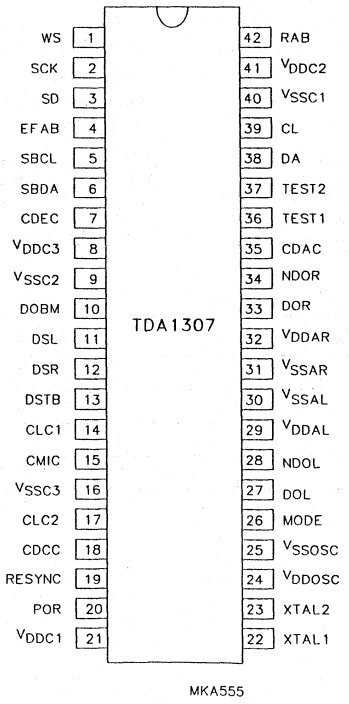


Fig.3 Pin configuration.

FUNCTIONAL DESCRIPTION

In the block diagram, Fig.1, a general subdivision into three main functional sections is illustrated. The actual signal processing takes place in the central sequence of blocks, a representation of the audio data path from top to bottom. The two blocks named Microprocessor Interface and Clock Generation and Distribution fulfil a general auxiliary function to the audio data processing path. The Microprocessor Interface provides access to all the blocks in the audio path that require or allow for configuration or selection, and manipulates data read-out from the Peak Detection block, all via a simple three-line interface. The Clock Generation and Distribution section, driven either by its integrated oscillator circuit with external crystal or by an externally provided master clock, provides the data processing blocks with timebases, manages the system mode dependent frequency settings, and conveniently generates clocks for external use by the system decoder IC and microprocessor. Following are detailed explanations of the functions of each block in the audio data processing path and their setting options manipulated by the microprocessor interface, the use of the microprocessor interface, and the functions of the clock section with its various system settings.

Clock generation and distribution

The clock generation section of the TDA1307 is designed to accommodate two main modes. The master mode, in which the TDA1307 is the master in the digital audio system, and for which the clock is generated by connecting a crystal of $768f_s$ (= 33.8688 MHz) to the crystal oscillator pins XTAL1 (pin 22) and XTAL2 (pin 23); and the slave mode, in which the TDA1307 is supplied a clock by the IC in the system that acts as the master (eg the digital audio interface receiver). In this event a clock signal frequency of $256f_s$ is input to pin XTAL2. Master or slave mode is programmed by means of pin CDCC (pin 18) logic 1 for master and logic 0 for slave mode. The circuit diagram of Fig.4 shows the typical connection of the external oscillator circuitry and crystal resonator for master mode operation. Note that the positive supply V_{DDOSC} is the reference to the oscillator circuitry. The LC network is used for suppression of the fundamental frequency component of the overtone crystal. Figure 5 shows how to connect for slave mode operation. A clock frequency of typical $256f_s$ and levels of 0 V/+5 V is input to XTAL1 via AC coupling (100 pF). The 10 kΩ resistor and the 10 nF capacitor are required to provide the necessary biasing for XTAL1 by filtering and feeding back the output signal of XTAL2.

Besides generating all necessary internal clocks for the audio data processing blocks and the clock to the DAC, the clock generation block further provides two clocks for external use when operating in master mode. Pin CDEC (pin 7), is used as the running clock for the system decoder IC, and pin CMIC (pin 15) is used as the running clock for the system microprocessor. CMIC outputs, by a fixed divider ratio to XTAL2, a clock signal at $96f_s$. For CDEC the divider ratio is programmable by means of pins CLC1 (pin 14) and CLC2 (pin 17). Table 1 gives the clock divider programming relationships.

Table 1 Clock divider programming.

CLC1	CLC2	CDEC OUTPUT FREQUENCY
0	0	$256f_s$
0	1	$384f_s$
1	0	$768f_s$
1	1	$192f_s$

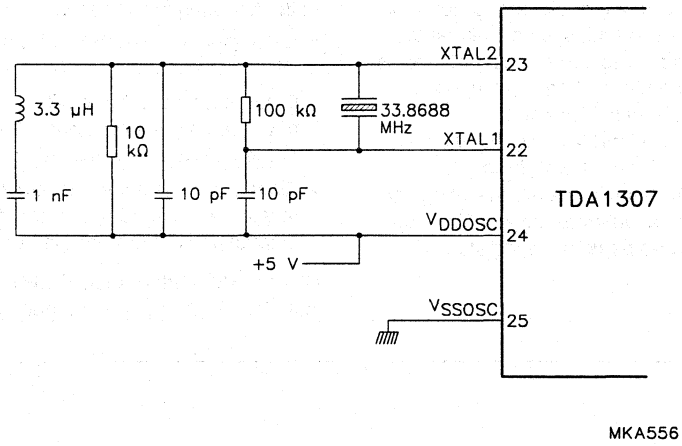


Fig.4 External crystal oscillator circuit.

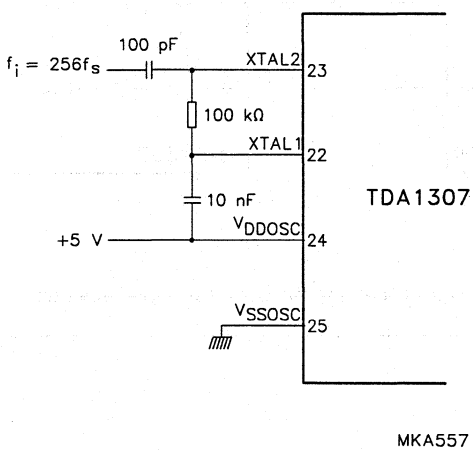


Fig.5 External clock input connections.

Microprocessor interface

The microprocessor interface provides access to virtually all of the functional blocks in the audio data processing section. Its destination is two-fold: system constants (such as input format and sample frequency) as well as system variables (attenuation, muting, de-emphasis, volume control data etc.) can be "written to" the respective blocks (command mode), and continuously collected stereo peak data "read from" the peak detection block (peak request). The system settings are stored in the TDA1307 in an internal register file. Peak data is read from the stereo peak value register.

THREE-LINE MICROPROCESSOR INTERFACE BUS

Communication is realized by a three-line bus, consisting of the following signals (see Fig.6):

- Clock input CL (pin 39), to be generated by the microprocessor,
- Command/request input RAB (pin 42), by which either of the two mode commands (RAB = 0) and peak request (RAB = 1) are invoked,
- Bidirectional data line DA (pin 38), which either receives command data from the microprocessor or outputs peak data from the peak detection block.

CL and RAB both default HIGH by internal pull-up, DATA is 3-state (high impedance, pull-up, pull-down).

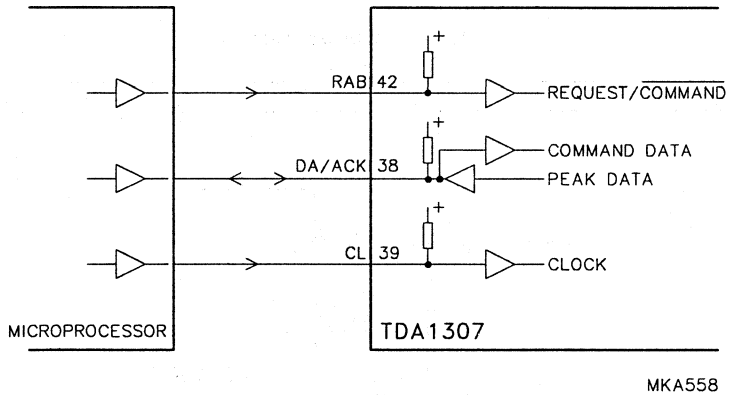


Fig.6 Three-line microprocessor interface bus.

INITIALIZATION OF THE BUS RECEIVER

The microprocessor interface section is initialized automatically by the power-on reset function, POR (pin 20). A LOW input on POR will initiate the reset procedure, which encompasses a functional reset plus setting of the initial states of the control words in the command register file. A wait time of at least one audio sample time after a LOW-to-HIGH transition of POR must be observed before communication can successfully be established between the TDA1307 and the microprocessor. In addition to the POR function, a software reset function issued from the microprocessor is provided (see section Organization and programming of the internal register file), which has the sole function of reinstating the initial values of the microprocessor control register. More information on initializing the TDA1307 can be found under Application information.

COMMAND PROTOCOL

The protocol for writing data to the TDA1307 is illustrated in Fig.7. The command mode is invoked by forcing RAB LOW. A unit command is given in the form of an 8-bit burst on the DA line, clocked on the rising edge of CL. The command consists of 4 address bits followed by 4 control data bits (both MSB first). A next command may be immediately issued while keeping RAB forced LOW. Only commands for which the MSB of the address bits is LOW are accepted; of the remaining set of addresses, only four have meaning (see section Organization and programming of the internal register file). The command input receiver is provided with a built-in protection against erroneous command transfer due to spikes, by a 2-bit debounce mechanism on lines DA and CL. The waveforms on these lines are sampled by the receiver at the internal system clock rate $256f_s$. A state transition on DA or CL is accepted only when the new state perseveres for two consecutive sampled waveform instants.

ORGANIZATION AND PROGRAMMING OF THE INTERNAL REGISTER FILE

Command data received from the microprocessor is stored in an internal register file (see Table 2), which is organized as a page of 10 registers, each containing a 4-bit command data word (D3 to D0). Access to the words in the register file involves two controls: selection of the address of a set of registers (by means of A3, A2, A1 and A0) and setting the number of the bank in which the desired register is located (by means of the "bank bits", B0 and B1). First the desired bank is selected by programming the command word at address 00002 (supplying the bank bits plus refreshing bits ATT and DIM). A subsequent addressing (one of three addresses, 1H, 4H and 6H) will yield access to the register corresponding to the last set bank.

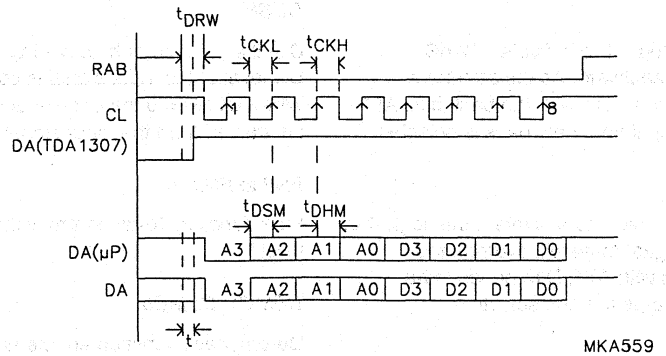


Fig.7 Microprocessor command protocol.

Table 2 Microprocessor control register file.

ADDRESS						D3	D2	D1	D0	INITIAL STATE
A3	A2	A1	A0	BANK						
				B0	B1					
0	0	0	0	X	X	BANK B0	BANK B1	ATT	DIM	0 0 1 1
0	0	0	1	0	1	FCON	DIT	FSS9	FSS8	0 0 0 0
				1	0	FSS7	FSS6	FSS5	FSS4	0 0 1 0
				1	1	FSS3	FSS2	FSS1	FSS0	1 0 0 0
0	1	0	0	0	1	DCEN	DCSH	FN9	FN8	0 1 1 1
				1	0	FN7	FN6	FN5	FN4	0 0 0 0
				1	1	FN3	FN2	FN1	FN0	1 1 0 1
0	1	1	0	0	1	DEMC1	DEMC0	RES0	RES1	0 0 0 0
				1	0	INS1	INS0	FS1	FS0	0 0 0 0
				1	1	RES2	NS	RST	STBY	1 0 0 0

Following is a list of the programming values for the various control words in the register file. Information on the meaning of the different controls can be found under the sections covering the corresponding signal processing blocks (see sections 'Multiple format input interface' to 'Third and fourth order noise shaping').

BANK B0, BANK B1

Programming of the bank bits is given in Table 2. The bank bits can be changed by addressing register location '0000'. Subsequent addressing will result in access of locations according to the last selected bank.

ATT

Attenuation control bit: logic 1 to activate –12 dB attenuation, logic 0 to deactivate. As the attenuate control bit shares a control word with the bank bits, ATT has to be refreshed each time a new bank is selected.

DIM

Digital mute control bit: logic 1 to activate mute, logic 0 to deactivate. An active digital mute will override the attenuation function. As with ATT, DIM needs to be refreshed with each change in bank selection.

FCON

Fade function control bit: logic 1 to activate the fade function, logic 0 to deactivate.

DIT

Dither control bit: logic 1 to activate dither addition, logic 0 deactivates.

FSS9 to FSS0

Fade function 10-bit control value to program fade speed, in number of samples per fade step.

DCEN

DC-filter enable bit: logic 1 enables subtraction of the DC-level from the input signal, logic 0 disables.

DCSH

DC-filter sample or hold control bit: When DCSH = 1 the DC-level of the input signal is continuously evaluated. When DCSH = 0 the once acquired DC value, to be subtracted from the input signal, is held constant.

FN9 to FN0

Fade function 10-bit control value to program volume level.

DEMC1, DEMC0

De-emphasis function enable and f_s selection bits.

Table 3 De-emphasis mode programming.

DEMC1	DEMC0	DEEMPHASIS FUNCTION
0	0	de-emphasis disabled
0	1	de-emphasis for f_s = 32.0 kHz
1	0	de-emphasis for f_s = 44.1 kHz
1	1	de-emphasis for f_s = 48.0 kHz

Table 4 Input format programming.

INS1	INS0	INPUT FORMAT
0	0	I²S up to 20 bits
0	1	Sony format 16 bits
1	0	Sony format 18 bits
1	1	Sony format 20 bits

Table 5 Sample frequency indication programming.

FS1	FS0	DOBM SAMPLE FREQUENCY INDICATION
0	0	f_s = 44.1 kHz
0	1	f_s = 48.0 kHz
1	0	no meaning
1	1	f_s = 32.0 kHz

RES2 to RES0

These are reserved locations and have no functional meaning in the TDA1307.

INS1, INS0

Input format selection control bits.

FS1, FS0

Sample frequency indication control bits for the digital output section.

NS

Control bit for Noise Shaper section. When NS = 1, 3rd order noise shaping is selected, when NS = 0, 4th order noise shaping is selected.

RST

Software reset function. When RST = 1 the contents of the microprocessor control registers will be immediately preset to their initial values as shown in Table 2. As part of this reset action, bit RST is automatically returned to its initial state 0, that being normal operation.

STBY

Standby mode control bit: When STBY = 1 the standby mode will be initiated (explained under the section treating the Digital Output block). STBY = 0 for normal activity.

PEAK DATA OUTPUT PROTOCOL

The peak data read-out protocol is illustrated in Fig.8. A peak request is performed by releasing RAB (which will be pulled HIGH by TDA1307) while CL = HIGH, and maintaining RAB = 1 throughout the peak data transmission. TDA1307 will acknowledge the peak request by returning a LOW state on the DA line. Upon this peak acknowledge, the microprocessor may commence collecting data from the internal peak data output register (16-bit Left, 16-bit Right channel peak data) by sending a clock onto the CL line. The contents of the peak data output register will not change during the peak request. The first peak bit, the MSB of the Left channel peak value, is output upon the first LOW-to-HIGH transition of CL. To access Right channel peak value, all 16 bits of channel Left have to be read out, after which up to 16 bits of Right channel peak data may be read out. The peak data readout procedure may be aborted at any instant by returning RAB LOW, marking the end of the peak request: the internal peak register will be reset and the peak detector will start collecting new peak data and transferring this to the peak data output register.

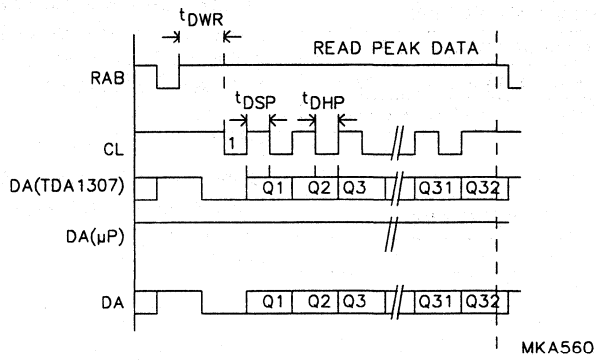


Fig.8 Peak data output protocol.

Multiple format input interface

Data input to the TDA1307 is accepted in four possible formats, I²S (with word lengths of up to 20 bits), and Sony formats of word lengths 16, 18 and 20-bit. The general appearance of the allowed formats is given in Fig.9. The selection of a format is achieved through programming of the appropriate bits in the microprocessor register file. Characteristic timing for the input interface is given in the diagram of Fig.10.

SYNCHRONIZATION

For correct data input to reach the central controller of TDA1307, synchronization needs to be achieved to the incoming $1f_s$ I²S or Sony format input signals. The incoming WS signal is sampled to detect whether its phase transitions occur at the correct synchronous timing instants. This sampling occurs at the TDA1307 internal clock rate, $256f_s$. After one phase transition of WS, the next is expected after a fixed delay, otherwise the condition is regarded as out-of-lock and a reset is performed, this operation is repeated until synchronization is achieved. To allow for slight disturbances causing unnecessary frequent resets, the critical WS transitions are expected within a tolerance window (–4 to +4 periods of the $256f_s$ internal sampling clock instants). The reset action is flagged on the RESYNC (pin 19) output, which may be optionally used for muting or related purposes. RESYNC becomes HIGH the instant a reset is initiated, and remains in that state for at least one sample period ($1/f_s$).

ERROR FLAG INPUT EFAB

The error flag input EFAB (pin 4) is intended as request line from the system decoder to the digital filter to indicate erroneous audio samples requiring concealment. A detected HIGH on input EFAB will be relayed by the input interface block to the error concealment block, where the samples flagged as erroneous will be processed accordingly.

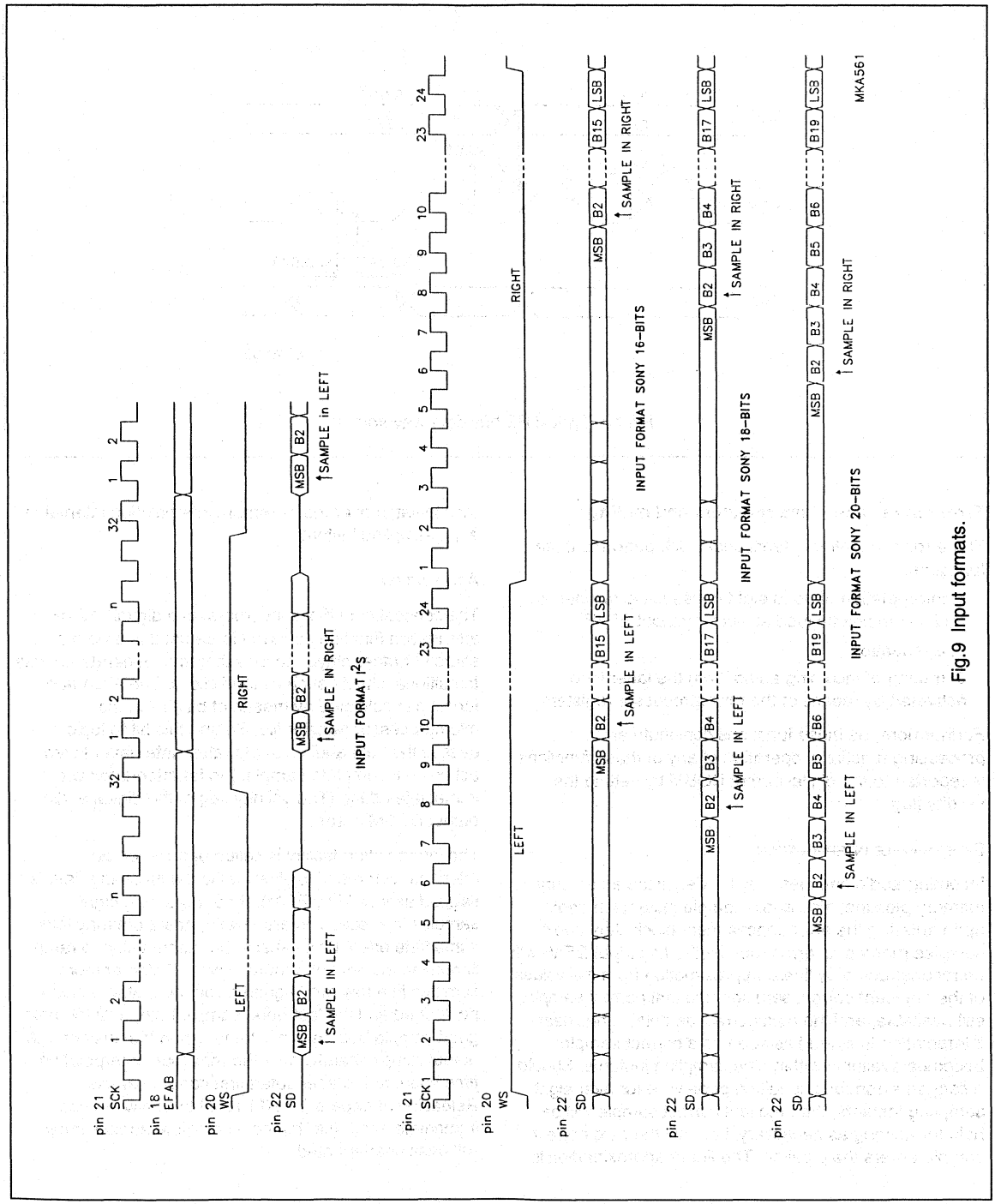


Fig.9 Input formats.

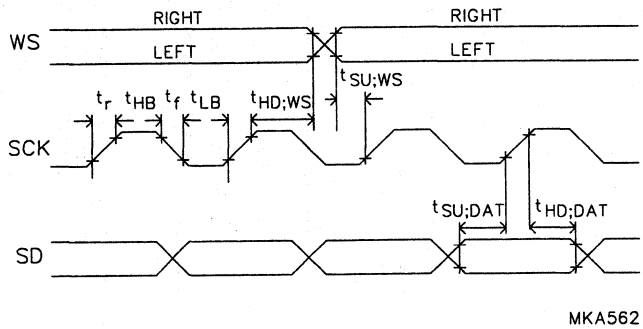


Fig.10 Typical I²S-bus data waveforms.

Error concealment, interpolation and muting

The error concealment functional block performs three functions:

1. interpolation of up to eight consecutive erroneous audio samples flagged as such by input EFAB
2. attenuation
3. muting of incoming audio, both the latter if so activated by means of the microprocessor registers.

Furthermore, as these functions constitute error processing functions, operation of any of these functions is reported to the digital output DOBM by setting the validity flag.

EIGHT-SAMPLE INTERPOLATION

Incoming audio samples may be visualized as entering a memory pipeline, nine audio sample instants in depth, upon entering the error concealment block. Any audio samples marked as erroneous by the flag input EFAB will be reconstructed by linear approximation from the values of the adjacent correct samples (the last correct sample still available, and the next correct sample). The linear interpolation is started as soon as a correct sample becomes available within nine sampling instants. Should a flagged erroneous condition persevere for over eight sampling instants, then the last correct sample will be held for as long as necessary, i.e. until the next correct sample enters the pipeline. The linear approximation is then initiated over the maximum interpolation interval of eight sampling instants.

ATTENUATION

The concealment block incorporates a digital −12 dB attenuation function intended to be used in program search or other player actions that may generate audible transitional effects such as loud clicks. The attenuate function is activated by means of bit ATT in the microprocessor register file. Setting this bit to logic 1 causes the next audio sample (attenuate never takes action on incomplete samples) to be attenuated with immediate effect. (The validity flag of the digital audio output DOBM is set.)

The interpolation facility is called upon when an attenuate command is given while the incoming data is flagged as invalid by EFAB. If no more than eight samples in succession are invalid, attenuate may take immediate effect (this causes the output value to ramp linearly to the final attenuated level). If nine or more samples in a row are flagged erroneous, attenuation is postponed and the last good sample held, until the next good sample becomes available. Upon that instant, the output ramps linearly, over the maximum interpolation time span, to the attenuated first correct sample. Releasing attenuate (bit ATT reset to 0) always has immediate effect (i.e. the next complete audio sample will pass unattenuated).

MUTING

The digital mute of the error concealment block immediately (i.e. on the next whole audio sample) sets the input to the digital filter to all zeros, regardless of any other current action in the error concealment block. The digital mute function is activated by means of bit DIM in the microprocessor register file. Setting this bit to logic 1 causes the next audio sample to be muted. (The validity flag of the digital audio output DOBM is set.)

Releasing the digital mute function (resetting bit DIM to 0) will cause the output of the error concealment block to approach the unaffected audio sample value by linear approximation, on the condition that the mute action spanned at least 8 consecutive audio samples. If there are samples in error at the time of releasing mute, the release action is postponed until good data becomes available, after which the linear ramp can be made over the maximum interpolation time span.

Digital output (DOBM)

The DOBM block constructs a biphase modulated digital audio output signal which complies to the IEC standard 958, to be used as a digital transmission link between digital audio systems. A variety of inputs are combined, arranged and modulated to finally form the output biphase-mark sequence. The inputs are the following:

- left and right audio data, word length 20-bit, as delivered by the error concealment block
- the Validity flag as output by the error concealment block
- subcode information, as acquired by input via pins SBDA (pin 6) and SBCL (pin 5)
- sampling frequency information as set by means of bits FS1 and FS0 in the microprocessor register file

As the digital output function is not always required, and can give rise to interference problems in high-quality audio conversion systems, the DOBM output can be switched ON or OFF by means of pin DSTB (digital output standby, 13). Leaving DSTB open-circuit will cause it to pull HIGH and deactivate the DOBM output; tying DSTB LOW enables the digital output function.

The programming of bits FS1 and FS0 is specified in Table 5 under section 'Microprocessor interface'. The DOBM block of TDA1307 translates the settings of these bits to the appropriate corresponding information in the digital audio output sequence (as specified by IEC 958).

The inputs SBDA (subcode data, 6) and SBCL (subcode clock, 5) allow for the merging of subcode data into the output DOBM signal. The input sequence via these inputs is defined as 10-bit burst words, arranged as illustrated in Fig.11; the bit nomenclature corresponds to that used in the IEC standard 958. Both subcode data and clock signals are normally supplied by the decoder of the digital audio system (e.g. SAA7310).

For set-up and hold timing of the SBDA and SBCL inputs, restrictions identical to the audio data inputs are valid.

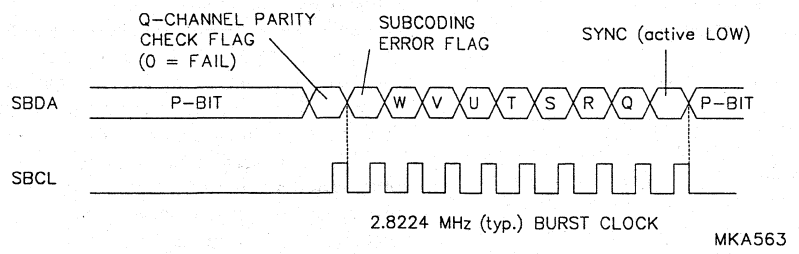


Fig.11 Format of subcode data input.

Digital silence detection

The TDA1307 is designed to detect digital silence conditions in channels left and right, separately, and report this via two separate output pins, one for each channel, DSL (pin 11) and DSR (pin 12). This function is implemented to allow for external manipulation of the audio signal upon absence of program material, such as muting or recorder control. The TDA1307 itself does not influence the audio signal as a result of digital silence; the sole function of this block is detection, and any further treatment must be accomplished externally.

An active LOW output is produced at these pins if the corresponding channel carries either all zeroes for at least 8820 consecutive audio samples (= 200 ms for f_s = 44.1 kHz).

The digital silence detection block receives its left and right audio data from the error concealment block (implying that a digital mute action will produce detection of a digital silence condition), and passes it unaffected to the next signal processing stage, the de-emphasis block.

De-emphasis filter

The TDA1307 incorporates selectable digital de-emphasis filters, dimensioned to produce, with extreme accuracy, the de-emphasis frequency characteristics for each of the three possible sample rates 32, 44.1 and 48 kHz. As a 20-bit dynamic range is maintained throughout the filter, considerable margin is kept with respect to the normal CD resolution of 16-bit i.e. the digital de-emphasis of TDA1307 is a truly valid alternative to analog de-emphasis in high-performance digital audio systems.

Selection of the de-emphasis filters is performed via the microprocessor interface, bits DEMC1 and DEMC0, for which the programming is given in Table 3.

Oversampling digital filter

The oversampling digital filter in the digital audio reconstruction system is of paramount influence to the fidelity of signal reproduction. Not only must the filter deliver a desired stop-band suppression while sustaining a certain tolerated pass-band ripple, but it must also be capable of faithfully reproducing signals of high energy content, such as signals of high level and frequency, squarewave-type signals and impulse-like signals. (All of these examples have their counterparts in actual music program material). Filters optimized only towards pass-band ripple and stop-band suppression are capable of entering states of overload because of the clustered energy content of these signals, thus introducing audible degradations in processing the mentioned types of excitations. To dimension a high-fidelity digital filter, a balance must be established between filter steepness and overload susceptibility.

The oversampling digital filter function in the TDA1307 is designed, in combination with the noise shaper, to deliver the highest fidelity in signal reproduction possible. Not only are stop-band suppression and pass-band ripple parameters to the design, but also the prevention of detrimental artifacts of too extreme filtering: impulse and high-level overload responses. The outcome is a patented design excelling in natural response to most conceivable audio stimuli. It is realized as a series of three half-band filters, each oversampling by a ratio of two, thus achieving an eight times oversampled and interpolated data output to be input to the noise shaper. Each stage has a finite impulse response with symmetrical coefficients, which makes for a linear phase response. Filter stages 1, 2 and 3 incorporate 119, 19 and 11 delay taps respectively. To maintain an output accuracy of 20 bits, an internal data path word length of 39 bits is used to supply the required headroom in multiplications. Requantization back to 20-bit word length is performed by noise shaping (thus effectively preventing rounding errors because they have effect in the audio frequency band), at the output of each filter section.

The successive half-band filter stages are, for efficiency, distributed over the audio data processing path: DC-filtering, peak value reading and volume control are performed between stages 1 and 2 (the $2f_s$ domain).

DC-canceling filter

A mechanism for optionally eliminating potential DC content of incoming audio data is implemented in the TDA1307 for three main reasons. Most importantly because it is called for by the implementation of volume control in the TDA1307. An audio signal that is to be subjected to volume control (= multiplication by a controlled attenuation factor) should be free of offset, otherwise the controlled multiplication will produce the undesired side effect of modulating the average DC content. The second reason is supplied by the implementation of audio peak data read-out in the TDA1307. As the peak value is obtained from the absolute value of the audio data referenced to zero DC level, its accuracy is impaired by the presence of residual DC information, progressively so for lower audio levels. The third reason is brought about by application of the

noise shaper. To optimize the dynamic behavior of the noise shaper especially for low-level signals, it is supplied a predefined offset, sometimes referred to as DC dither. Taking no precautions against DC content of the source audio data may render the DC dither potentially ineffective.

In applications where the DC content of the audio information may be expected, application of the selectable DC filter may be opted for. It is implemented as a first-order high-pass filter with a corner frequency of 2 Hz. Control of the DC filter is achieved by accessing the appropriate bits DCEN (DC filter enable) and DCSH (DC filter sample or hold) in the microprocessor register file. The principle of operation is illustrated in Fig.12. The output of the DC filter, referred to in the diagram as 'audio output' always equals the audio input subtracted by the output of the low-pass branch . Depending on the control bit DCSH, this subtraction value is either the last value held constant or a value continuously adapting to incoming DC content. The DC filter is effectively switched ON or OFF via control bit DCEN, which selects the input of the low-pass section either to be the audio input data (the output of the low-pass section will settle to the low frequency content of the audio data so that the filter is ON) or a preset value of zero (low-pass output will settle to zero meaning 'filter OFF). The constant mode is implemented to provide a mode in which a stable subtraction value is guaranteed; in this mode however the high-pass function is inhibited so there is no adaptation to changes in the DC content of the incoming source information.

Peak detection

The TDA1307 provides a convenient way to monitor the peak value of the audio data, for left and right channels individually, by way of read-out via the microprocessor interface. Peak value monitoring has its applications mainly in digital volume unit measurement and display, and in automatic recording level control. The peak level measurement of the TDA1307 occurs with a resolution of 16-bit, providing a dynamic range amply suitable for all practical applications.

The output of the peak detection block is a register of two 16-bit words, one for each channel, representing the absolute value of the accumulated peak value, accessible via the microprocessor interface. The peak detection block continuously monitors the audio information arriving from the DC-canceling filter, comparing its absolute value to the value currently stored in the peak register. Any new value greater than the currently held peak value will cause the register to assume the new, greater value. Upon a peak request (for which the protocol is described in section 'Peak data output protocol'), the contents of the peak register are transferred to the microprocessor interface. After a read action, the peak register will be reset, and the collection of new peak data started.

The peak detection block receives data that has been processed by the first half-band stage of the oversampling interpolating digital filter (in the $2f_s$ domain, but the peak detection 'samples' at $1f_s$ for efficiency). This means that the scaling applied in this first half-band

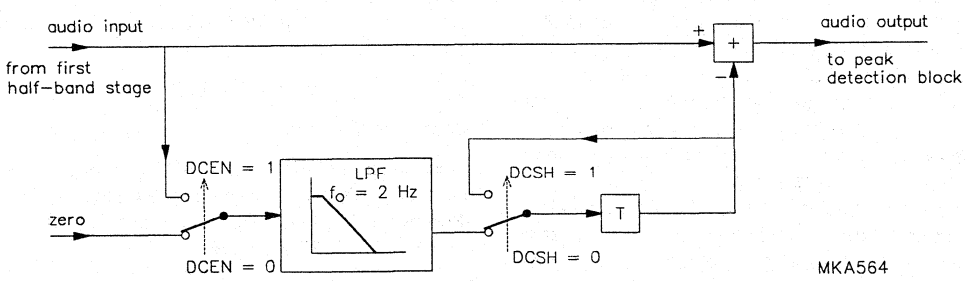


Fig.12 Schematic diagram of the DC filter.

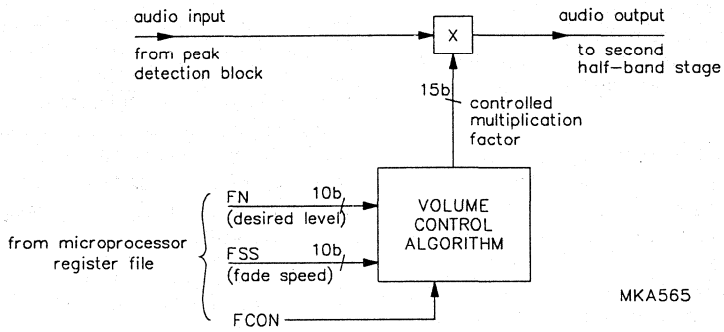


Fig.13 Schematic diagram of the volume control block.

stage is noticeable in the measured peak value. The frequency-independent attenuation factor of the first half-band filter equals 0.175 dB - this results in a possible range for the output peak value of 0 to 32114. When the audio signal may be expected to carry DC content, use of the DC canceling filter of TDA1307 is recommended, to ensure correct and accurate peak detection.

Fade function and volume control

One of the main features of TDA1307 is a patented, advanced digital volume control with inherent fading function, exhibiting an accuracy and smoothness unsurpassed in presently available digital filters. Only the desired volume and the fade speed need be instructed to the TDA1307, which can be realized in a single instruction via the microprocessor interface. The volume control function then autonomously performs automatic fade-in or fade-out to the desired volume by a natural, exponential approach. It allows for volume control to an accuracy of 0.1 dB over the range from 0 dB of full scale to beyond –100 dB. The speed of approach can be set over a wide range, varying from less than one second to over 23 seconds for a complete fade. Furthermore the fade algorithm manages the additional fading resolution, in excess of the 0.1 dB available for the volume desired level, needed to ensure gradual changes in volume at all times. Fig.13 illustrates the volume control block.

Three data entities in the microprocessor register file pertain to the volume control block: a 10-bit control value for the desired volume (bits FN9 to FN0), a 10-bit control value for the fade speed (bits FSS9 to FSS0), and the fade function override bit, FCON. The volume control word ranges from 0 (representing a desired volume level or 0 dB) to 1023 (representing maximum desired volume level of zero or $-\infty$ dB). For values 1 to 1023, an LSB change of the volume control word represents 0.1 dB change of volume level. In changing from one volume level to the next desired volume level, the volume control block calculates and applies intermediate volume levels according to an exponential approach curve. The speed at which the approach curve progresses is determined by the value of the fade speed control word, FSS. FSS + 2 is the amount of time delay applied, in units of audio sample instants, before a next value on the exponential curve is calculated and applied.

The total duration of an exponential fade operation is the product of the desired amount of volume change FN (in LSBs of the 10-bit control word) and the amount of delay per fade step FSS (in LSB times seconds), expressed as follows:

$$t_{fade,\ exp,\ total} = \Delta\ FN \times (FSS + 2) / f_s$$

Where f_s is the base-band sampling frequency.

Thus the longest fade time achievable, occurring in the event of maximum desired volume change $\Delta FN = 1023$, slowest speed setting FSS = 1023, and in the event that $f_s = 44.1$ kHz, is 23.7 seconds

To smooth out fast volume changes however, the TDA1307 fade function adds extra resolution to the volume control by gradually changing from one exponential step to the next, by a linear transition. Whereas the 10-bit FN-value could not accomplish discrete attenuation steps finer than 0.1dB, the linear

transitional approach enhances volume change resolution to 15-bit. The volume level therefore never changes faster than one LSB of the 15-bit attenuation factor per audio sample. As soon as the linear transition reaches the value determined by the exponential approach, the attenuation value remains stable until the next exponential value is due, which will again initially be approached linearly. For exponential fade speeds higher than the linear approach can follow, the approach remains linear unless the exponential approach curve is intersected. For fast volume decrease, the start of the approach will be linear, whereas for a fast volume increase, the course of the fade approach will be exponential at first, then saturating to linear.

The fastest fade speed, for large volume changes, is therefore determined by the linear approach. For a maximum volume change at maximum speed, follows a fade time of $(2^{15} - 1)/44100 = 0.74$ seconds.

For immediate return to the maximum volume level without altering the volume and fade speed settings, bit FCON in the register file can be used. With this bit set to 1, the fade function is active and operates as described above. Resetting FCON to 0 will immediately deactivate the fade function, that is, return the volume level to maximum at the start of the next audio sample. Changing state of FCON from 0 to 1 will cause a fade according to the current settings of volume and speed control words FN and FSS.

In Fig.14, a few fading examples illustrate the operation of the TDA1307 advanced digital volume control.

Dither and scaling

Prior to input to the noise shaper, final preprocessing is performed upon the eight times oversampled and interpolated audio data stream in the form of scaling and dither addition. The fixed scaling factor, a frequency-independent attenuation of 3 dB, is applied to the signal in order to provide the noise shaper with sufficient headroom. The application of dither is optional, selectable by means of bit DIT in the microprocessor register file.

With DIT set to 1, fixed dither levels of value $2^{-6} + 2^{-5}$ and $2^{-6} - 2^{-5}$ are added alternately to the audio signal, at an alternation rate of $4f_s$. This amounts to a combination of an AC dither signal of frequency $4f_s$ and amplitude −24 dB of full-scale, with a DC dither (offset) of 3.125% of full-scale peak amplitude. With DIT set to 0, no dithering, AC or DC, is performed.

Although the addition of dither is made selectable in the TDA1307, it is generally recommended for use always, as dither is essential to the accurate conversion of low-level signals and reproduction of silence conditions by noise-shaping circuits.

Third and fourth order noise shaping

The noise shaper constitutes the final audio processing stage of TDA1307, which takes the eight times oversampled and interpolated audio data stream from the digital filter as input, and by extreme oversampling and 1-bit end quantization processes the signal so that it can be converted to analog by a one-bit digital-to-analog converter. The order of the noise shaper is selectable, between 3rd and 4th order, by means of the register file bit NS (NS = 0: 3rd order, NS = 1: 4th order). Together with the final oversampling ratio, the noise shaper order determines the dynamic range (or accuracy) that the noise shaper can achieve. (The oversampling ratio will depend on the system clock frequency and application mode used.) Table 6 gives the dynamic range of the noise shaper as a function of these two parameters.

Figures 15 and 16 show noise spectral density simulations of the third and fourth order noise shaper respectively, with a stimulus frequency of 1 kHz at a level of −10 dB f_s, for 192 x 44.1 kHz oversampling. From the slope of the shaped noise spectrum outside the audio band, the order of noise shaping is apparent. It is important to note that, in contrast to normal fourth-order noise shaping, where an audio post-filter of equal order would be needed to compensate the slope of the quantization noise, the fourth-order noise shaper of the TDA1307 actually only needs third order post-filtering to obtain the same amount of stop-band suppression as with third order. The noise density of the fourth order noise shaper starts at a lower level for low frequencies, and only slightly exceeds the third-order curve in the 200 to 300 kHz region.

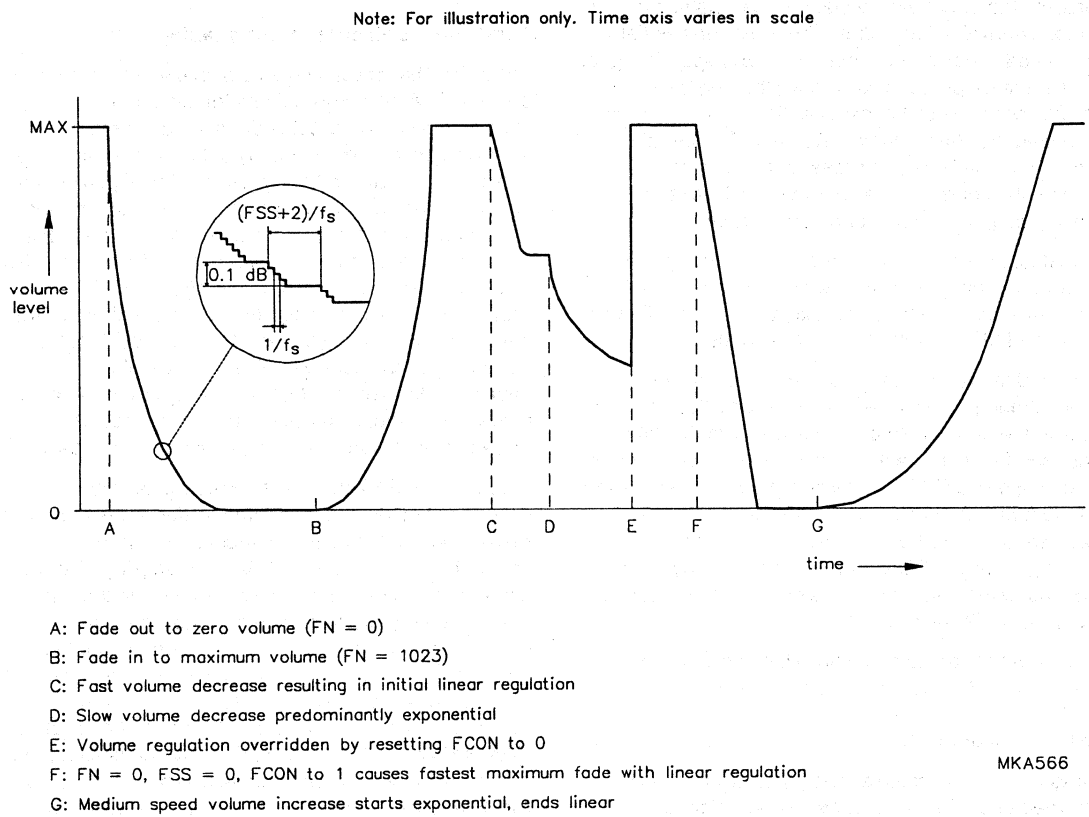


Fig.14 Volume control examples.

Table 6 Noise shaper dynamic range.

OVERSAMPLING/ORDER	3rd ORDER	4th ORDER
$128f_s$	105 dB	118 dB
$192f_s$	117 dB	134 dB

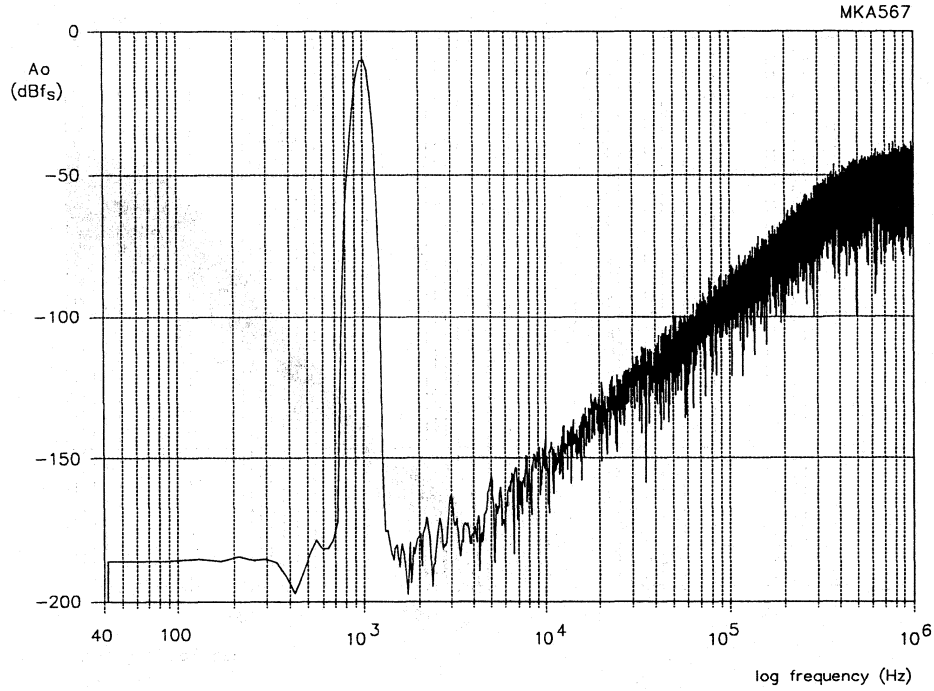


Fig.15 Noise shaper output spectrum (N = 3; $192f_s$).

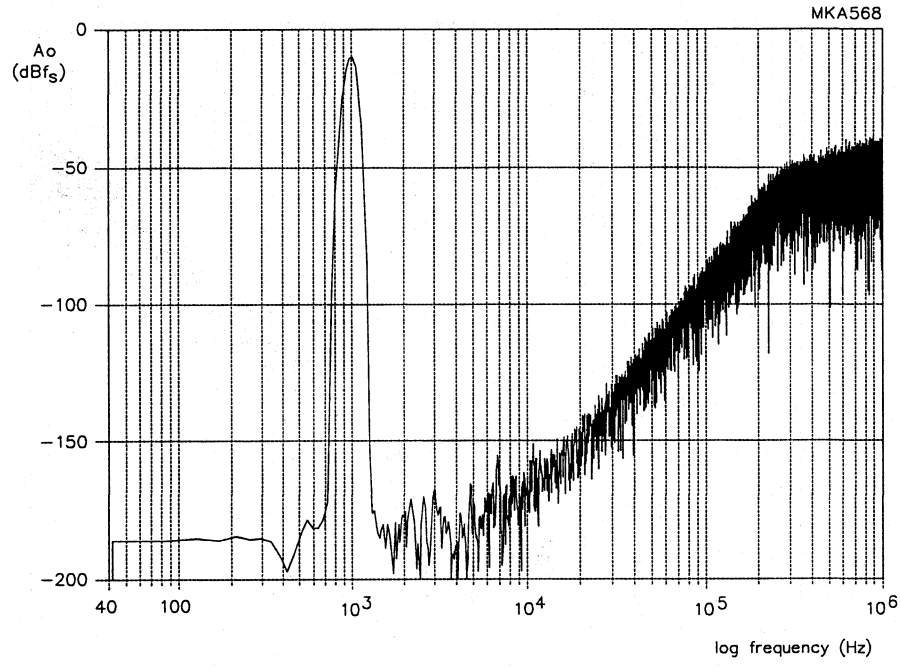


Fig.16 Noise shaper output spectrum (N = 4; $192f_s$).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltages (pins 8, 21, 24, 29, 32 and 41)		−0.5	+6.5	V
V_I	maximum input voltage	note 1	−0.5	V_{DD} + 0.5	V
I_{IK}	DC clamp input diode current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	–	±10	mA
I_{OK}	DC output clamp diode current; (output type. 4 mA)	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V	–	±20	mA
I_O	DC output source or sink current; (output type. 4 mA)	-0.5 V $< V_O < V_{DD} + 0.5$ V	–	±20	mA
I_{DD}, I_{SS}	DC V_{DD} or GND current per supply pin		–	±50	mA
$P_{O, cell}$	power dissipation per output (type. 4 mA)		–	50	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−20	+70	°C
V_{es}	electrostatic handling	100 pF; 1.5 kW	−2000	+2000	V

Note

1. Input voltage should not exceed 6.5 V.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	39 K/W

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −20 °C to +70 °C and oscillator frequency 33.8688 MHz unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{DDC1,2,3}$	supply voltage (pins 8, 21 and 41)		4.5	5.0	5.5	V
V_{DDOSC}	supply voltage (pin 24)		4.5	5.0	5.5	V
V_{DDAR}	supply voltage (pin 32)		4.5	5.0	5.5	V
V_{DDAL}	supply voltage (pin 29)		4.5	5.0	5.5	V
V_{diff}	maximum difference between supplies		–	–	tbf	V
$I_{DDC1,2,3}$	supply current (pins 8, 21 and 41)	V_{DD} = 5 V	–	tbf	–	mA
I_{DDOSC}	supply current (pin 24)	V_{DD} = 5 V	–	tbf	–	mA
I_{DDAR}	supply current (pin 32)	V_{DD} = 5 V	–	tbf	–	mA
I_{DDAL}	supply current (pin 29)	V_{DD} = 5 V	–	tbf	–	mA
Inputs						
CLC1, CLC2, EFAB, SCK, WS, SD, SBCL, DA, SBDA, CDCC, TEST1 and TEST2						
V_{IL}	LOW level input voltage	note 1	–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	note 1	$0.7V_{DD}$	–	–	V
I_{LI}	input leakage current	note 2	−1	–	+1	mA
R_I	input resistance	note 3	17	–	134	kΩ
C_I	input capacitance		–	–	10	pF
CL, RAB, POR, DSTB and MODE						
V_{IL}	LOW level input voltage	note 1	–	–	$0.2V_{DD}$	V
V_{IH}	HIGH level input voltage	note 1	$0.8V_{DD}$	–	–	V
R_I	input resistance	note 3	17	–	134	kΩ
C_I	input capacitance		–	–	10	pF
Outputs						
CDEC and CMIC (type 4 mA)						
V_{OL}	LOW level output voltage	I_{OL}= 4 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = −4 mA	V_{DD}−0.5	–	–	V
C_L	load capacitance		–	–	30	pF
CDAC (type tbf mA)						
V_{OL}	LOW level output voltage	I_{OL} = 8 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = −8 mA	V_{DD}−0.5	–	–	V
C_L	load capacitance		–	–	tbf	pF
DOR, DOL, NDOR and NDOL (type custom mA)						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = −2 mA	V_{DD}−0.5	–	–	V
C_L	load capacitance		–	–	tbf	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DOBM (type 12 mA)						
V_{OL}	LOW level output voltage	I_{OL} = 12 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = –12 mA	V_{DD}–0.5	–	–	V
C_L	load capacitance		–	–	50	pF
DSR, DSL and RESYNC (type 2 mA)						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = –2 mA	V_{DD}–0.5	–	–	V
C_L	load capacitance		–	–	50	pF
DA (type 2 mA)						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = –2 mA	V_{DD}–0.5	–	–	V
C_L	load capacitance		–	–	50	pF
R_{Lint}	internal load resistance		17	–	134	kΩ
Crystal oscillator						
INPUT: XTAL1						
gm	mutual conductance	f = 100 kHz	–	tbf	–	mS
G_v	small-signal voltage gain	G_v = gm x R_O	–	tbf	–	V/V
I_{LI}	input leakage current	note 2	–1	–	+1	mA
C_I	input capacitance		–	10	–	pF
V_{IL}	LOW level input voltage	I_{IL} = tbf	–	tbf	–	V
V_{IH}	HIGH level input voltage	I_{IH} = –tbf	–	tbf	–	V
OUTPUT: XTAL2						
I_{OL}	LOW level output current	V_{OL} = tbf	–	tbf	–	mA
I_{OH}	HIGH level output current	V_{OH} = tbf	–	tbf	–	mA
Timing						
f_{XTAL}	operating frequency		33.8688			MHz
SCK, WS, DATA, SBDA, SBCL and EFAB (see Figs 8 and 9)						
f_{CL}	CL clock frequency	note 3	–	256f_s	–	Hz
f_{SCK}	SCK clock frequency		–	256f_s	–	Hz
f_{WS}	WS clock frequency		–	f_{XTAL}/ 768	–	Hz
t_{LB}	clock time LOW		110	–	–	ns
t_{HB}	clock time HIGH		110	–	–	ns
t_r	input rise time		–	–	20	ns
t_f	input fall time		–	–	20	ns
$t_{SU:DAT}$	data set-up time		20	–	–	ns
$t_{HD:DAT}$	data hold time		0	–	–	ns
$t_{SU:WS}$	WS set-up time		20	–	–	ns
$t_{HD:WS}$	WS hold time		0	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MICROCONTROLLER INTERFACE (see Figs 6 and 7)						
f_{CK}	CL input clock frequency		–	tbf	–	kHz
t_{CKL}	input clock time LOW		2.0	–	–	ms
t_{CKH}	input clock time HIGH		2.0	–	–	ms
t_{DSM}	microprocessor data set-up time after CL LOW-to-HIGH transition		1.0	–	–	ms
t_{DHM}	microprocessor data hold time after CL LOW-to-HIGH transition		2.0	–	–	ms
t_{DSP}	peak data set-up time after CL LOW-to-HIGH transition		2.0	–	–	ms
t_{DHP}	peak data hold time after CL LOW-to-HIGH transition		2.0	–	–	ms
t_{dRW}	delay to write after read		2.0	–	–	ms
t_{dWR}	delay to read after write		2.0	–	–	ms
DOBM circuit						
f_{DOBM}	data output frequency		–	$128f_s$	–	Hz
t_r	output rise time	C_L = 50 pF	–	–	10	ns
t_f	output fall time	C_L = 50 pF	–	–	10	ns
$t_{SU;DAT}$	data set-up time		tbf	–	–	ns
$t_{HD;DAT}$	data hold time		tbf	–	–	ns
CLOCK GENERATOR CIRCUIT (note 4)						
f_{XTAL1}	XTAL1 input clock frequency	slave mode	–	$256f_s$	–	Hz
f_{CDEC}	CDEC output clock frequency		–	$256f_s$	–	Hz
f_{CMIC}	CMIC output clock frequency		–	$96f_s$	–	Hz

Notes

1. Minimum V_{IL}, maximum V_{IH} are peak values to allow for transients.
2. $I_{I(min)}$ measured at V_I = 0 V: $I_{I(max)}$ measured at $V_I = V_{DD}$: Not valid for pins with pull-up/pull-down resistors.
3. $I_{I(min)}$ measured at V_I = 0 V (pull-up): $I_{I(max)}$ measured at $V_I = V_{DD}$ (pull-down): Valid for pins with pull-up/pull-down resistors.
4. Crystal frequency: 33.8688 MHz ($768f_s$), the oscillator circuit oscillates at a frequency that is approximately 0.01% above the crystal frequency.

QUALITY SPECIFICATION

In accordance with UZW-BO/FQ-0601

APPLICATION INFORMATION

Application modes

TDA1307 can be used as a digital reconstruction filter for CD, DCC, DAB and DAT applications. The configuration for these different applications is given in Table 7.

Table 7 Application modes.

MODE	CDCC	CRYSTAL	CLOCK INPUT	BITSTREAM OUTPUT	SAMPLING FREQUENCY
CD	1	$768f_s$	–	$192f_s$	44.1 kHz
DCC	0	–	$256f_s$	$128f_s$	32.0 / 44.1 / 48.0 kHz
DAB	0	–	$256f_s$	$128f_s$	32.0 kHz
DAT	0	–	$256f_s$	$128f_s$	32.0 / 44.1 / 48.0 kHz

The crystal frequency for TDA1307, when operating in master mode, is $768f_s$ (f_s = 44.1 kHz). TDA1307 can also operate in slave mode, in which the clock input receives a clock signal of $256f_s$ (f_s = 32.0, 44.1 or 48.0 kHz). In the latter configuration, no resonator is connected to TDA1307.

Basic application

Figures 17 to 20 show connections for an example of a complete bitstream reconstruction system, using TDA1307 together with TDA1547, as implemented in a demonstration application printed-circuit board. Figure 15 shows the connections pertaining to TDA1307. Both master and slave operation is possible, by setting of switches J1 and J2, and by programming the desired mode and frequency divisions by switch block SW1. Both test pins of TDA1307 are tied to ground in order to obtain immunity to crosstalk from the adjacent clock output CDAC. At pin POR(pin 20), an RC-timing network presets a typical power-on-reset LOW-time (10 ms for an instantaneously setting 5 V supply).

Typical application with TDA1547 Bitstream DAC

The high-quality one-bit audio data stream produced by the TDA1307 is optimumly converted to analog using the TDA1547 high-performance bitstream digital-to-analog converter. The TDA1547 takes the data outputs DOL (pin 27) and DOR(pin 33) of the TDA1307 as input, clocked by TDA1307 output CDAC (pin 35), and converts the digital data to "one-bit" analog values (positive reference value and negative reference value) through a differentially configured high-speed, high-accuracy switched capacitor network.
This differential application can be further enhanced to a double-differential application, combining the assertive data outputs with the complementary data outputs NDOL (pin 28) and NDOR (pin 34) into a set of two TDA1547s, by which it is possible to achieve additional noise margin. The application of Figs 15 to 17 is an example of a differential application. A schematic diagram of the double differential mode application is illustrated in Fig.20.

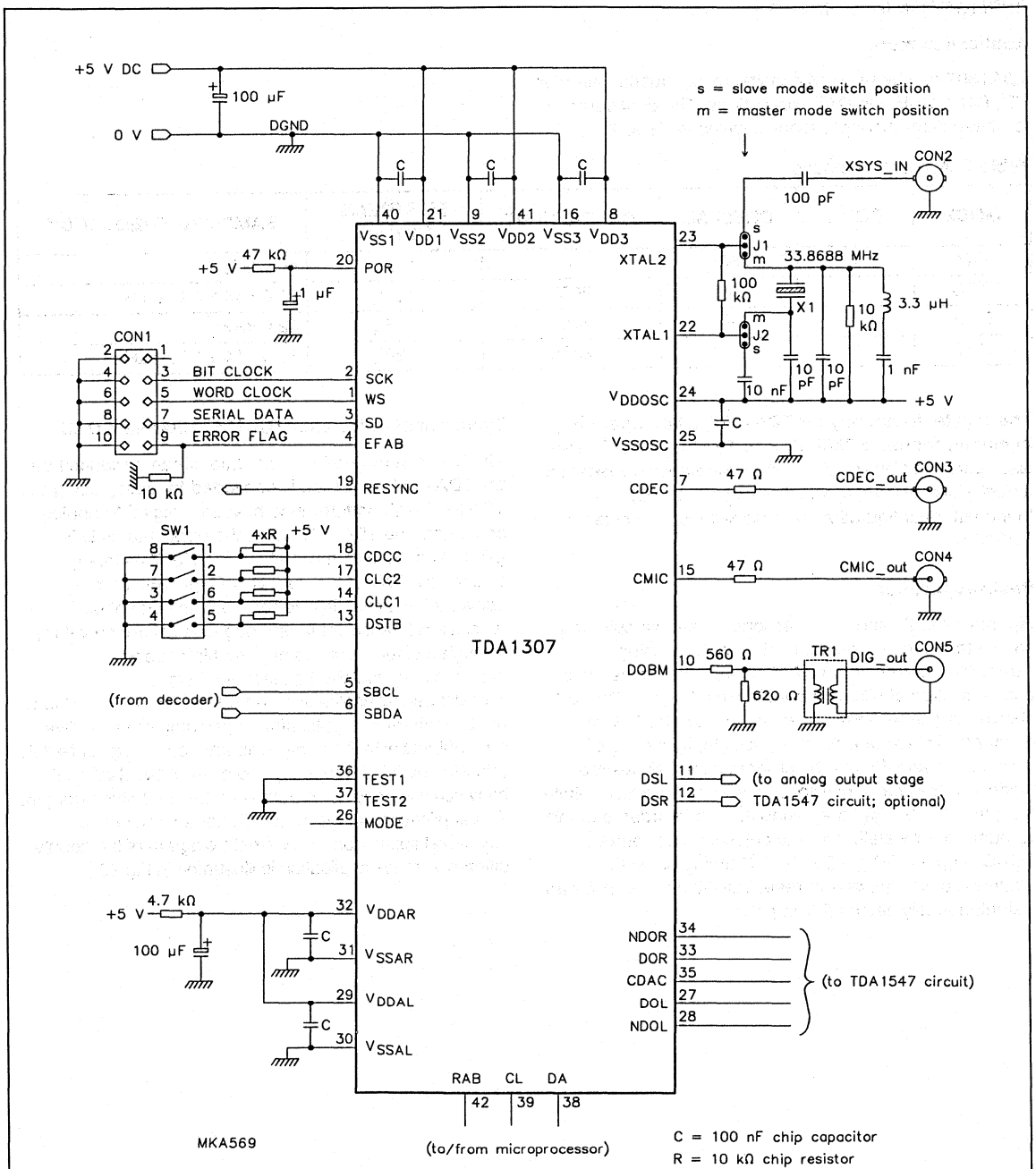


Fig.17 Basic connections TDA1307.

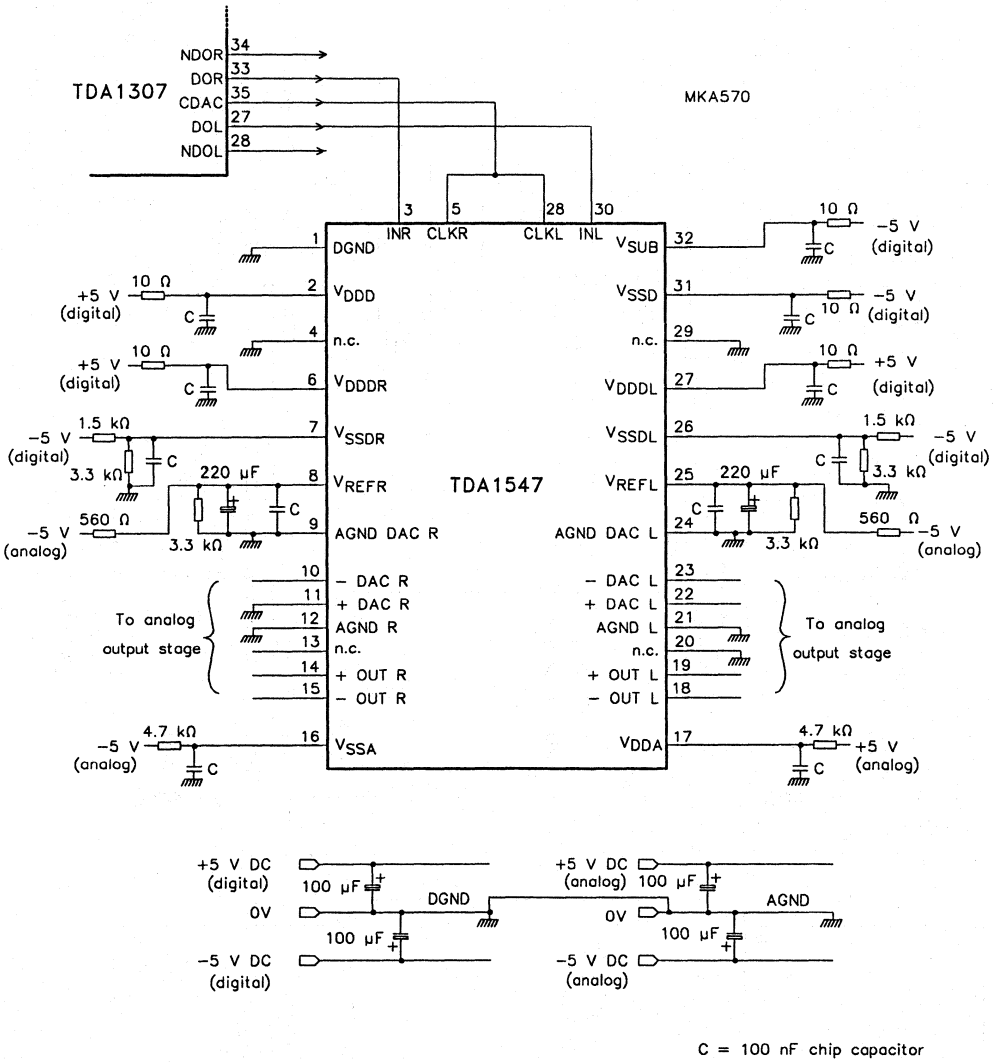


Fig.18 Connections for TDA1307.

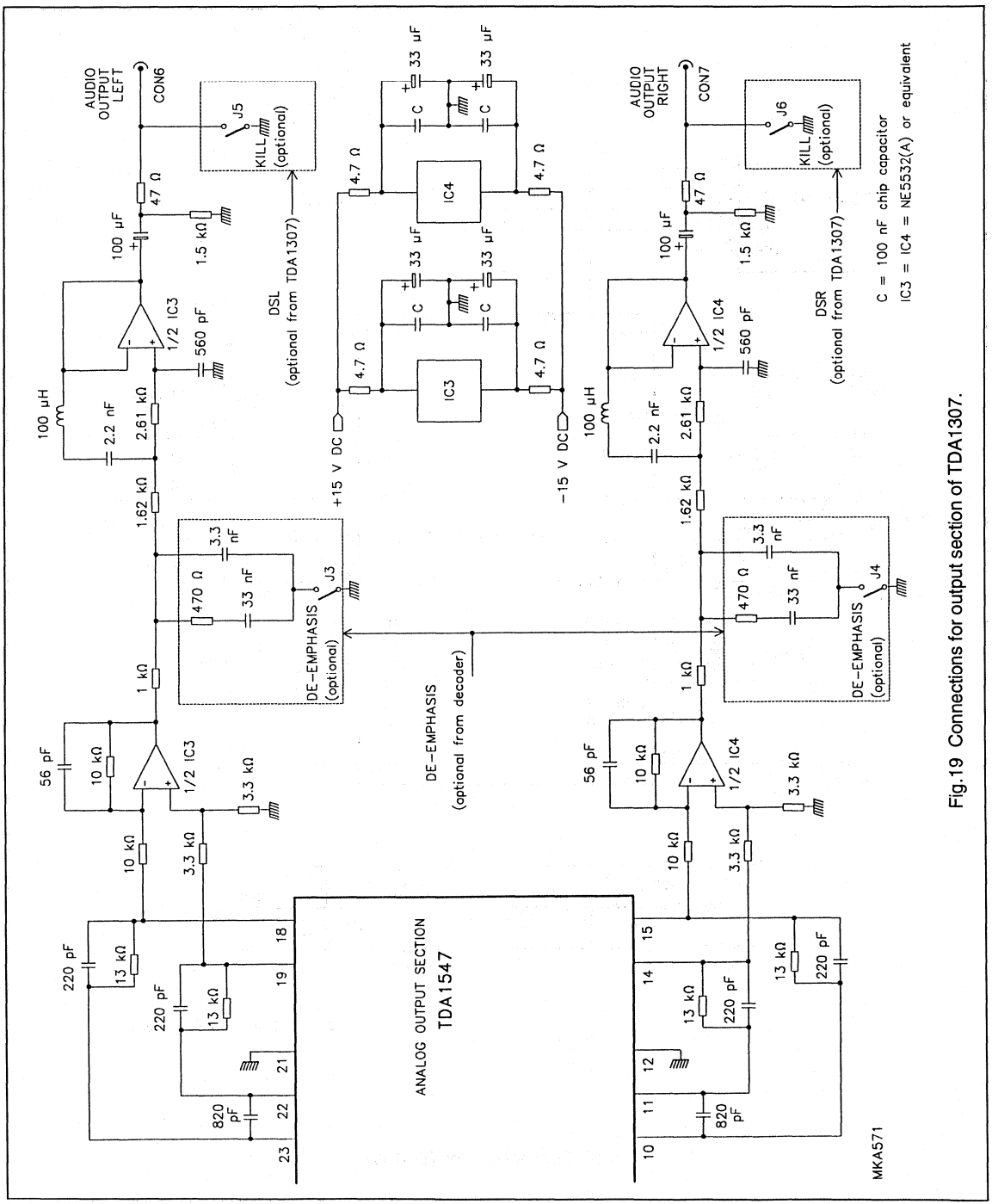


Fig.19 Connections for output section of TDA1307.

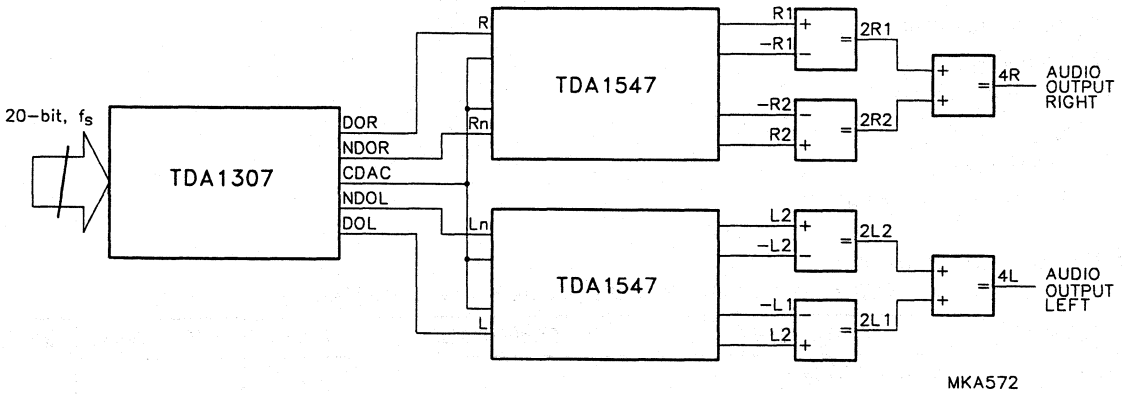


Fig.20 Schematic diagram for double differential application.

Class AB stereo headphone driver TDA1308

FEATURES

- Wide temperature range
- No switch ON/OFF clicks
- Excellent power supply ripple rejection
- Low power consumption
- Short-circuit resistant
- High performance
  - high signal-to-noise ratio
  - high slew rate
  - low distortion
- Large output voltage swing.

GENERAL DESCRIPTION

The TDA1308 is an integrated class AB stereo headphone driver contained in an SO8 or a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications.

QUICK REFERENCE DATA

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; f_i = 1 kHz; R_L = 32 Ω; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage					
	single		3.0	5.0	7.0	V
	dual		1.5	2.5	3.5	V
V_{SS}	negative supply voltage		−1.5	−2.5	−3.5	V
I_{DD}	supply current	no load	–	3	5	mA
P_{tot}	total power dissipation	no load	–	15	25	mW
P_o	maximum output power	THD < 0.1%; note 1	–	60	–	mW
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	note 1				
			–	0.03	0.06	%
			–	−70	−65	dB
		R_L = 5 kΩ	–	−101	–	dB
S/N	signal-to-noise ratio		100	110	–	dB
α_{cs}	channel separation		–	70	–	dB
		R_L = 5 kΩ	–	105	–	dB
PSRR	power supply ripple rejection	f_i = 100 Hz; $V_{ripple(p-p)}$ = 100 mV	–	90	–	dB
T_{amb}	operating ambient temperature		−40	–	+85	°C

Note

1. V_{DD} = 5 V; $V_{O(p-p)}$ = 3.5 V (at 0 dB).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1308	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TDA1308T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

BLOCK DIAGRAM

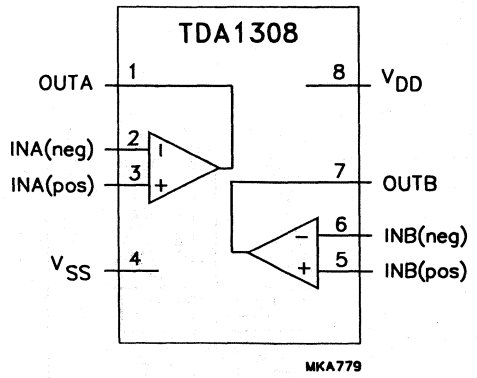


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUTA	1	output A
INA(neg)	2	inverting input A
INA(pos)	3	non-inverting input A
V_{SS}	4	negative supply
INB(pos)	5	non-inverting input B
INB(neg)	6	inverting input B
OUTB	7	output B
V_{DD}	8	positive supply

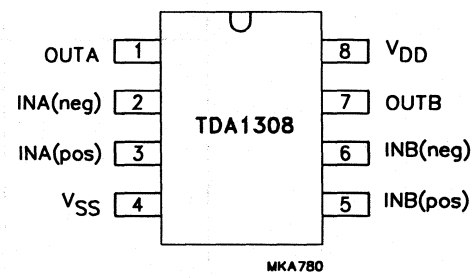


Fig.2 Pin configuration.

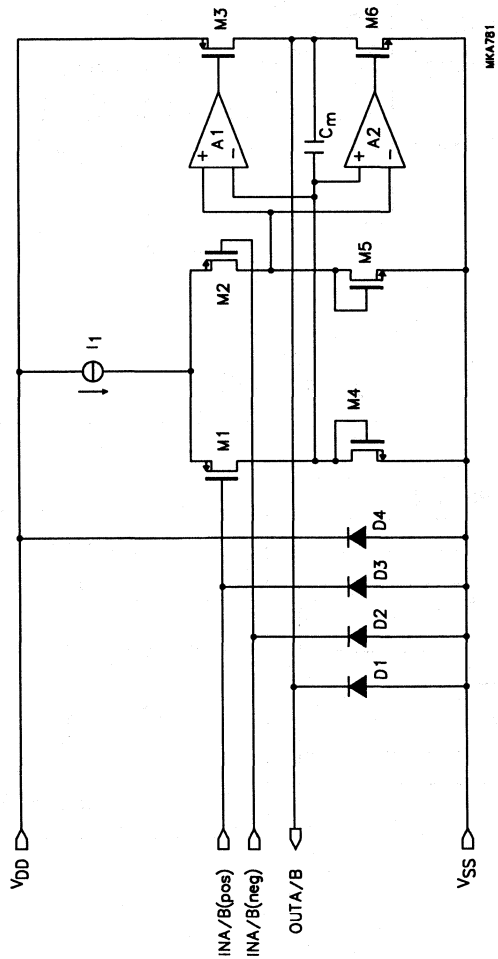


Fig.3 Equivalent schematic diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		0	8.0	V
$t_{SC(O)}$	output short-circuit duration	T_{amb} = 25 °C; P_{tot} = 1 W	20	–	s
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{esd}	electrostatic discharge	note 1	−2000	+2000	V
		note 2	−200	+200	V

Notes

1. Human body model: C = 100 pF; R = 1500 Ω; 3 pulses positive plus 3 pulses negative.
2. Machine model: C = 200 pF: L = 0.5 mH: R = 0 Ω; 3 pulses positive plus 3 pulses negative.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	DIP8	109	K/W
	SO8	210	K/W

QUALITY SPECIFICATION

In accordance with *"UZW-BO/FQ-0601"*. The numbers of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9398 510 63011.

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; f_i = 1 kHz; R_L = 32 Ω; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage					
	single		3.0	5.0	7.0	V
	dual		1.5	2.5	3.5	V
V_{SS}	negative supply voltage		−1.5	−2.5	−3.5	V
I_{DD}	supply current	no load	–	3	5	mA
P_{tot}	total power dissipation	no load	–	15	25	mW
DC characteristics						
$V_{I(os)}$	input offset voltage		–	10	–	mV
I_{bias}	input bias current		–	10	–	pA
V_{CM}	common mode voltage		0	–	3.5	V
G_v	open-loop voltage gain	R_L = 5 kΩ	–	70	–	dB
I_O	maximum output current	(THD + N)/S < 0.1%	–	60	–	mA
R_O	output resistance		–	0.25	–	Ω
V_O	output voltage swing	note 1	0.75	–	4.25	V
		R_L = 16 Ω; note 1	1.5	–	3.5	V
		R_L = 5 kΩ; note 1	0.1	–	4.9	V
PSRR	power supply rejection ratio	f_i = 100 Hz; $V_{ripple(p-p)}$ = 100 mV	–	90	–	dB
α_{cs}	channel separation		–	70	–	dB
		R_L = 5 kΩ	–	105	–	dB
C_L	load capacitance		–	–	200	pF
AC characteristics						
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	note 2	–	−70	−65	dB
			–	0.03	0.06	%
		note 2; R_L = 5 kΩ	–	−101	–	dB
			–	0.0009	–	%
S/N	signal-to-noise ratio		100	110	–	dB
f_G	unity gain frequency	open-loop; R_L = 5 kΩ	–	5.5	–	MHz
P_o	maximum output power	(THD + N)/S < 0.1%	–	60	–	mW
C_i	input capacitance		–	3	–	pF
SR	slew rate	unity gain inverting	–	5	–	V/μs
B	power bandwidth	unity gain inverting	–	20	–	kHz

Notes

1. Values are proportional to V_{DD}; (THD + N)/S < 0.1%.
2. V_{DD} = 5.0 V; $V_{O(p-p)}$ = 3.5 V (at 0 dB).

TEST AND APPLICATION INFORMATION

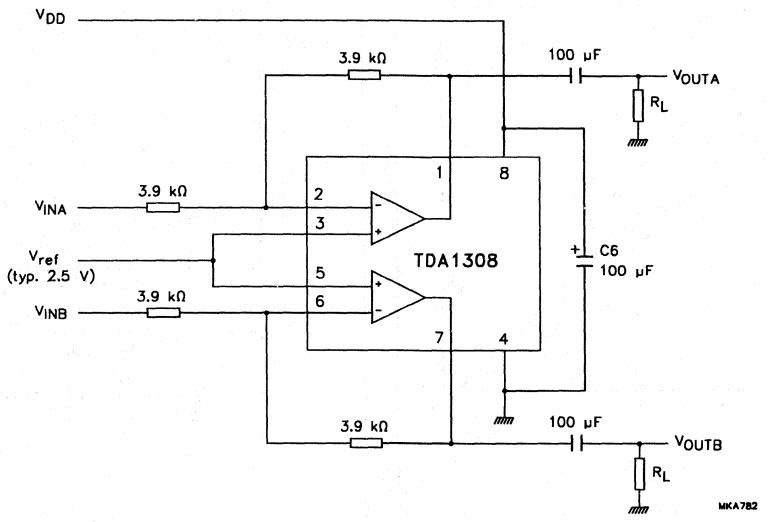


Fig.4 Measurement circuit for inverting application.

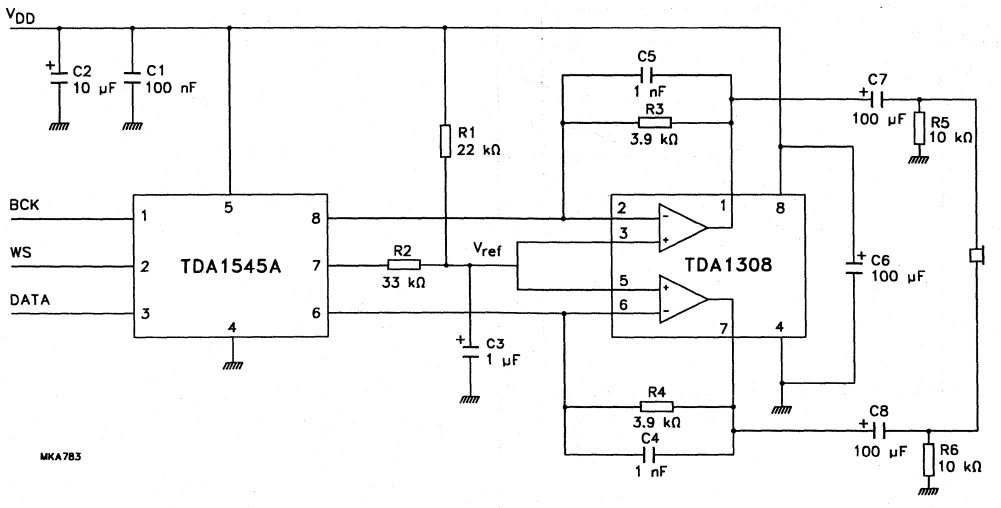


Fig.5 Example of application with TDA1545A (stereo continuous calibration DAC).

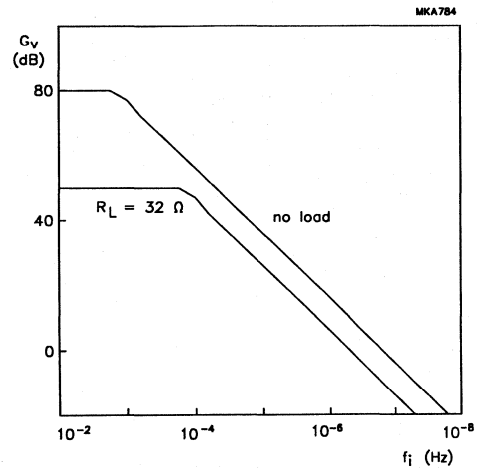


Fig.6 Open-loop gain as a function of input frequency.

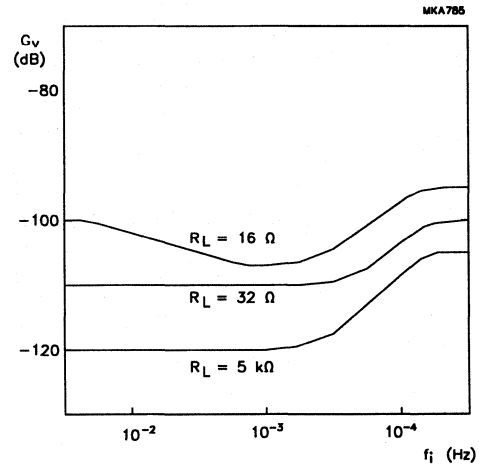


Fig.7 Crosstalk as a function of input frequency.

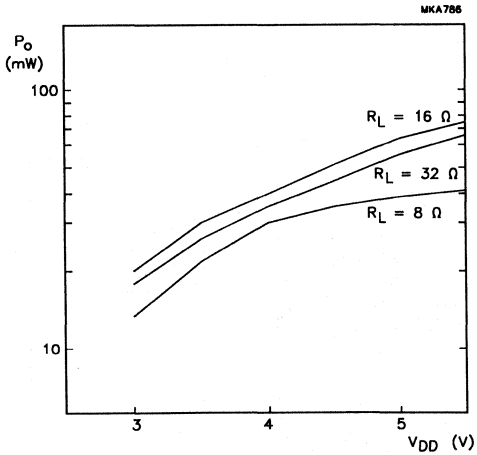


Fig.8 Output power as a function of supply voltage.

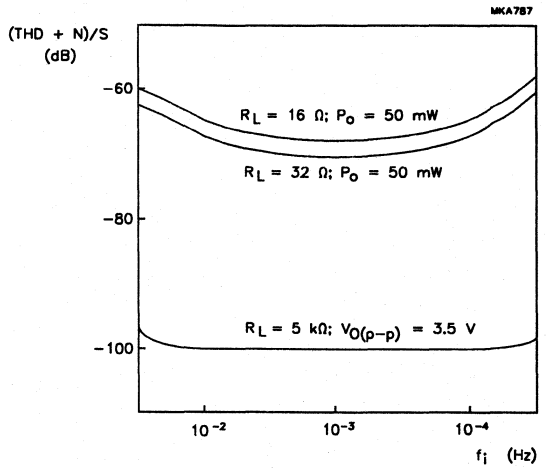


Fig.9 Total harmonic distortion plus noise-to-signal ratio as a function of input frequency.

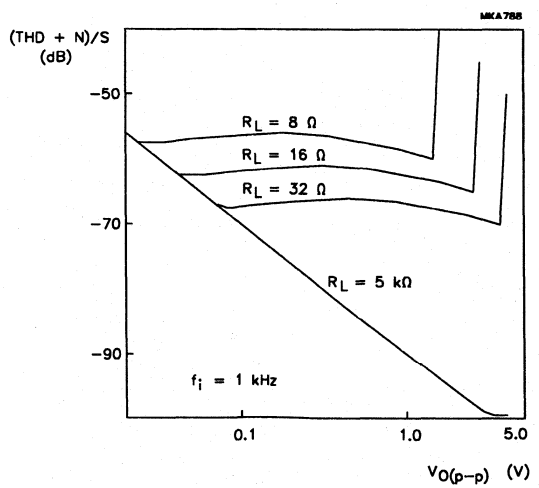
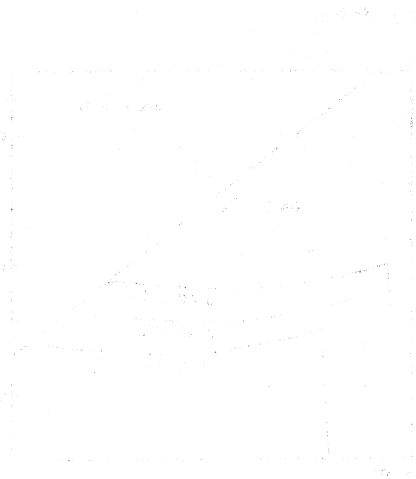


Fig.10 Total harmonic distortion plus noise-to-signal ratio as a function of output voltage level.

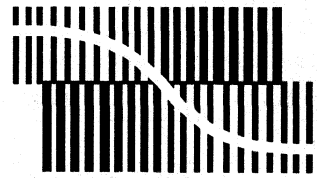


Low-voltage low-power stereo bitstream ADC/DAC

TDA1309H

FEATURES

- Low power
- Low supply voltage (2.7 V)
- Integrated high-pass filter to cancel DC offset (ADC)
- Analog loop-through function
- Multiple digital input/output formats possible
- $256f_s$ system clock frequency
- Several power-down modes
- Digital de-emphasis (DAC)
- Overload detector to enable automatic recording level adjustment (ADC)
- Input pads suitable for 5.5 V; low supply voltage interfacing
- High dynamic range
- DAC requires only one capacitor for post-filtering
- Small 44-pin quad flat pack with 0.8 mm pitch.



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The TDA1309H is a single chip stereo analog-to-digital and digital-to-analog converter employing bitstream conversion techniques. The low voltage requirement makes the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates recording and playback functions.

APPLICATION

- Portable digital audio equipment.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1309H	QFP44[1]	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm; high stand-off height	SOT307-1

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

QUICK REFERENCE DATA

$V_{DDD} = V_{DDA} = V_{DDO} = 3$ V; $V_{SSD} = V_{SSA} = V_{SSO} = 0$ V; $T_{amb} = 25$ °C; full scale sine wave input; mode 1; $f_i = 1$ kHz; 16-bit input data; conversion rate = 44.1 kHz; measurement bandwidth = 10 Hz to 20 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{DDA(AD)}$	ADC analog supply voltage (pin 8)		2.7	3.0	3.3	V
$V_{DDA(DA)}$	DAC analog supply voltage (pin 25)		2.7	3.0	3.3	V
V_{DDO}	operational amplifiers supply voltage (pin 19)		2.7	3.0	3.3	V
V_{DDD}	ADC and DAC digital supply voltage (pin 28)		2.7	3.0	3.3	V
$V_{DDD(F)}$	digital filters supply voltage (pin 34)		2.7	3.0	3.3	V
$I_{DDA(AD)}$	ADC analog supply current (pin 8)		–	8	12.5	mA
$I_{DDA(DA)}$	DAC analog supply current (pin 25)		–	3.5	7	mA
I_{DDO}	operational amplifiers supply current (pin 19)		–	12	18	mA
I_{DDD}	ADC and DAC digital supply current (pin 28)		–	0.2	0.5	mA
$I_{DDD(F)}$	digital filters supply current (pin 34)		–	20	30	mA
$I_{PD(DA)}$	DAC power-down current		–	15	20	mA
$I_{PD(AD)}$	ADC power-down current		–	7	10	mA
T_{amb}	operating ambient temperature		–20	–	+75	°C
Analog-to-digital converter						
V_I	input voltage	note 1	–	0.5	0.54	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–80	dB
		at –60 dB	–	–35	–30	dB
S/N	idle channel signal-to-noise ratio	$V_I = 0$ V	90	95	–	dB
α_{cs}	channel separation		–	90	–	dB
Digital-to-analog converter						
$V_{O(rms)}$	output voltage (RMS value)	note 2	0.43	0.5	0.57	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–78	dB
		at –60 dB	–	–38	–34	dB
		at –60 dB; note 3	–	–44	–	dB
S/N	signal-to-noise ratio	code 0000H	90	99	–	dB
		code 0000H; note 3	–	104	–	dB
α_{cs}	channel separation		90	100	–	dB

Notes

1. The input voltage for full scale digital output is a function of $V_{DDA(AD)}$.
2. At full scale digital input; no de-emphasis; $V_{O(rms)}$ is a function of $V_{DDA(DA)}$.
3. 18-bit input data.

BLOCK DIAGRAM

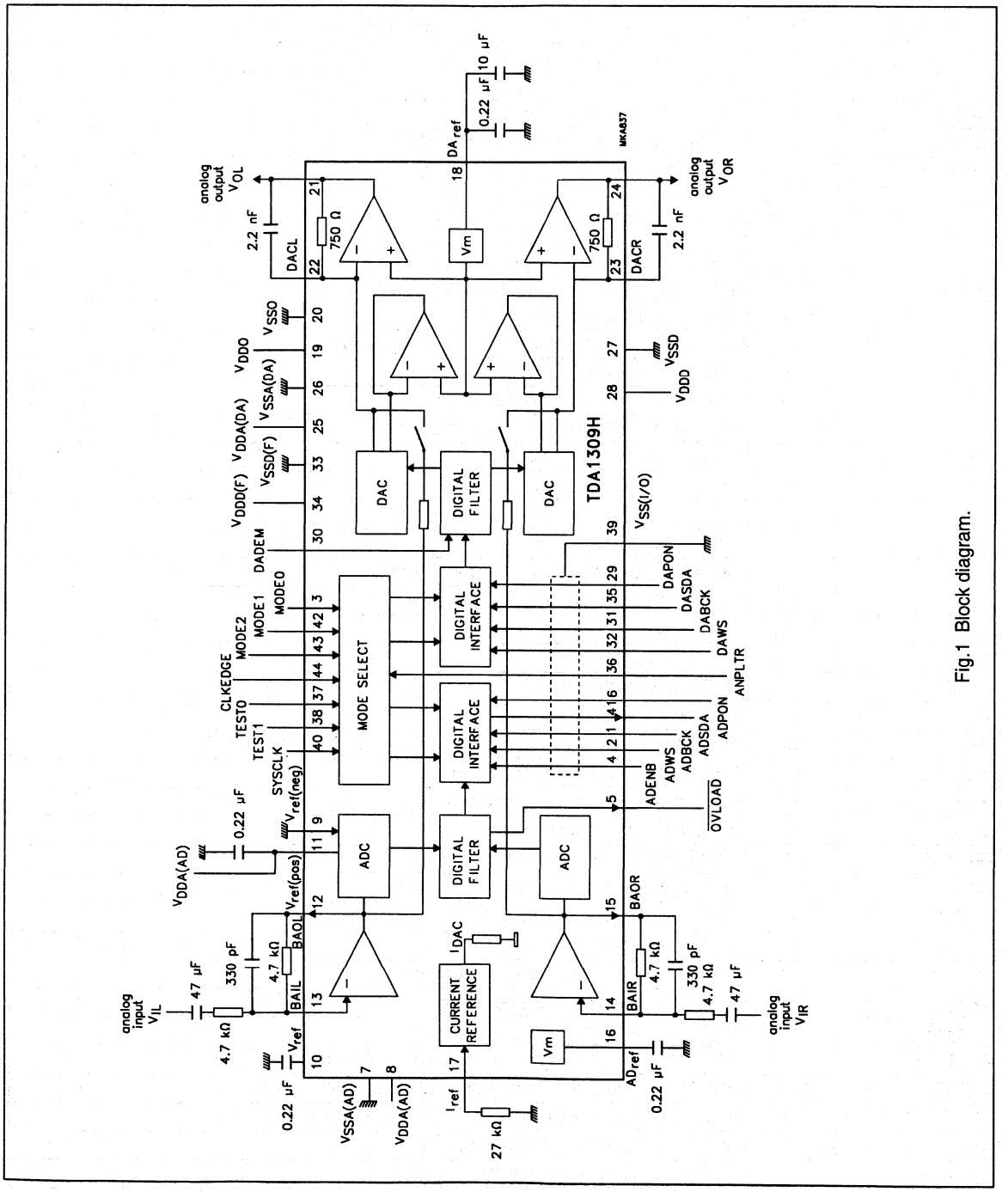


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
ADBCK	1	ADC input bit clock; $32f_s$ or $64f_s$
ADWS	2	ADC word select input at f_s
MODE0	3	ADC/DAC mode select input
ADENB	4	ADC serial data enable input (active HIGH)
$\overline{\text{OVLOAD}}$	5	ADC output overload flag (active LOW)
ADPON	6	ADC power-on-mode input (active HIGH)
$V_{SSA(AD)}$	7	ADC analog ground supply voltage
$V_{DDA(AD)}$	8	ADC analog supply voltage
$V_{ref(neg)}$	9	ADC negative reference voltage input (ground)
V_{ref}	10	ADC decoupling capacitor
$V_{ref(pos)}$	11	ADC positive reference voltage decoupling capacitor
BAOL	12	ADC input amplifier output left
BAIL	13	ADC input amplifier virtual ground left
BAIR	14	ADC input amplifier virtual ground right
BAOR	15	ADC input amplifier output right
AD_{ref}	16	ADC decoupling capacitor
I_{ref}	17	ADC/DAC reference current resistor input
DA_{ref}	18	DAC decoupling capacitor
V_{DDO}	19	ADC/DAC operational amplifier supply voltage
V_{SSO}	20	ADC/DAC operational amplifier ground supply voltage
V_{OL}	21	DAC output voltage left
DACL	22	DAC output current left
DACR	23	DAC output current right
V_{OR}	24	DAC output voltage right
$V_{DDA(DA)}$	25	DAC analog supply voltage
$V_{SSA(DA)}$	26	DAC analog ground supply voltage
V_{SSD}	27	ADC/DAC digital ground supply voltage
V_{DDD}	28	ADC/DAC digital supply voltage
DAPON	29	DAC power-on-mode input (active HIGH)
DADEM	30	DAC digital de-emphasis input (active HIGH)
DABCK	31	DAC input bit clock; $32f_s$ or $64f_s$
DAWS	32	DAC word select input at f_s
$V_{SSD(F)}$	33	ADC/DAC digital filters ground supply voltage
$V_{DDD(F)}$	34	ADC/DAC digital filters supply voltage
DASDA	35	DAC serial data input
ANLPTR	36	ADC/DAC analog loop-through input (active HIGH)
TEST0	37	ADC/DAC enable test mode 0 input (LOW is normal mode)
TEST1	38	ADC/DAC enable test mode 1 input (LOW is normal mode)
$V_{SS(I/O)}$	39	ADC/DAC digital input/output supply voltage
SYSCLK	40	ADC/DAC system clock input ($f_{sys} = 256f_s$)

SYMBOL	PIN	DESCRIPTION
ADSDA	41	ADC serial data output
MODE1	42	ADC/DAC mode 1 select input
MODE2	43	ADC/DAC mode 2 select input
CLKEDGE	44	ADC/DAC input bit clock rising/falling edge

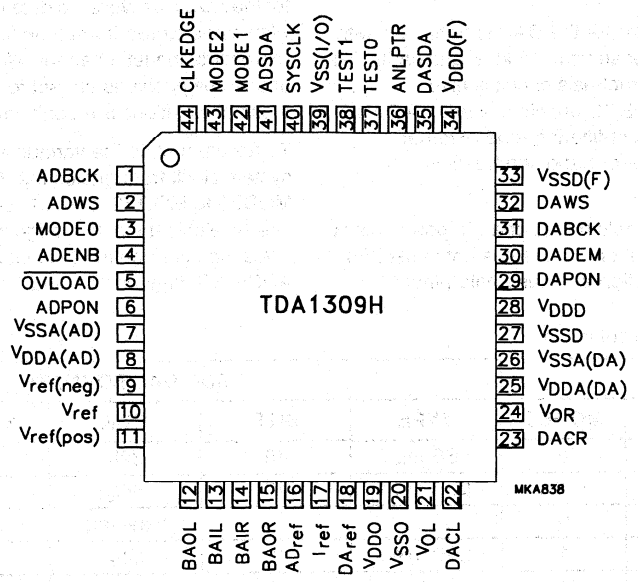


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Figure 1 illustrates the various components of the TDA1309H.
The analog-to-digital converter is a bitstream type converter, both channels are sampled simultaneously. The digital-to-analog converter is a BCC (Bitstream Continuous Calibration) type converter. The digital filter for the ADC is a bit serial IIR filter that produces a fairly linear phase response up to 15 kHz. A high-pass filter is incorporated in the down-sampling path to remove DC offsets. An overload detection circuit is incorporated to facilitate automatic recording level adjustment.

The digital up-sample filter for the DAC is partly IIR, with virtual linear phase response up to 15 kHz, and partly FIR. A switchable digital de-emphasis circuit is also incorporated. Due to the BCC principle used, the DAC needs only single pole post-filtering (one external capacitor) to meet the out-of-band suppression requirement.

The ADC and DAC channels have separate power-down modes, to reduce power if one of them is not in use. An analog loop-through function enables analog-input analog-output mode without using the ADC and DAC converters or filters, thereby switching them off to reduce power consumption.

The digital interfaces accommodates, 16 and 18-bit, I^2S-bus and LSB fixed formats. The ADC digital output can be made 3-state by means of the ADENB signal, this enables the use of a digital bus.

The TDA1309H interface accommodates slave mode only, therefore, the system ICs must provide the system clock, bit clock and word clock signals. For the DAC, the TDA1309H accepts the data together with these clocks, for the ADC it delivers the data in response to these clocks. Within one stereo frame, the first sample always represents the left channel. When sending data the unused bit positions are set to zero, when receiving data these bit positions are don't cares.

To accommodate the various interface formats and system clock frequencies four control pins are provided, MODE0 to MODE2 for mode selection and CLKEDGE which selects the active edge of the BCK signal. Table 1 gives the interface mode selection, Fig.3 illustrates the ADC/DAC data formats and Fig.4 the operating modes.

Table 1 Interface mode selection.

MODE			ADC/DAC FORMATS				
MODE 2	MODE 1	MODE 0	TYPE	BITS	BCK	SYS; f_{sys}	FIGURE
0	0	0	LSB fixed	16	$32f_s$	$256f_s$	3(a)
0	0	1	LSB fixed	16	$64f_s$	$256f_s$	3(b)
0	1	0	reserved				
0	1	1	LSB fixed	18	$64f_s$	$256f_s$	3(c)
1	0	0	I^2S-bus	16	$32f_s$	$256f_s$	3(d)
1	0	1	I^2S-bus	16	$64f_s$	$256f_s$	3(e)
1	1	0	reserved				
1	1	1	I^2S-bus	18	$64f_s$	$256f_s$	3(f)

Table 2 Clock edge mode.

CLKEDGE	VALID EDGE OF BCK	
	ADC	DAC
0	falling	rising
1	rising	falling

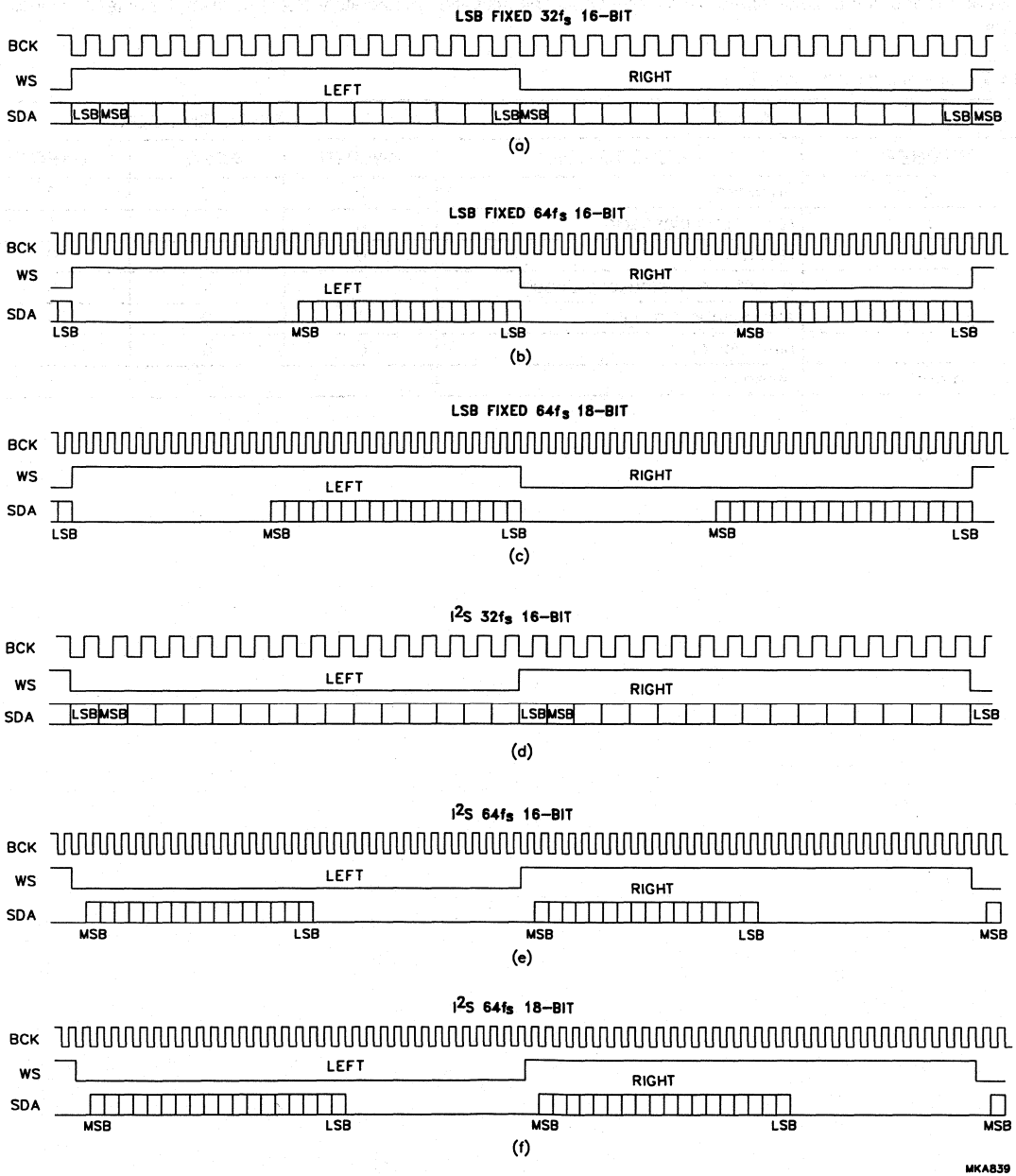


Fig.3 DAC and ADC data formats.

There are different modes in which the TDA1309H can operate. These modes can be selected as shown in Table 3 and Fig.4. In mode a, the digital filters clock is switched off. Switching over to one of the ADC active modes (b, c or d) initiates a reset sequence of the digital filters. This mode should be activated immediately after power-on for at least 2 clock periods.

Table 3 Operating mode selection.

MODE		DEVICE PIN LOGIC		
NUMBER	**DESCRIPTION**	**ANLPTR**	**ADPON**	**DAPON**
a	not used	0	0	0
b	record and playback	0	1	1
c	record only	0	1	0
d	record and analog loop-through	1	1	0
e	analog loop-through	1	0	0
f	playback only	0	0	1
g and h	reserved	1	X[1]	1

Note

1. X = don't care.

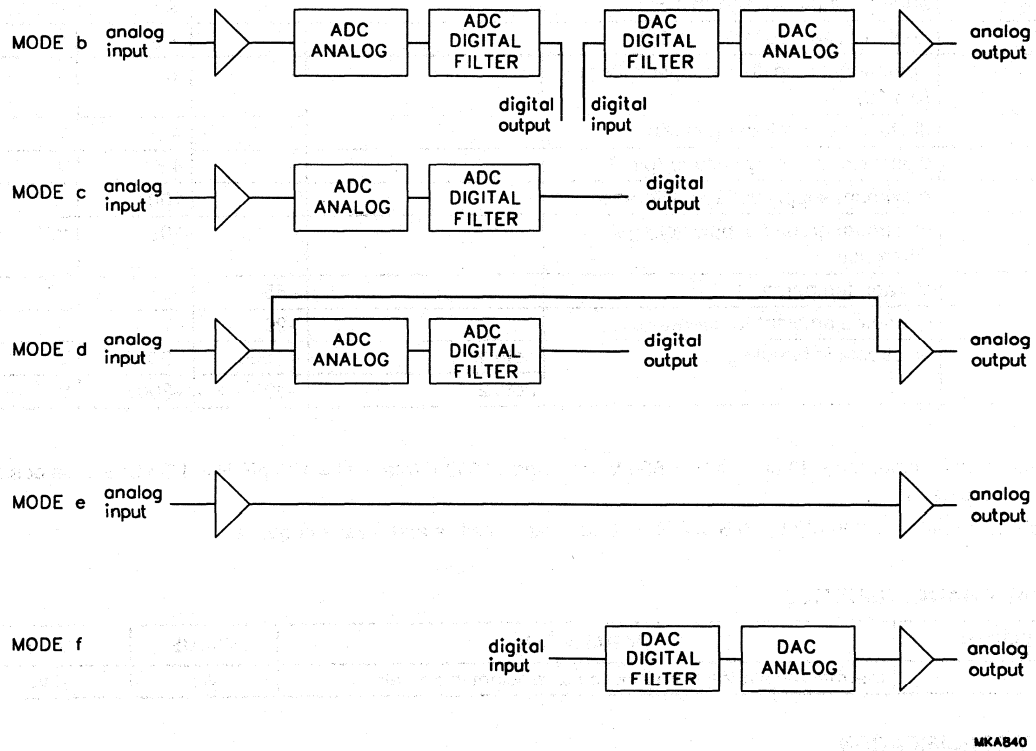


Fig.4 Schematic diagram of operating modes.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DDA(AD)}$	analog supply voltage (pin 8)		–	4.5	V
$V_{DDA(DA)}$	analog supply voltage (pin 25)		–	4.5	V
V_{DDO}	operational amplifiers supply voltage (pin 19)		–	4.5	V
V_{DDD}	digital supply voltage (pin 28)		–	4.5	V
$V_{DDD(F)}$	digital filters supply voltage (pin 34)		–	4.5	V
ΔV_{DD}	maximum supply voltage difference		–	100	mV
ΔV_{SS}	maximum ground supply voltage difference		–	100	mV
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	operating ambient temperature		–20	+75	°C
V_{es}	electrostatic handling	note 1	–3000	+3000	V
		note 2	–300	+300	V

Notes

1. Human body model: (pins 43 and 44 = –1500 V (min) and +1500 V (max); C = 100 pF; R = 1.5 kΩ; 3 zaps positive and 3 zaps negative.
2. Machine model: C = 200 pF; L = 0.5 μH; R = 10 Ω; 3 zaps positive and 3 zaps negative.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	60	K/W

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611E"*. The number of this quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9398 510 63011.

CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = 3$ V; $V_{SSD} = V_{SSA} = V_{SSO} = 0$ V; $T_{amb} = 25$ °C; full scale sine wave input; mode 1; $f_i = 1$ kHz; 16-bit input data; conversion rate = 44.1 kHz; measurement bandwidth = 10 Hz to 20 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{DDA(AD)}$	ADC analog supply voltage (pin 8)		2.7	3.0	3.3	V
$V_{DDA(DA)}$	DAC analog supply voltage (pin 25)		2.7	3.0	3.3	V
V_{DDO}	operational amplifiers supply voltage (pin 19)		2.7	3.0	3.3	V
V_{DDD}	ADC/DAC digital supply voltage (pin 28)		2.7	3.0	3.3	V
$V_{DDD(F)}$	digital filters supply voltage (pin 34)		2.7	3.0	3.3	V
$I_{DDA(AD)}$	ADC analog supply current (pin 8)		–	8	12.5	mA
		ADC power-down	–	0.3	1	mA
$I_{DDA(DA)}$	DAC analog supply current (pin 25)		–	3.5	7	mA
		DAC power-down	–	1.4	2	mA
I_{DDO}	operational amplifiers supply current (pin 19)		–	12	18	mA
		DAC power-down	–	5.5	9	mA
		ADC power-down	–	7	11	mA
		ADC/DAC power-down	–	0	–	mA
I_{DDD}	ADC/DAC digital supply current (pin 28)		–	0.2	0.5	mA
$I_{DDD(F)}$	digital filters supply current (pin 34)		–	20	30	mA
		DAC power-down	–	15	20	mA
		ADC power-down	–	7	10	mA
$I_{DDD(F)q}$	digital filters quiescent current		–	–	100	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital converter						
$V_{I(rms)}$	input voltage (RMS value)	note 1	–	0.5	0.54	V
I_I	input current (pins 13 and 14)		–	–	10	nA
ΔV_O	unbalance between channels		–	–	0.3	dB
RES	resolution	16-bit format	–	16	–	bits
		18-bit format	–	18	–	bits
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–80	dB
		at –20 dB	–	–75	–	dB
		at –60 dB	–	–35	–30	dB
S/N	idle channel signal-to-noise ratio	V_i = 0 V	90	95	–	dB
α_{cs}	channel separation		–	90	–	dB
PSRR	power supply rejection ratio	note 2	tbf	tbf	tbf	dB
Digital-to-analog converter						
$V_{O(rms)}$	output voltage (RMS value)	note 3	0.43	0.5	0.57	V
ΔV_O	unbalance between channels		–	0.1	–	dB
R_L	load resistance		5	–	–	kΩ
C_L	load capacitance	note 4	–	–	200	pF
RES	resolution	16-bit format	–	16	–	bits
		18-bit format	–	18	–	bits
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–78	dB
		at –20 dB	–	–75	–	dB
		at –60 dB	–	–38	–34	dB
		at –60 dB; note 5	–	–44	–	dB
S/N	idle channel signal-to-noise ratio	code 0000H	90	99	–	dB
		code 0000H; note 5	–	104	–	dB
α_{cs}	channel separation		90	100	–	dB
PSRR	power supply rejection ratio	note 2	tbf	tbf	tbf	dB
Analog loop-through (mode e)						
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–	dB
S/N	signal-to-noise ratio	code 0000H	–	95	–	dB
G_{ltr}	loop-through gain	note 1	–	–1.1	–	dB
E_{os}	DC offset error		–	1.0	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital decimation filter						
$f_{s(o)}$	output sample frequency		28	44.1	54	kHz
$f_{s(i)}$	input sample frequency		–	$128f_s$	–	
f_{sys}	system clock frequency		$256f_s$	–	$256f_s$	
B	signal bandwidth	f_i = 44.1 kHz	0.002	–	20	kHz
A_{sup}	aliasing suppression	$f_{s(o)} - B < f_{s(i)} < 2f_{s(o)} - B$; note 6	60	–	–	dB
		$f_{s(i)} > 2f_{s(o)} - B$; note 6	80	–	–	dB
α	frequency response	f_i = 20 Hz to 20 kHz	–0.2	–	+0.2	dB
Φ_{nl}	phase non-linearity	f_i = 20 Hz to 20 kHz	–	–	tbf	deg
OL_{det}	overload detection level		–	tbf	–	dB
Digital-to-analog interpolation filter						
$f_{s(o)}$	output sample frequency		–	$64f_s$	–	
$f_{s(i)}$	input sample frequency		28	44.1	54	kHz
f_{sys}	system clock frequency		$256f_s$	–	$256f_s$	
B	signal bandwidth	f_i = 44.1 kHz	0.002	–	20	kHz
α	frequency response	f_i = 20 Hz to 20 kHz	–0.2	–	+0.2	dB
Φ_{nl}	phase non-linearity	f_i = 20 Hz to 20 kHz	–	–	tbf	deg
SUP	out-of-band suppression		40	50	–	dB
Digital part; note 7						
INPUTS (PINS 1 TO 4, 6, 29 TO 32, 35 TO 38 AND 40 TO 44)						
V_{IL}	LOW level input voltage		–0.5	–	$0.3V_{DDD}$	V
I_{IL}	LOW level input current	$V_I = V_{SSD}$	–	–	10	µA
I_{IH}	HIGH level input current	$V_I = V_{DDD}$	–	–	10	µA
$C_{I(max)}$	maximum input capacitance		–	–	10	pF
INPUTS (PINS 1 TO 4, 6, 29 TO 32, 35 TO 38 AND 40 TO 42)						
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	–	5.5	V
INPUTS (PINS 43 AND 44)						
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	–	V_{DDD} + 0.5	V
OUTPUTS (PINS 5 AND 41)						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = –2 mA	V_{DDD} – 0.5	–	–	V
$\|I_{OZ}\|$	3-state leakage current	$V_O = V_{DDD}$ or V_{SSD}	–	–	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
BIT CLOCK; BCK (SEE FIG.5)						
T_{cy}	clock period		300	–	–	ns
t_{HC}	clock HIGH time		100	–	–	ns
t_{LC}	clock LOW time		100	–	–	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
t_{suWS}	set-up time WS to rising edge of BCK		20	–	–	ns
t_{hWS}	hold time WS to rising edge of BCK		0	–	–	ns
t_{suDA}	set-up time SDA (DAC) to rising edge of BCK		20	–	–	ns
t_{hDA}	hold time SDA (DAC) to rising edge of BCK		0	–	–	ns
t_{hAD}	hold time SDA (ADC) to falling edge of BCK		0	–	–	ns
t_{dAD}	delay time SDA (ADC) to falling edge of BCK		–	–	80	ns
SYSTEM CLOCK; SYSCLK (SEE FIG.6)						
T_{cy}	clock period		72	–	–	ns
t_{HC}	clock HIGH time		22	–	–	ns
t_{LC}	clock LOW time		22	–	–	ns
t_r	rise time		–	–	10	ns
t_f	fall time		–	–	10	ns
t_{suWS}	set-up time WS to rising edge of SYSCLK		30	–	–	ns
t_{hWS}	hold time WS to rising edge of SYSCLK		0	–	–	ns
t_{suBCK}	set-up time BCK to rising edge of SYSCLK		30	–	–	ns
t_{hBCK}	hold time BCK to rising edge of SYSCLK		0	–	–	ns

Notes

1. V_I for full scale digital output is a function of $V_{DDA(AD)}$, 0.5 V (RMS) (at 3 V the digital voltages are equivalent to −1.1 dB in the digital domain).
2. V_{ripple} = 1% of the supply voltage and f_{ripple} = 100 Hz.
3. At full scale digital input; no de-emphasis; $V_{O(rms)}$ is a function of $V_{DDA(DA)}$.
4. For a load capacitance greater than 33 pF a series resistor of 200 Ω is recommended.
5. 18 bits input data.
6. The aliasing suppression frequency is mirrored around $128f_s$.
7. All digital voltages = 2.7 to 3.3 V; all ground supply voltages = 0 V; T_{amb} = −20 to +75 °C.

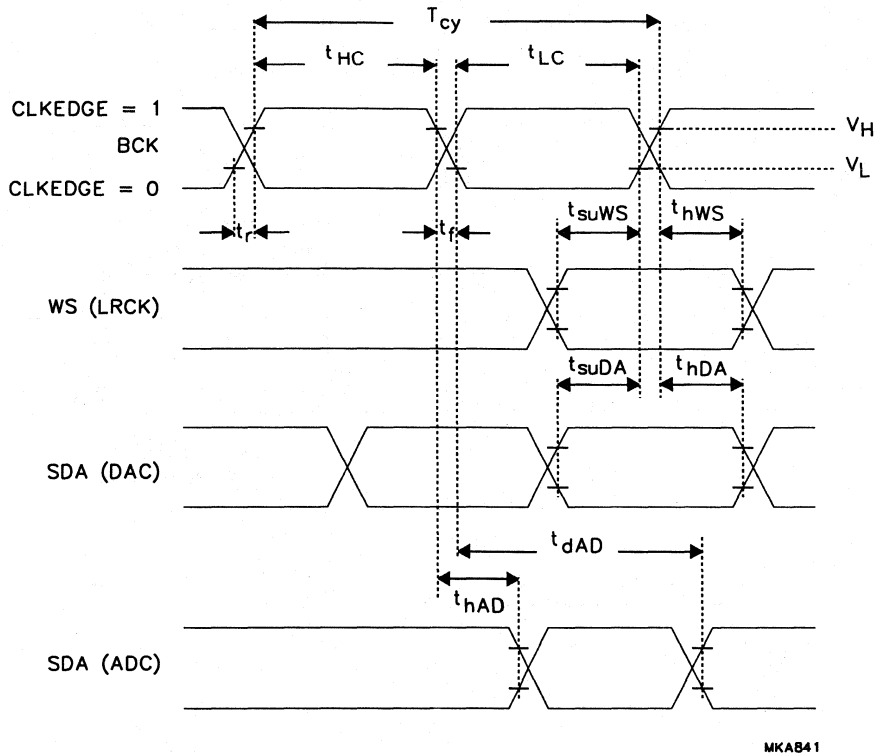


Fig.5 Serial timing of BCK related signals.

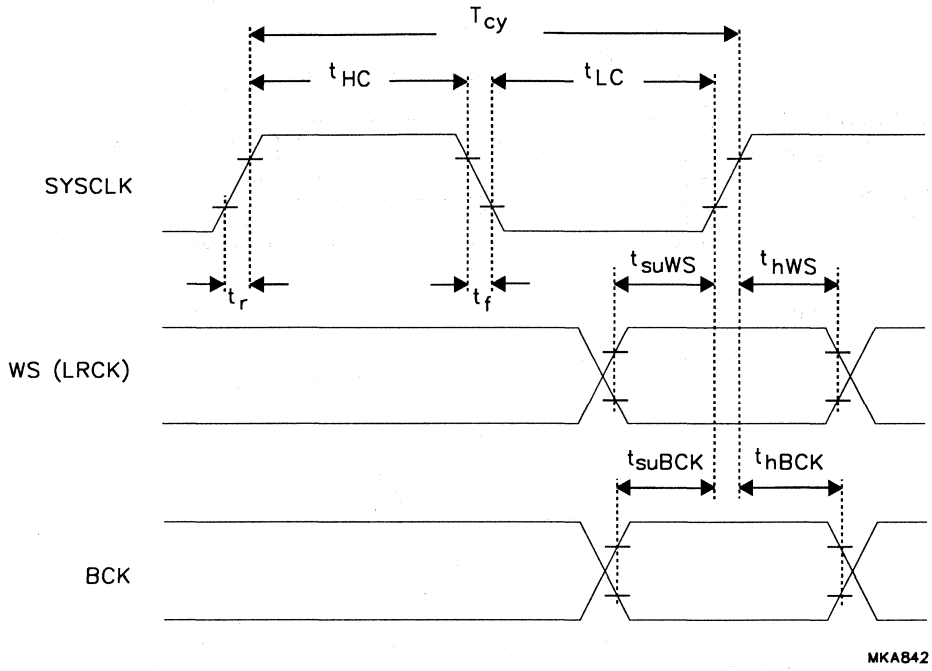


Fig.6 Serial timing of SYSCLK related signals.

Stereo Continuous Calibration DAC (CC-DAC)

TDA1310A

FEATURES

- Space saving package DIL8 or SO8
- Low power consumption
- Wide dynamic range (16-bit resolution)
- Continuous Calibration (CC) concept
- Easy application:
  - Single 3 to 5 V supply rail
  - Output current and bias current are proportional to the supply voltage
- Fast settling time permits 2×, 4× and 8× oversampling (serial input) or double speed operation at 4× oversampling
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range (-40 t +85 °C)
- Compatible with most current Japanese input formats:
  - Time multiplexed
  - Two's complement
  - TTL
- No zero-crossing distortion.

GENERAL DESCRIPTION

The TDA1310A is a device of a new generation of Digital-to-Analog Converters (DACs) which embodies the innovative technique of Continuous Calibration. The largest bit-currents are repeatedly generated by one single current reference source. This duplication is based upon an internal charge storage principle having an accuracy insensitive to ageing, temperature and process variations.

The TDA1310A is fabricated in a 1.0 μm CMOS process and features an extremely low power dissipation, small package size and easy application. Furthermore, the accuracy of the intrinsic high coarse-current combined with the implemented symmetrical offset decoding method precludes zero-crossing distortion and ensures high quality audio reproduction. Therefore, the CC-DAC is eminently suitable for use in (portable) digital audio equipment.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1310A	8	DIL8	plastic	SOT97DE
TDA1310AT	8	SO8	plastic	SOT96AG

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V at code 0000H	–	3.0	4.0	mA
I_{FS}	full scale output current	V_{DD} = 5 V	0.9	1.0	1.1	mA
		V_{DD} = 3 V	–	0.6	–	mA
(THD+N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level	–	–65	–61	dB
			–	0.05	0.08	%
		at –60 dB signal level	–	–30	–24	dB
			–	3	6	%
		at –60 dB signal level; A-weighted	–	–33	–	dB
			–	2.2	–	%
		at –60 dB signal level; A-weighted; R3 = R4 = 11 kΩ; (see Fig.1); I_{FS} = 2 mA	–	1.7	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	92	–	dB
		A-weighted; I_{FS} = 2 mA; R3 = R4 = 11 kΩ; see Fig.1	–	95	–	dB
t_{CS}	current settling time to ±1 LSB		–	0.2	–	µs
BR	input bit rate at data input		–	–	18.4	Mbits/s
f_{clk}	clock frequency at clock input BCK		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (I_{OL}; I_{OR})		–	$\pm 400 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–40	–	+85	°C
P_{tot}	total power dissipation	V_{DD} = 5 V at code 0000H	–	15	20	mW
		V_{DD} = 3 V at code 0000H	–	6.0	–	mW

BLOCK DIAGRAM

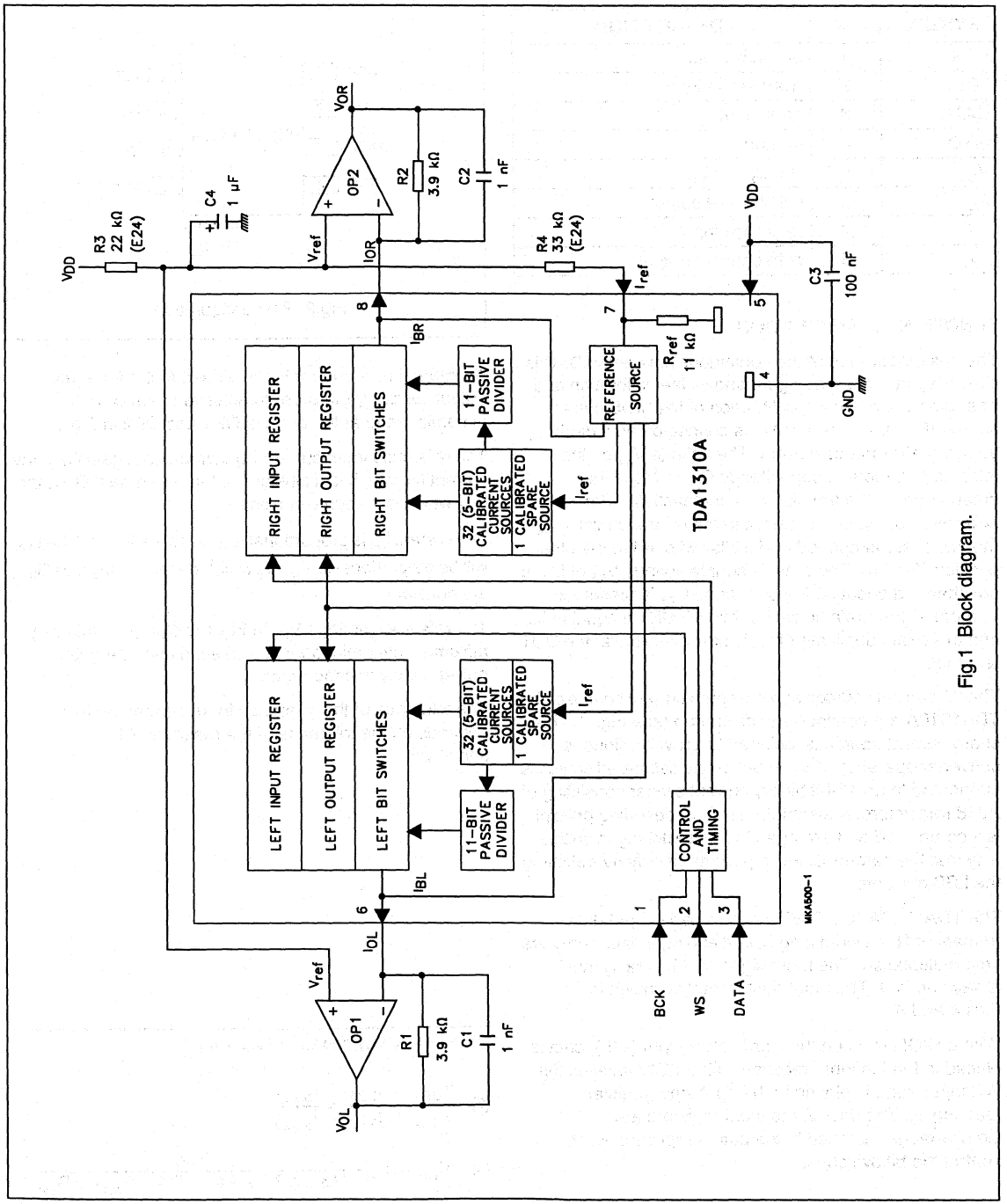


Fig.1 Block diagram.

Stereo Continuous Calibration DAC (CC-DAC)

TDA1310A

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	supply voltage
I_{OL}	6	left channel output
I_{ref}	7	reference input
I_{OR}	8	right channel output

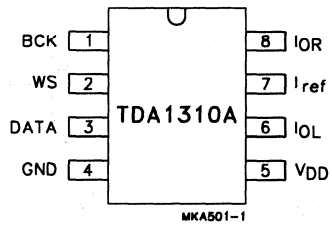


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The basic operation of the continuous calibration DAC is illustrated in Fig.3. The figure shows the calibration and operation cycle. During calibration of the MOS current source (Fig.3a) transistor M1 is connected as a diode by applying a reference current. The voltage V_{gs} on the intrinsic gate-source capacitance C_{gs} of M1 is then determined by the transistor characteristics. After calibration of the drain current to the reference value I_{ref}, the switch S1 is opened and S2 is switched to the other position (Fig.3b). The gate-to-source voltage V_{gs} of M1 is not changed because the charge on C_{gs} is preserved. Therefore, the drain current of M1 will still be equal to I_{ref} and this exact duplicate of I_{ref} is now available at the OUT terminal.

The 32 current sources and the spare current source of the TDA1310A are continuously calibrated (see Fig.1). The spare current source is included to allow continuous converter operation. The output of one calibrated source is connected to an 11-bit binary current divider consisting of 2048 transistors. A symmetrical offset decoding principle is incorporated and arranges the bit switching in such a way that the zero-crossing is performed only by switching the LSB currents.

The TDA1310A (CC-DAC) accepts serial input data formats of 16-bit word length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The input data format is shown in Figs 4 and 5.

With a HIGH level on the word select input (WS), data is placed in the left input register, with a LOW level on the WS input, data is placed in the right input register (see Fig.1). The data in the input registers are simultaneously latched in the output registers which control the bit switches.

An internal bias current I_{bias} is added to the full scale output current I_{FS} in order to achieve the maximum dynamic range at the outputs OP1 and OP2 in Fig.1.

The reference input current I_{ref} controls with gain G_{FS}, the current I_{FS} which is a sink current and with gain G_{bias} the I_{bias} which is a source current(1).

The current I_{ref} is proportional to V_{DD} so the I_{FS} and the I_{bias} will be proportional to V_{DD} as well(2) because G_{FS} and G_{bias} are constant.

The reference voltage V_{ref} in Fig.1 is $\frac{2}{3}V_{DD}$. In this way maximum dynamic range is achieved over the entire power supply voltage range.

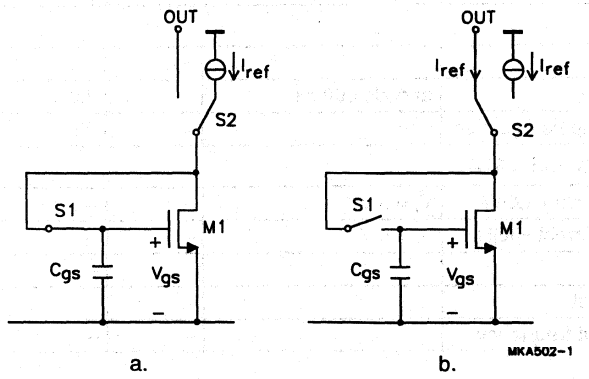
The tolerance of the reference input current in Fig.1 depends on the tolerance of the resistors R3, R4 and R_{ref}(3).

(1) $I_{FS} = G_{FS} \times I_{ref}$ and $I_{bias} = G_{bias} \times I_{ref}$

(2) $$\frac{V_{DD1}}{V_{DD2}} = \frac{I_{FS1}}{I_{FS2}} = \frac{I_{bias1}}{I_{bias2}}$$

(3) $$\Delta I_{ref} = I_{ref} - \frac{V_{DD}}{R3 + \Delta R3 + R4 + \Delta R4 + R_{ref} + \Delta R_{ref}}$$

Calibration principle



a. Calibration.
b. Operation.

Fig.3 Calibration principle.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–	6	V
T_{stg}	storage temperature		–55	+150	°C
T_{xtal}	maximum crystal temperature		–	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic handling	note 1	–2000	+2000	V
		note 2	–200	+200	V

Notes

1. Human body model; C = 100 pF; R = 1500 Ω; 3 zaps positive and negative.
2. Machine model; C = 200 pF; L = 0.5 µH; R = 10 Ω; 3 zaps positive and negative.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	DIL8	100	K/W
	SO8	210	K/W

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; measured in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	supply current	at code 0000H	–	3.0	4.0	mA
SVRR	supply voltage ripple rejection	note 1	–	30	–	dB
Digital inputs; pins WS, BCK and DATA						
$\|I_{IL}\|$	input leakage current LOW	V_I = 0 V	–	–	10	µA
$\|I_{IH}\|$	input leakage current HIGH	V_I = 5 V	–	–	10	µA
f_{clk}	clock frequency		–	–	18.4	MHz
BR	bit rate data input		–	–	18.4	Mbits/s
f_{WS}	word select input frequency		–	–	384	kHz
Timing (see Fig.4)						
t_r	rise time		–	–	12	ns
t_f	fall time		–	–	12	ns
t_{CY}	bit clock cycle time		54	–	–	ns
t_{BCKH}	bit clock pulse width HIGH		15	–	–	ns
t_{BCKL}	bit clock pulse width LOW		15	–	–	ns
$t_{SU;DAT}$	data set-up time		12	–	–	ns
$t_{HD;DAT}$	data hold time to bit clock		2	–	–	ns
$t_{HD;WS}$	word select hold time		2	–	–	ns
$t_{SU;WS}$	word select set-up time		12	–	–	ns
Analog input; pin I_{ref}						
R_{ref}	reference resistor	see Fig.1	7.4	11.0	14.6	kΩ
Analog outputs; pins I_{OL} and I_{OR}						
RES	resolution		–	–	16	bits
V_{DCC}	DC output voltage compliance		2.0	–	V_{DD} – 1	V
I_{FS}	full-scale current		0.9	1.0	1.1	mA
TC_{FS}	full-scale temperature coefficient		–	$\pm 400 \times 10^{-6}$	–	
I_{bias}	bias current		643	714	785	µA
G_{FS}	reference input current to full scale output current gain		11.9	13.2	14.5	
G_{bias}	reference input current to bias current gain		8.48	9.42	10.36	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
(THD+N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level; note 2	–	–65	–61	dB
			–	0.05	0.08	%
		at –60 dB signal level; note 2	–	–30	–24	dB
			–	3	6	%
		at –60 dB signal level; A-weighted; note 2	–	–33	–	dB
			–	2.2	–	%
		at –60 dB signal level; A-weighted; note 2; R3 = R4 = 11 kΩ; see Fig.1; I_{FS} = 2 mA	–	1.7	–	%
		at 0 dB signal level; f = 20 Hz to 20 kHz	–	–65	–61	dB
			–	0.05	0.08	%
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
α_{cs}	channel separation		86	95	–	dB
$\lvert\Delta I_O\rvert$	unbalance between outputs I_{OL} and I_{OR}	note 1	–	0.2	0.3	dB
$\lvert t_d\rvert$	time delay between outputs I_{OL} and I_{OR}		–	±0.2	–	µs
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	92	–	dB
		A-weighted; I_{FS} = 2 mA; R3 = R4 = 11 kΩ; see Fig.1	–	95	–	dB

Notes

1. V_{ripple} = 1% of supply voltage; f_{ripple} = 100 Hz.
2. Measured with 1 kHz sine wave generated at sampling rate of 192 kHz.

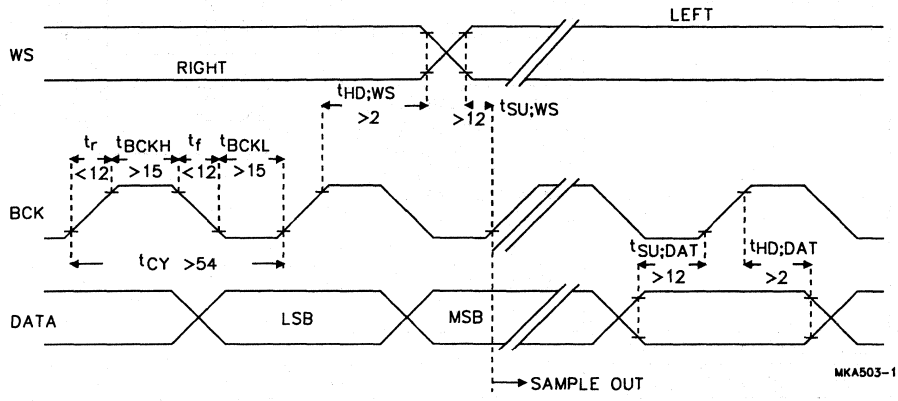


Fig.4 Timing and input signals.

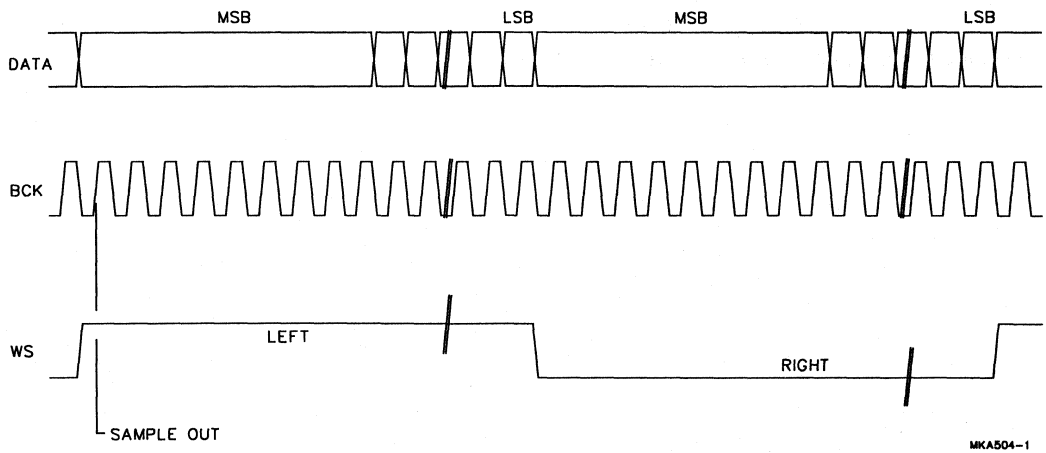
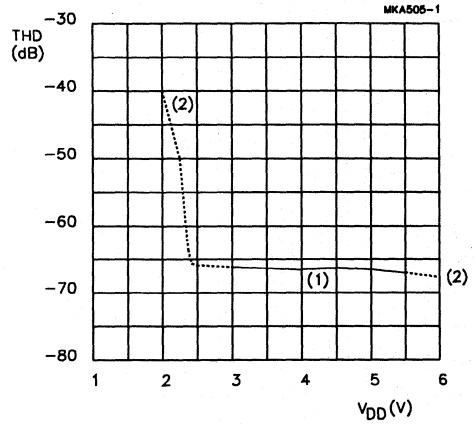


Fig.5 Format of input signals.

APPLICATION INFORMATION

Remark: the graphs are constructed from average measurement values of a small amount of engineering samples, therefore **no** guarantee for typical values is implied.

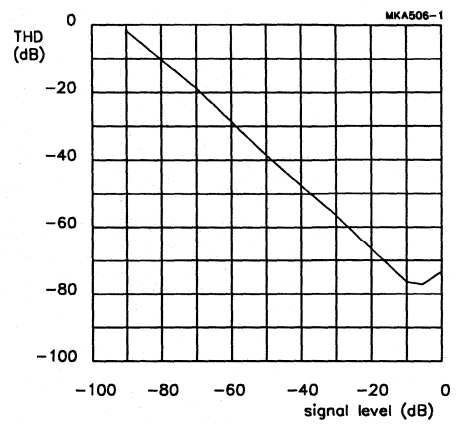


Measured with a 1 kHz sinewave generated at a sample frequency (f_s) = 192 kHz.

(1) Measured within the specified operation supply voltage range (3 to 5.5 V).

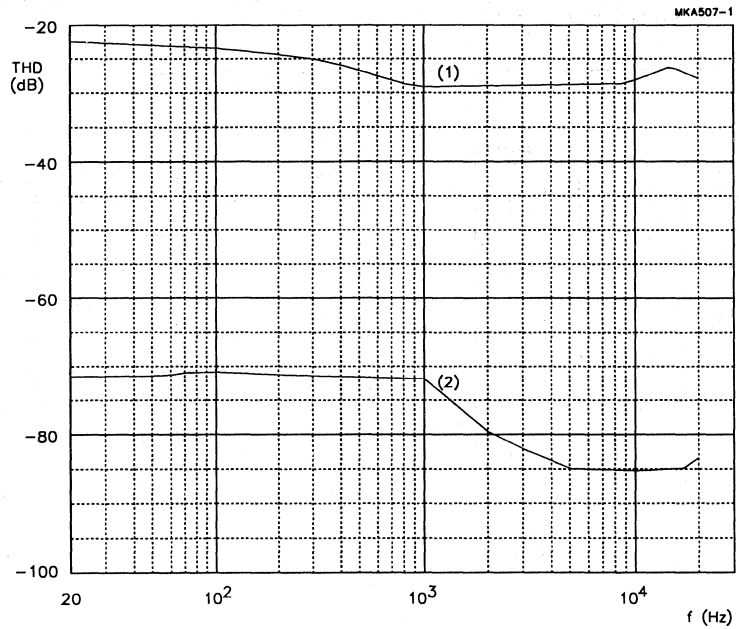
(2) Measured outside the specified operating supply voltage range (2 to 3 V and 5.5 to 6 V).

Fig.6 Total harmonic distortion as a function of supply voltage ($4f_s$).



Measured with a 1 kHz sinewave generated at a sample frequency (f_s) = 192 kHz.

Fig.7 Total harmonic distortion as a function of signal level ($4f_s$).



(1) Measured including all distortion plus noise at a signal level of −60 dB.
(2) Measured including all distortion plus noise at a signal level of 0 dB.

Fig.8 Total harmonic distortion as a function of frequency ($4f_s$).

Stereo continuous calibration DAC (CC-DAC)

TDA1311A; TDA1311AT

FEATURES

- Voltage output
- Space saving package SO8 or DIL8
- Low power consumption
- Wide dynamic range (16-bit resolution)
- Continuous Calibration (CC) concept
- Easy application:
  single 4 to 5.5 V rail supply
  output current and bias current are proportional to the supply voltage
  integrated current-to-voltage converter
- Fast settling time permits 2x, 4x and 8x oversampling (serial input) or double speed operation at 4x oversampling
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range (−40 °C to +85 °C)
- Compatible with most current Japanese input formats: time multiplexed, two's complement, TTL
- No zero-crossing distortion
- Cost efficient.

GENERAL DESCRIPTION

The TDA1311A; AT is a voltage-driven digital-to-analog converter and is new generation of DAC devices which embodies the innovative technique of Continuous Calibration (CC). The largest bit-currents are repeatedly generated by one single current reference source. This duplication is based upon an internal charge storage principle which has an accuracy insensitive to ageing, temperature matching and process variations.
The TDA1311A; AT is fabricated in a 1.0 μm CMOS process and features an extremely low-power dissipation, small package size and easy application. Furthermore, the accuracy of the intrinsic high coarse-current combined with the implemented symmetrical offset decoding method preclude zero-crossing distortion and ensures high quality audio reproduction. Therefore, the CC-DAC is eminently suitable for use in (portable) digital audio equipment.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1311A	8	DIL	plastic	SOT97DE8
TDA1311AT	8	SO8	plastic	SOT96AE3

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage		4	5	5.5	V
I_{DD}	supply current	V_{DD} = 5 V at code 0000H	–	3.4	6.0	mA
V_{FS}	full scale output voltage	V_{DD} = 5 V	1.8	2.0	2.2	V
(THD+N)/S	total harmonic distortion plus noise	at 0 dB signal level	–	–68	–63	dB
			–	0.04	0.07	%
		at –60 dB signal level	–	–30	–24	dB
			–	3	6	%
		at –60 dB signal level; A-weighted	–	–33	–	dB
			–	2	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	92	–	dB
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
BR	input bit rate at data input		–	–	18.4	Mbits/s
f_{BCK}	clock frequency at clock input		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (I_{OL}; I_{OR})		–	±400	–	ppm
T_{amb}	operating ambient temperature		–40	–	+85	°C
P_{tot}	total power dissipation	V_{DD} = 5 V at code 0000H	–	17	30	mW

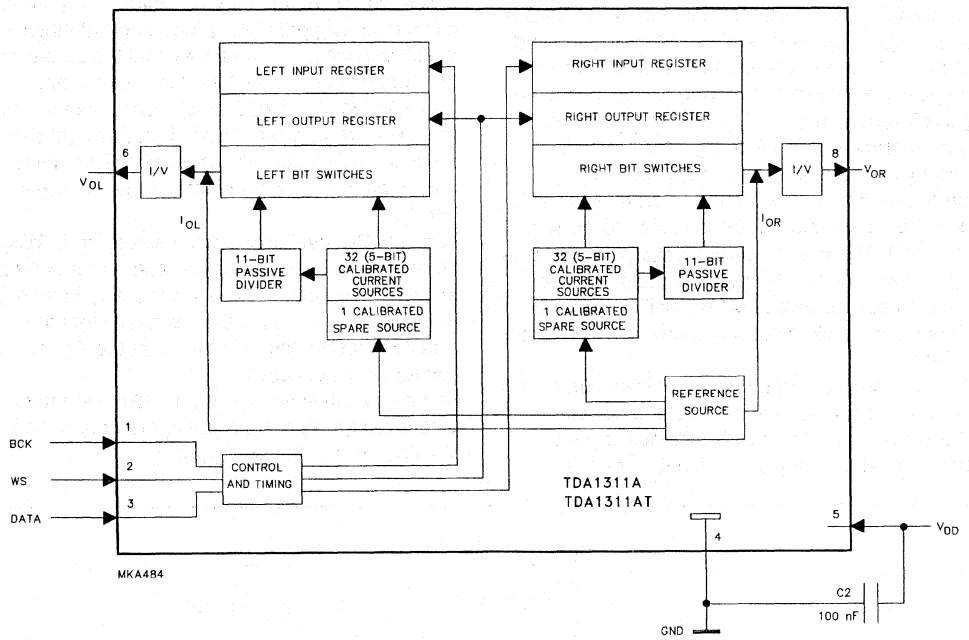


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	positive supply voltage
V_{OL}	6	left channel output
n.c.	7	not connected
V_{OR}	8	right channel output

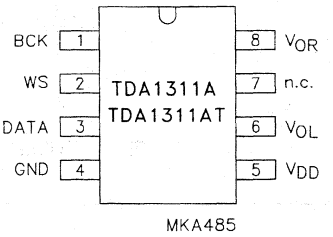


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The basic operation of the continuous calibration DAC is illustrated in Fig.3. The figure shows the calibration and operation cycle. During calibration of the MOS current source (Fig.3a) transistor M1 is connected as a diode by applying a reference current. The voltage V_{gs} on the intrinsic gate-source capacitance C_{gs} of M1 is then determined by the transistor characteristics. After calibration of the drain current to the reference value I_{REF}, the switch S1 is opened and S2 is switched to the other position (Fig.3b). The gate-to-source voltage V_{gs} of M1 is not changed because the charge on C_{gs} is preserved. Therefore, the drain current of M1 will still be equal to I_{REF} and this exact duplicate of I_{REF} is now available at the OUT terminal.

The 32 current sources and the spare current source of the TDA1311A; AT are continuously calibrated (see Fig.1). The spare current source is included to allow continuous converter operation. The output of one calibrated source is connected to an 11-bit binary current divider consisting of 2048 transistors. A symmetrical offset decoding principle is incorporated that arranges the bit switching in such a way that the zero-crossing is performed only by switching the LSB currents.

The TDA1311A; AT (CC-DAC) accepts serial input data formats of 16-bit word length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The input data format is shown in Figs 4 and 5 .

With a HIGH level on the word select input (WS), data is placed in the left input register and with a LOW level on the WS input, data is placed in the right input register (see Fig.1). The data in the input registers are simultaneously latched in the output registers which control the bit switches.

An internal offset voltage V_{OS} is added to the full scale output voltage V_{FS}; V_{OS} and V_{FS} are proportional to V_{DD}: $V_{DD1}/V_{DD2} = V_{FS1}/V_{FS2} = V_{OS1}/V_{OS2}$.

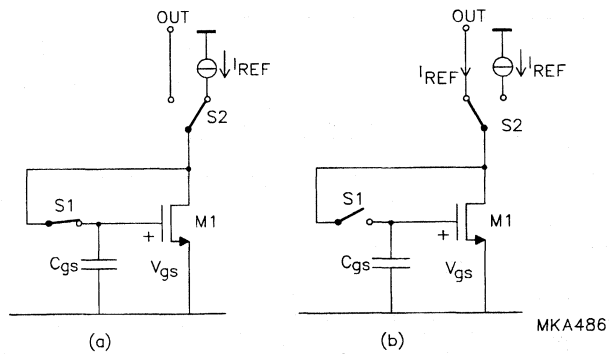


Fig.3 Calibration principle: (a) calibration, (b) operation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage		–	6	V
T_{stg}	storage temperature		–55	+150	°C
T_{XTAL}	maximum crystal temperature		–	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic handling	note 1	–2000	+2000	V
		note 2	–200	+200	V

Notes

1. Human body model: C = 100 pF, R = 1500 Ω, 3 pulses positive and 3 pulses negative.
2. Machine model: C = 200 pF, L = 0.5 μH, R = 10 Ω, 3 pulses positive and 3 pulses negative.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	DIL8	100 K/W
	SO8	210 K/W

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; measured in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		4.0	5.0	5.5	V
I_{DD}	supply current	at code 0000H	–	3.4	6.0	mA
Digital inputs; pins WS, BCK and DATA						
$\|I_{IL}\|$	input leakage current LOW	V_I = 0.8 V	–	–	10	μA
$\|I_{IH}\|$	input leakage current HIGH	V_I = 2.4 V	–	–	10	μA
f_{BCK}	clock frequency		–	–	18.4	MHz
BR	bit rate data input		–	–	18.4	Mbits/s
f_{WS}	word select input frequency		–	–	384	kHz
Timing (see Fig.4)						
t_r	rise time		–	–	12	ns
t_f	fall time		–	–	12	ns
t_{CY}	bit clock cycle time		54	–	–	ns
t_{BCKH}	bit clock pulse width HIGH		15	–	–	ns
t_{BCKL}	bit clock pulse width LOW		15	–	–	ns
$t_{SU;DAT}$	data set-up time		12	–	–	ns
$t_{HD;DAT}$	data hold time to bit clock		2	–	–	ns
$t_{HD;WS}$	word select hold time		2	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (see Fig.4)						
$t_{SU;WS}$	word select set-up time		12	–	–	ns
Analog outputs; pins V_{OL} and V_{OR}						
V_{FS}	full-scale voltage		1.8	2.0	2.2	V
TC_{FS}	full-scale temperature coefficient		–	±400	–	ppm
V_{OS}	offset voltage	$V_{DD} = V_{OL/ORmax}$	0.45	0.50	0.55	V
(THD+N)/S	total harmonic distortion plus noise	at 0 dB signal level; note 1	–	–68	–63	dB
			–	0.04	0.07	%
		at –60 dB signal level; note 1	–	–30	–24	dB
			–	3	6	%
		at –60 dB signal level; A-weighted; note 1	–	–33	–	dB
			–	2	–	%
		at 0 dB signal level; f = 20 Hz to 20 kHz	–	–65	–61	dB
			–	0.05	0.09	%
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
α	channel separation		75	80	–	dB
$\lvert dI_O \rvert$	unbalance between outputs	note 1	–	0.2	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		–	±0.2	–	µs
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	92	–	dB

Note

1. Measured with 1 kHz sinewave generated at sampling rate of 192 kHz.

QUALITY SPECIFICATION

In accordance with SNW-FQ-0611.

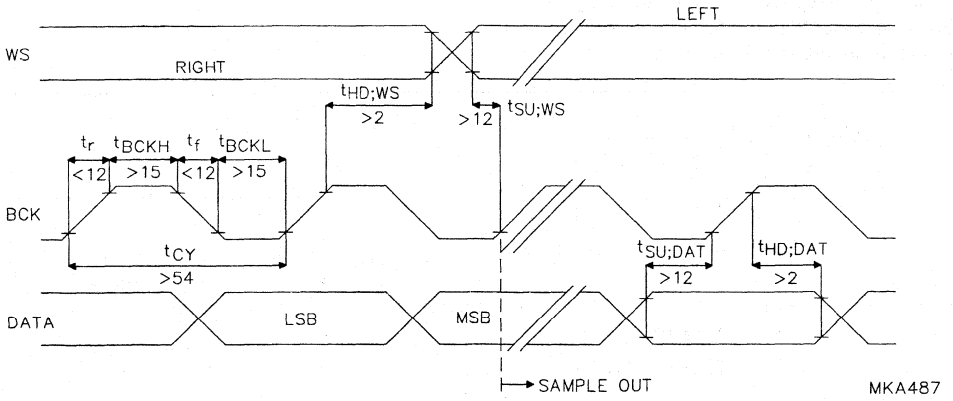


Fig.4 Timing and input signals.

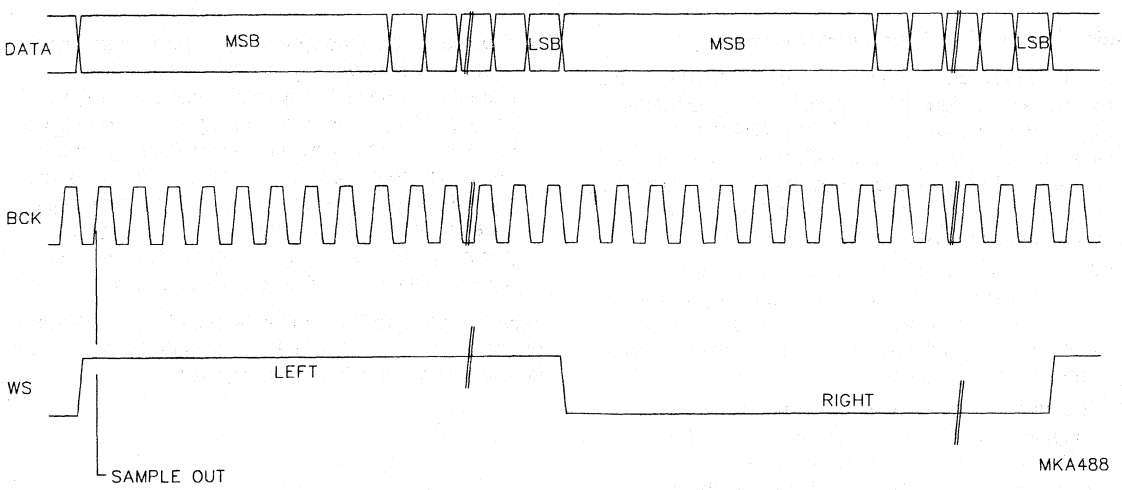


Fig.5 Format of input signals.

APPLICATION INFORMATION

Basic application example

A typical example of a CD-application with the TDA1311A; AT is shown in Fig.6. It features typical decoupling components and a third-order analog post-filter stage providing a line output.

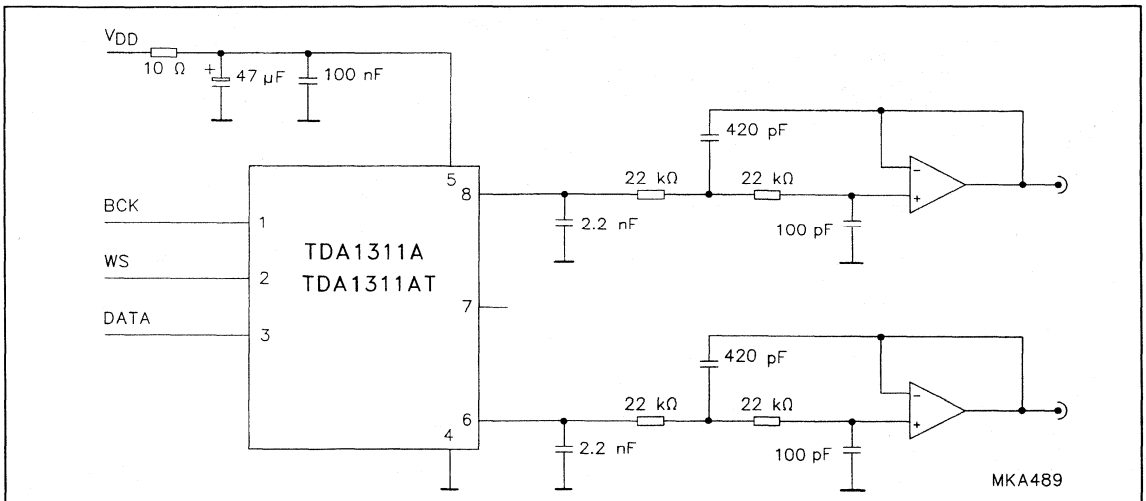


Fig.6 Example of a 3rd order filter application.

Attention to printed circuit board layout

The TDA1311A and even more so the TDA1311AT offers great ease in designing-in to printed-circuit boards due to its small size and low pin count. The TDA1311A; AT being a mixed-signal IC in CMOS, some attention needs to be paid to layout and topology of the application PCB. Following some basic rules will yield the desired performance. The most important considerations are:

1. Supply: care should be taken to supply the TDA1311A; AT with a clean, noiseless V_{DD}, for a good noise performance of the analog parts of the DAC. Supply purity can easily be achieved by using an RC-filtered supply.
2. Grounding: preferably a ground plane should be used, in order to have a low-impedance return available at any point in the layout. It is advantageous to make a partitioning of the ground plane according to the nature of the expected return currents (digital input returns separate from supply returns and separate from the analog section).
3. Topology: the capacitor decoupling high-frequency supply interference from V_{DD} to GND should be placed as close as is physically possible to the IC body, ensuring a low-inductance path to ground. The digital input conductors may be shielded by ground leads running alongside. The placement of a passive ground plane underside the entire IC surface gives "free" additional decoupling from the IC body to ground as well as providing a shield between the digital input pins and the analog output pins.

Figure 7 shows recommended layouts for printed-circuit boards for the SO8 and DIL8 versions respectively. Both layouts use a single-interconnect layer.

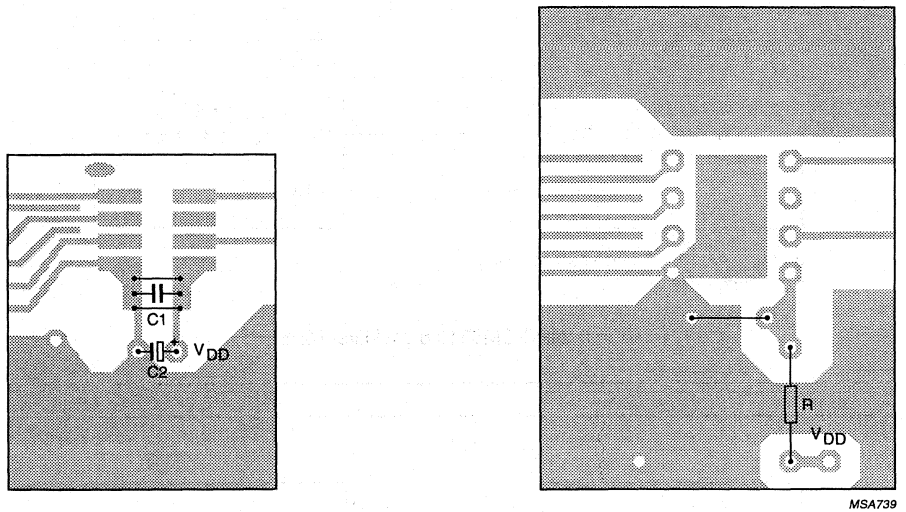


Fig.7 Recommended printed-circuit board layouts.

Interface examples

The following figures (Figs 8 to 14) show examples of connections to commonly used decoder and digital filter ICs. The digital interface part is shown only, for clarity. The diagrams are for guidance purposes only - **no** guarantee for industrial exploitation is implied.

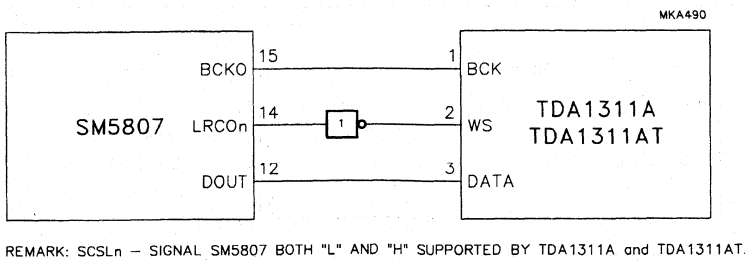
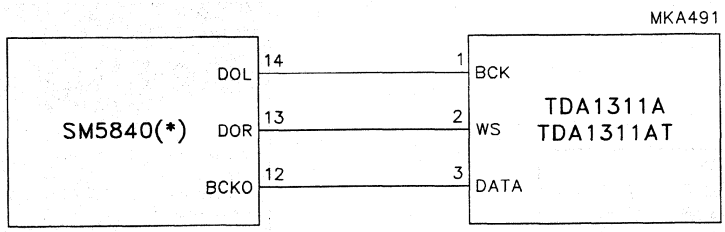
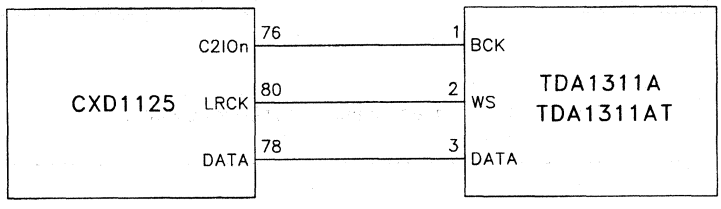


Fig.8 NPC SM5807 digital filter (4FS).



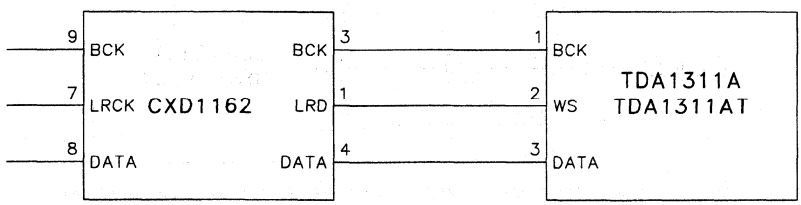
OMODn PIN 19: "L" FOR 4FS OPERATION.
* VERSIONS A/B/G

Fig.9 NPC SM5840 digital filter (4FS).



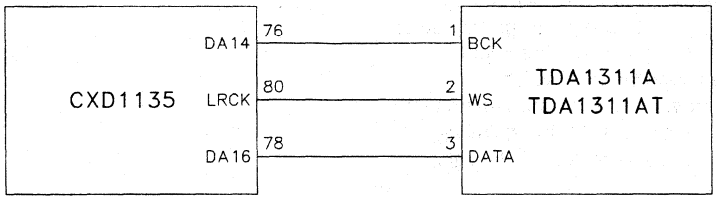
MODE SELECT:
MD1 PIN 55: "L"
MD2 PIN 56: "L" TO USE DOTX FUNCTION
MD3 PIN 57: "H"
PSSL PIN 59: "L"
SLOB PIN 58: "L"

Fig.10 Sony CXD1125 decoder (1FS).



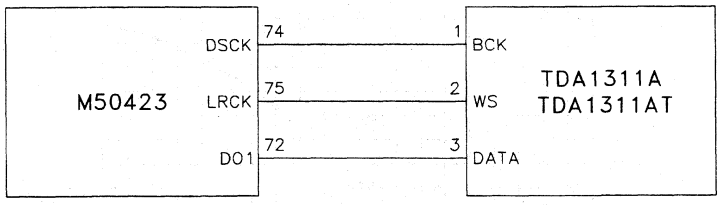
REMARK: CXD1162 INPUT CONNECTABLE TO CXD1125
IN THE SAME WAY AS FOR TDA1311A; AT TO CXD1125

Fig.11 Sony CXD1162 digital filter (4FS).



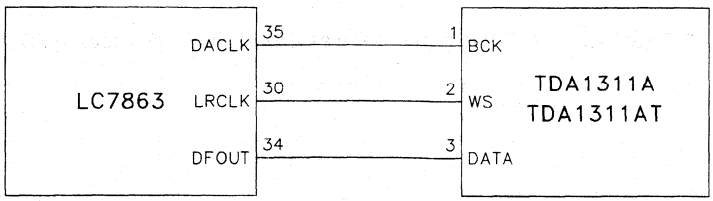
MODE SELECT:
MD1 PIN 55: "L"
MD2 PIN 56: "L" TO USE DOTX FUNCTION
MD3 PIN 57: "H" FOR 1FS; "L" FOR 2FS
PSSL PIN 59: "L"
SLOB PIN 58: "L"

Fig.12 Sony CXD1135 decoder (1FS) and digital filter (2FS).



MODE SELECT:
DOBSEL PIN 7: "L"
DASEL1 PIN 8: "H"
DASEL2 PIN 9: "L"
DASEL3 PIN 10: "H"
DASEL4 PIN 11: "L"

Fig.13 Mitsubishi M50423 decoder (1FS) and digital filter (4FS).



MODE SELECT:
DFOFF PIN 27: "L"
MSBF PIN 38: "H"

Fig.14 Sanyo LC7863 decoder (1FS).

Evaluation of audio parameters

The following measurement graphs are performed on singular engineering samples; therefore **no** guarantee of typical parameter values is implied. Measurement conditions are typical, as stated in the section Characteristics, unless otherwise indicated. The normal measurement set-up includes a 20 kHz band-limiting filter for bandwidth definition, and an A-weighting filter where indicated.

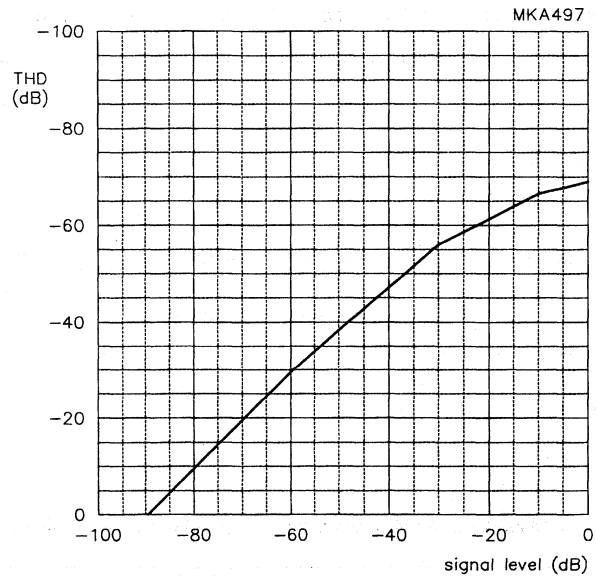
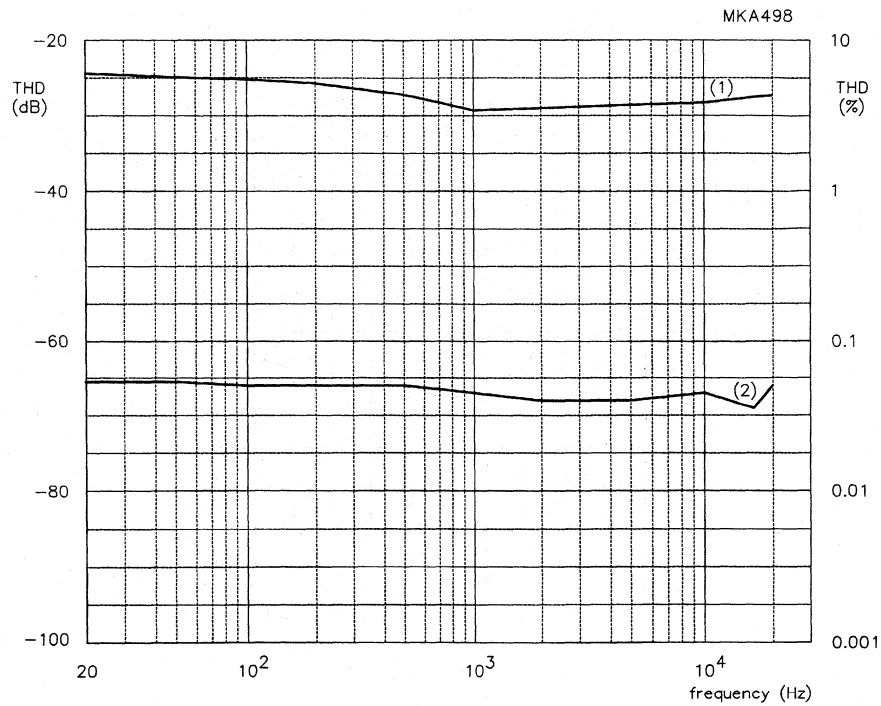
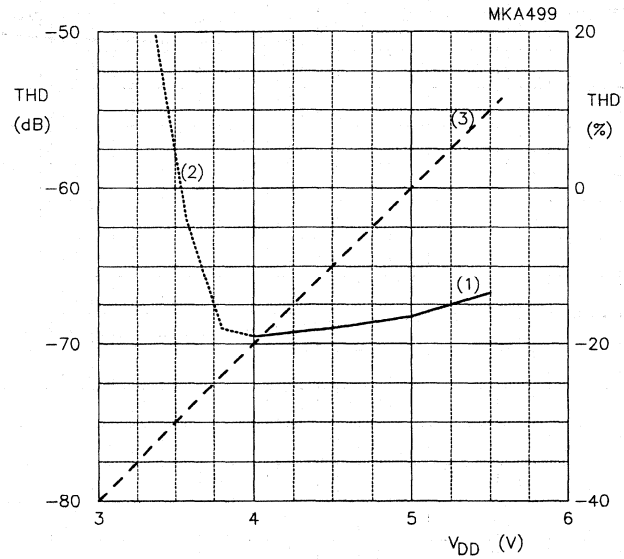


Fig.15 Total harmonic distortion plus noise as a function of signal level (4FS).



(1) Measured including all distortion plus noise at a signal level of −60 dB.
(2) Measured including all distortion plus noise at a signal level of 0 dB.

Fig.16 Total harmonic distortion plus noise as a function of frequency (4FS).



(1) Measured including all distortion plus noise within the specified operating supply voltage range.
(2) Measured including all distortion plus noise outside the specified operating supply voltage range.
(3) V_{FS} relative to nominal.

Fig.17 Total harmonic distortion plus noise as a function of supply voltage (4FS).

Stereo continuous calibration DAC (CC-DAC)

TDA1312A; TDA1312AT

FEATURES

- 8 x oversampling (simultaneous input) possible
- Voltage output
- Space saving package SO8 or DIL8
- Low power consumption
- Wide dynamic range (16-bit resolution)
- Continuous Calibration (CC) concept
- Easy application:
  single 4 to 5.5 V rail supply
  output current and bias current are proportional to the supply voltage
  integrated current-to-voltage converter
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range (−40 °C to +85 °C)
- Compatible with most current Japanese input formats: time multiplexed, two's complement and TTL
- No zero-crossing distortion
- Cost efficient.

GENERAL DESCRIPTION

The TDA1312A; 1312AT is a voltage driven D/A converter and is a device of a new generation of digital-to-analog converters which embodies the innovative technique of Continuous Calibration (CC). The largest bit-currents are repeatedly generated by one single current reference source. This duplication is based upon an internal charge storage principle having an accuracy insensitive to ageing, temperature matching and process variations.

The TDA1312A; 1312AT is fabricated in a 1.0 μm CMOS process and features an extremely low power dissipation, small package size and easy application. Furthermore, the accuracy of the intrinsic high coarse-current combined with the implemented symmetrical offset decoding method preclude zero-crossing distortion and ensures high quality audio reproduction. Therefore, the CC-DAC is eminently suitable for use in (portable) digital audio equipment.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1312A	8	DIL	plastic	SOT97DE
TDA1312AT	8	SO8	plastic	SOT96AG

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4	5	5.5	V
I_{DD}	supply current	V_{DD} = 5 V; at code 0000H	–	3.4	6.0	mA
V_{FS}	full scale output voltage	V_{DD} = 5 V	1.8	2.0	2.2	V
(THD+N)/S	total harmonic distortion plus noise	at 0 dB signal level	–	–68	–63	dB
			–	0.04	0.07	%
		at –60 dB signal level	–	–30	–24	dB
			–	3	6	%
		at –60 dB signal level; A-weighted	–	–33	–	dB
			–	2	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted; at code 0000H	86	92	–	dB
t_{CS}	current settling time to ±1 LSB		–	0.2	–	µs
BR	input bit rate at data input		–	–	18.4	Mbits/s
f_{BCK}	clock frequency at clock input		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (I_{OL}; I_{OR})		–	±400	–	ppm
T_{amb}	operating ambient temperature		–40	–	+85	°C
P_{tot}	total power dissipation	V_{DD} = 5 V; at code 0000H	–	17	30	mW

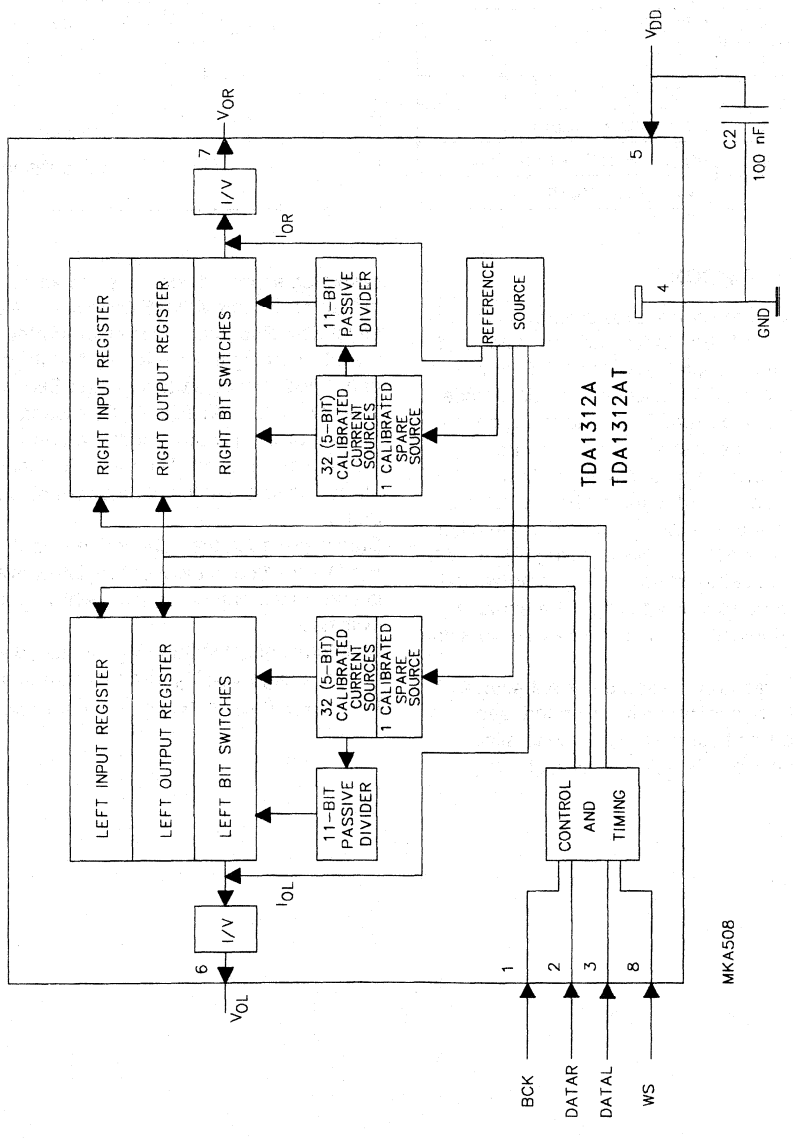


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
DATAR	2	right data input
DATAL	3	left data input
GND	4	ground
V_{DD}	5	positive supply voltage
V_{OL}	6	left channel output
V_{OR}	7	right channel output
WS	8	word select input

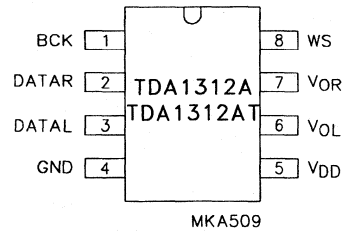


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The basic operation of the continuous calibration DAC is illustrated in Fig.3. The figure shows the calibration and operation cycle. During calibration of the MOS current source (Fig.3(a)) transistor M1 is connected as a diode by applying a reference current. The voltage V_{gs} on the intrinsic gate-source capacitance C_{gs} of M1 is then determined by the transistor characteristics. After calibration of the drain current to the reference value I_{ref}, the switch S1 is opened and S2 is switched to the other position (Fig.3(b)). The gate-to-source voltage V_{gs} of M1 is not changed because the charge on C_{gs} is preserved. Therefore, the drain current of M1 will still be equal to I_{REF} and this exact duplicate of I_{REF} is now available at the OUT terminal.

The 32 current sources and the spare current source of the TDA1312A; AT are continuously calibrated (see Fig.1). The spare current source is included to allow continuous converter operation. The output of one calibrated source is connected to an 11-bit binary current divider consisting of 2048 transistors. A symmetrical offset decoding principle is incorporated and arranges the bit switching in such a way that the zero-crossing is performed only by switching the LSB currents.

The TDA1312A; AT (CC-DAC) accepts serial input data formats of 16-bit word length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The input data format is shown in Figs.4 and 5.

Data is placed in the right and left input registers (see Fig.1). The data in the input registers is simultaneously latched in the output registers which control the bit switches.

An internal offset voltage V_{OFF} is added to the full scale output voltage V_{FS}; V_{OFF} and V_{FS} are proportional to V_{DD}: Where $V_{DD1}/V_{DD2} = V_{FS1}/V_{FS2} = V_{OFF1}/V_{OFF2}$.

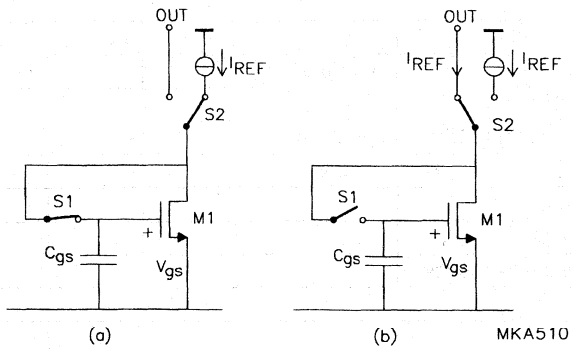


Fig.3 Calibration principle; (a) calibration (b) operation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–	6.0	V
T_{stg}	storage temperature		–55	+150	°C
T_{XTAL}	maximum crystal temperature		–	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic handling	note 1	–2000	+2000	V
		note 2	–200	+200	V

Notes

1. Human body model: C = 100 pF; R = 1500 Ω; 3 zaps positive and negative.
2. Machine model: C = 200 pF; L = 0.5 µH; R = 10 Ω; 3 zaps positive and negative.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	DIL8	100 K/W
	SO8	210 K/W

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; measured in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	positive supply voltage		4.0	5.0	5.5	V
I_{DD}	supply current	at code 0000H	–	3.4	6.0	mA
Digital inputs; pins WS, BCK and DATA						
$\|I_{IL}\|$	input leakage current LOW	V_I = 0 V	–	–	10	µA
$\|I_{IH}\|$	input leakage current HIGH	V_I = 5 V	–	–	10	µA
f_{BCK}	clock frequency		–	–	18.4	MHz
BR	bit rate data input		–	–	18.4	Mbits/s
f_{WS}	word select input frequency		–	–	384	kHz
Timing (see Fig.4)						
t_r	rise time		–	–	12	ns
t_f	fall time		–	–	12	ns
t_{CY}	bit clock cycle time		54	–	–	ns
t_{BCKH}	bit clock pulse width HIGH		15	–	–	ns
t_{BCKL}	bit clock pulse width LOW		15	–	–	ns
$t_{SU;DAT}$	data set-up time		12	–	–	ns
$t_{HD;DAT}$	data hold time to bit clock		2	–	–	ns
$t_{HD;WS}$	word select hold time		2	–	–	ns
$t_{SU;WS}$	word select set-up time		12	–	–	ns
Analog outputs; pins V_{OL} and V_{OR}						
V_{FS}	full-scale voltage		1.8	2.0	2.2	V
TC_{FS}	full-scale temperature coefficient		–	±400	–	ppm
V_{OFF}	offset voltage	at code 1000H	0.42	0.47	0.52	V
(THD+N)/S	total harmonic distortion plus noise	at 0 dB signal level; note 1	–	–68	–63	dB
			–	0.04	0.07	%
		at –60 dB signal level; note 1	–	–30	–24	dB
			–	3	6	%
		at –60 dB signal level; A-weighted; note 1	–	–33	–	dB
			–	2	–	%
		at 0 dB signal level; f = 20 Hz to 20 kHz	–	–65	–61	dB
			–	0.05	0.09	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog outputs; pins V_{OL} and V_{OR}						
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
α	channel separation		75	80	–	dB
$\lvert\delta I_O\rvert$	unbalance between outputs	note 1	–	0.2	0.3	dB
$\lvert t_d\rvert$	time delay between outputs		–	±0.2	–	µs
S/N	signal-to-noise ratio at bipolar zero	A-weighted; at code 0000H	86	92	–	dB

Note

1. Measured with 1 kHz sinewave generated at sampling rate of 192 kHz.

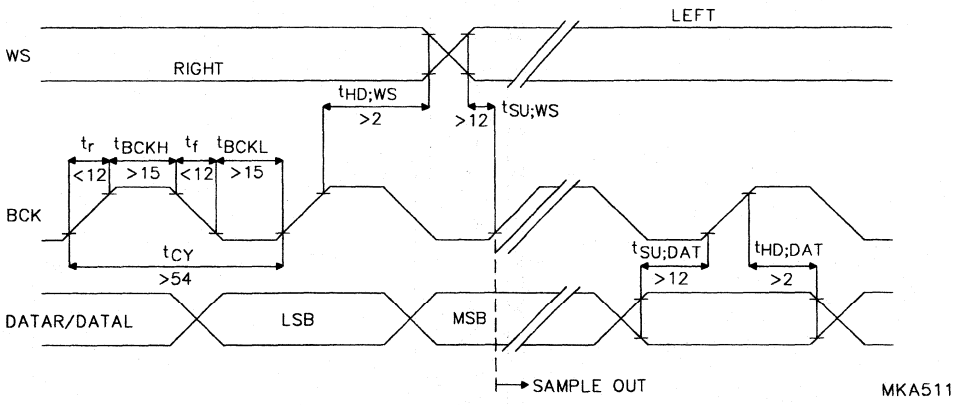


Fig.4 Input signals timing.

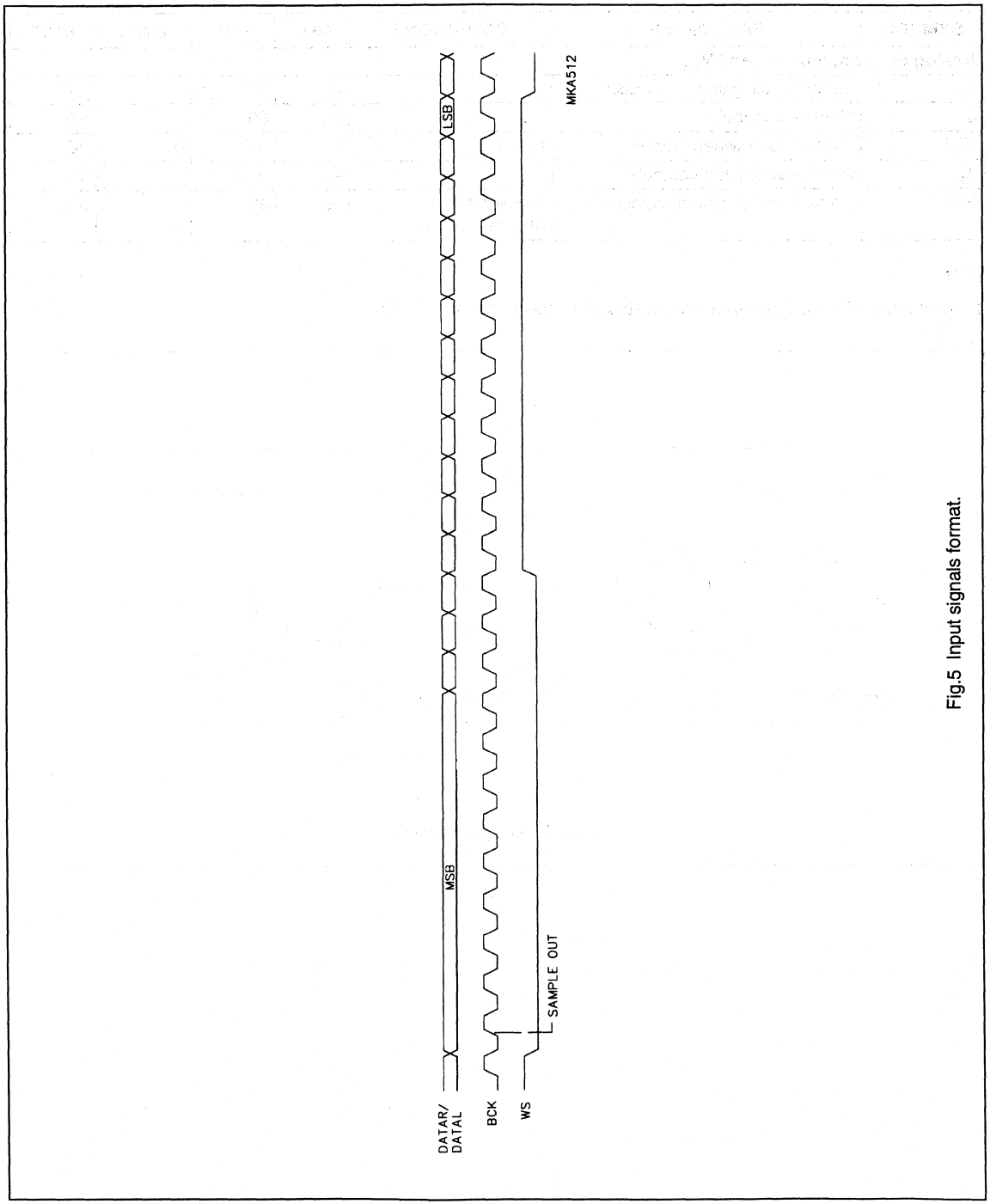


Fig.5 Input signals format.

Stereo continuous calibration DAC (CC-DAC)

TDA1313; TDA1313T

FEATURES

- 4/8 x oversampling (multiplexed/simultaneous input) possible
- Voltage output (capable of driving headphone)
- Space saving package (SO16 or DIL16)
- Low power consumption
- Wide dynamic range (16-bit resolution)
- Continuous Calibration concept
- Easy application:
  single 3 to 5.5 V supply rail
  output voltage is proportional to the supply voltage
  integrated current-to-voltage converter
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range (−40 °C to +85 °C)
- Compatible with most current Japanese input format multiplexed/simultaneous, two's complement and CMOS)
- No zero crossing distortion
- Cost efficient
- High signal-to-noise ratio
- Low total harmonic distortion.

GENERAL DESCRIPTION

The TDA1313; 1313T is a voltage driven digital-to-analog converter, and is of a new generation of DACs which incorporates the innovative technique of Continuous Calibration (CC). The largest bit-currents are repeatedly generated from one single current reference source. This duplication is based upon an internal charge storage principle having an accuracy which is insensitive to ageing, temperature and process variations.
The TDA1313; 1313T is fabricated in a 1.0 µm CMOS process and features an extremely low power dissipation, small package size and easy application. Furthermore, the accuracy of the intrinsic high coarse-current combined with the implemented symmetrical offset decoding method preclude zero-crossing distortion and ensures high quality audio reproduction. Therefore, the CC-DAC is eminently suitable for use in (portable) digital audio equipment.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1313	16	DIL	plastic	SOT38GG
TDA1313T	16	SO16	plastic	SOT109AG

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V; at code 0000H	–	8	9.5	mA
V_{FS}	full scale output voltage	V_{DD} = 5 V	3.8	4.2	4.6	V
(THD+N)/S	total harmonic distortion plus noise	at 0 dB signal level	–	–88	–81	dB
			–	0.004	0.009	%
		at 0 dB signal level; see Fig.8	–	–70	–	dB
			–	0.03	–	%
		at –60 dB signal level	–	–36	–28	dB
			–	1.6	4.0	%
		at –60 dB; A-weighted	–	–38	–	dB
			–	1.3	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	93	98	–	dB
t_{CS}	current setting time to ±1LSB		–	0.2	–	µs
BR	input bit rate at data input		–	–	18.4	Mbits/s
f_{BCK}	clock frequency at clock input		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (V_{OL}; V_{OR})		–	400	–	ppm
T_{amb}	operating ambient temperature		–40	–	+85	°C
P_{tot}	total power dissipation	V_{DD} = 5 V; at code 0000H	–	40	53	mW
		V_{DD} = 3 V; at code 0000H	–	15	–	mW

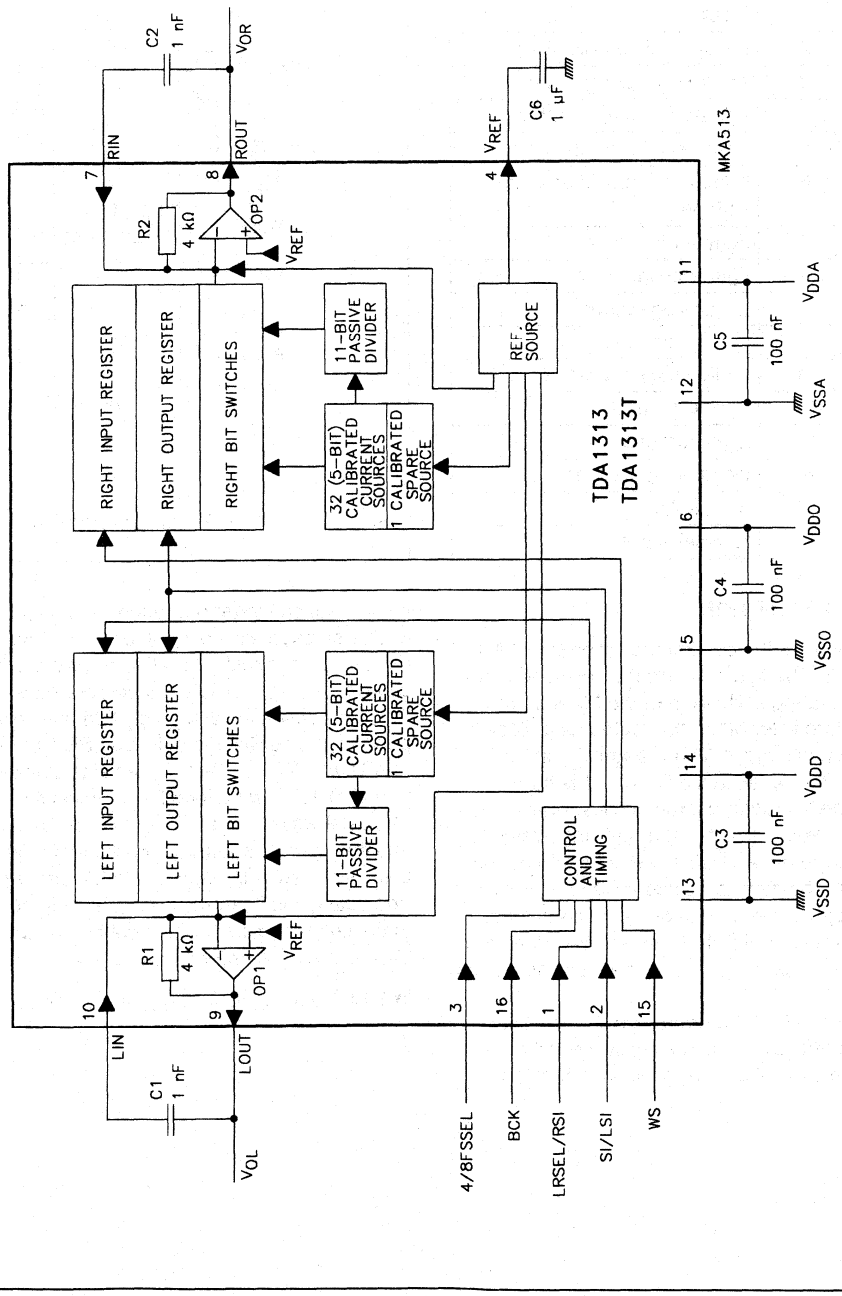


Fig.1 Block diagram.

Stereo continuous calibration DAC (CC-DAC)

TDA1313; TDA1313T

PINNING

SYMBOL	PIN	DESCRIPTION
LRSEL/RSI	1	left/right select; right serial input
SI/LSI	2	serial input; left serial input
4/8FSSEL	3	4/8 oversampling select
V_{REF}	4	reference voltage output
V_{SSO}	5	operational amplifier ground
V_{DDO}	6	operational amplifier supply voltage
RIN	7	right analog input
ROUT	8	right analog output
LOUT	9	left analog output
LIN	10	left analog input
V_{DDA}	11	analog supply voltage
V_{SSA}	12	analog ground
V_{SSD}	13	digital ground
V_{DDD}	14	digital supply voltage
WS	15	word select
BCK	16	bit clock input

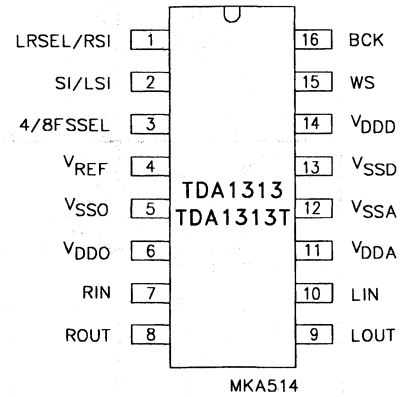


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The basic operation of the continuous calibration DAC is illustrated in Fig.3. The figure shows the calibration and operation cycle. During calibration of the MOS current source (Fig.3a) transistor M1 is connected as a diode by applying a reference current. The voltage V_{gs} on the intrinsic gate-source capacitance C_{gs} of M1 is then determined by the transistor characteristics. After calibration of the drain current to the reference value I_{REF}, the switch S1 is opened and S2 is switched to the other position (Fig.3b). The gate-to-source voltage V_{gs} of M1 is not changed because the charge on C_{gs} is preserved. Therefore, the drain current of M1 will still be equal to I_{REF} and this exact duplicate of I_{REF} is now available at the I_O terminal.

In the TDA1313; 1313T, 32 current sources and one spare current source are continuously calibrated (see Fig.1). The spare current source is included to allow continuous converter operation. The output of one calibrated source is connected to an 11-bit binary current devider which consists of 2048 transistors. A symmetrical offset decoding principle is incorporated and arranges the bit switching in such a way that the zero-crossing is performed by switching only the LSB currents.

The TDA1313; T (CC-DAC) accepts serial input data format of 16 bit word length. The most significant bit (bit 1) must always be first. The timing is illustrated in Fig.4 and the input data formats are illustrated in Figs 5 and 6. Data is placed in the right and left input registers (Fig.1). The data in the input registers is simultaneously latched to the output registers which control the bit switches. V_{REF} and V_{FS} are proportional to V_{DD}.

Where: $V_{DD1}/V_{DD2} = V_{FS1}/V_{FS2} = V_{REF1}/V_{REF2}$

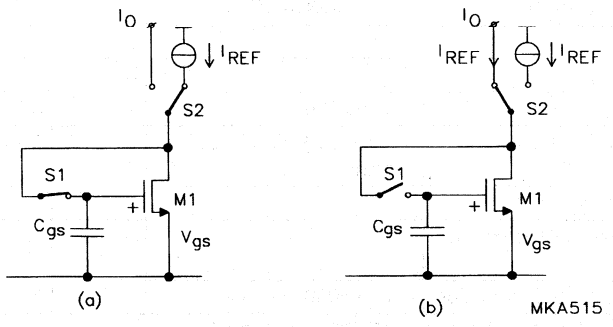


Fig.3 Calibration principle; (a) calibration (b) operation.

Table 1 Mode application.

4/8FSSEL	LRSEL/RSI	MODE	FIGURE
0	1	4FS/left = HIGH	6
0	0	4FS/left = LOW	6
1	data right	8FS	5

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–	6.0	V
T_{XTAL}	maximum crystal temperature		–	+150	°C
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{ES}	electrostatic handling	note 1	–2000	+2000	V
		note 2	–200	+200	V

Notes

1. Human body model: C = 100 pF; R = 1500 Ω; 3 zaps positive and negative.
2. Machine model: C = 200 pF; L = 0.5 µH; R = 10 Ω; 3 zaps positive and negative.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air DIL16 SO16	 75 K/W 120 K/W

CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = 5$ V; $T_{amb} = 25$ °C; measured in Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	total supply current	at code 0000H	–	8.0	9.5	mA
I_{DDD}	digital supply current	at code 0000H; no clock running	–	0.2	–	mA
I_{DDA}	analog supply current		–	4.6	5.5	mA
I_{DDO}	operational amplifier supply current		–	3.4	4	mA
PSRR	power supply ripple rejection	at code 0000H; note 1	–	30	–	dB
Digital inputs; pins WS, BCK, 4/8FSSEL, LRSEL/RSI and SI/LSI						
$\|I_{IL}\|$	input leakage current LOW	$V_I = 0.V$	–	–	10	µA
$\|I_{IH}\|$	input leakage current HIGH	$V_I = 5.5$ V	–	–	10	µA
f_{BCK}	clock frequency		–	–	18.4	MHz
BR	bit rate data input		–	–	18.4	Mbits/s
f_{WS}	word select input frequency		–	–	384	kHz
Timing (see Fig.4)						
t_r	rise time		–	–	12	ns
t_f	fall time		–	–	12	ns
t_{CY}	bit clock cycle time		54	–	–	ns
t_{BCKH}	bit clock pulse width HIGH		15	–	–	ns
t_{BCKL}	bit clock pulse width LOW		15	–	–	ns
$t_{SU;DAT}$	data set-up time		12	–	–	ns
$t_{HD;DAT}$	data hold time to bit clock		10	–	–	ns
$t_{HD;WS}$	word select hold time		10	–	–	ns
$t_{SU;WS}$	word select set-up time		12	–	–	ns
Analog outputs; pins V_{OL} and V_{OR}						
V_{FS}	full-scale voltage		3.8	4.2	4.6	V
TC_{FS}	full-scale temperature coefficient		–	±400	–	ppm
R_L	load resistance		3	–	–	kΩ
C_L	load capacitance		–	–	200	pF
V_{REF}	reference output voltage		3.16	3.33	3.5	V
V_{DC}	output DC voltage		2.25	2.5	2.75	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog outputs; pins V_{OL} and V_{OR}						
(THD+N)/S	total harmonic distortion plus noise	at 0 dB signal level; note 2	–	–88	–81	dB
			–	0.004	0.009	%
		at 0 dB signal level; see Fig.8	–	–70	–	dB
			–	0.03	–	%
		at –60 dB signal level; note 2	–	–36	–28	dB
			–	1.6	4.0	%
		at –60 dB signal level; A-weighted; note 2	–	–38	–	dB
			–	1.3	–	%
		at 0 dB signal level; f = 20 Hz to 20 kHz	–	–84	–70	dB
			–	0.006	0.03	%
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
α	channel separation		86	95	–	dB
		see Fig.8	–	70	–	dB
$\lvert\delta I_O\rvert$	unbalance between outputs	note 2	–	0.2	0.3	dB
$\lvert t_d\rvert$	time delay between outputs		–	±0.2	–	µs
S/N	signal-to-noise ratio at bipolar zero	A-weighted; at code 0000H	93	98	–	dB

Notes

1. V_{ripple} = 1% of the supply voltage; f_{ripple} = 100 Hz.
2. Measured with 1 kHz sinewave generated at a sampling rate of 384 kHz.

QUALITY SPECIFICATION

In accordance with UZW-BO/FQ-0601.

TEST AND APPLICATION INFORMATION

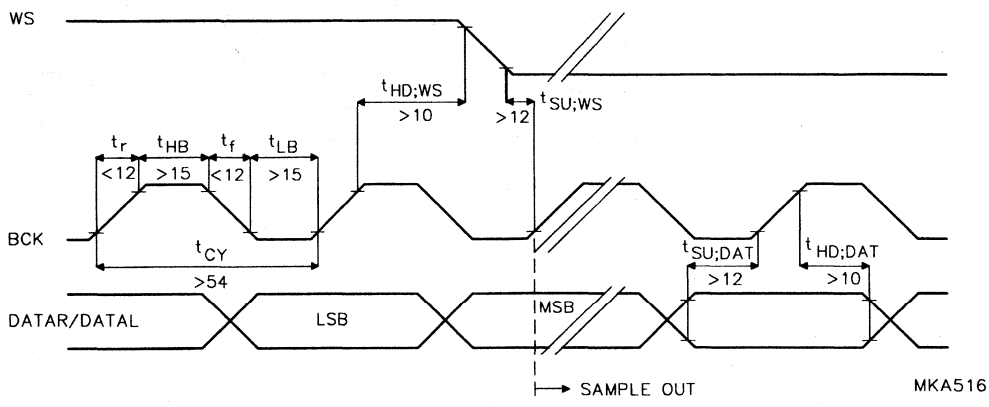


Fig.4 Timing of input signals.

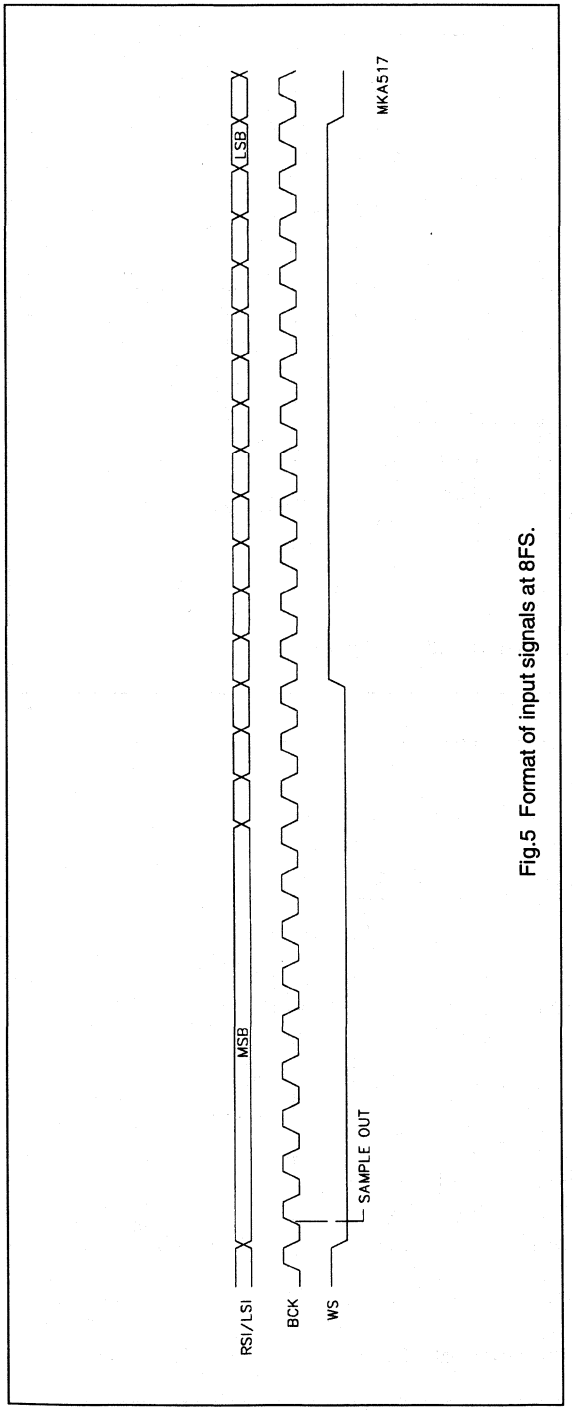


Fig.5 Format of input signals at 8FS.

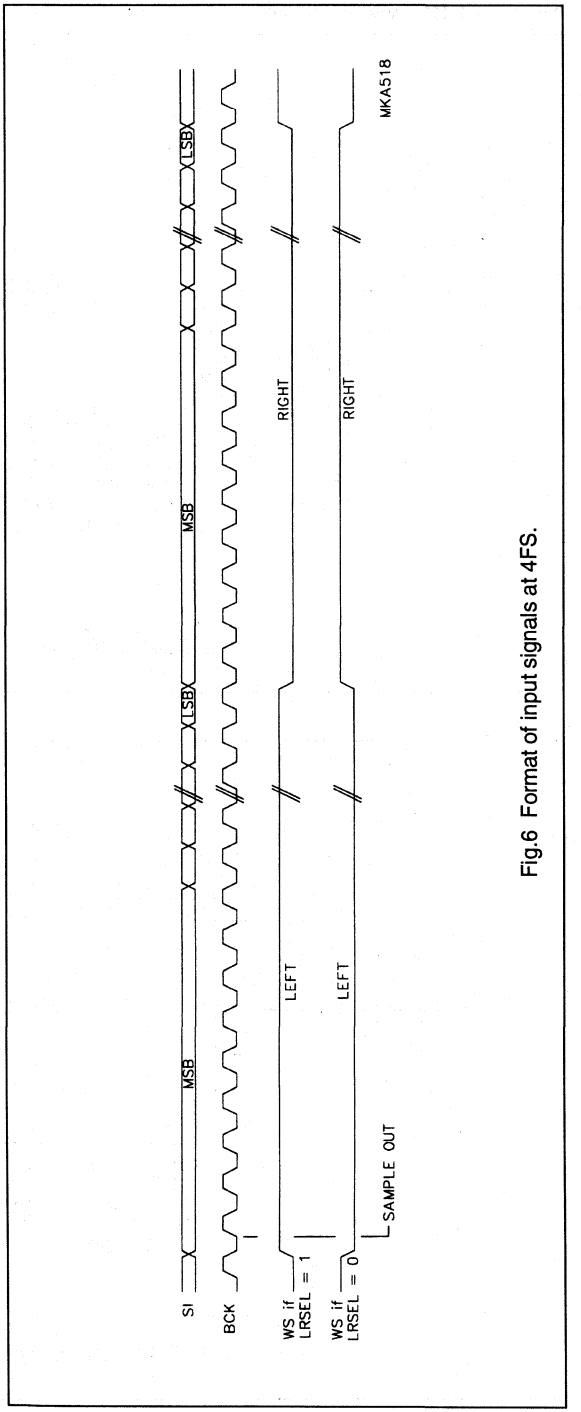


Fig.6 Format of input signals at 4FS.

APPLICATION INFORMATION

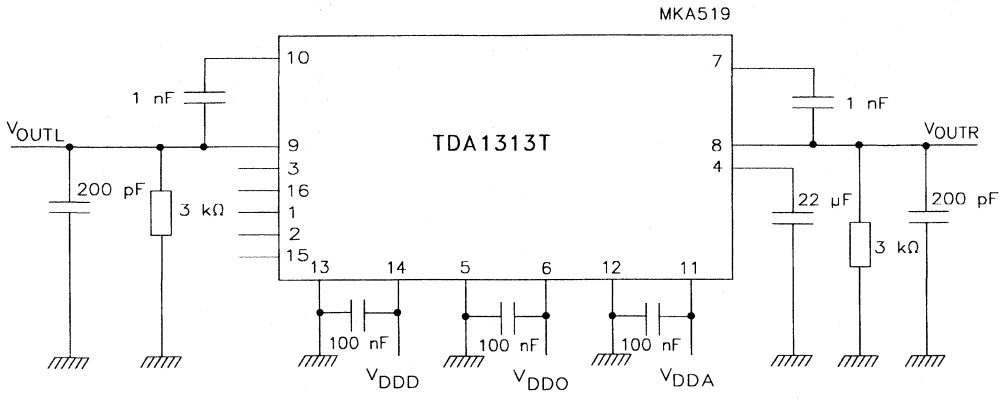


Fig.7 TDA1313T as line driver with 3 kΩ/200 pF load.

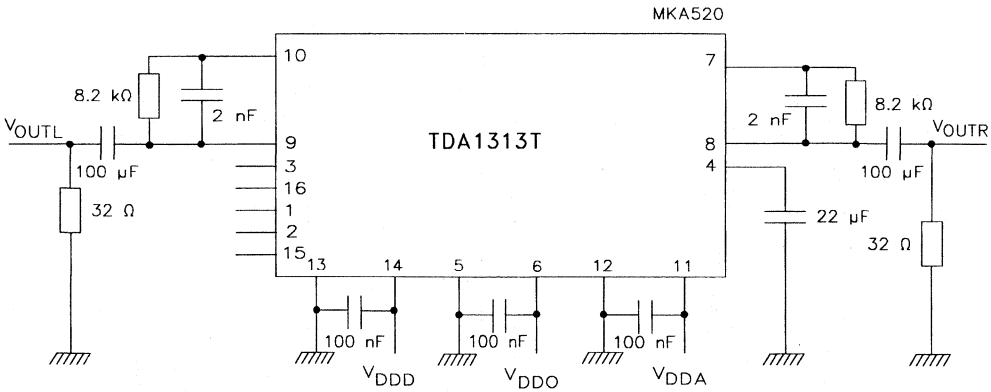


Fig.8 TDA1313T as headphone driver with 32 Ω load.

Quadruple filter DAC TDA1314T

FEATURES

- High dynamic range to enable digital DSP (Digital Signal Processor) volume control
- 18 bits data input format for each of the four channels
- Four times bit-serial oversampling filter
- 1st-order $4f_{as}$ (audio sampling frequency) noise shaper
- Four very low noise DACs
- Only 1st-order analog post filtering required
- Smooth power-on of the DAC output currents
- Because of the automatic digital PLL divider range setting the master clock is selectable in a wide $4f_{as}$ integer range
- Insensitive to jitter on the I^2S-bus signals with respect to the DAC total harmonic distortion deterioration.

APPLICATIONS

- Stand-alone quadruple low noise DAC
- Car radio DAC in conjunction with DSP.

GENERAL DESCRIPTION

The TDA1314T is a quadruple very low noise high dynamic range DAC which is intended for use in motor cars and is controlled by the car radio DSP. Each channel incorporates an 8th-order IIR up-sampling filter from 1ASF to 4ASF followed by a 1st-order noise shaper and DAC. The DAC currents are converted to audio voltage signals using operational amplifiers (one per channel).

QUICK REFERENCE DATA

V_{ref} = 2.5 and 5 V; T_{amb} = 25 °C; all voltages referenced to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
$I_{O(DAC)}$	DAC output current (FS)	R_{ref} = 20.5 kΩ	±0.4	±0.5	±0.6	mA
$V_{O(DAC)}$	DAC output voltage, nominal DAC operational amplifier output voltage	$R_L \geq 5$ kΩ; R_{fb} = 3 kΩ	1.0	–	4.0	V
RES	DAC resolution	length of data input word	–	–	18	bits
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	f_i = 1 kHz; 0 dB signal level	–	–66	–56	dB
DR	dynamic range of DAC	f_i = 1 kHz; –60 dB signal level	92	96	–	dB
DS	digital silence	no signal; A-weighted	–	–110	–100	dB
P_{tot}	total power dissipation		–	85	–	mW
T_{amb}	operating ambient temperature		–40	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1314T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

BLOCK DIAGRAM

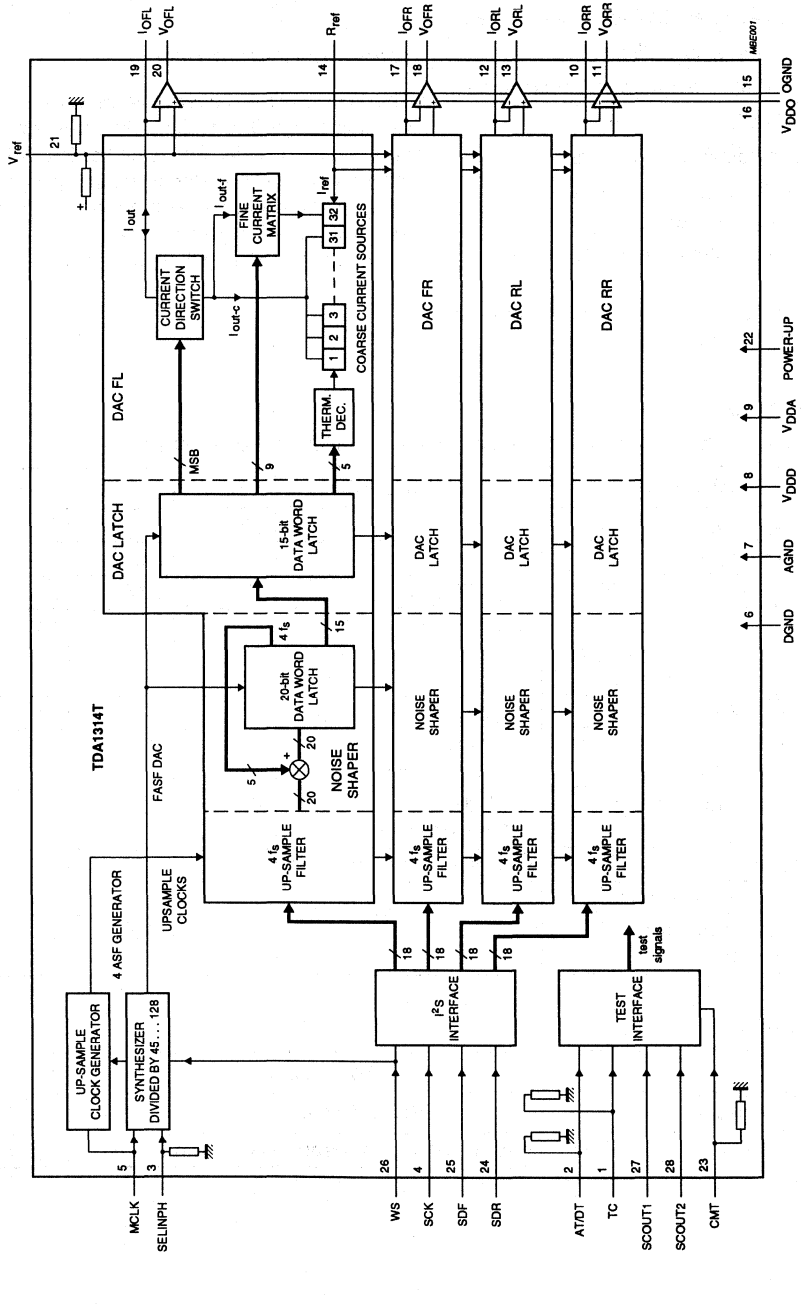


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TC	1	test control signal input (test/operational)
AT/DT	2	analog test/digital test select input
SELINPH	3	select in-phase $4f_{as}$ mode/scan input signal 1 in test mode
SCK	4	serial clock input; I^2S-bus
MCLK	5	master clock input; $f_i = N \times 4f_{as}$ ($45 \leq N \leq 128$)
DGND	6	digital ground
AGND	7	analog ground
V_{DDD}	8	digital supply voltage
V_{DDA}	9	analog supply voltage
I_{ORR}	10	DAC output current; rear right
V_{ORR}	11	DAC output voltage; rear right
I_{ORL}	12	DAC output current; rear left
V_{ORL}	13	DAC output voltage; rear left
R_{ref}	14	resistor reference input for DACs current
OGND	15	operational amplifier ground
V_{DDO}	16	operational amplifier supply
I_{OFR}	17	DAC output current; front right
V_{OFR}	18	DAC output voltage; front right
I_{OFL}	19	DAC output current; front left
V_{OFL}	20	DAC output voltage; front left
V_{ref}	21	reference voltage input ($\frac{1}{2}$ operational amplifier supply voltage)
POWER-UP	22	analog mute input for all DACs
CMT	23	current mirror input test signal
SDR	24	serial data input for rear DACs (I^2S-bus); scan input signal 2 in test mode
SDF	25	serial data input for front DACs (I^2S-bus)
WS	26	word select input (I^2S-bus)
SCOUT1	27	scan output signal 1 in test mode; $4f_{as}$ signal
SCOUT2	28	scan output signal 2 in test mode; PLL lock indicator

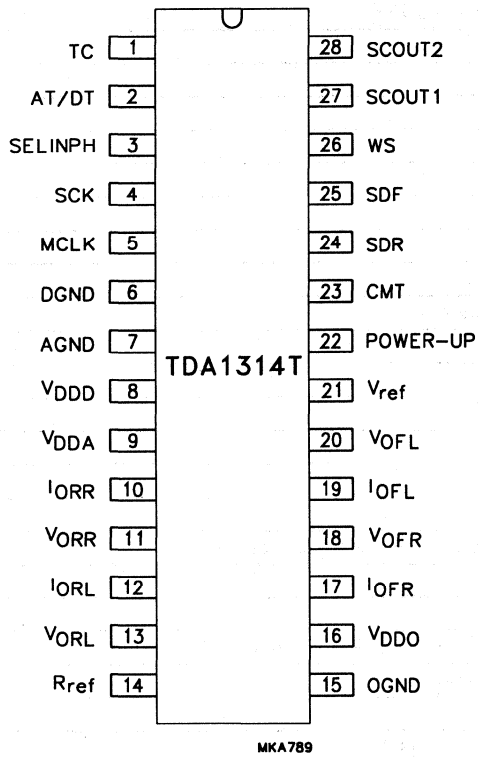


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

I²S-bus interface

The word select input (pin 26) is connected to the word select line of the I²S-bus interface. This interface has a standard I²S-bus specification as described in the Philips *"I²S-bus specification"* (ordering number 9398 332 10011). Figure 4 shows an excerpt of the Philips I²S-bus specification interface report with respect to the general timing and format of the I²S-bus. WS logic 0 means left channel word, logic 1 means right channel word.

The serial clock input (pin 4) must be in accordance with the I²S-bus specification, i.e. a continuous clock.

Serial data front (SDF, pin 25) and serial data rear (SDR, pin 24) are the I²S-bus serial data lines to be processed in the DACs for the loudspeakers of the car (see Fig.2, blocks DACFL and DACFR for the front loudspeakers and blocks DACRL and DACRR for the right loudspeakers). FL stands for Front Left, FR for Front Right, RL for Rear Left and RR for Rear Right. In order to utilize the capabilities of this IC fully, the data word length should be 18 bits. Signals derived from this block are 4 × 18-bit parallel data words which are applied to the $4f_s$ up-sample filters.

4ASF generator

SYNTHESIZER

SELINPH (pin 3) and WS (pin 26) are the data inputs for this block which generates the FASFDAC, this being the $4f_{as}$ signal (at 4 times the audio sample frequency), which is used to latch the data words to the DACs and as a reference to the clock generator block for the up-sample filters. It consists of a digital PLL operating at the master clock signal MCLK (pin 5). In normal mode (i.e. in the event that the MCLK signal on pin 5 is a jitter free clock, with a frequency of integer multiples between 45 and 128, of 4 times the frequency of the WS signal) this block is able to generate a jitter free FASFDAC signal for optimum performance of the DAC. This mode is called the free running mode.

If, in some applications, there is considerable jitter on the MCLK while WS is more stable (less jitter), the phase-locked mode should be selected. This mode is normally not used and is not recommended.

UP-SAMPLE GENERATOR

This block generates the clocks for the up-sample filters.The external pinning of the $4f_{as}$ generator block is:

- MCLK (see Fig.4), which is a jitter free (maximum 30 ns jitter) external clock at any multiple integer from 45 to 128 times $4f_{as}$ (4 times the frequency of WS) of the I^2S-bus input, thus for a sample frequency of 38 kHz this clock frequency will range from 6.840 MHz to 19.456 MHz in multiples of 152 kHz.
- The select in-phase (SELINPH) or free running mode of the synthesizer 45 to 128. In the normal application the free-running mode is used and this pin is not connected (this pin is pulled down by an internal resistor). The phase-locked mode can be selected by hard-wiring this pin to V_{DDD} (pin 8). However, this mode is not recommended.

Test interface

This block controls the circuit in the test mode, which can be either an analog or digital test mode. Test pins TC (pin 1), AT/DT (pin 2), CMT (pin 23), SCOUT1 (pin 27) and SCOUT2 (pin 28) are not connected in Fig.6.

Up-sample filter and noise shaper

The signal flow applied to the up-sample filter and noise shaper blocks is the 4×18-bit parallel data words in two's complement format from the I^2S-bus interface at the audio sampling frequency. The signal flow from these blocks is the 4×15-bit parallel data words in two's complement format at a frequency of $4f_{as}$. Each of the four digital filters is a four times up-sampling filter. This up-sampling filter is an elliptic filter of 8th order.

The filters produce an attenuation of 29 dB (min) for signals outside the audio band. The noise shaper operates at $4f_{as}$ and reduces the word length from 22 bits to 15 bits which is the word length of the DAC.

DAC input signals

The following signals are input to the DAC blocks FL, FR, RL and RR:

- DATA WORD (bits 10 to 14). These 5 bits are used to control, via a thermometer decoder, the current of the 32 coarse current sources of the analog DAC part. The value of this data word determines the total coarse current flowing to the DAC current output. The value of the current of each coarse current source is determined by the following:

  R_{ref}; this is the current reference input at pin 14 and is at the same voltage level as V_{ref}. A resistor connected to OGND results in a current. This being the reference current of the coarse current sources and subsequently of the DAC in total.
- DATA WORD (bits 1 to 9). A current from one of the coarse current sources is fed into a 512 transistor matrix. The value of the DATA WORD (bits 1 to 9) determines which part of one coarse current flows to the DAC current output.
- DATA WORD (bit 15). This data word MSB controls the direction of the flow of the DAC output current by switching the current direction switch.
- V_{ref}. Voltage reference pin internally connected to a resistor divider to obtain half of the power supply voltage. This voltage is buffered and used as reference voltage input for the operational amplifiers and as a reference voltage in the DAC.
- POWER-UP. The analog signal on this pin controls the current biasing circuit of the DACs. This pin is connected internally via a high value resistor to V_{DDA}. Together with an external capacitor a soft switch-on of the DAC output currents is obtained. This pin can also be used as the analog mute input for all DAC output currents by pulling it to ground.

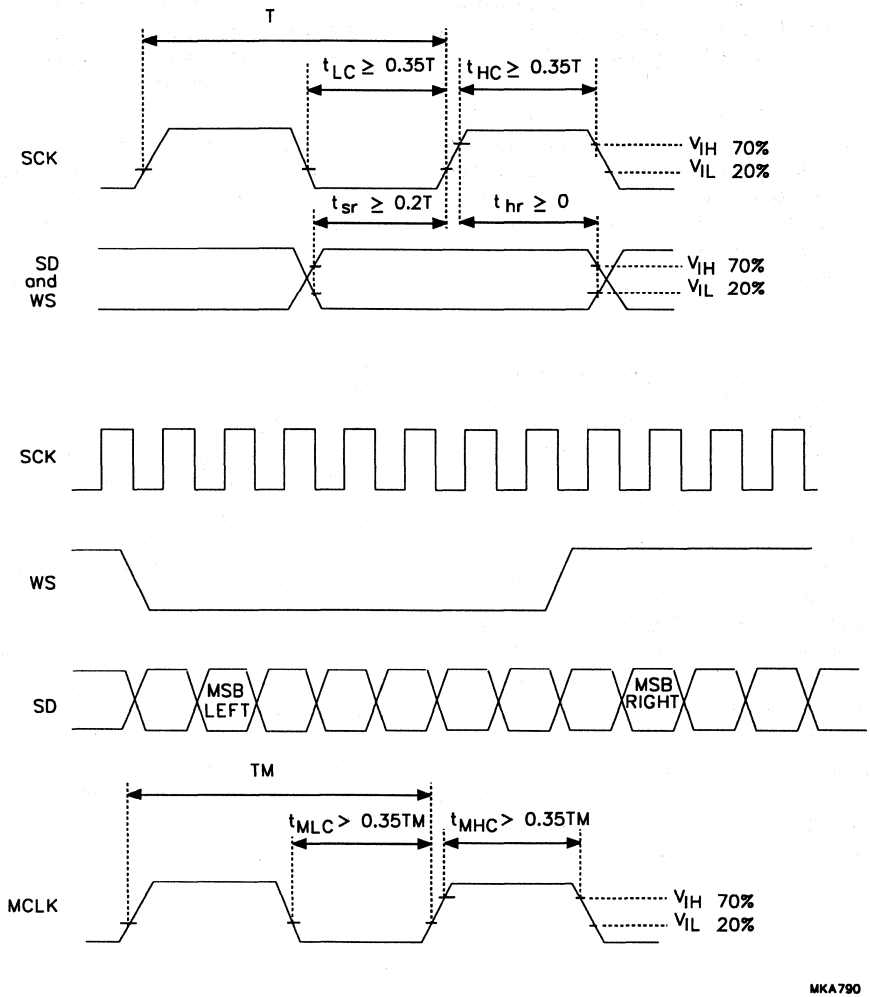


Fig.3 I²S-bus timing and format.

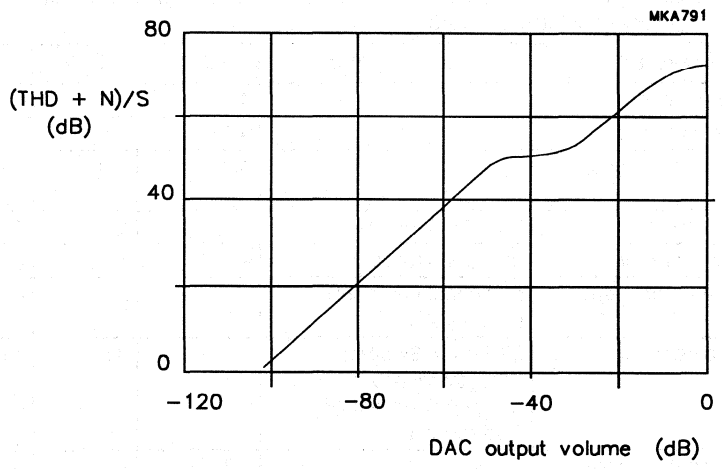


Fig.4 Total harmonic distortion plus noise-to-signal ratio as a function of output volume.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	0	6.0	V
V_{DDA}	analog supply voltage	note 1	0	6.0	V
V_{DDO}	operational amplifier supply voltage	note 1	0	6.0	V
V_n	voltage on any other pin		0	V_{DD}	V
T_{xtal}	crystal temperature		–	+150	°C
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{es}	electrostatic handling	note 2	−2000	+2000	V

Notes

1. All voltages (pins 6, 7 and 15) referenced to ground.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	76	K/W

DC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{DDA} = V_{DDO} = 4.75 to 5.25 V; all voltage referenced to ground (pins 6, 7 and 15); measured in test circuit of Fig.6; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
V_{DDA}	analog supply voltage		4.75	5.0	5.25	V
V_{DDO}	operational amplifier supply voltage		4.75	5.0	5.25	V
I_{DDD}	digital supply current	MCLK = 6.84 MHz	–	10	17	mA
I_{DDA}	analog supply current	at digital silence	–	5	8	mA
I_{DDO}	operational amplifiers supply current	no operational amplifier load resistor	–	2	4	mA
P_{tot}	total power dissipation	MCLK = 6.84 MHz; at digital silence; no operational amplifier load resistor	–	85	145	mW
V_{IH}	HIGH level input voltage pins 1 to 5 and 23 to 26		$0.7V_{DDD}$	–	–	V
V_{IL}	LOW level input voltage pins 1 to 5 and 23 to 26		–	–	$0.2V_{DDD}$	V
V_{OH}	HIGH level output voltage pins 27 and 28	V_{DDD} = 4.5 V; I_O = –4 mA	4.1	–	–	V
		V_{DDD} = 5.5 V; I_O = –4.5 mA	5.1	–	–	V
V_{OL}	LOW level output voltage pins 27 and 28	V_{DDD} = 4.5 V; I_O = 4 mA	–	–	0.4	V
		V_{DDD} = 5.5 V; I_O = 4.5 mA	–	–	0.4	V
V_{ref}	reference input voltage	with respect to OGND	$0.45V_{DDO}$	$0.5V_{DDO}$	$0.55V_{DDO}$	V
Z_I	input impedance at pin 21	with respect to V_{DDO}	15	20	30	kΩ
		with respect to OGND	15	20	30	kΩ
V_I	input voltage pin 14	with respect to OGND	$0.43V_{DDO}$	$0.5V_{DDO}$	$0.57V_{DDO}$	V
$I_{ODAC(max)}$	maximum output current from DACs pins 10, 12, 17 and 19	R_{ref} = 20.5 kΩ; V_{DDO} = 5 V	400	500	600	μA
$V_{O(os)}$	DC offset voltage at pins 10, 12, 17 and 19	with respect to V_{ref}	–	5	–	mV
$V_{OH(O)}$	HIGH level output voltage of operational amplifiers at pins 11, 13, 18 and 20	note 1; R_L > 5 kΩ; R_{fb} = 3 kΩ; maximum signal	V_{DDO} – 1.3	V_{DDO} – 1	V_{DDO} – 0.45	V
$V_{OL(O)}$	LOW level output voltage of operational amplifiers at pins 11, 13, 18 and 20	note 1; R_L > 5 kΩ; R_{fb} = 3 kΩ; maximum signal	0.45	1.0	1.3	V
R_{pu}	internal resistance at pin 22	with respect to V_{DDO}	110	160	240	kΩ
R_{pd}	internal resistance at pins 1 to 3 and 23	V_i = V_{DDD}; with respect to DGND	27	–	80	kΩ

Note

1. R_L is the AC impedance of the external circuitry connected to the audio outputs in the application diagram of Fig.6.

AC CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = 5$ V; $T_{amb} = 25$ °C; all voltages referenced to ground (pins 6, 7 and 15) measured in test circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ANALOG						
DACs						
SVRR	supply voltage ripple rejection pins 9 and 16	f_{ripple} = 1 kHz; V_{ripple} = 100 mV (peak); C_{Vref} = 22 µF	30	46	–	dB
$\Delta I_{O(DAC)}$	maximum deviation of output level of the 4 DAC output currents with respect to the average of the 4 outputs	maximum volume	–	–	0.38	dB
α_{DAC}	crosstalk between the 4 DAC current outputs	2 outputs at digital silence; 2 outputs at maximum volume	–	–90	–60	dB
RES	DAC resolution		–	–	18	bits
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	f_i = 1 kHz; 0 dB signal	–	–66	–56	dB
		f_i = 1 kHz; –60 dB signal; A-weighted	–	–36	–32	dB
DR	dynamic range	f_i = 1 kHz; –60 dB signal; A-weighted	92	96	–	dB
DS	digital silence	f_i = 20 Hz to 17 kHz; A-weighted	–	–110	–100	dB
Operational amplifiers						
G_v	open loop voltage gain		–	85	–	dB
PSRR	power supply ripple rejection	f_{ripple} = 3 kHz; V_{ripple} = 100 mV (peak)	–	90	–	dB
(THD + N)/S	total harmonic distortion plus noise as a function of the operational amplifiers signal	R_L > 5 kΩ (AC); R_{fb} = 3 kΩ; V_O = 0.28 V (p-p); f_i = 1 kHz; A-weighted	–	–82	–	dB
f_{ug}	unity gain frequency	open loop	–	4.5	–	MHz
Z_o	output impedance	R_L > 5 kΩ	–	1.5	150	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DIGITAL						
I^2S-BUS, UP-SAMPLING FILTER AND NOISE SHAPER						
f_{SCK}	serial clock input frequency	ASF = 38 kHz	1.368	–	19.456	MHz
t_{LC}	serial clock LOW time	at 20% V_{DDD}; $T = \frac{1}{f_{SCK}}$	0.35T	–	–	µs
t_{HC}	serial clock HIGH time	at 70% V_{DDD}; $T = \frac{1}{f_{SCK}}$	0.35T	–	–	µs
f_{WS}	word select input frequency		38	44.1	48	kHz
t_{sr}	set-up time from SDF, SDR and WS to HIGH going edge of SCK	$T = \frac{1}{f_{SCK}}$	0.2T	–	–	µs
t_{hr}	hold time from SDF, SDR and WS to HIGH going edge of SCK	$T = \frac{1}{f_{SCK}}$	0	–	–	µs
f_{MCLK}	master clock input frequency	$N \times 4 \times f_{WS}$; where N = integer	$45 \times 4f_{WS}$	$64 \times 4f_{WS}$	$128 \times 4f_{WS}$	kHz
t_{MLC}	master clock LOW time	$TM = \frac{1}{f_{SCK}}$	0.35TM	–	–	µs
t_{MHC}	master clock HIGH time	$TM = \frac{1}{f_{SCK}}$	0.35TM	–	–	µs
PR	pass band ripple of digital filter	with sample-and-hold from DAC	–	0.46	–	dB
α_{SB}	stop band attenuation	f_i > 22 kHz; no post filter	29	–	–	dB

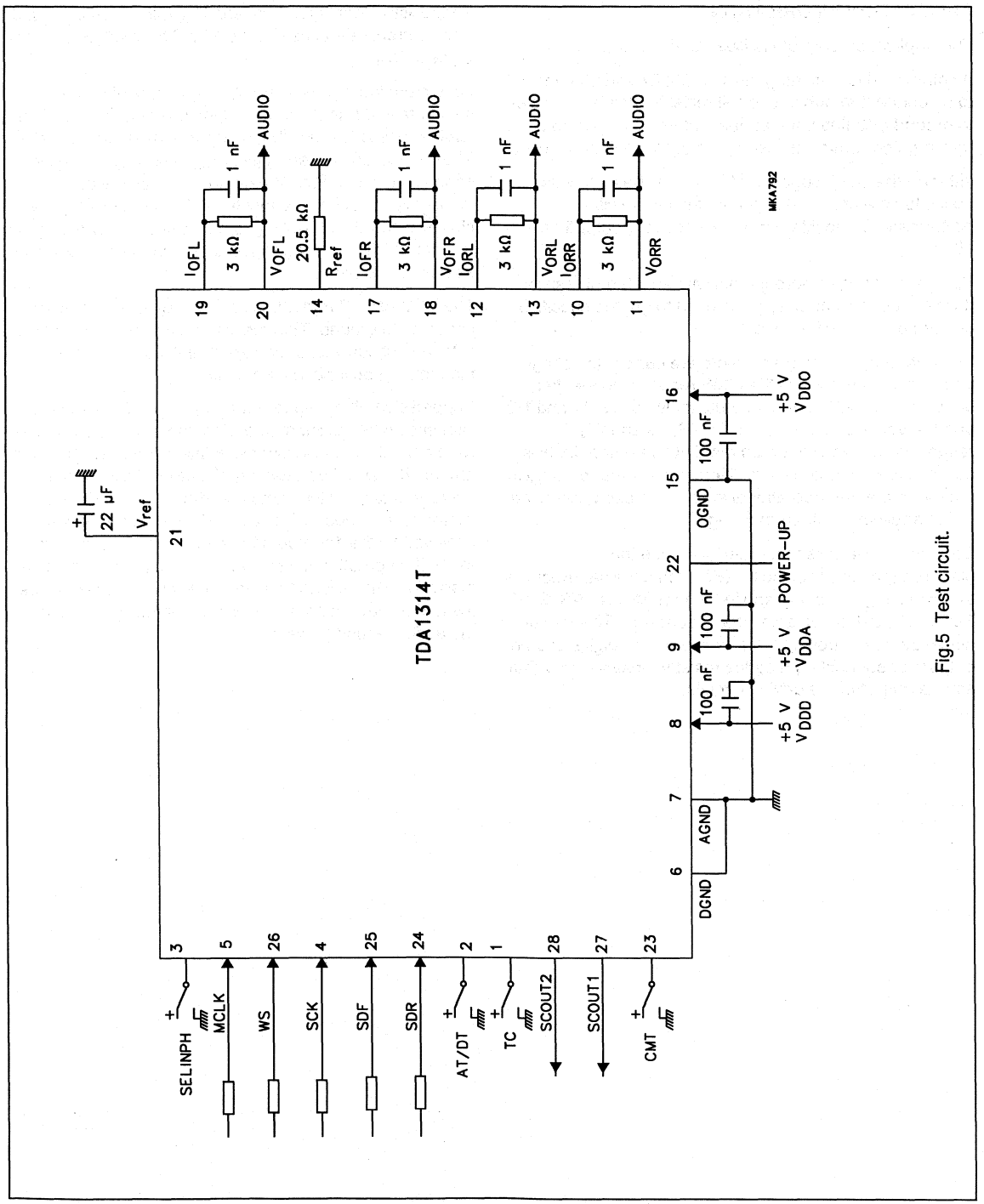


Fig.5 Test circuit.

APPLICATION INFORMATION

The application diagram is illustrated in Fig.6.

All pins used for testing (pins 1, 2, 23, 27 and 28 need not to be connected due to internal resistors being connected to ground or being used as test outputs. In the normal free-running mode it is also not required to connect pin 3.

Jitter on the clock edges of MCLK must be as low as possible so as not to deteriorate the DAC THD performance. The jitter time must not be greater than 30 ns.

V_{ref} is the voltage reference pin with an internal resistor divider. A capacitor of 22 µF is used to get the specified power ripple rejection ratio.

The output operational amplifiers are current-to-voltage converters by means of the 3 kW resistors connected between the DAC current outputs (pins 10, 12, 17 and 19) and the voltage outputs (pins 11, 13, 18 and 20) respectively. The voltage on the DAC current outputs is equal to the operational amplifiers virtual ground at V_{ref} in the event that the operational amplifier is used according to the application diagram of Fig.6.

Care should be taken, in order to reduce the electromagnetic compatibility (EMC) that the bandwidth of the digital signals being applied to pins MCLK, WS, SCK, SDF and SDR is not larger than necessary. This can be achieved by controlling the slew rate of the digital source outputs or connecting a series resistor close to the digital source output of the driving circuits.

The resistor connected between R_{ref} (pin 14) and ground is the current reference of the DACs. The voltage on R_{ref} is equal to V_{ref}.

On the printed-circuit board V_{SSA} (pin 7) is also the substrate and has the most negative voltage of the IC, a large as possible ground plane is therefore recommended. The connection between V_{SSA}, V_{SSD} and V_{SSO} must be as short as possible. Pins V_{DDO} and V_{DDA} (pins 9 and 16) must have capacitors connected to the V_{SSA} ground plane closest to the chip. Pin V_{DDD} (pin 8) is fed via a small series resistor (25 Ω). This resistor must be connected as close as possible to pin 8.

The POWER-UP (pin 22) is connected via an electrolytic capacitor to ground. This results in a smooth rising of the DAC output currents at power-on. If this is not required then this capacitor can be omitted.

Suppression of the higher harmonics by the up-sample filter should be sufficient to protect the amplifiers and the tweeter loudspeakers from excessive HF noise. The band around $4f_s$ cannot be attenuated by the 4ASF filter and is only attenuated by the sample-and-hold effect of the DAC. At frequencies above 100 kHz, additional attenuation achieved by the 1st order post filter, which is built around the buffer operational amplifiers. In total a 2nd order level of filtering can be found above 100 kHz. In terms of power the audio out-of-band power is approximately 15×10^{-4} of the audio in-band power.

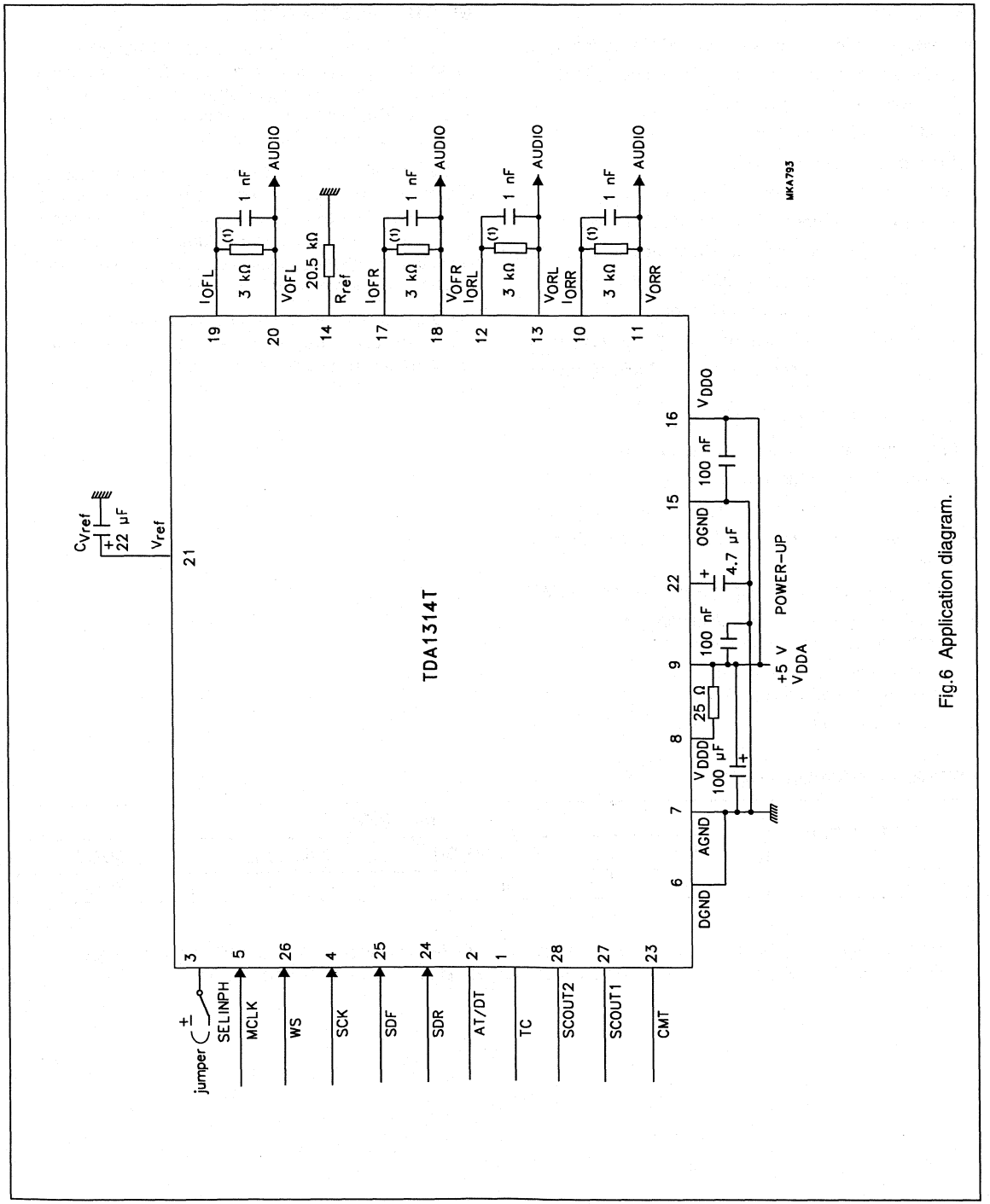


Fig.6 Application diagram.

Digital audio input/output circuit (DAIO) TDA1315H

FEATURES

- Transceiver for SPDIF and *"IEC 958"* encoded signals
- High sensitivity input for transformer-coupled links
- TTL-level input for optical links
- Built-in IEC input selector
- Built-in IEC feed-through function
- Automatic sample frequency (f_s) detection
- System clock recovery from IEC input signal
- Low system clock drift when IEC input signal is removed
- Error detection and concealment
- PLL lock detection in transmit mode
- Serial audio interface conforms to I^2S-bus format
- Auxiliary I^2S-bus input for Analog-to-Digital Converter (ADC)
- Audio output selector
- Microcontroller-controlled and stand-alone mode
- 128-byte buffer for user data
- Bytewise exchange of user data with microcontroller
- Decoding of Compact Disc (CD) subcode Q-channel data
- Support for serial copy management system (SCMS)
- Light Emitting Diode (LED) drive capability (sample frequency and error indication)
- Pin-selectable device address for microcontroller interface
- Power-down mode.

GENERAL DESCRIPTION

The Digital Audio Input/Output circuit (DAIO) of the TDA1315H is a complete transceiver for biphase-mark encoded digital audio signals that conform to the SPDIF and *"IEC 958"* interface standards (consumer mode), made in the full CMOS-process C200.

In the receive mode, the device adjusts automatically to one of the three standardized sample frequencies (32, 44.1 or 48 kHz), decodes the input signal and separates audio and control data. A clock signal of either 256 or 384 times the sample frequency is generated to serve as a master clock signal in digital audio systems.

In the transmit mode, the device multiplexes the audio, control and user data and encodes it for subsequent transmission via a cable or optical link.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1315H	44	QFP[1]	plastic	SOT307-2

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* are followed. The pocketbook can be ordered using the code 9398 510 34011.

QUICK REFERENCE DATA

All inputs are TTL compatible; all outputs are CMOS compatible; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	$V_{DDD} = V_{DDA}$	3.4	5.0	5.5	V
I_{DDAq}	analog quiescent current	PD = 1; T_{amb} = 25 °C	–	–	10	µA
I_{DDDq}	digital quiescent current	PD = 1; T_{amb} = 25 °C	–	–	10	µA
I_{DDA}	analog supply current	f_s = 48 kHz; CLKSEL = 0; when IECIN1 input is used	–	2.6	–	mA
I_{DDD}	digital supply current	f_s = 48 kHz; CLKSEL = 0	–	13	–	mA
Power						
P_{tot}	total power dissipation	f_s = 48 kHz; CLKSEL = 0; when IECIN1 input is used	–	80	–	mW
Temperature						
T_{amb}	operating ambient temperature		–20	–	+70	°C
IEC interface; pin IECIN1 (high sensitivity IEC input)						
$V_{i(p-p)}$	AC input voltage (peak-to-peak value)		0.2	–	V_{DD}	V
Control part						
CHMODE, UNLOCK, $\overline{FS32}$, $\overline{FS44}$, $\overline{FS48}$ AND COPY (OPEN-DRAIN OUTPUTS)						
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	–	–	0.5	V
RESET, SCK, LCLK, LMODE AND SYSCLKI (HYSTERESIS INPUTS)						
V_{tHL}	negative-going threshold	V_{DD} = 4.5 to 5.5 V	0.6	–	–	V
V_{tLH}	positive-going threshold	V_{DD} = 4.5 to 5.5 V	–	–	2.4	V
V_{hys}	input voltage hysteresis	V_{DD} = 4.5 to 5.5 V	–	0.7	–	V
Clock and timing						
V_{ref}	output reference voltage		–	2.1	–	V
RC_{int} (PIN 44)*						
I_{CHfr}	charge-pump output current	frequency detector loop	–	±12	–	µA
I_{CHph}	charge-pump output current	phase detector loop	–	±24	–	µA

BLOCK DIAGRAM

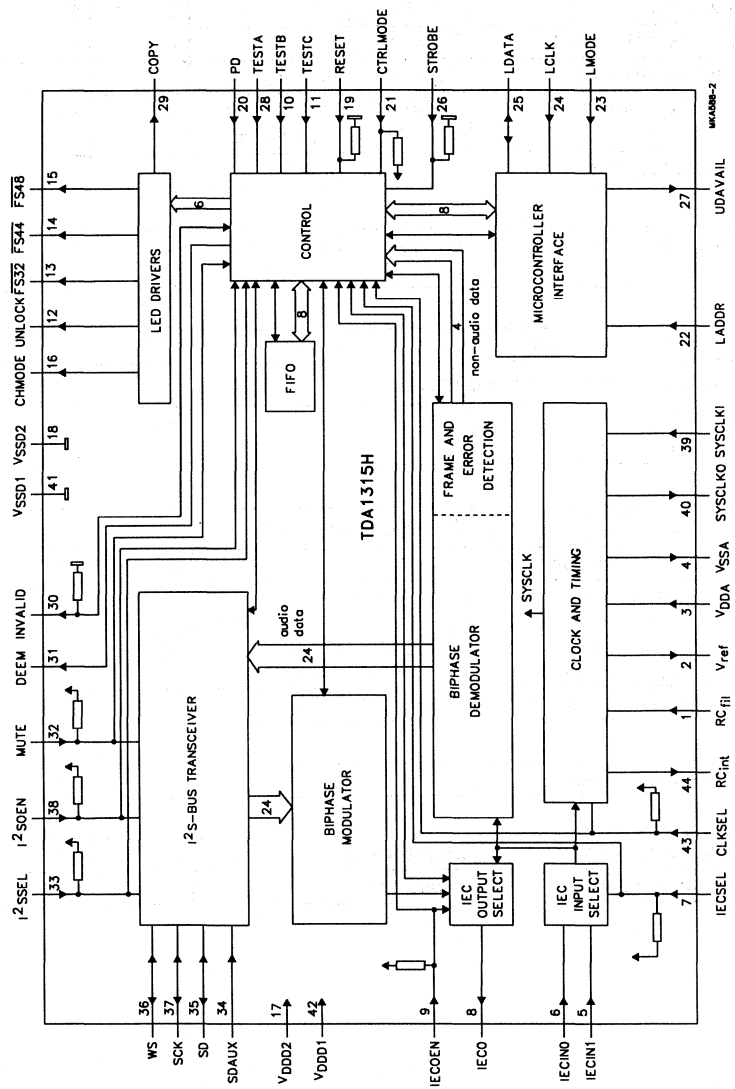


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	PADCELL	DESCRIPTION
RC_{fil}	1	E029	PLL loop filter input
V_{ref}	2	E029	decoupling internal reference voltage output
V_{DDA}	3	E008	analog supply voltage
V_{SSA}	4	E004	analog ground
IECIN1	5	E007	high sensitivity IEC input
IECIN0	6	IPP04	TTL level IEC input
IECSEL	7	IUP04	select IEC input 0 or 1 (0 = IECIN0; 1 = IECIN1); this input has an internal pull-up resistor
IECO	8	OPFH3	digital audio output for optical and transformer link
IECOEN	9	IUP04	digital audio output enable (0 = enabled; 1 = disabled/3-state); this input has an internal pull-up resistor
TESTB	10	IPP04	enable factory test input (0 = normal application; 1 = scan mode)
TESTC	11	IPP04	enable factory test input (0 = normal application; 1 = observation outputs)
UNLOCK	12	OPP41A	PLL out-of-lock (0 = not locked; 1 = locked); this output can drive an LED
$\overline{FS32}$	13	OPP41A	indicates sample frequency = 32 kHz (active LOW); this output can drive an LED
$\overline{FS44}$	14	OPP41A	indicates sample frequency = 44.1 kHz (active LOW); this output can drive an LED
$\overline{FS48}$	15	OPP41A	indicates sample frequency = 48 kHz (active LOW); this output can drive an LED
CHMODE	16	OPP41A	use of channel status block (0 = professional use; 1 = consumer use); this output can drive an LED
V_{DDD2}	17	E008	digital supply voltage 2
V_{SSD2}	18	E009	digital ground 2
RESET	19	IDP09	initialization after power-on, requires only an external capacitor connected to V_{DDD}; this is a Schmitt-trigger input with an internal pull-down resistor
PD	20	IPP04	enable power-down input in the standby mode (0 = normal application; 1 = standby mode)
CTRLMODE	21	IUP04	select microcontroller/stand-alone mode (0 = microcontroller; 1 = stand-alone); this input has an internal pull-up resistor
LADDR	22	IPP04	microcontroller interface address switch input (0 = 000001; 1 = 000010)
LMODE	23	IPP09	microcontroller interface mode line input
LCLK	24	IPP09	microcontroller interface clock line input
LDATA	25	IOF24	microcontroller interface data line input/output
STROBE	26	IDP04	strobe for control register (active HIGH); this input has an internal pull-down resistor
UDAVAIL	27	OPF23	synchronization for output user data (0 = data available; 1 = no data)
TESTA	28	IPP04	enable factory (scan) test input (0 = normal application; 1 = test clock enable)
COPY	29	OPP41A	copyright status bit (0 = copyright asserted; 1 = no copyright asserted); this output can drive an LED
INVALID	30	IOD24	validity of audio sample input/output (0 = valid sample; 1 = invalid sample); this pin has an internal pull-down resistor
DEEM	31	OPF23	pre-emphasis output bit (0 = no pre-emphasis; 1 = pre-emphasis)
MUTE	32	IUP04	audio mute input (0 = permanent mute; 1 = mute on receive error); this pin has an internal pull-up resistor

SYMBOL	PIN	PADCELL	DESCRIPTION
I^2SSEL	33	IUP04	select auxiliary input or normal input in transmit mode
SDAUX	34	IPP04	auxiliary serial data input; I^2S-bus
SD	35	IOF24	serial audio data input/output; I^2S-bus
WS	36	IOF24	word select input/output; I^2S-bus
SCK	37	IOF29	serial audio clock input/output; I^2S-bus
I^2SOEN	38	IUP04	serial audio output enable (0 = enabled; 1 = disabled/3-state); this input has an internal pull-up resistor
SYSCLKI	39	IPP09	system clock input (transmit mode)
SYSCLKO	40	OPFA3	system clock output (receive mode)
V_{SSD1}	41	E009	digital ground 1
V_{DDD1}	42	E008	digital supply voltage 1
CLKSEL	43	IUP04	select system clock (0 = $384f_s$; 1 = $256f_s$); this input has an internal pull-up resistor
RC_{int}	44	E029	integrating capacitor output

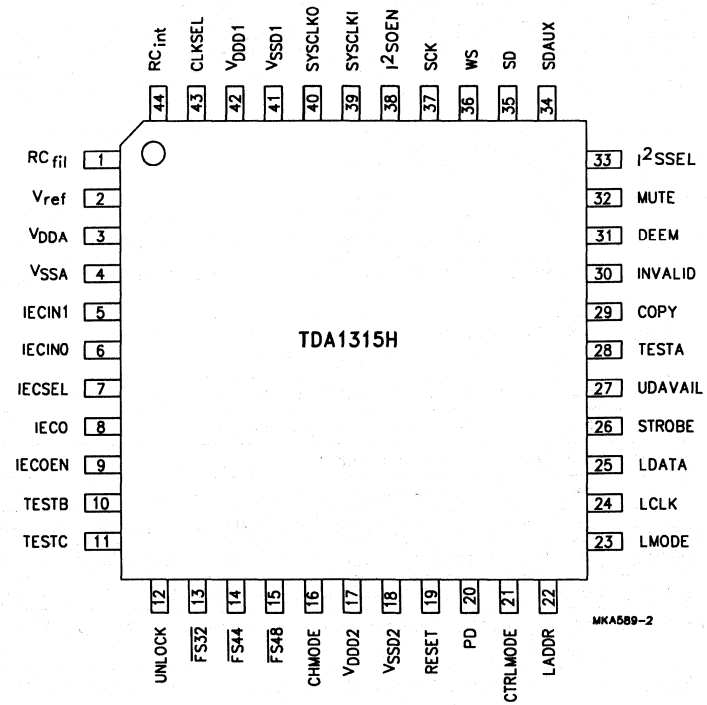


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Modes of operation

With respect to the control of the device and the exchange of non-audio data, a microcontroller (host) mode and a stand-alone mode can be considered. The selection of the mode is performed at pin CTRLMODE.

In the stand-alone mode, the device configuration is solely determined by pins. In the host mode an internal control register, or pins or both can be used to change the default settings.

With respect to the direction of the digital audio data, the device can be operated in either a transmit or a receive mode under control of a microcontroller. In the stand-alone mode the device is only a receiver. In the receive mode the input signal can also be made available at the output pin IECO (feed-through) to ease the cascading of digital audio equipment.

The device can be brought to standby mode at all times by activating the PD pin (power down). In this mode all functions are disabled, all outputs 3-stated, supply current is minimized and the contents of the register are saved.

General

For those applications where it is important to save power, the PD pin is provided, which, when activated, puts the TDA1315H in standby mode by disabling all functions and 3-stating all outputs, while saving register contents.

As illustrated in Fig.1, the TDA1315H contains the following major functional blocks:

- IEC input section
- Biphase demodulator
- Frame and error detection
- Clock and timing section
- IEC output section
- Biphase modulator
- Audio section (I^2S-bus transceiver)
- Non-audio section (control and FIFO)
- User (microcontroller) interface.

IEC INPUT SECTION

There are two biphase signal inputs to the IEC input section. IECIN0 accepts TTL levels from, for example, an optical input device, while IECIN1 is designed for coaxial cable inputs and requires signal levels of minimum 200 mV (p-p) via an external coupling capacitor. The selection of the active input channel is performed by pin IECSEL or by the control register or both. In the receive mode, the selected input signal is applied internally to the biphase audio output section to enable a feed-through function.

BIPHASE DEMODULATOR

In the biphase demodulator, the received signal (for details see Chapter "References" [1.] and [2.]) is converted to binary data and separated into audio and non-audio data for further processing in their dedicated sections. The demodulated input signal is also required for frame and error detection.

FRAME AND ERROR DETECTION

In the frame and error detection block, the framing information from the received biphase signal is retrieved to synchronize the biphase demodulator and to allow access to the audio and non-audio data bits. An out-of-lock condition of the PLL is flagged at UNLOCK. The validity of audio samples is indicated at pin INVALID.

CLOCK AND TIMING SECTION

In the clock and timing section, the timing information inherent to the received biphase signal is retrieved and a symmetrical master clock signal is generated and output at pin SYSCLKO. Depending on the mode of operation, the frequency of this master clock can be selected by pin CLKSEL, by the control register or both to be either $256f_s$ or $384f_s$ (f_s = audio sampling frequency). This section contains all the circuitry of a Phase-Locked Loop (PLL), except for the loop filter components, which are connected externally to pins RC_{int} and RC_{fil}. When the input signal is interrupted, the oscillator will slowly drift to the centre frequency in order to keep the system operating on a proper frequency. In the transmit mode, all required timing signals are input at pin SYSCLKI and are derived from an externally supplied system clock of either $256f_s$ or $384f_s$. The input HIGH time of that clock may be in the range between 30% to 70% of the clock period.

IEC OUTPUT SECTION

In the IEC output section, either the received (feed-through function) or the generated biphase signal is selected for output at pin IECO, depending on the receive/transmit mode. The output can be enabled/disabled by pin IECOEN, by the control register or both, and can drive a suitable optocoupler and a transformer in parallel.

BIPHASE DEMODULATOR

In the biphase modulator section, audio and non-audio data are combined into subframes, frames and blocks, and encoded in the biphase-mark format during transmit mode. Although there are always 24 audio bits per sample in a subframe, the number of significant bits can be selected as 16, 18, 20 or 24 via the control register (host mode).

AUDIO SECTION

In the audio section, the left and right channel audio samples are taken from the demodulated data frames and are output serially in accordance with the I²S-bus format (for details see Chapter "References" [3.] pins SD, SCK and WS) when the TDA1315H is in the receive mode (I²S-bus transmitter). The audio output signals are concealed or muted in case certain errors were detected during reception. Mute can be enforced by pin MUTE or via the control register (host mode) and affects, depending on the receive/transmit mode, the I²S-bus or IEC output signals. MUTE is internally synchronized with the audio data. In the transmit mode, there is an additional I²S-bus data input SDAUX made available to accept audio data from, for example, an ADC. This input can be selected either by pin I²SSEL, by the control register or both. The I²S-bus Port can be enabled/disabled by pin I²SOEN, by the control register or both. In the transmit mode, I²S-bus data and timing are supplied by an external source, the TDA1315H then becomes an I²S-bus receiver. In this event, selection of an I²S-bus source determines which signal is to be output at IECO. Although the phase relationship between system clock (SYSCLKI) and I²S timing (SCK) is not critical they must be synchronous with each other, i.e. be derived from the same source.

Receive mode

The IEC subframe format defines 20 bits for an audio sample, plus 4 auxiliary bits, which can be used to extend the word length. By default, all 24 data bits per sample are output via the I²S-bus Port. This can be changed, however, to 16, 18 or 20 bits via bits 2 and 3 in byte 1 of the control register. The remaining bits will then be zero. The serial audio clock frequency at pin SCK is $64 \times f_s$, i.e. there are 32 clock pulses per audio sample (left or right channel):

Apart from detecting the out-of-lock condition of the PLL, received data is checked for the errors listed below. All detected errors will be flagged in the status register and two of them brought out to a pin. Depending on the type of error, different measures are taken.

- Validity flag set. This error condition is also output at pin INVALID, simultaneously with the data. The corresponding audio sample is not modified.
- Parity check error. A concealment operation is performed on both audio channels (left and right), i.e. the last correctly received stereo sample is output again.
- Biphase violation (other than preambles). A concealment operation (hold) is performed on both audio channels (left and right), i.e. the last correctly received stereo sample is output again.
- PLL is out-of-lock. This error condition is also output at pin UNLOCK. Both audio output channels (left and right) are set to zero (mute). The error condition is sampled with the HIGH-to-LOW transition of WS, i.e. muting becomes effective when the outputting of a stereo sample begins. When the PLL has locked again, muting is released only after a full block of audio samples has been received, free of errors.The INVALID output will always be set to LOW simultaneously with this muting.

In the receive mode it is possible to select the auxiliary I²S-bus data input SDAUX for output at pin SD. However, there will be no suitable system clock available in the event of an open IEC input or a disabled IEC source and output SD will be muted when the TDA1315H is not in lock. Regardless of which source is selected, a MUTE command will always mute the output signal at pin SD and set the INVALID output to LOW regardless of the validity bit value. When mute command is disabled, muting will be released when the outputting of the next stereo sample begins.

Table 1 Summary of validity and muting in the receive mode.

INPUT CONDITIONS[1]					OUTPUTS	
PLL LOCKED	MUTE ACTIVATED	SDAUX SELECTED	I²SOUT ENABLED	VALIDITY BIT	INVALID	SD
X	X	X	no	X	3-state	3-state
No	X	X	yes	X	0	0
X	yes	X	yes	X	0	0
Yes	no	no	yes	0	0	IEC
Yes	no	no	yes	1	1	IEC
Yes	no	yes	yes	X	0	SDAUX

Note

1. X = don't care.

When the I²S-bus output Port is disabled by pin I²SOEN in the stand-alone mode, pins WS, SCK, SD and INVALID will immediately become 3-state. If, however, this is performed in the host mode via the I²SOEN pin or the corresponding bit in the control register, only SD and INVALID will become 3-state immediately. Pins WS and SCK will only become 3-state after the rising edge of STROBE when the STROBE pulse changes the setting from receive to transmit mode. Thus in the host mode, when remaining in the receive mode, I²SOEN only influences the SD and INVALID pins. Pins WS and SCK are always enabled. When the I²S-bus output Port is re-enabled, data output will start with the beginning of a new stereo sample.

Transmit mode

Although the IEC subframe format supports up to 24 bits per audio sample, the number of significant bits can be selected as 16, 18, 20 or 24 via the control register. Because the I²S-bus Port then operates as a receiver, the timing has to be selected so that all data bits can be received. Any bits unused or unsupplied will be set to logic 0.

The information regarding audio samples that may be unreliable or invalid has to be entered at pin INVALID simultaneously with the data input to pin SD. The timing will be the same as in the CD decoder ICs (e.g. the EFAB signal of the SAA7310, see Chapter "References" [5.].

As the I²S-bus Port is used as an input, it must be disabled by the correct combination of pin I²SOEN and the corresponding bit in the control register. The pins WS and SCK are set to 3-state on the rising edge of STROBE, whenever the transmit mode is activated. I²SOEN influences only the data pin SD. This allows for three different configurations:

- Transmit mode #1, I²SOEN = 1, I²SSEL = 1. In this instance, I²S-bus timing and data are derived from an external source and entered at pins WS, SCK and SD. Output will be at pin IECO, if IECOEN permits.
- Transmit mode #2, I²SOEN = 1, I²SSEL = 0. In this instance, I²S-bus timing is derived from an external source and entered at pins WS and SCK and is also supplied to another I²S-bus source, such as an ADC. Data from that other I²S-bus source is entered at pin SDAUX. Output will be at pin IECO, if IECOEN permits. In this instance, I²SSEL acts as a source selector for pins SD and SDAUX.
- Transmit mode #3, I²SOEN = 0, I²SSEL = 0. In this instance, I²S-bus timing is derived from an external source and entered at pins WS and SCK and is also supplied to another I²S-bus source, such as an ADC. Data from the other I²S-bus source is entered at pin SDAUX. Output will be at pin IECO, if IECOEN permits, and at pin SD. In this mode, SDAUX data is available both at the IEC output (a type of digital monitor function) and on the I²S-bus (e.g. for digital signal processing purposes).

The remaining combination ($I^2SOEN = 0$, $I^2SSEL = 1$) is not used. WS, SCK and SD are then 3-state.

Because the SDAUX input normally receives a signal from an ADC, the signal at pin INVALID will not be interpreted when this input is selected. All samples are assumed to be valid. In all transmit modes, INVALID is an input pin.

Whenever MUTE is activated in any of the transmit modes, the audio data of the IEC output signal will be muted and the validity bit set to logic 0, regardless of the INVALID input value. When SDAUX is selected, MUTE will also affect the output at pin SD.

Table 2 Summary of validity and muting in the transmit mode.

INPUT CONDITIONS[1]			IEC OUTPUT SIGNAL	
MUTE ACTIVATED	**SDAUX SELECTED**	**INVALID INPUT**	**VALIDITY BIT**	**AUDIO BITS**
No	no	0	0	from SD
No	no	1	1	from SD
No	yes	X	0	from SDAUX
Yes	X	X	0	0

Note

1. X = don't care.

NON-AUDIO SECTION

In the non-audio section, the first 30 channel status bits are taken from each block of data. A selection of 16 bits is then assembled as two bytes and transferred to the user interface. In the event of an incorrect IEC signal, i.e. no consumer mode, an error will be flagged at pin CHMODE. The error signal will return to its passive state after a full block of consumer mode data has been received. The user data bits are searched for the beginning of a 'message' (see Section "User data"), which is then stored bytewise in a buffer that can be read by an external microcontroller via the user interface. In the transmit mode, channel status and user data bits are taken from an internal buffer that has been written to by an external microcontroller via the user interface. These bits are required for frame composition in the biphase modulator.

The non-audio section supports only the consumer mode of the *"IEC 958"* specification and handles the channel status and user data information.

The non-audio section can be operated in the stand-alone mode (receive only) and the host mode (transmit/receive).

In the stand-alone mode, a few bits from the channel status are brought out to pins, the user data is not available. In the host mode, channel status and user data are exchanged using a microcontroller. After a RESET in the host mode, the TDA1315H provides general format by default.

Channel status

The channel status consists of 30 bits, a number of which are reserved for future standardization. The 16 most significant bits (MSBs), arranged as two bytes, are exchanged using an external microcontroller. The mapping of the channel status bits into these two bytes is given in Tables 3 and 4. All SCMS operations (Serial Copy Management System) will be performed in the microcontroller and no manipulation in the TDA1315H is possible. Bit 0 is always the first bit on the user interface.

In the receive mode, an error signal is generated at pin CHMODE if a professional mode signal is received. Even then, two bytes of information, mapped as defined in Tables 3 and 4, are generated for output. Although there are two bytes of channel status available for output, only the first byte can be read. To identify future modes of the channel status, both mode bits (bits 6 and 7 in the channel status) are available (inverted) from the TDA1315H status register. The channel status is created from the left channel subframes of the IEC signal (preambles 'B' and 'M').

Whenever the channel status, as defined in Tables 3 and 4 (16 bits), differs from the previously received channel status, a bit will be set in the TDA1315H status register. This helps to reduce the data traffic by enabling the microcontroller to read the channel status only after it has changed.

In the transmit mode, the microcontroller supplies consumer mode (Mode 0) channel status data as described in Table 3. Both bytes need to be transferred.

Table 3 First byte of transferred channel status.

BIT	DESCRIPTION	BIT IN CHANNEL STATUS
0 and 1	clock accuracy	29 and 28
2 and 3	sample frequency	25 and 24
4	pre-emphasis	3
5	copyright	2
6	audio/data	1
7	consumer/professional use	0

Table 4 Second byte of transferred channel status.

BIT	DESCRIPTION	BIT IN CHANNEL STATUS
0	category code	15
1	category code	14
2	category code	13
3	category code	12
4	category code	11
5	category code	10
6	category code	9
7	category code	8

User data

In principle, the user data bits may be used in any way required by the user. In order to guarantee compatibility between signals of any source, attempts have been made for the standardization of a user data format. The basic idea is to transfer 'messages' that consist of 'information units'. As messages are, typically, asynchronous with the IEC audio block structure, their transfer relies on software protocol. Currently, the applications for CD subcode and DAT have been accepted. Their general format complies with that protocol and can be described as follows:

- User data is transferred in the form of messages.
- Messages consist of information units, i.e. groups of 8 bits (bytes).
- Messages are separated by more than 8 zero bits (0).
- Information units within a message may be separated by 0 up to and including 8 zero bits.
- The MSB of each byte is sent first in the user data channel.
- The MSB of each byte is a 1-bit (1, start bit).
- For CD subcode, one byte consists of bits 1QRSTUVW.

Normally, the exchange of user data between the TDA1315H and the microcontroller is based on the general format described above. In the event of CD subcode, this means that 96 bytes need to be transferred for each subcode frame. In order to reduce the amount of data traffic, it is possible to separate the Q-channel bits from the user data and transfer only them. This mode can be enabled by a bit in the control register and leads to the transfers of only 12 bytes per subcode frame. As there is no check in the TDA1315H whether user data is from a CD source, this Q-channel decoding can be employed whenever the user data format permits.

Receive mode

User data bits are extracted from the received IEC subframes and searched for the beginning of a message.

When Q-channel decoding is disabled (in the control register), the data bytes of a message are stored in a buffer for subsequent external interpretation or processing. Any 0 bits between information units and between messages are skipped.

It is essential to maintain synchronization of messages, even if not all bytes of a message can be exchanged with the microcontroller in a single transfer, or if there are several messages in the buffer. When user data is transferred in the general format described earlier, the beginning of a message is indicated in the buffer by a 1 bit in the MSB position of the first byte of that message. In all subsequent bytes of the same message, the MSB will be zero. This is illustrated in Table 5 for the CD subcode.

The user data buffer is implemented as a FIFO (First-In, First-Out) with a size of 128 bytes. This allows the storing of a full CD subcode frame. A synchronization signal at pin UDAVAIL supports the transfer of user data to the microcontroller. This signal goes LOW when there is at least 1 byte of user data in the buffer, and returns HIGH only after the last received byte has been read. This is illustrated in Fig.3.

Based on the timing of the CD subcode, the microcontroller should start reading data within 17 ms after UDAVAIL has gone LOW, otherwise the buffer will fill completely and the most recent data will be lost.

Table 5 Synchronization of user data.

MSB	USER DATA						LSB	FUNCTION
0	..	..	..	..	..	..	..	–
1	Q1	R1	S1	T1	U1	V1	W1	start of message
0	Q2	R2	S2	T2	U2	V2	W2	–
0	Q3	R3	S3	T3	U3	V3	W3	–
0	..	..	..	..	..	..	..	–
0	..	..	..	..	..	..	..	–
0	Q95	R95	S95	T95	U95	V95	W95	–
0	Q96	R96	S96	T96	U96	V96	W96	–
1	Q1	R1	S1	T1	U1	V1	W1	start of next message
0	Q2	R2	S2	T2	U2	V2	W2	–
0	Q3	R3	S3	T3	U3	V3	W3	–
0	..	..	..	..	..	..	..	–

Although the MSB is first within the IEC user data channel, the LSB is sent first on the user interface to be compatible with other data, i.e. the first byte of a subcode user data frame will be output as follows:

1. Bit sent = W1.
2. Bit sent = V1.
3. Bit sent = U1.
4. Bit sent = T1.
5. Bit sent = S1.
6. Bit sent = R1.
7. Bit sent = Q1.
8. Bit sent = 1.

When Q-channel decoding is enabled, only the Q-channel bits are taken from the user data frame and stored in the buffer. Again, any separating 0 bits are skipped. Table 6 shows how data is arranged in the buffer.

Table 6 Layout of Q-channel data.

MSB	USER DATA						LSB
..	..	..	..	..	..	..	..
Q89	Q90	Q91	Q92	Q93	Q94	Q95	Q96
Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
Q9	Q10	Q11	Q12	Q13	Q14	Q15	Q16
Q17	Q18	Q19	Q20	Q21	Q22	Q23	Q24
..	..	..	..	..	..	..	..
..	..	..	..	..	..	..	..
Q89	Q90	Q91	Q92	Q93	Q94	Q95	Q96
Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
..	..	..	..	..	..	..	..

In this instance, synchronization of Q-channel frames must be maintained by the microcontroller. It is recommended to read decoded Q-channel data in groups of 12 bytes otherwise synchronization of subcode frames may be lost quickly. Again, the data transfer is supported by the signal at pin UDAVAIL. This time it goes LOW when there is at least one full frame (12 bytes) of Q-channel data in the buffer, and goes HIGH again, when less than 12 bytes are in the buffer. This is illustrated in Fig.4.

An initial synchronization can be obtained by clearing the buffer via the control register, then start counting bytes modulo 12. Again, the LSB is sent first on the user interface, i.e. the first byte of a Q-channel frame will be output as follows:

1. Bit sent = Q8.
2. Bit sent = Q7.
3. Bit sent = Q6.
4. Bit sent = Q5.
5. Bit sent = Q4.
6. Bit sent = Q3.
7. Bit sent = Q2.
8. Bit sent = Q1.

Writing to the buffer is disabled when the FIFO is full. It is re-enabled when there is at least 1 byte free. Any data overrun condition will be flagged as an error in the status register. When this has occurred, the appropriate strategy for data handling is decided by the microcontroller. It can, for example, clear the buffer via the control register, thereby discarding all remaining data, or it can start reading data rapidly. Clearing the buffer turns UDAVAIL HIGH. The response to reading data is the same as described previously, depending on the mode of reception, i.e. Q-channel decoding or normal message protocol.

For the period that the user data register is selected, the microcontroller has to poll UDAVAIL each time after reading one byte in normal mode, or 12 bytes in Q-channel mode. Possible actions by the microcontroller are as follows:

- If UDAVAIL = 0: reading the next byte in normal mode or the next 12 bytes in Q-channel mode.
- If UDAVAIL = 1: either wait until UDAVAIL goes LOW and continue reading user data byte(s), or write data, read other data or deselect the TDA1315H by foreign addressing.
  - **Remark:** it is allowed to address the TDA1315H for reading user data again when UDAVAIL is still HIGH, but it is forbidden to apply clock pulses until UDAVAIL has gone LOW.

Remark: whenever the buffer is empty (UDAVAIL = 1), normally zeroes will be read, even when the microcontroller tries to read more bytes. Doing so, however, poses the risk of reading not all zeroes. In this event new data is stored in the buffer during reading, thereby losing synchronization. To assure correct information will be read, the microcontroller should perform an addressing sequence (not necessarily to the TDA1315H), whenever an UDAVAIL HIGH is detected before reading further.

Transmit mode

User data bits are supplied by the microcontroller in the general message format only, Q-channel encoding is not available in the TDA1315H. Again, UDAVAIL can be used to synchronize transfers. It goes HIGH, when the buffer contains at least 112 bytes, and goes LOW only when there are no more than 16 bytes in the buffer. This is illustrated in Fig.5.

Thus, after UDAVAIL has gone LOW, the microcontroller can write a full CD subcode frame (96 data bytes plus 2 synchronization bytes) to the buffer without needing to poll the state of pin UDAVAIL. In the event that no data are available in the buffer, the user data bits in the IEC output signal will be set to zero. Should the microcontroller attempt to write more data than the buffer can hold, writing will be disabled and the data overrun bit set in the status register. Any bytes that have been transferred but not written into the buffer are lost.

Four zero bits will be inserted automatically between user data bytes (information units). The gap between messages can be achieved by writing a single byte containing all zeroes to the buffer.

USER INTERFACE

The user interface is an interface between the data processing sections of the TDA1315H and the user. The basic mode of operation (control by a host or stand-alone operation) is selected by pin CTRLMODE. In the host mode, all data, control and status information is, in principle, exchanged with a microcontroller although the device configuration can also be changed by pin control. Up to 2 TDA1315Hs can be used on the same user interface by setting different device addresses via the LADDR pin. In the stand-alone mode (receive only), no microcontroller is needed because important information is brought out to pins $\overline{FS32}$, $\overline{FS44}$ and $\overline{FS48}$, being an indication of sample frequency, copyright protection (COPY) (see Chapter "References" [2.]) and use of pre-emphasis (DEEM).

Stand-alone mode

In this mode, the TDA1315H is automatically configured as a receiver. The configuration, i.e., the mode of operation of the device, is determined by pins CTRLMODE, IECSEL, IECOEN, CLKSEL, I²SSEL and I²SOEN. Because all of the pins have internal pull-up resistors, the default configuration can be changed by pulling a pin LOW.

The output signals listed below are provided from the channel status. However, all of them are switched off when the PLL is not locked. This includes the situation where no IEC input signal is available:

- Sample frequency is 32 kHz (pin $\overline{FS32}$)
- Sample frequency is 44.1 kHz (pin $\overline{FS44}$)
- Sample frequency is 48 kHz (pin $\overline{FS48}$)
- Copyright status bit (pin COPY)
- Pre-emphasis bit (pin DEEM).

As there will be no output signals from the channel status in the event that non-consumer IEC signals are received, the I²S-bus output will still output data in 24 bits format. An LED can be connected to pin CHMODE to provide an indication of such a situation.

Host mode

In this mode, the exchange of data and control information between the TDA1315H and a microcontroller is via a serial hardware interface, which comprises the following pins:

- LDATA to microcontroller interface data line.
- LCLK to microcontroller interface clock line.
- LMODE to microcontroller interface mode line.
- LADDR to microcontroller interface address switch.

Two different modes of operation can be distinguished:

1. Addressing mode.
2. Data transfer mode.

The addressing mode is used to select a device for subsequent data transfer and to define the direction of that transfer as well as the source or destination registers. The addressing mode is characterized by LMODE being LOW and a burst of 8 clock pulses at LCLK, accompanied by 8 data bits. The fundamental timing is illustrated in Fig.6.

Data bits 0 to 1 indicate the type of subsequent data transfer as given in Table 7. The direction of the channel status and user data transfers depends on the transmit/receive mode.

Data bits 2 to 7 represent a 6-bit device address, with bit 7 being the MSB and bit 2 the LSB. The address of the TDA1315H is 000001 (LADDR = 0) or 000010 (LADDR = 1). Should the TDA1315H receive a different address, it will immediately 3-state the LDATA pin and deselect its microcontroller interface logic. A dummy address of 000000 is defined for the deselection of all devices that are connected to the serial microcontroller bus.

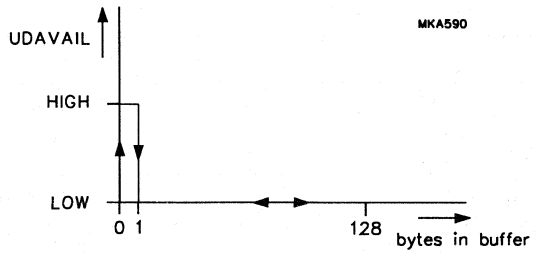


Fig.3 User data handshake.

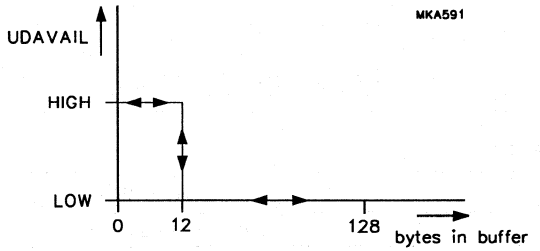


Fig.4 Q-channel handshake.

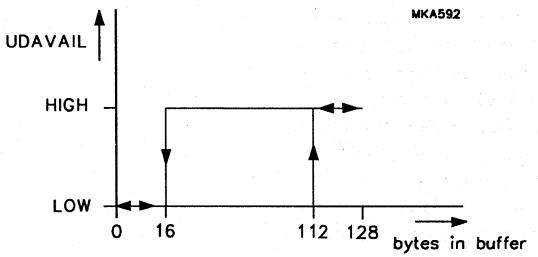


Fig.5 Transmit mode handshake.

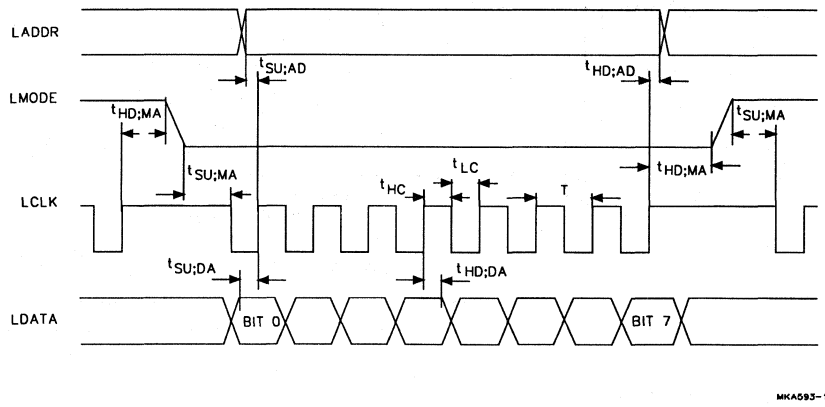


Fig.6 Addressing mode timing.

Table 7 Selection of data exchange.

BIT 1	BIT 0	TRANSFER	DIRECTION
0	0	channel status	input/output
0	1	user data	input/output
1	0	control	input
1	1	status	output

In the data transfer mode, the microcontroller exchanges data with the TDA1315H after it has addressed the device and defined the type of data for that exchange. The selection remains active until the TDA1315H receives a new type of data or is deselected. The fundamental timing of data transfers is illustrated in Fig.7, where LDATA denotes the data from the TDA1315H to the microcontroller (LDATA read). The timing for the opposite direction is essentially the same as in the addressing mode (LDATA write).

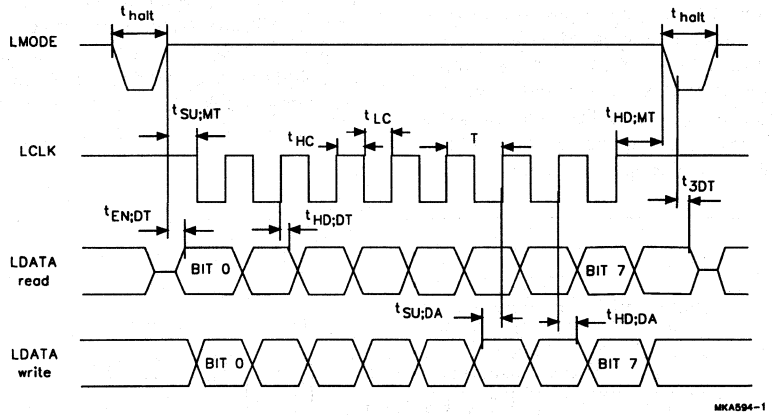


Fig.7 Data transfer mode timing.

All transfers are bytewise, i.e. they are based on groups of 8 bits. Data will be stored in the TDA1315H after the eighth bit of each byte has been received. It is possible to read only the first byte of the channel status and of the TDA1315H status register.

A multi-byte transfer is illustrated in Fig.8. As some other devices, which are expected to connect to the same microcontroller bus lines, require an indication of when 8 bits have been transferred, a so-called halt mode has been defined. It is characterized by the following conditions: LMODE = LOW, LDATA = 3-state and LCLK = HIGH. The TDA1315H does not need this mode to distinguish one byte from the next, however, it will not make any difference when this occurs. When not used, there is no need to increase the time between the last LCLK pulse of a byte and the first LCLK pulse of the next byte.

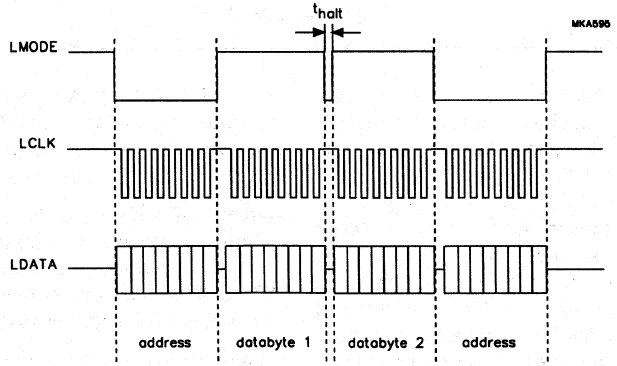


Fig.8 Multi-byte transfer.

DAIO control

Under microcontroller control, there is also a transmit mode available. Therefore, setting the device configuration is slightly different from the stand-alone mode. Most functions or modes can be set by pins or by the control register or by both. Negative logic is used to implement this 'OR' function. The initial setting of the control register is all ones. For most functions, the TDA1315H can be configured only by pins, as explained for the stand-alone mode. The principle of this type of control is illustrated in Fig.9. However, for changing CLKSEL, I²SSEL and the receive/transmit mode, there is a configuration register, which is updated only by an externally supplied STROBE signal. This allows synchronization with other ICs.

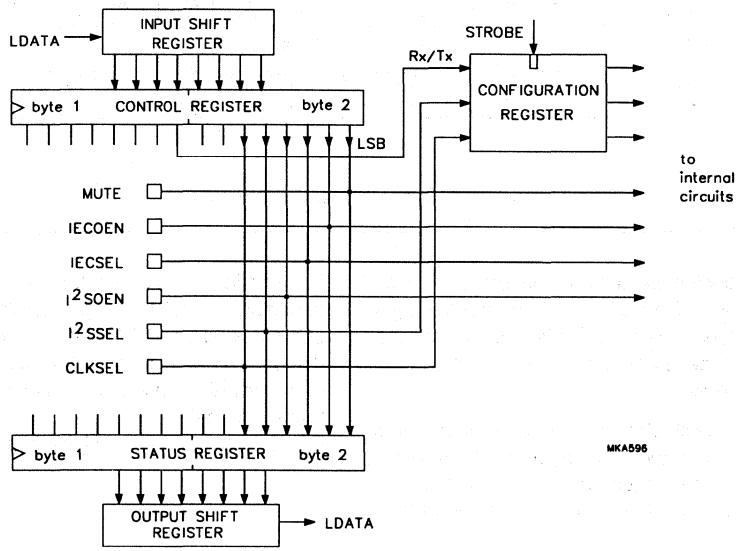


Fig.9 Mode control.

At pin LDATA, control information is first entered serially into a shift register and then latched in the control register when complete. The bits of the second byte (6 are used) of this register are internally ORed with their corresponding pins, so that either a LOW or a logic 0 bit will result in a logic 0 state (active LOW). These combined states are then entered in the status register. The resulting CLKSEL and I²SSEL information is supplied to the configuration register, i.e. these bits will only be executed in the TDA1315H, together with the receive/transmit bit, after a STROBE has been received. This applies to the host mode. In the stand-alone mode, the configuration register is transparent and any configuration changes are executed immediately. When the TDA1315H status is read, the contents of the status register are output serially at pin LDATA, thereby reflecting the 'OR' combination of configuration control bits and associated pins (negative logic). The microcontroller is thereby able to determine whether a pin is open-circuit or tied to ground.

When a STROBE is applied in the receive mode (to switch to transmit mode), the outputs WS and SCK are disabled one or two system clock periods after the rising edge of STROBE. At the same time SYSCLKO will be forced LOW and will be disabled one system clock later.

In the transmit mode it is possible to set the receive/transmit bit to zero and then poll the locking status of the TDA1315H and wait with a STROBE until the TDA1315H is in-lock. This method can be used to check whether there is an IEC source, since the TDA1315H will

not lock without one. It should be noted that the locking status bit and the UNLOCK pin are only valid, i.e. its value has a meaning, when you are in either the receive mode or the receive/transmit bit is set to zero in the transmit mode.

When the configuration is changed to the receive mode, WS, SCK, INVALID and SYSCLKO outputs are enabled one or two system clock periods after the falling edge of STROBE. SYSCLKO will always be initially LOW, for a short time, and then pulses will appear always starting with the rising edge.

In general WS and SCK outputs are always enabled/disabled simultaneously. Output INVALID will only be enabled when SD, WS and SCK are all enabled. The mode timing is illustrated in Fig.10.

The control register consists of two bytes. The meaning of the control register bits is given in Tables 8 and 9. All bits default to a logic HIGH state after a reset to the TDA1315H. This requires a reset for proper initialization when CTRLMODE is changed after power-up. The LSB (bit 0) is always transferred first.

Table 8 First byte of control register.

BIT	DESCRIPTION	FUNCTION
0	transmit/receive mode	0 = receive 1 = transmit
1	decode subcode Q-channel	0 = enable 1 = disable
3 and 2	number of bits to transfer	00 = 16 bits 01 = 18 bits 10 = 20 bits 11 = 24 bits
4[1]	clear user data buffer	0 = clear 1 = leave as is
5	reserved	0 = undefined 1 = default
6	reserved	0 = undefined 1 = default
7	reserved	0 = undefined 1 = default

Note

1. Bit 4 is reset to HIGH after the TDA1315H has cleared the buffer and has either caused UDAVAIL to go HIGH in the receive mode or LOW in the transmit mode.

Table 9 Second byte of control register.

BIT	DESCRIPTION	FUNCTION
0	audio mute	0 = enabled 1 = disabled
1	IEC output enable	0 = enabled 1 = disabled
2	select IEC input	0 = TTL level 1 = high sensitivity
3	I^2S-bus output enable	0 = enabled 1 = disabled
4	select I^2S-bus source	0 = SDAUX 1 = SD
5	select clock frequency	0 = $384f_s$ 1 = $256f_s$
6	reserved	0 = undefined 1 = default
7	reserved	0 = undefined 1 = default

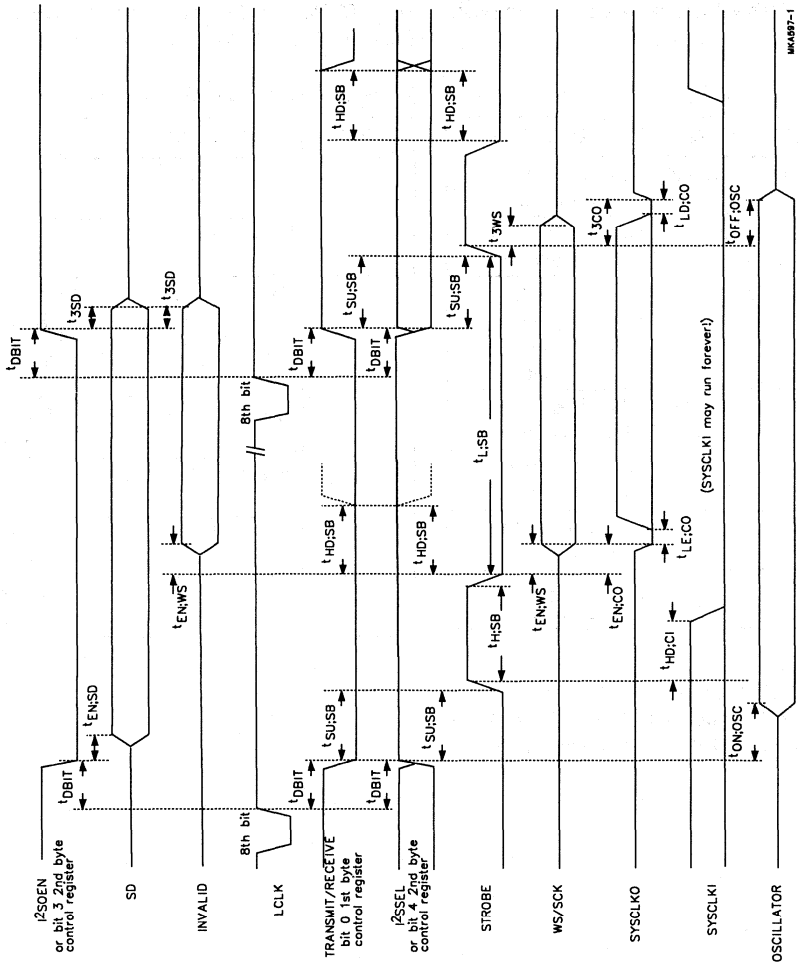


Fig.10 Mode switching and timing STROBE input.

Status

The status register consists of two bytes. A description of the status register bits is given in Tables 10 and 11. After a reset all bits in the status register will be one.

The various error conditions of the TDA1315H are reflected in bits 0 to 6 of the first byte. The error bits are set (LOW) when the corresponding error conditions occur, they are reset (HIGH) only after the register has been read by the microcontroller. Bit 7 reflects the active transmit/receive state. It is updated after the TDA1315H configuration, as determined by bit 0 of the first control register byte, has been changed. This allows verification of the mode change to, for example, release a mute signal after a successful change.

Table 10 First byte of status register.

BIT	DESCRIPTION	FUNCTION
0	channel status mode	0 = professional 1 = consumer
1	PLL lock condition	0 = not locked 1 = locked
2	validity flag	0 = error 1 = no error
3	parity check	0 = error 1 = no error
4	biphase violation	0 = error 1 = no error
5	user data overrun	0 = error 1 = no error
6	channel status check	0 = change 1 = no change
7	direction of data	0 = receive 1 = transmit

Table 11 Second byte of status register.

BIT	DESCRIPTION	FUNCTION
0	audio mute	0 = enabled 1 = disabled
1	IEC output enable	0 = enabled 1 = disabled
2	select IEC input	0 = TTL level 1 = high sensitivity
3	I^2S-bus output enable	0 = enabled 1 = disabled
4	select I^2S-bus source	0 = SDAUX 1 = IEC or CD
5	select clock frequency	0 = $384f_s$ 1 = $256f_s$
6[1]	channel status (bit 7)	0 = bit 7 set 1 = bit 7 reset
7[1]	inverse mode bit (bit 6)	0 = bit 6 set 1 = bit 6 reset

Note

1. Bits 6 and 7 in the second byte of the status register contain the inversion of bits 7 and 6, respectively, of the channel status, which are used as mode bits.

Reset and standby mode

Figure 11 illustrates the timing for the toggling between normal and standby mode.

In Figs 11 and 12, when activating PD or RESET, 0 ns can be taken for $t_{ON;OSC}$ when the oscillator is running (e.g. receive mode).

The TDA1315H uses its internal oscillator for the reset and standby function. This means that it is not necessary, in any mode, to apply a clock at the SYSCLKI input for the TDA1315H to perform the reset or standby function.

For resetting the TDA1315H only a small pulse is necessary at the RESET input. The device then automatically starts the oscillator (in the event that it is not running). The system will then do a synchronous reset (internally) during approximately 3 internal clock periods. This t_{RESET} starts after the falling edge of RESET or when the oscillator has started, whichever occurs last. Only when this resetting has been accomplished will the external pin programming (e.g. CLKSEL, I²SOEN etc.) be read by the TDA1315H. The TDA1315H is then ready for use.

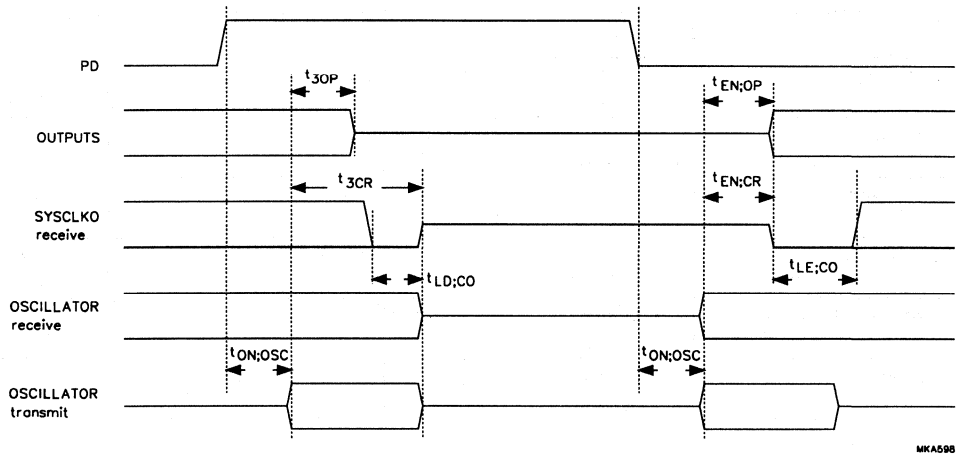


Fig.11 Standby mode timing.

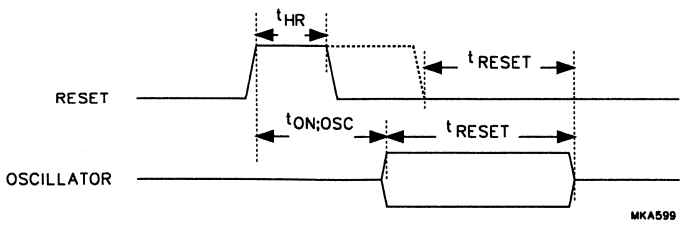


Fig.12 RESET timing.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 3, 17 and 42)		−0.5	+6.5	V
I_{DD}	supply current per pin (pins 3, 17 and 42)		–	50	mA
V_{all}	voltage supplied to all pins	without current limitations	−0.5	V_{DD} + 0.5	V
$I_{I/O}$	input/output current on any pin except supply pins and pins 8, 12 to 16, 29 and 40	note 1	–	±10	mA
I_I	input current pins 12 to 16 and 29	$V_O > V_{DD}$ + 0.5 V; output disabled; note 1	–	±10	mA
$I_{I/O}$	input/output current pins 12 to 16 and 29	$V_O < V_{DD}$ + 0.5 V; note 1	–	±20	mA
I_8	input/output current pin 8	note 1	–	±60	mA
I_{40}	input/output current pin 40	note 1	–	±80	mA
P_{tot}	total power dissipation		–	500	mW
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		−20	+70	°C

Note

1. In all events and, also, when applied voltages are below −0.5 V or above V_{DD} + 0.5 V this current limitation should be taken into account to prevent device damage.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	80	K/W

CHARACTERISTICS

$V_{DDD1} = V_{DDD2} = V_{DDA}$ = 3.4 to 5.5 V; T_{amb} −20 to +70 °C; rise, fall, set-up and hold times are specified between 10% and 90% of full amplitude; delays between 50%; times to and from 3-state with R_L = 1.5 kΩ to ½V_{DD}; typical values are valid at the typical supply voltage of 5 V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	$V_{DDD} = V_{DDA}$	3.4	5.0	5.5	V
I_{DDD}	digital supply current	PD = 1; T_{amb} = 25 °C	–	–	10	µA
I_{DDA}	analog supply current	PD = 1; T_{amb} = 25 °C	–	–	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THE FOLLOWING PARAMETERS ARE TYPICAL FOR RECEIVE MODE; ALL OUTPUTS ENABLED (NOT LOADED); T_{amb} = 25 °C; V_{DD} = 5 V						
I_{DDD}	digital supply current	f_s = 48 kHz; CLKSEL = 0	–	13	–	mA
I_{DDA}	analog supply current	f_s = 48 kHz; CLKSEL = 0; when IECIN1 input is used	–	2.6	–	mA
P_{tot}	total power dissipation	f_s = 48 kHz; CLKSEL = 0; when IECIN1 input is used	–	80	–	mW
TTL input switching levels (without Schmitt-trigger)						
APPLICABLE TO PERIPHERAL TYPES: IPP04, IUP04, IDP04, IOF24 AND IOD24						
V_{IL}	LOW level input voltage	V_{DD} = 3.4 V	–	–	0.5	V
		V_{DD} = 4.5 V	–	–	0.8	V
		V_{DD} = 5.5 V	–	–	0.8	V
V_{IH}	HIGH level input voltage	V_{DD} = 3.4 V	1.5	–	–	V
		V_{DD} = 4.5 V	2.0	–	–	V
		V_{DD} = 5.5 V	2.0	–	–	V
TTL input thresholds (with Schmitt-trigger)						
APPLICABLE TO PERIPHERAL TYPES: IPP09, IDP09 AND IOF29						
V_{tHL}	negative-going threshold	V_{DD} = 3.4 V	0.3	–	–	V
		V_{DD} = 4.5 V	0.6	–	–	V
		V_{DD} = 5.5 V	0.6	–	–	V
V_{tLH}	positive-going threshold	V_{DD} = 3.4 V	–	–	1.9	V
		V_{DD} = 4.5 V	–	–	2.4	V
		V_{DD} = 5.5 V	–	–	2.4	V
V_{hys}	hysteresis voltage	V_{DD} = 3.4 V	–	0.6	–	V
		V_{DD} = 4.5 V	–	0.6	–	V
		V_{DD} = 5.5 V	–	0.8	–	V
Input pull-up and pull-down resistor values; note 1						
APPLICABLE TO PERIPHERAL TYPES: IUP04, IDP04, IDP09 AND IOD24						
R_{pull}	pull-up or pull-down resistors	V_{DD} = 3.4 V	32	–	203	kΩ
		V_{DD} = 4.5 V	21	–	134	kΩ
		V_{DD} = 5.5 V	17	–	104	kΩ
Outputs sink and source capabilities						
APPLICABLE TO PERIPHERAL TYPES: OPF23, IOF24, IOD24, AND IOF29 (2 mA OUTPUTS)						
V_{OL}	LOW level output voltage	V_{DD} = 3.4 V; I_O = 1.5 mA	–	–	0.5	V
		V_{DD} = 4.5 V; I_O = 2 mA	–	–	0.5	V
		V_{DD} = 5.5 V; I_O = 2.25 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	V_{DD} = 3.4 V; I_O = −1.5 mA	2.9	–	–	V
		V_{DD} = 4.5 V; I_O = −2 mA	4.0	–	–	V
		V_{DD} = 5.5 V; I_O = −2.25 mA	5.0	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
APPLICABLE TO PERIPHERAL TYPE: OPP41A (4 mA OUTPUT)						
V_{OL}	LOW level output voltage	V_{DD} = 3.4 V; I_O = 3 mA	–	–	0.5	V
		V_{DD} = 4.5 V; I_O = 4 mA	–	–	0.5	V
		V_{DD} = 5.5 V; I_O = 4.5 mA	–	–	0.5	V
APPLICABLE TO PERIPHERAL TYPE: OPFH3 (12 mA OUTPUT)						
V_{OL}	LOW level output voltage	V_{DD} = 3.4 V; I_O = 9 mA	–	–	0.5	V
		V_{DD} = 4.5 V; I_O = 12 mA	–	–	0.5	V
		V_{DD} = 5.5 V; I_O = 13.5 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	V_{DD} = 3.4 V; I_O = −9 mA	2.9	–	–	V
		V_{DD} = 4.5 V; I_O = −12 mA	4.0	–	–	V
		V_{DD} = 5.5 V; I_O = −13.5 mA	5.0	–	–	V
APPLICABLE TO PERIPHERAL TYPE: OPFA3 (16 mA OUTPUT)						
V_{OL}	LOW level output voltage	V_{DD} = 3.4 V; I_O = 12 mA	–	–	0.5	V
		V_{DD} = 4.5 V; I_O = 16 mA	–	–	0.5	V
		V_{DD} = 5.5 V; I_O = 18 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	V_{DD} = 3.4 V; I_O = −12 mA	2.9	–	–	V
		V_{DD} = 4.5 V; I_O = −16 mA	4.0	–	–	V
		V_{DD} = 5.5 V; I_O = −18 mA	5.0	–	–	V
Input and 3-state (OFF state) leakage currents						
APPLICABLE TO PERIPHERAL TYPES: IPP04 AND IPP09						
$\|I_{LI}\|$	input leakage current	V_I = 0 or 5.5 V; V_{DD} = 5.5 V	–	–	±1	μA
APPLICABLE TO PERIPHERAL TYPES: OPF23, OPFH3, OPFA3, OPP41A, IOF24 AND IOF29						
$\|I_{OZ}\|$	3-state leakage current	V_O = 0 or 5.5 V; V_{DD} = 5.5 V	–	–	±5	μA
IEC interface; note 2; (for timing see Chapter "References" [1.])						
IECO (PIN 8)						
t_{dIEC}	output delay with respect to IECINx	receive mode	$2T_c$	–	$3T_c$ + 50	ns
IECIN1 (PIN 5)						
$V_{i(p-p)}$	AC input voltage (peak-to-peak value)		0.2	–	V_{DD}	V
I_i	input current	V_I = 0 or 5 V; V_{DD} = 5 V	–	±550	–	μA
V_{bias}	DC bias voltage		–	$0.5V_{DD}$	–	V
I²S-bus interface; (for timing see Chapter "References" [3.])						
SD INPUT/OUTPUT (PIN 35)						
t_{dSDAUX}	output delay with respect to SDAUX		–	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Microcontroller interface (see Figs 6 and 7)						
T	LCLK period		$T_c + 50$	–	–	ns
t_{HC}	LCLK HIGH period		25	–	–	ns
t_{LC}	LCLK LOW period		25	–	–	ns
$t_{SU;AD}$	LADDR set-up time		25	–	–	ns
$t_{HD;AD}$	LADDR hold time		25	–	–	ns
$t_{SU;MA}$	LMODE set-up time	addressing mode	$\frac{1}{2}(T_c + 50)$	–	–	ns
$t_{HD;MA}$	LMODE hold time	addressing mode	$\frac{1}{2}(T_c + 50)$	–	–	ns
$t_{SU;MT}$	LMODE set-up time	halt mode	25	–	–	ns
$t_{HD;MT}$	LMODE hold time	halt mode	25	–	–	ns
$t_{SU;DA}$	LDATA set-up time	write and addressing mode	25	–	–	ns
$t_{HD;DA}$	LDATA hold time	write and addressing mode	25	–	–	ns
$t_{EN;DT}$	LDATA enable time	data read mode	–	–	50	ns
$t_{HD;DT}$	LDATA hold time	data read mode; note 3	$\frac{1}{2}T_c$	–	$T_c + 50$	ns
t_{3DT}	LDATA disable time	data read mode	–	–	50	ns
t_{halt}	LMODE halt time		0	–	–	ns
Mode switching and STROBE (see Fig.10)						
$t_{H;SB}$	STROBE HIGH time		$3T_c + 50$	–	–	ns
$t_{L;SB}$	STROBE LOW time		$3T_c + 50$	–	–	ns
$t_{SU;SB}$	set-up time before STROBE	for pins or bits	$-T_c + 50$	–	–	ns
$t_{HD;SB}$	hold time after STROBE	for pins or bits	$2T_c + 50$	–	–	ns
t_{DBIT}	delay LCLK to internal bit	control register	$2T_c$	–	$3T_c + 50$	ns
$t_{EN;SD}$	SD enable time		T_c	–	$2T_c + 50$	ns
t_{3SD}	SD and INVALID disable time		–	–	$T_c + 50$	ns
$t_{EN;WS}$	WS, SCK and INVALID enable time		T_c	–	$2T_c + 50$	ns
t_{3WS}	WS and SCK disable time		T_c	–	$2T_c + 50$	ns
$t_{EN;CO}$	SYSCLKO enable time		T_c	–	$2T_c + 50$	ns
t_{3CO}	SYSCLKO disable time		$2T_c$	–	$3T_c + 50$	ns
$t_{LE;CO}$	SYSCLKO LOW time	when enabled	$\frac{1}{2}T_s$	–	$1.5T_s + 50$	ns
$t_{LD;CO}$	SYSCLKO LOW time	when disabled	$T_c - T_s$	–	$T_c + 50$	ns
$t_{HD;CI}$	SYSCLKI hold time		$3T_c + 50$	–	–	ns
$t_{ON;OSC}$	oscillator start-up time	C_{ref} in µF; note 4	0	–	$\frac{1}{10}C_{ref}$	s
$t_{OFF;OSC}$	oscillator switch-off time		$2T_c$	–	$3T_c + 50$	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Standby mode (see Fig.11)						
t_{3OP}	outputs disable time		–	–	$T_c + 50$	ns
$t_{EN;OP}$	outputs enable time		–	–	$T_c + 50$	ns
t_{3CR}	SYSCLKO disable time	receive mode	T_c	–	$2T_c + 50$	ns
$t_{EN;CR}$	SYSCLKO enable time	receive mode	–	–	$T_c + 50$	ns
RESET (see Fig.12)						
t_{HR}	RESET HIGH time		25	–	–	ns
t_{RESET}	internal RESET time		–	–	2	µs
Clock and timing (pins SYSCLKI and SYSCLKO)						
$\delta_{SYSCLKI}$	input clock duty factor		30	50	70	%
$\delta_{SYSCLKO}$	output clock duty factor		45	50	55	%
$\Delta t/t$	SYSCLKO output clock jitter	$\Delta V_{DDA} < 10$ µV	–	$\pm 50 \times 10^{-6}$	–	
k_{oL}	VCO conversion gain	RC_{fil} to SYSCLKO; CLKSEL = 1	–	225×10^6	–	rad/s/V
k_{oH}	VCO conversion gain	RC_{fil} to SYSCLKO; CLKSEL = 0	–	250×10^6	–	rad/s/V
$2f_{rL}$	VCO frequency tuning range	at SYSCLKO; CLKSEL = 1	–	16	–	MHz
$2f_{rH}$	VCO frequency tuning range	at SYSCLKO; CLKSEL = 0	–	22	–	MHz
f_{cL}	VCO centre frequency	at SYSCLKO; $RC_{fil} = V_{ref}$; CLKSEL = 1	–	12.5	–	MHz
f_{cH}	VCO centre frequency	at SYSCLKO; $RC_{fil} = V_{ref}$; CLKSEL = 0	–	19	–	MHz
V_{ref} OUTPUT (PIN 2)						
V_{ref}	output reference voltage		–	2.1	–	V
I_{ref}	output reference current	$V_{ref} = 0$ V	–	28	–	µA
RC_{fil} INPUT (PIN 1)						
V_{trL}	input tuning voltage	f_s = 32 to 48 kHz; CLKSEL = 1	–	100	–	mV
V_{trH}	input tuning voltage	f_s = 32 to 48 kHz; CLKSEL = 0	–	150	–	mV
$\|I_{LI}\|$	input leakage current	$V_I = 0$ or 5.5 V; $V_{DD} = 5.5$ V; TESTB = 1	–	–	±1	µA
R_{tr}	transmission-gate resistor	$V_{ref} = 2.1$ V; $V_{DD} = 5$ V; note 5	–	1	–	MΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RC_{int} OUTPUT (PIN 44)						
C_o	parallel output capacitance		–	5	–	pF
$I_{ch(fr)}$	output charge current	frequency detector loop	–	±12	–	µA
$I_{ch(ph)}$	output charge current	phase detector loop	–	±24	–	µA
SYSCLKI INPUT (PIN 39); TRANSMIT MODE; V_{DD} = 3.4 TO 5.5 V						
f_{iclk}	input clock frequency	CLKSEL = 1; note 6	–	–	16(6)	MHz
		CLKSEL = 0; note 6	–	–	24(6)	MHz
SYSCLKO OUTPUT (PIN 40); RECEIVE MODE; V_{DD} = 3.4 TO 5.5 V						
$f_{oclk(l)}$	output clock frequency lower limit oscillator	CLKSEL = 1	2(8)	–	8.06(7)	MHz
		CLKSEL = 0	4(8)	–	12.09(7)	MHz
$f_{oclk(u)}$	output clock frequency upper limit oscillator	CLKSEL = 1	12.42(7)	–	26(8)	MHz
		CLKSEL = 0	18.63(7)	–	37(8)	MHz

Notes

1. Pull-up specified at input to V_{SS}, pull-down specified at input to V_{DD}.
2. Most timing specifications are related to clock periods. Two basic periods are of importance:

   T_c, this is the internal clock period of the TDA1315H being $1/128 f_s$ seconds.

   T_s, this is the system clock period such as SYSCLKI or SYSCLKO, being $1/256 f_s$ or $1/384 f_s$ seconds.

   It should be noted that in the receive mode clock frequencies are only reliable when the TDA1315H is in-lock.
3. In the transmit mode, when SYSCLKI is $384 f_s$ and 30% or 70% duty cycle: $t_{HD;DT}$ is $0.43 T_c$ minimum.
4. This time strongly depends on the external decoupling capacitor connected to V_{ref} (pin 2). When the capacitor is initially empty, it must first be charged before the oscillator can start.
5. Internally this resistor will be connected between RC_{fil} and V_{ref}, when there is no signal on the selected IEC input in receive mode, or when the oscillator is turned off. This is to prevent the oscillator to drift to extreme low or high frequencies. See also Chapter "Characteristics" with regards to $f_{oclk(l)}$ and $f_{oclk(u)}$.
6. These figures are theoretical limits for the TDA1315H. In the application, the maximum frequencies at f_s = 48 kHz will be fixed. Consequently f_{iclk} = 12.288 MHz (CLKSEL = 1) and f_{iclk} = 18.432 MHz (CLKSEL = 0).
7. These frequencies mean that the TDA1315H is guaranteed to lock in the range f_s = 31.5 to 48.5 kHz over the whole supply voltage range and specified temperature range.
8. These are the limit frequencies that the internal oscillator may reach under extreme conditions when the VCO input (pin RC_{fil}) would be controlled far beyond its normal tuning range. An internal resistor however, prevents that these frequencies can be reached when there is no signal to lock-on to. See also Chapter "Characteristics" regarding R_{tr}.

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611E"*. The number of this quality specification can be found in the *"Quality Reference Pocketbook"*. The pocketbook can be ordered using the code 9398 510 34011.

TEST AND APPLICATION INFORMATION

Figures 13 to 15 indicate typical systems environment of the TDA1315H. They are intended to give examples of which external blocks may be added to compose a system for particular requirements. The loop filter configuration and values in the examples meet the requirements for mid-end and high-end audio applications.

Test information

Table 12 Test pin functions.

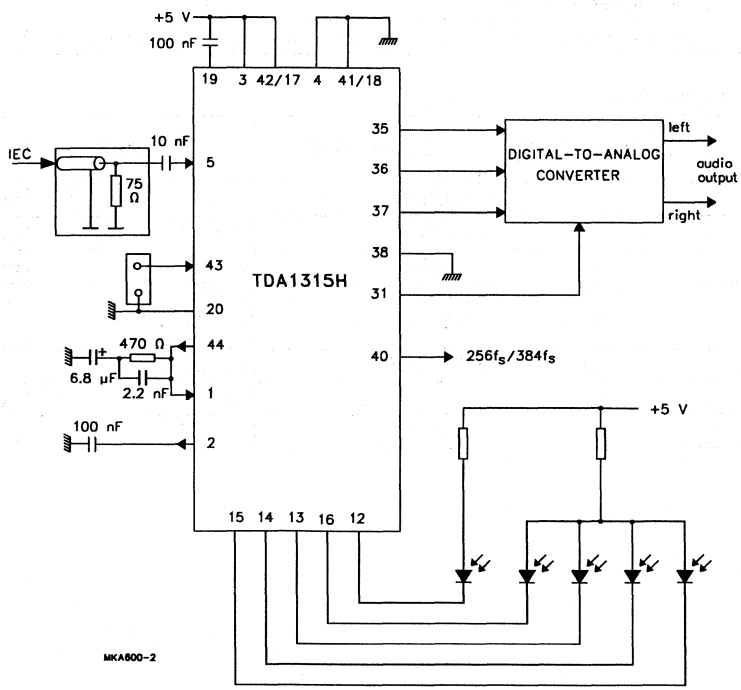
TEST PIN	DESCRIPTION
TESTA = 0	normal application operation
TESTA = 1	test mode i.e. system clock equals SYSCLKI
TESTB = 0	normal mode when TESTA = 1
TESTB = 1	scan mode when TESTA = 1; high-ohmic resistor between RC_{fil} and V_{ref} pins always disabled
TESTC = 0	normal operation
TESTC = 1	CHMODE equals system clock; IECO equals IECIN1 slicer output; RAM test enabled

Table 13 Implemented test scan chains.

SCAN NUMBER	LENGTH (BITS)	SCAN INPUT	OUTPUT	ACTIVE EDGE OF SYSCLKI
1	54	IECSEL	$\overline{FS32}$	negative
2	54	IECOEN	$\overline{FS44}$	negative
3	54	LADDR	$\overline{FS48}$	negative
4	54	MUTE	COPY	negative
5	53	LMODE	CHMODE	negative
6	53	STROBE	UDAVAIL	negative
7	51	I^2SSEL	DEEM	negative
8	31	CLKSEL	UNLOCK	positive

Stand alone application (receive only)

A very simple implementation of the stand-alone application is illustrated in Fig.13. In simple terms, it is an IEC-to-analog converter. The IEC signal is input via a shielded cable and enters the TDA1315H via its high-sensitivity input. The audio output is supplied to a DAC via the enabled I²S-bus Port, the DEEM output can be used to switch a de-emphasis network in and out of the signal path. The system clock frequency can be selected and is available should any digital filters in the DAC block require such a clock. The sample frequency of the received signal together with any out-of-lock condition of the phase-locked loop and the presence of a professional mode IEC signal can be displayed with LEDs.



When in a system both IECIN1 and IECIN0 inputs are used, the signal that is applied to the IECIN0 input must be kept away from the IECIN1 input on the printed-circuit board. Steep slopes of the IECIN0 input can be seen by the sensitive adjacent IECIN1 input. An extra capacitance parallel to the 75 Ω resistor, close to the TDA1315H, can help reduce the crosstalk if required. A suitable value is 180 pF.

Fig.13 Simple stand-alone application.

Microcontroller based application (receive and/or transmit)

The microcontroller-based application is illustrated in Fig.14. Functional blocks are shown for both the receive and the transmit mode. Here, the IEC signal is input via an optical fiber link and an associated optocoupler and enters the TDA1315H at its TTL-level input. The I²S-bus output signal is applied to a digital signal processing module, which may contain signal processors, DACs, a recording device etc. An ADC can be an optional source for that module. As the microcontroller can obtain all status information and data via the serial bus, it will provide display information and also will control the whole system, including the receive/transmit switch. For simplicity reasons, pin-based mode selection is not shown in this diagram. In the transmit mode, both system clock and I²S-bus timing are derived from a central timing block. The IEC output signal feeds an optical fiber link via a suitable optocoupler.

Concerning the wide supply voltage range of the TDA1315H, it is not possible to have a transformer-coupled IEC output that fulfils the *"IEC 958"* standard over the full supply voltage range. The output will have an amplitude of 0.5 V (p-p) with a tolerance of ±20%.

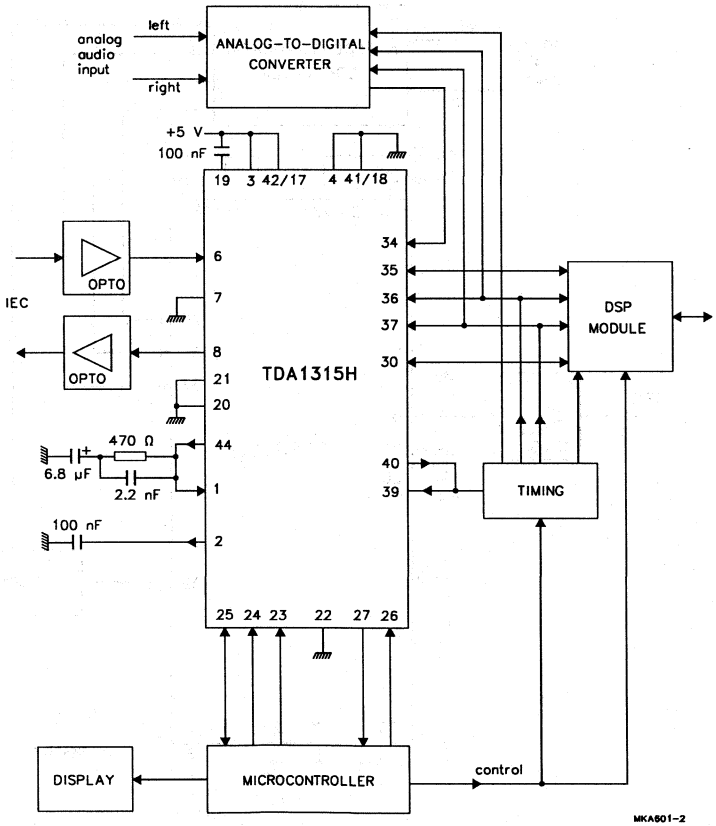


Fig.14 Microcontroller-based application.

Transmit mode only application (also possible without microcontroller)

In Fig.15 an example is given, how the TDA1315H can be operated as a transmitter without microcontroller. When the CTRLMODE pin is LOW, a reset applied to theTDA1315H will result in a default transmit mode. When the user is not interested in sending non-default channel status data (zeros) or user data, it remains always possible to encode audio data at the I^2S bus to the IEC output. When no microcontroller is used, the TDA1315H will remain fully pin programmable when STROBE is connected to supply permanently.

When the receive mode is not used, a dedicated loop-filter for the PLL is not necessary. However, for correct operation the TDA1315H does need a functional oscillator. The minimum configuration is defined by keeping pin 44 (RC_{int} output) floating and connecting pin 1 (RC_{fil} input) to pin 2 (V_{ref} output). For the resetting and standby functions the oscillator will operate correctly.

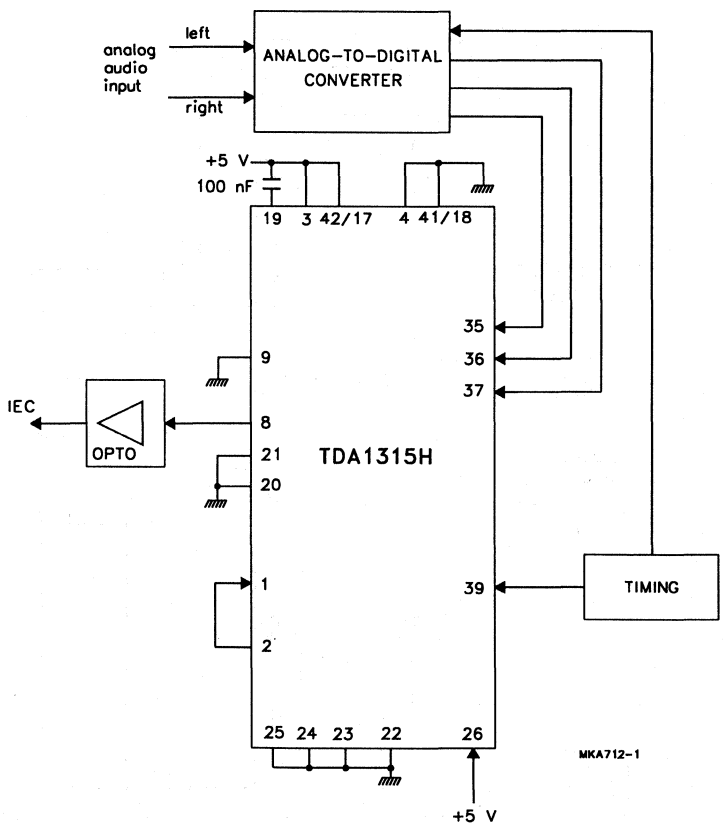


Fig.15 Transmit-mode-only application.

REFERENCES

1. *"Digital audio interface"*, first edition 1989-03, international standard *"IEC 958"*.
2. *"Digital audio interface for domestic use"*, Philips/Sony, September 1983.
3. *"I²S-bus specification"*, release 2-86, Philips export B.V., order number 9398 332 10011.
4. *"Amendment to document IEC 958: Digital audio interface"*, Project number. 84.11.02107.
5. *"SAA7310, development data sheet"*, Philips Semiconductors, October 1987, order number 9397 153 90142.

DCC read amplifier TDA1318

FEATURES

- Differential inputs for a low-power head configuration
- Low-noise current sources for the sense currents of the DCC head
- Reduced power consumption by separate on/off switching of the circuits and sense current of the DCC and CC parts of the IC
- The IC can be used with both the first and second generation DCC digital signal processing ICs
- High-impedance outputs in the OFF state so that the outputs of the ICs can be connected in parallel for dual decks or for decks with electrical auto-reverse heads
- AGC of DCC preamplifiers (can be switched off)
- Possibility of analog audio via DCC preamplifiers (analog via digital readers, ADR mode)
- Single 5 V supply.

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

The TDA1318 amplifies, filters and multiplexes signals arriving from magneto-resistive thin film heads (MRHs) which are suitable for DCC (Digital Compact Cassette) and CC (Compact Cassette) systems. The device also has current sources to provide sense currents through the DCC-MRHs and two amplifiers for magnetic feedback and biasing.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS[1]			MIN.	TYP.	MAX.	UNIT
		CS	SD	ADR				
V_{DD}	supply voltage	–	–	–	4.5	5.0	5.5	V
V_{CCM}	supply voltage feedback amplifiers	–	–	–	4.5	5.0	5.5	V
I_{DDDCC}	supply current DCC mode (note 2)	1	1	0	–	31	41	mA
$I_{DDDCCadr}$	supply current DCC mode (ADR)	1	1	1	–	31	41	mA
I_{DDCC}	supply current CC mode	1	0	0	–	9.7	13	mA
$I_{DDCCadr}$	supply current CC mode (ADR)	1	0	1	–	17.8	24.5	mA
I_{CCM}	supply current feedback amplifiers	1	1	1	–	8.5	12	mA
		1	0	0				
		1	0	1				
I_{DD}	supply current (ADC reference ON)	0	1	–	–	1.6	2.2	mA
$I_{DD(Q)}$	total quiescent current in OFF mode	0	0	–	–	–	300	µA
P_{tot}	total power dissipation, DCC mode	–	–	–	–	250	–	mW
T_{amb}	operating ambient temperature	–	–	–	–30	–	+85	°C

Notes

1. In the conditions column 0 = LOW; 1 = HIGH.
2. ADR = 1 when pin INL and/or INR is connected to V_{SS}.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1318H	44	QFP44S10[1]	plastic	SOT307-2

Note

1. When using IR reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocket book"* (order number 9398 510 34011) are followed.

BLOCK DIAGRAM

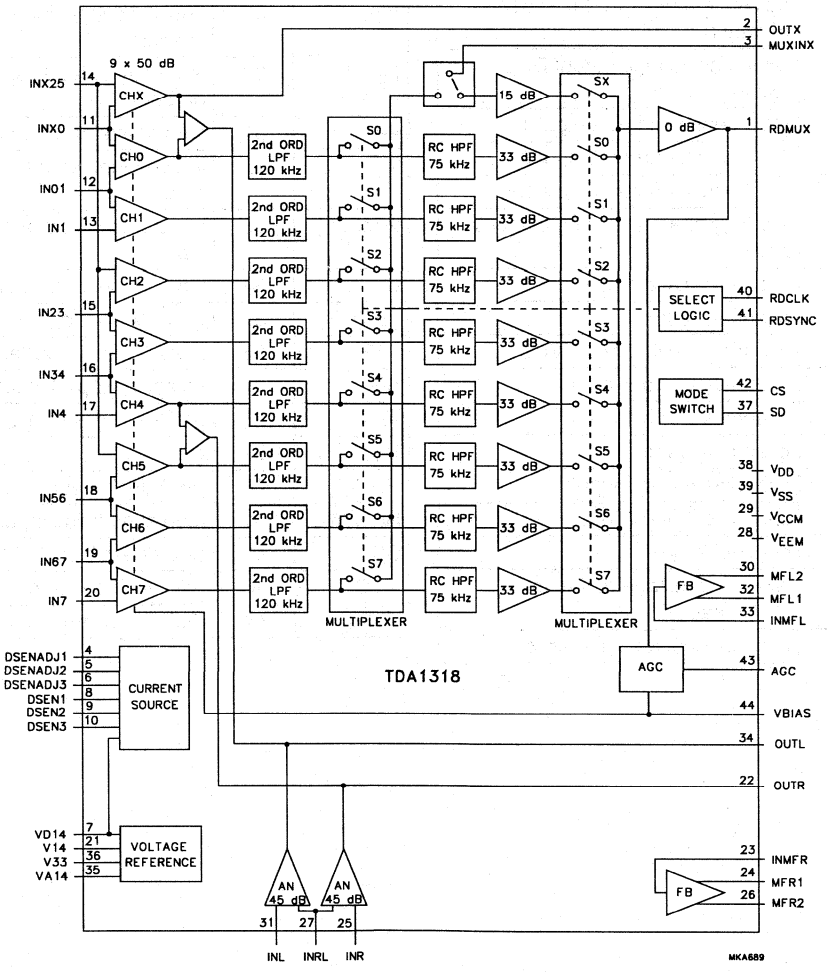


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RDMUX	1	output for sampled and multiplexed auxiliary and main data signals
OUTX	2	auxiliary channel preamplifier output
MUXINX	3	auxiliary channel multiplexer input
DSENAD J1	4	adjustment pin for DCC sense current 1
DSENAD J2	5	adjustment pin for DCC sense current 2
DSENAD J3	6	adjustment pin for DCC sense current 3
VD14	7	reference voltage output DCC sense
DSEN1	8	DCC sense current output 1
DSEN2	9	DCC sense current output 2
DSEN3	10	DCC sense current output 3
INX0	11	auxiliary channel input/channel 0 input
IN01	12	channels 0 and 1 input
IN1	13	channel 1 input
INX25	14	channels AUX, 2 and 5 input
IN23	15	channels 2 and 3 input
IN34	16	channels 3 and 4 input
IN4	17	channel 4 input
IN56	18	channels 5 and 6 input
IN67	19	channels 6 and 7 input
IN7	20	channel 7 input
V14	21	reference voltage output for DCC/analog inputs
OUTR	22	right channel analog output

SYMBOL	PIN	DESCRIPTION
INMFR	23	right channel feedback amplifier input
MFR1	24	right channel feedback amplifier output 1
INR	25	right channel analog input
MFR2	26	right channel feedback amplifier output 2
INRL	27	right/left channel analog input
V_{EEM}	28	ground for feedback amplifiers
V_{CCM}	29	positive supply for feedback amplifiers
MFL2	30	left channel feedback amplifier output 2
INL	31	left channel analog input
MFL1	32	left channel feedback amplifier output 1
INMFL	33	left channel feedback amplifier input
OUTL	34	left channel analog output
VA14	35	reference voltage output CC sense
V33	36	ADC reference voltage output
SD	37	select DCC part input
V_{DD}	38	positive supply voltage
V_{SS}	39	ground
RDCLK	40	read clock input
RDSYNC	41	read sync pulse input
CS	42	chip select input
AGC	43	AGC time constant
VBIAS	44	DCC preamplifier control voltage

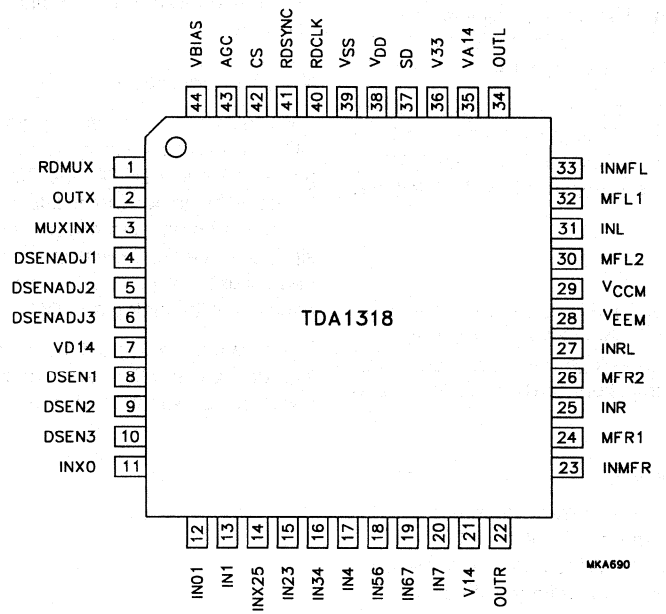


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

DCC data amplifiers

For DCC operation the TDA1318 has eight channels for the main data and one channel for the auxiliary data. The eight main data channels have low-noise preamplifiers, pre-equalisation for frequencies from 1 kHz to 50 kHz (1st order high-pass filter, –3 dB point 75 kHz) and low-pass filtering for anti-aliasing (2nd order active, –3 dB point 120 kHz). The auxiliary channel has a preamplifier with a flat frequency response. A continuous output (OUTX) is available for this channel. All inputs are differential and must be AC-coupled to the MRHs. The inputs are internally biased by V14.

Automatic gain control

The DCC part is equipped with an AGC circuit which diminishes the gain of the DCC preamplifiers when the level at output RDMUX exceeds a preset value. In this way, an optimum voltage swing at the RDMUX output is obtained. The response time of the AGC can be set by an external capacitor at pin 43. There is a fixed relation between the source and sink current at this pin. This results in a fixed relationship between decay and recovery time of the gain. The AGC can be switched off by connecting pin 43 to V_{SS}. In this condition the preamplifier gains are maximum, as specified in Chapter "Characteristics".

Multiplexer

A multiplexing circuit switches the nine digital channels sequentially to the output. The AUX data is switched to the output buffer during two clock periods, the eight main data channels are all sampled for one clock period. The effective sample frequency is one tenth of the clock frequency at RDCLK. Multiplexer timing is illustrated in Fig.4.

Analog amplifiers

For Compact Cassette operation the TDA1318 has two low-noise preamplifiers, and two amplifiers for the magnetic feedback current. The analog amplifier inputs are differential, and must be AC-coupled to the MRHs. The analog inputs are internally biased by V14.

When one of the analog inputs, INL or INR, is connected to V_{SS} the circuit is set to the ADR mode. In this condition the analog amplifiers are switched OFF and four DCC preamplifiers are available for amplification of the left and right analog signals.

Feedback amplifiers

Two feedback amplifiers are available for driving a coil in the MRH, thus providing a feedback loop in order to improve the linearity of the analog audio response. In the DCC mode the feedback amplifiers can be used for biasing the MRH (for ADR = 1).

Current and voltage sources

Separate, adjustable low-noise current sources are present for the sense currents of the DCC MRHs. The DC output voltages V14, VA14, VD14, and V33 are derived from an internal bandgap voltage reference source.

VD14 is a reference voltage for the DCC sense current sources. VA14 (referenced to V_{SS}) can be used to control external sense current sources. V33 (referenced to V_{SS}) can be used as reference voltage for an analog-to-digital converter.

Modes of operation

The amplifiers and sense current circuits of the DCC and CC parts can be switched ON or OFF separately by the mode switch signals CS and SD. In addition, a connection of one of the analog inputs INL or INR to V_{SS} is recognized as the ADR mode, thereby providing amplification of audio signals by the DCC preamplifiers. This enables the use of heads containing only DCC readers as well as heads equipped with analog and DCC readers.

The data and analog output buffers have high-output impedance in the OFF state, thus allowing the outputs of ICs to be connected in parallel.

Table 1 Total supply current per mode.

MODE	CS	SD	ADR	TYP. $I_{DD} + I_{CCM}$ (mA)	MAX. $I_{DD} + I_{CCM}$ (mA)
OFF	0	0	X	<0.3	0.3
ADC reference only	0	1	X	1.6	2.2
CC	1	0	0	18.2	25.0
CC via DCC inputs	1	0	1	26.3	36.5
DCC (analog and digital readers)	1	1	0	31.0	41.0
DCC (digital readers only)	1	1	1	39.5	53.0

Table 2 Modes of operation.

MODE	CONTROL SIGNAL			DCC PART	CC PART	FB AMPS	ADC REF	OUTPUTS SWITCHED OFF	OUTPUTS ENABLED
	CS	SD	ADR[1]						
OFF	0	0	X	off	off	off	off	OUTX; RDMUX; OUTL; OUTR	–
ADC reference only	0	1	X	off	off	off	on	OUTX; RDMUX; OUTL; OUTR	V33
CC	1	0	0	off	on	on	off	OUTX; RDMUX	OUTL; OUTR
CC via DCC inputs	1	0	1	on[2]	on[3]	on	off	OUTX; RDMUX	OUTL; OUTR
DCC (analog and digital readers)	1	1	0	on	off	off	on	OUTL; OUTR	V33; OUTX; RDMUX
DCC (digital readers only)	1	1	1	on	off	on	on	OUTL; OUTR	V33; OUTX; RDMUX

Notes

1. ADR = 1 when pin INL and/or INR is connected to V_{SS}.
2. Preamplifiers only; AGC disabled.
3. Output stages only; VA14 off.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	$V_{SS} = 0$; $V_{EEM} = 0$	−0.3	5.5	V
V_{CCM}	supply voltage feedback amplifiers		−0.3	5.5	V
ΔV	difference in ground potential between V_{SS} and V_{EEM}		0	0	V
V_I	voltage on any pin	$V_{DD} + 0.5 < 5.5$ V	0.3	$V_{DD} + 0.5$	V
I_{EEM}	maximum ground current (pin 28)		–	±120	mA
I_{CCM}	maximum supply current (pin 29)		–	±120	mA
I_n	maximum current on pins 24, 26, 30 and 32		–	±80	mA
I_{DD}	maximum supply current (pin 38)		–	±80	mA
I_{SS}	maximum ground current (pin 39)		–	±80	mA
I_{max}	maximum current on all other pins		–	±20	mA
P_{tot}	total power dissipation		–	350	mW
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		−30	+85	°C
V_{es}	electrostatic handling		−2000	+2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	90 K/W

CHARACTERISTICS

V_{DD} = 5 V; V_{CCM} = 5 V; V_{SS} = V_{EEM} = 0 V; f_{clk} = 3.072 MHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		4.5	5.0	5.5	V
V_{CCM}	supply voltage feedback amplifiers		4.5	5.0	5.5	V
I_{DDDCC}	supply current DCC part	CS = 1; SD = 1; ADR = 0	21	31	41	mA
		CS = 1; SD = 1; ADR = 1	21	31	41	mA
I_{DDCC}	supply current CC amplifiers	CS = 1; SD = 0; ADR = 0	7	9.7	13	mA
		CS = 1; SD = 0; ADR = 1	12.5	17.8	24.5	mA
I_{CCM}	supply current feedback amplifiers	note 1	6.0	8.5	12	mA
I_{DD}	supply current (ADC reference ON)	CS = 0; SD = 1	1.1	1.6	2.2	mA
I_{tot}	total current in OFF state of I_{DD} and I_{CCM}	CS = 0; SD = 0	–	–	300	µA
V_{ref}	reference voltage for DCC inputs (pin 21)	I_o < –1 mA	1.3	1.4	1.5	V
	reference voltage for DCC sense (pin 7)	I_o < –20 µA	1.25	1.4	1.55	V
	reference voltage for CC sense (pin 35)	I_o < –20 µA	1.25	1.4	1.6	V
	reference voltage for ADC (pin 36)	I_o < –2.5 mA	3.2	3.3	3.4	V
DCC part						
AMPLIFIER CHANNEL 0 TO 7; NOTE 2						
G	amplifier gain	f_i = 50 kHz	75	78	81	dB
		f_i = 100 kHz	75	80	83	dB
ΔG	relative gain	f_i = 10 kHz; note 3	–14	–12	–10	dB
		f_i = 300 kHz; note 3	–22	–12	–3	dB
V_O	DC output voltage	note 4	1.8	2.1	2.4	V
V_{os}	DC offset voltage between channels	note 4	–	–	300	mV
$V_{n(ref)}$	input referred noise voltage	f_i = 50 kHz; R_{source} = 70 Ω	–	1.9	–	nV√Hz
$\Delta V_{n(ref)}$	3 × standard deviation in amplitude spread of input referred noise	f_i = 50 kHz; R_{source} = 70 Ω	–	0.5	–	nV√Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion	f_i = 10 kHz; V_1 = 0.5 V (RMS)	–	–40	–30	dB
Z_i	input impedance to V_{SS}		8	11	–	kΩ
SR	supply rejection	f_i = 50 kHz; note 5	–	–18	–30	dB
α_{cs}	channel separation	f_i = 10 kHz	30	40	–	dB
AMPLIFIER AUXILIARY CHANNEL; CHANNEL X; NOTE 2						
G_2	amplifier gain at pin 2	f_i = 100 Hz to 100 kHz	48	51	54	dB
G_1	amplifier gain at pin 1	f_i = 100 Hz to 100 kHz; note 6	62	65	68	dB
$V_{n(ref)}$	input referred noise voltage	f_i = 10 kHz; R_{source} = 70 Ω	–	1.9	–	nV√Hz
$\Delta V_{n(ref)}$	3 × standard deviation in amplitude spread of input referred noise	f_i = 10 kHz; R_{source} = 70 Ω	–	0.5	–	nV√Hz
$V_{2(rms)}$	maximum output voltage (RMS value)	f_i = 10 kHz	0.5	–	–	V
THD	total harmonic distortion	f_i = 1 kHz; V_1 = 0.5 V (RMS)	–	–40	–30	dB
SR	supply rejection	f_i = 1 kHz; note 5	–	–6	–15	dB
$R_{L(DC)}$	DC load to V_{SS} (pin 2)		10	–	–	kΩ
$C_{L(AC)}$	AC load to V_{SS} (pin 2)		–	–	100	pF
Z_o	output impedance at pin 2 in OFF state	see Table 2	1	–	–	MΩ
OUTPUT BUFFER: PIN 1 (RDMUX)						
$V_{1(rms)}$	maximum output voltage (RMS value)	R_L = 2 kΩ	0.5	–	–	V
$R_{L(DC)}$	DC load to V_{SS}		2	–	–	kΩ
t_{set}	settling time	R_L = 2 kΩ; C_L = 100 pF; setting within 10 mV	–	100	150	ns
Z_o	output impedance in OFF state	see Table 1	1	–	–	MΩ
$V_{1(rms)}$	AGC level (RMS value)	note 7	120	270	410	mV
ΔV_1	AGC voltage range		8	9.5	12	dB
I_{source}	AGC source current (pin 43)		–	80	–	µA
I_{sink}	AGC sink current (pin 43)		–	0.7	–	µA
SELECTED LOGIC AND MODE SWITCH: PINS RDCLK, RDSYNC, CS AND SD						
V_{IH}	HIGH level input voltage		2.2	–	5.0	V
V_{IL}	LOW level input voltage		0	–	1.0	V
I_{LI}	input leakage current		–10	0	+10	µA
C_i	input capacitance	note 8	–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{su}	set-up time RDCLK and RDSYNC	note 9	20	–	–	ns
t_h	hold time RDCLK and RDSYNC	note 9	20	–	–	ns
t_r	rise time	note 9	–	–	50	ns
V_{ADR}	ADR mode detection level (pins 25 and 31)		0	–	0.4	V
V_{TEST}	test mode detection level (pin 27)		0	–	0.4	V
SENSE CURRENT SOURCE						
$I_{DSEN(min)}$	minimum output current	note 10	–	–	5	mA
$I_{DSEN(max)}$	maximum output current	note 11	20	–	–	mA
I_{no}	output noise current	note 11	–	20	–	pA√Hz
Z_o	output impedance	I_{DSEN} = 10 mA	20	–	–	kΩ
CC part						
ANALOG AMPLIFIER						
G	amplifier gain	f_i = 20 Hz to 20 kHz	43	45	47	dB
$V_{i(rms)}$	input voltage level (RMS value)	f_i = 1 kHz	–	2.75	–	mV
$V_{n(ref)}$	input referred noise voltage	f_i = 10 kHz; R_{source} = 300 Ω	–	2.8	–	nV√Hz
$\Delta V_{n(ref)}$	3 × standard deviation in amplitude spread of input referred noise	f_i = 10 kHz; R_{source} = 300 Ω	–	1.0	–	nV√Hz
$V_{o(rms)}$	maximum output voltage (RMS value)	f_i = 1 kHz	0.5	–	–	V
THD	total harmonic distortion	f_i = 1 kHz; V_o = 0.5 V (RMS)	–	–60	–50	dB
SR	supply rejection	f_i = 1 kHz; note 5	–	37	–	dB
α_{cs}	channel separation	f_i = 1 kHz	40	–	–	dB
$R_{L(DC)}$	DC load to V_{SS} (pins 22 and 34)		10	–	–	kΩ
$C_{L(AC)}$	AC load to V_{SS} (pins 22 and 34)		–	–	300	pF
Z_o	output impedance in OFF state (pins 22 and 34)	see Table 2	1	–	–	MΩ
ANALOG INPUT VIA DCC PREAMPLIFIERS						
G	amplifier gain	f_i = 20 Hz to 20 kHz	48	51	54	dB
$V_{i(rms)}$	input voltage level (RMS value)	f_i = 1 kHz	–	1.4	–	mV
$V_{n(ref)}$	input referred noise voltage	f_i = 10 kHz; R_{source} = 70 Ω	–	1.9	–	nV√Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta V_{n(ref)}$	3 × standard deviation in amplitude spread of input referred noise	f_i = 10 kHz; R_{source} = 70 Ω	–	0.5	–	nV√Hz
$V_{o(rms)}$	maximum output voltage (RMS value)	f_i = 1 kHz	0.5	–	–	V
THD	total harmonic distortion	f_i = 1 kHz; V_1 = 0.5 V (RMS)	–	–40	–30	dB
SR	supply rejection	f_i = 1 kHz; auxiliary data channel; see Fig.6	–	–6	–	dB
α_{cs}	channel separation	f_i = 1 kHz	40	–	–	dB
FEEDBACK AMPLIFIER						
$I_{o(rms)}$	maximum output current (RMS value)	note 12	30	–	–	mA
THD	total harmonic distortion	note 13	–	–60	–50	dB
B	bandwidth	note 14	50	–	–	kHz

Notes

1. CS = 1, SD = 1, ADR = 1; CS = 1, SD = 0, ADR = 0; CS = 1, SD = 0, ADR = 1; feedback amplifiers unloaded. The supply pins for the feedback amplifiers are pins 28 and 29. The supply pins for all other circuits are pins 38 and 39 (see Tables 1 and 2).
2. AGC circuit OFF (maximum gain; pin 43 connected to V_{SS}).
3. Gain relative to gain at f_i = 50 kHz. See Fig.5 for typical frequency response.
4. Difference between minimum and maximum DC level at the outputs of the data channels. To be measured at pin 1.
5. See Figs 6 and 7 for typical supply rejection.
6. Pin 2 AC-coupled to pin 3 via 100 nF capacitor.
7. Measured with a continuous sinewave of 10 kHz at pin 1, multiplexer in a fixed position. A 1 V (RMS) sinewave corresponds with a multiplexed DCC signal of 4.3 V (p-p).
8. Periodically sampled, not tested.
9. Timing relationship between the edges of RDCLK and RDSYNC is illustrated in Fig.3. Figure 4 illustrates the action of the multiplexer switches.
10. The output current can be adjusted by connecting a resistor between the adjust pin and V_{SS}. A 68 Ω resistor will produce 10 mA (typ.) through the MRHs (see Fig.9).
11. A resistor of 210 Ω connected between sense current output and V_{DD}; frequency range from 10 kHz to 100 kHz; sense current = 10 mA; pin 7 decoupled to V_{SS} by 10 μF capacitor.
12. Closed loop; unity gain; f_i = 1 kHz; THD < –45 dB; R_L = 40 Ω; in accordance with Fig.10.
13. Closed loop; unity gain; f_i = 1 kHz; 10 mA (RMS) output current into 40 Ω; in accordance with Fig.10.
14. Closed loop; unity gain; –3 dB bandwidth; measured in test circuit of Fig.10.

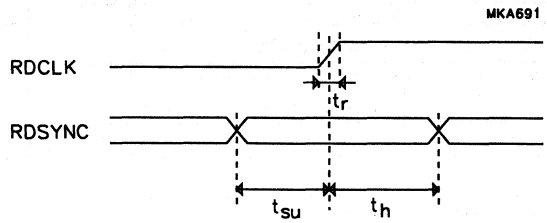


Fig.3 Timing relationship between the edges of RDCLK and RDSYNC.

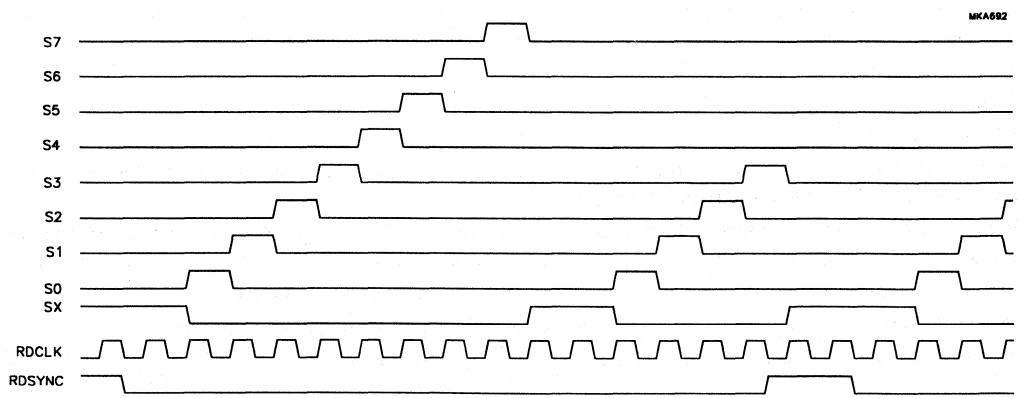


Fig.4 Multiplexer timing diagram.

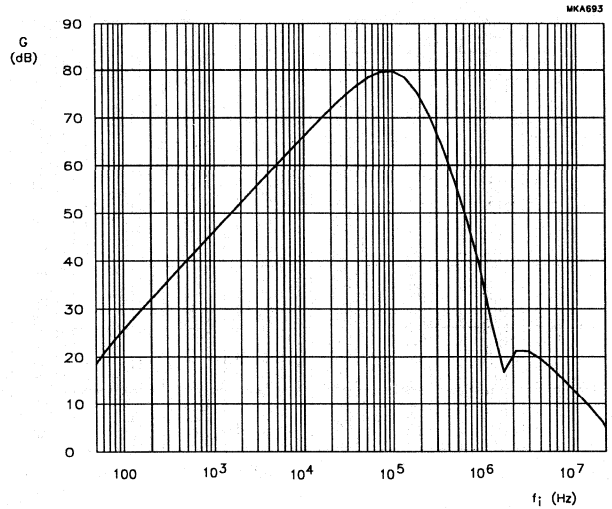


Fig.5 Typical gain of main data channel (AGC off).

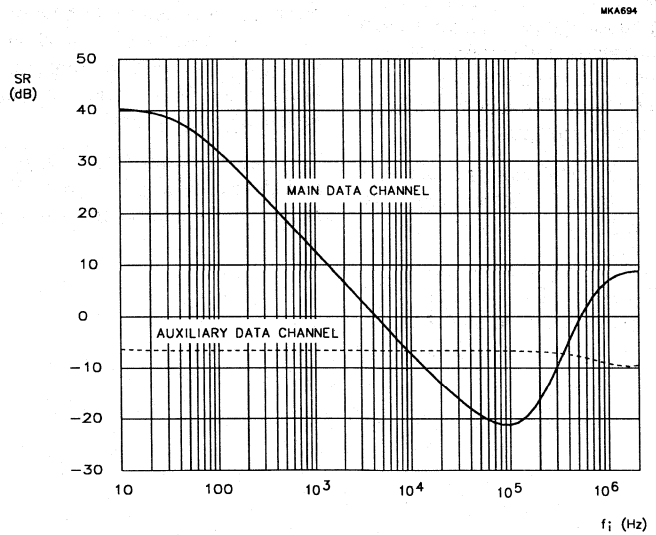


Fig.6 Typical supply rejection of main data and auxiliary data channel (AGC off).

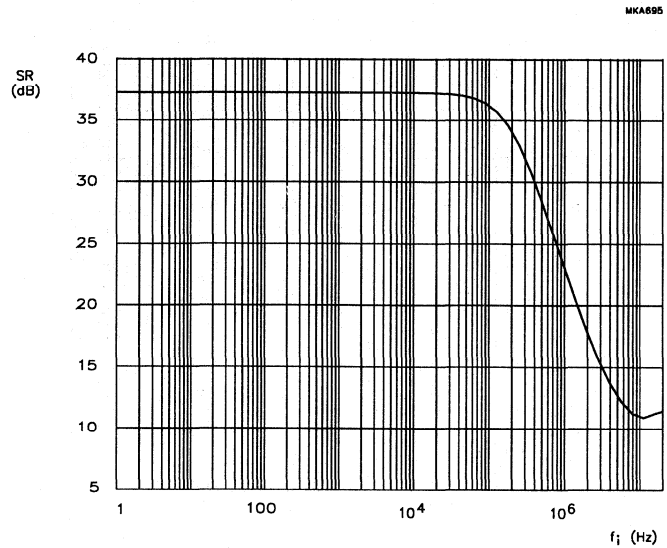


Fig.7 Typical supply rejection of analog amplifier.

TEST INFORMATION

The circuit can be set to the TEST mode by connecting pin 27 to V_{SS}. In this configuration the multiplexer at pin 3 allows monitoring of the input stage and low-pass filter of each digital amplifier, and also allows input to the high-pass filter of the second stage. The test multiplexer operates in phase with the output multiplexer.

Measurement of the gain of the digital channels can be carried out in two steps: the gain from DCC input to pin 3, and the gain from pin 3 to pin 1.

Figure 8 illustrates how to use pin 3 in the test mode; $C_L < 20$ pF, $R_L > 100$ kΩ, $C_i > 47$ nF, $R_{bias} = 1$ kΩ. The DC voltage, when driving pin 3, should be 0.7 V greater than the measured DC level at pin 3 in order to shut-off the emitter follower. The impedance of the sense current source outputs can be measured from the difference in sense current when applying different voltages to the sense current output. This voltage can vary from 1.5 V to V_{DD}. Figure 9 illustrates the principle of the sense current sources.

The feedback amplifiers consist of two operational amplifiers providing one input and a differential output with respect to the internal 2.5 V reference (see Fig.10).

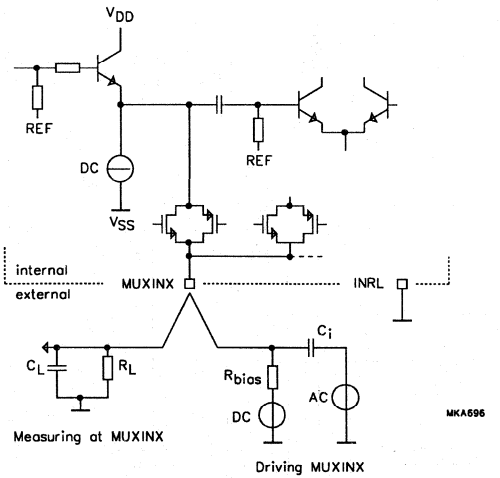


Fig.8 Test by using MUXINX (pin 3).

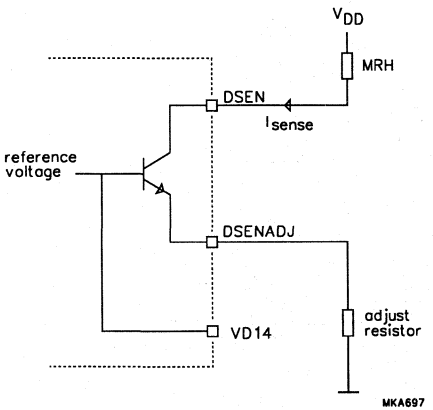


Fig.9 Principle of the sense current source.

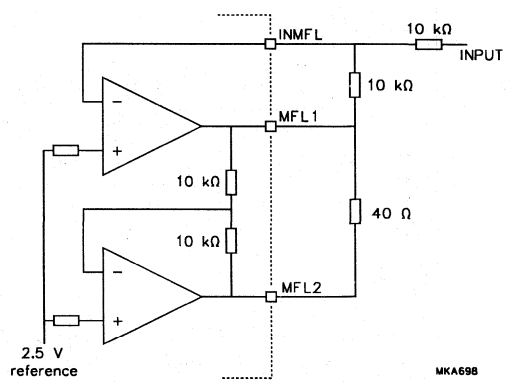


Fig.10 Principle of the feedback amplifier and test circuit.

APPLICATION INFORMATION

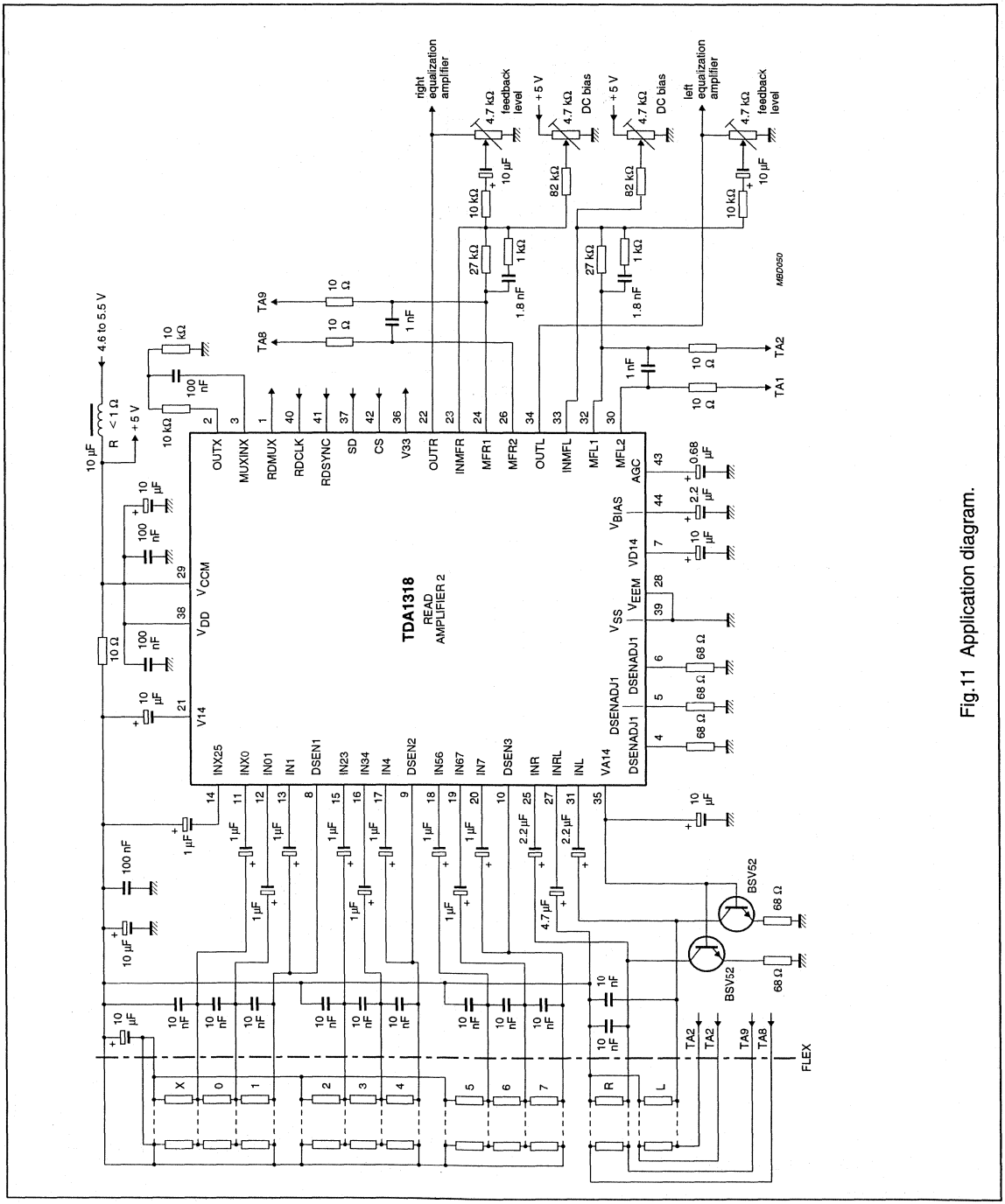


Fig.11 Application diagram.

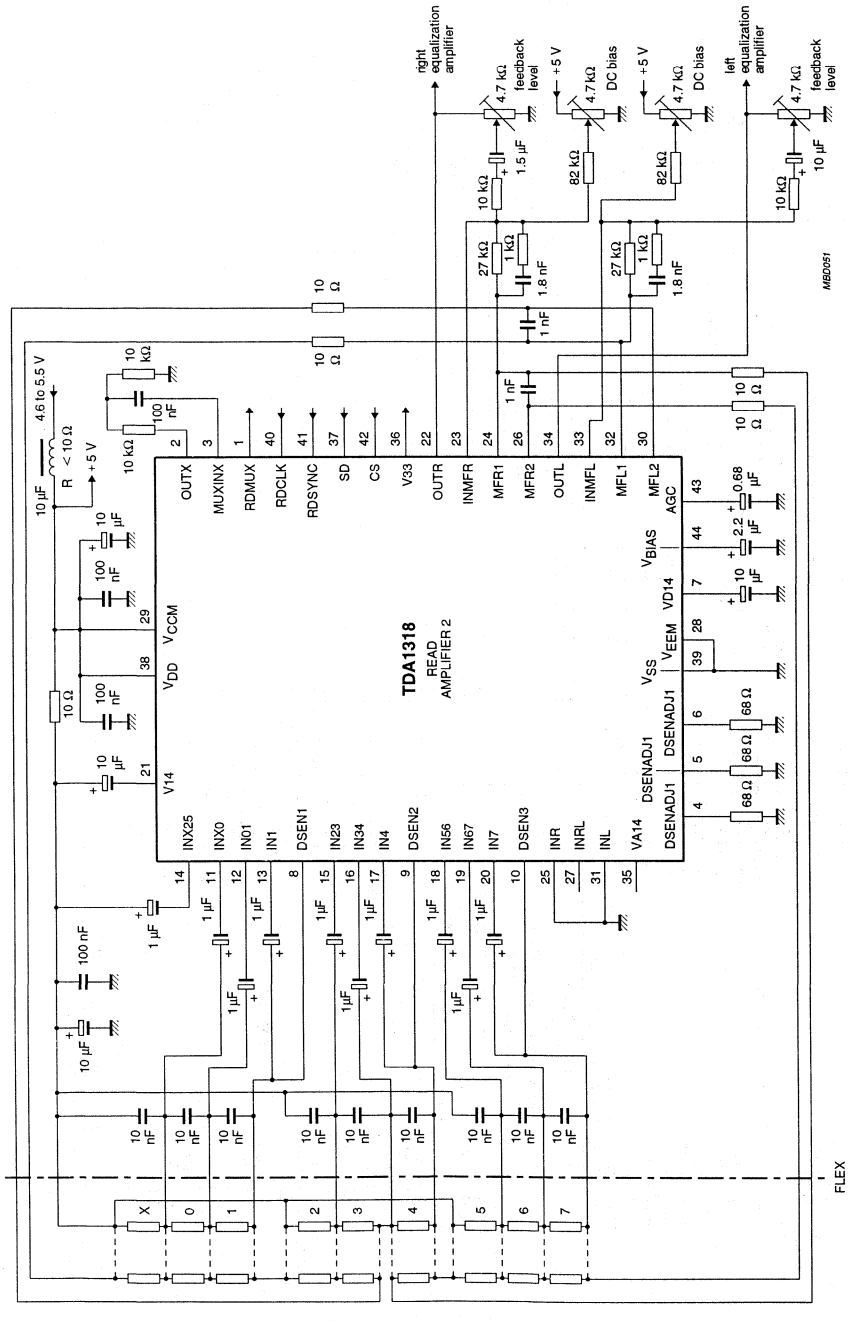


Fig.12 Application diagram, read amplifier 2 in ADR mode.

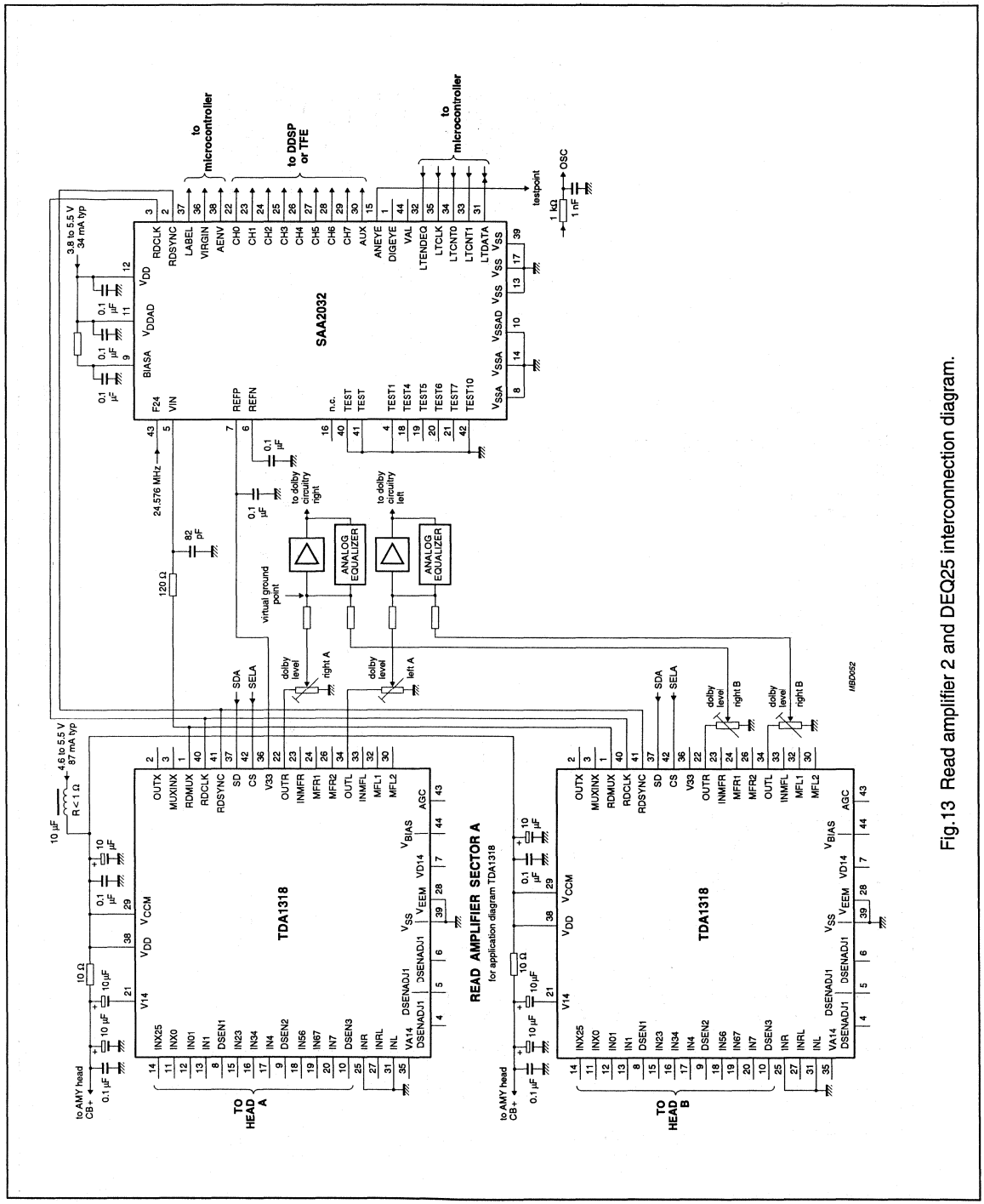


Fig.13 Read amplifier 2 and DEQ25 interconnection diagram.

DCC write amplifier (write 2) TDA1319T

FEATURES

- Bidirectional high current output drivers
- Single point current setting
- Extra erase current for the auxiliary channel
- Increased current for auxiliary data
- Low standby power consumption
- Short-circuit protection to ground
- Serial data input
- Reduced RF emission due to slope control of write current.

GENERAL DESCRIPTION

The TDA1319T has been designed to drive an inductive recording head which is suitable for DCC (Digital Compact Cassette) systems.
The bidirectional current outputs are controlled by a two-wire serial bus.
The amplitude of the write current can be set using an external resistor. The circuit can be switched to the standby mode to minimize supply current consumption.

DIGITAL dcc COMPACT CASSETTE

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.75	5.0	5.5	V
V_{DDO}	supply voltage (write outputs)		4.75	5.0	5.5	V
I_{DD}	supply current	note 1	–	7.5	11	mA
I_{DDO}	supply current (write outputs)	note 2	–	–	255	mA
		note 3	–	–	365	mA
		note 4	–	–	285	mA
I_{sb}	total standby current	note 5	–	2	3	mA
T_{amb}	operating ambient temperature		–30	–	+85	°C

Notes

1. 1 kΩ erase adjust resistor connected between pins 5 and 6, no load at pin 9.
2. Momentary maximum value during write data; see Table 1; I_O = 225 mA.
3. Momentary maximum value during erase AUX; see Table 1 and Fig.5; resistor R_e connected between pins 5 and 6 (see Fig.7).
4. Momentary maximum value during write AUX; see Table 1; I_O = 255 mA.
5. Standby mode; see Table 1; $I_{sb} = I_{DD} + I_{DDO} + I_{clamp}$.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1319T	24	SO24L	plastic	SOT137-1

BLOCK DIAGRAM

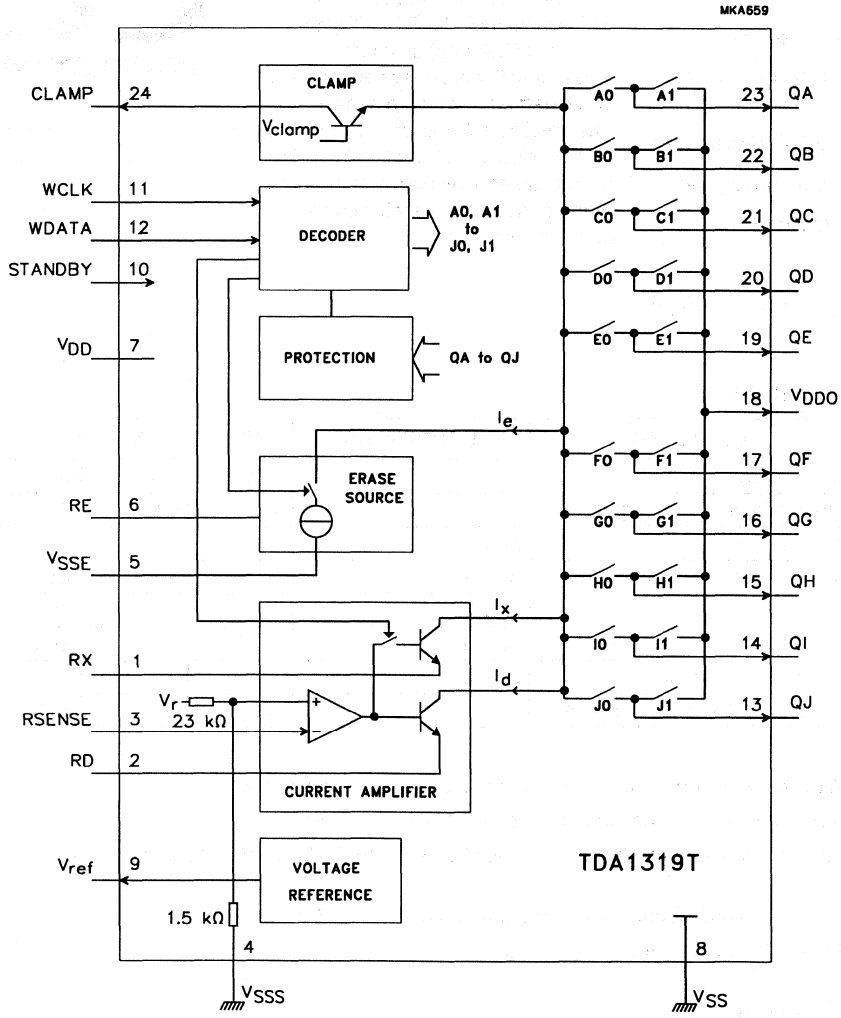


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RX	1	auxiliary current adjust resistor
RD	2	data current adjust resistor
RSENSE	3	sense voltage positive input
V_{SSS}	4	sense voltage ground
V_{SSE}	5	erase current source ground
RE	6	erase current adjust resistor
V_{DD}	7	supply voltage
V_{SS}	8	ground
V_{ref}	9	reference voltage output
STANDBY	10	standby mode control input
WCLK	11	write clock input
WDATA	12	write data input
QJ	13	write pulse output
QI	14	write pulse output
QH	15	write pulse output
QG	16	write pulse output
QF	17	write pulse output
V_{DDO}	18	supply voltage (write outputs)
QE	19	write pulse output
QD	20	write pulse output
QC	21	write pulse output
QB	22	write pulse output
QA	23	write pulse output
CLAMP	24	clamp current output

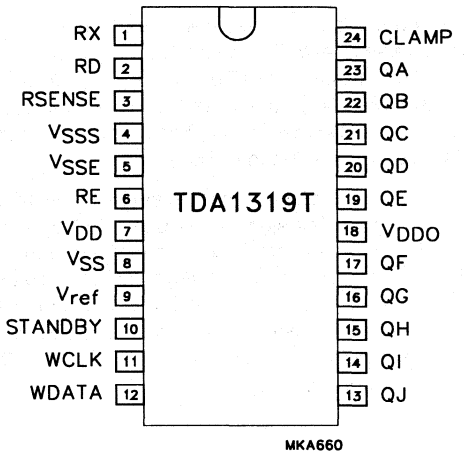


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1319T is designed to drive the nine elements of the multichannel recording head (as used in a DCC recorder) by forcing a current through the selected path. A brief functional description of each block (see Fig.1) is given below.

Decoder

The IC is controlled by the 32-bit wide serial dataword which is clocked in at WDATA (pin 12). The clock frequency (WCLK, pin 11) is 3.072 MHz with a clock period of 325 ns. The write pulses are made available at the outputs QA to QJ (see Fig.4). The timing sequence of the write pulses is illustrated in Fig.5.

The operating mode of the IC can be set by the first 3 bits of data (see Fig.5). The signals TCH0 to TCH7 and TERAUX determine the direction of the write current. When TCHn is HIGH, the current flows as indicated in Fig.4. When TCHn is LOW current flows in the opposite direction. The various modes of operation are given in Table 1. The standby mode can also be forced by setting the STANDBY input (pin 10) HIGH.

Current amplifier

The write current at the outputs is regulated by the current amplifier. The value of the current I_d can be set using an external resistor R_d, connected between pin 2 and V_{SS} (see Fig.9). The current through R_d also flows at the outputs. The current amplifier regulates the voltage across R_d, which is measured between RSENSE and V_{SSS} (pins 3 and 4), to a value of 150 mV (see Chapter "Characteristics"). This force-sense technique eliminates the influence of parasitic series impedances.

The output of the current amplifier is internally switched to the output pins QA to QJ. During AUX write (outputs QA and QB active) an additional current I_x is added to the write current. This current can be controlled by a resistor R_x connected between RX (pin 1) and V_{SS}. R_X must be $6.7 \times R_d$ for 1.2 dB current increase.

During the erase mode of the auxiliary channel (TERAUX = HIGH; see Table 1) it is possible to let an additional output current Ie flow through QA and QB (pins 23 and 22). This extra current can be adjusted with an external resistor R_e connected between pins 6 and 5. Pin 5 must be externally connected to ground. A typical value of the extra current can be calculated from the response curve of Fig.7.

Voltage reference

A reference voltage is available at pin 9. This voltage is derived from a bandgap reference source and can be used to modify the voltage sensed by the current amplifier, e.g. for external temperature compensation.

Outputs

Each channel is selected in sequence. Depending on the dataword, the current is directed forward or reversed through the heads. The outputs that are not selected are kept floating to prevent any incorrect current flow. A simplified schematic of one output stage is illustrated in Fig.3. In the HIGH state (one of the switches A1 to J1 is closed) the output is internally connected to a fixed voltage V_{OH} (see Chapter "Characteristics"). In the LOW state (one of the switches A0 to J0 is closed) the output is connected to the current amplifier. The voltage developed across the output pin pairs must not exceed a certain value, otherwise the lower switch transistor (Fig.3) will become saturated.

Clamp circuit

During the periods that the head elements are not selected, the clamp circuit accommodates the write current. This current is directed through an external resistor from pin 24 to the supply, in order to have less dissipation in the IC. The clamping results in a constant current being drawn from the supply and therefore reduces emission of interferences (the DC level at pin 24 must not fall lower than 1.8 V).

Standby

The circuit is in the standby mode when TDAPLB = 1 and TAUPLB = 1 (see Table 1 and Fig.6), or when a HIGH level is applied to pin 10. After a HIGH-to-LOW transition at pin 10, the IC will remain in the standby mode until TDAPLB = 0 or TAUPLB = 0. When the IC is in the standby mode, the current amplifier is switched off to minimize the power consumption, switches A to J are open-circuit and the voltage reference and the erase source are switched off.

Protection

The IC is immediately switched to standby mode when a short-circuit to ground at an output pin is detected ($V_o < 0.5$ V; see Fig.6, "SHORT"). When the short-circuit condition is removed, the IC will resume operation. The state of the decoder is not affected by a "SHORT".

Table 1 Modes of operation.

DATA CHANNELS 0 TO 7	AUXILIARY CHANNELS	CONTROL BITS[1]			REMARKS
		TDAPLB (DATA CHANNEL PLAYBACK)	TAUPLB (AUXILIARY CHANNEL PLAYBACK)	TERAUX (AUXILIARY CHANNEL ERASE)	
Read	read	1	1	X	standby mode
Write (I_d)	read	0	1	X	
Write (I_d)	write ($I_d + I_x$)	0	0	0	
Write (I_d)	erase ($I_d + I_x + I_e$)	0	0	1	
Read	write ($I_d + I_x$)	1	0	0	
Read	erase ($I_d + I_x + I_e$)	1	0	1	

Note

1. X = don't care; 0 = LOW; 1 = HIGH.

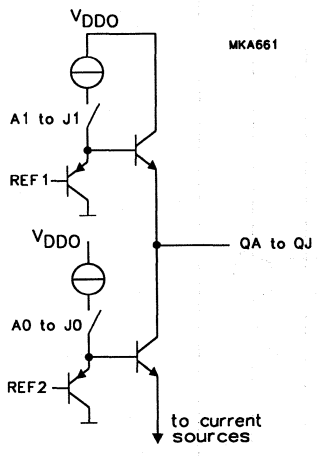


Fig.3 Simplified schematic of ONE output stage.

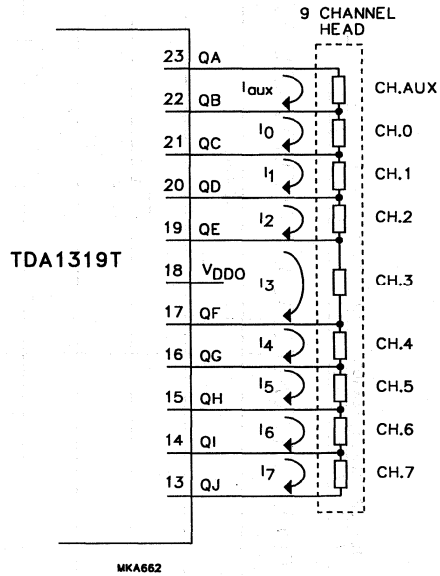


Fig.4 Output current definition.

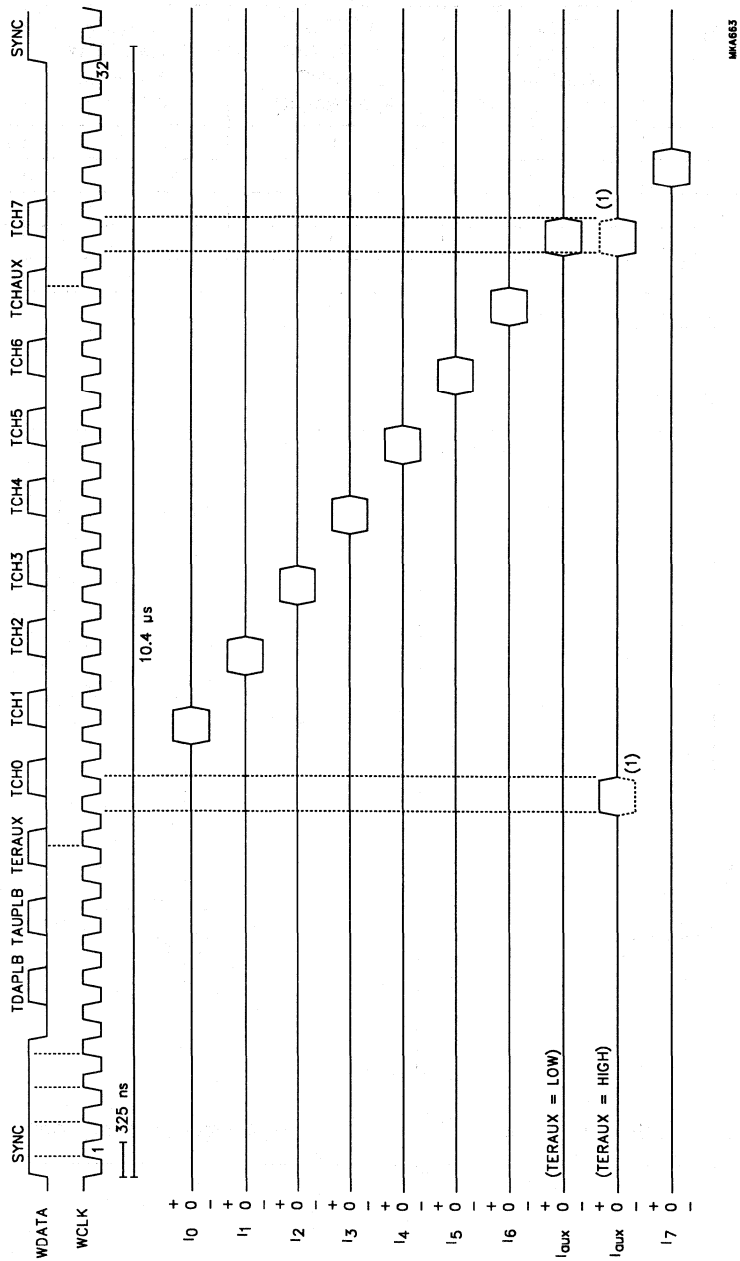


Fig.5 Data format and timing sequence of write pulse.

(1) Erase pulses are inverted every other cycle of 32 clock pulses.

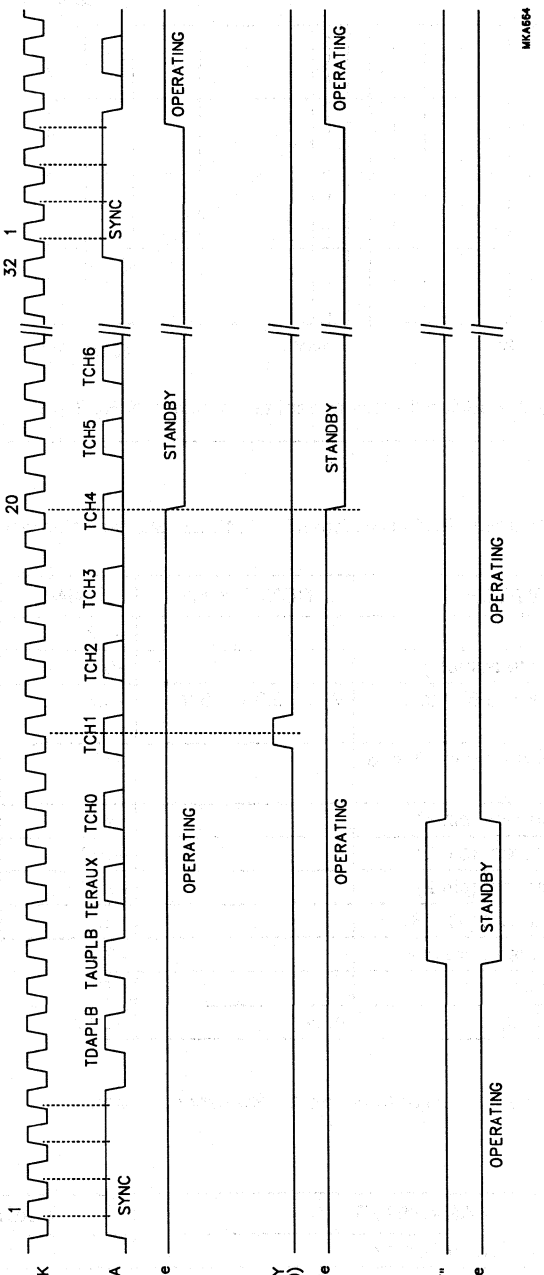


Fig.6 Timing of the standby mode (via WDATA, STANDBY or "SHORT").

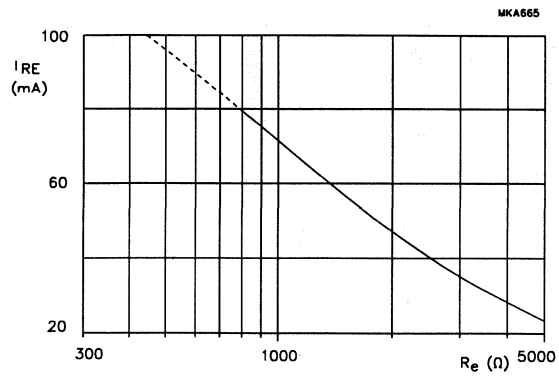


Fig.7 Additional erase current as a function of R_e (typ.).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); all voltages referenced to ground (pin 8); all currents are positive into the IC.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	+5.5	V
V_{DDO}	supply voltage (write outputs)		−0.3	+5.5	V
V_I	input voltage (pins 1 to 6, 9 to 17 and 19 to 24)	V_{DD} + 0.3 < 5.5 V	−0.3	V_{DD} + 0.3	V
I_n	maximum input current (pins 3, 4, 6 and 9 to 12)		−10	+10	mA
I_1	maximum input current (pin 1)		−40	+40	mA
I_5	maximum input current (pin 5)		−100	+40	mA
I_2	maximum input current (pin 2)		−250	+40	mA
I_{18}	maximum input current (pin 18)		−40	+400	mA
T_{amb}	operating ambient temperature		−30	+85	°C
T_{stg}	storage temperature		−55	+150	°C
V_{es}	electrostatic handling	note 1	−2000	+2000	V

Note

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	65 K/W

CHARACTERISTICS

$V_{DD} = V_{DDO} = 5$ V; $f_{clk} = 3.072$ MHz; $T_{amb} = 25$ °C; outputs QA to QJ resistively loaded; resistors connected in accordance with Fig.9; all voltages referenced to V_{SS} (pin 8); unless otherwise specified..

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		4.75	5.0	5.5	V
V_{DDO}	supply voltage (write outputs)		4.75	5.0	5.5	V
I_{DD}	supply current	note 1	–	7.5	11	mA
I_{DDO}	supply current (write outputs)	note 2	–	–	255	mA
		note 3	–	–	365	mA
		note 4	–	–	285	mA
I_{sb}	total standby current	note 5	–	2	3	mA
$P_{d(av)}$	average power dissipation	note 6	–	645	–	mW
Digital inputs (pins 10 to 12)						
V_{IH}	HIGH level input voltage		3.5	–	5.0	V
V_{IL}	LOW level input voltage		0	–	1.5	V
I_{IL}	input leakage current		–10	–	+10	μA
t_{su}	WDATA set-up time	see Fig.8	30	–	–	ns
t_h	WDATA hold time	see Fig.8	30	–	–	ns
Outputs (pins 9, 13 to 17 and 19 to 23)						
V_{ODATH}	HIGH level data output voltage	note 7	–	3.7	–	V
V_{OAUXH}	HIGH level auxiliary output voltage	note 8	–	3.7	–	V
$I_{O(min)}$	minimum output current		–	–	25	mA
$I_{ODAT(max)}$	maximum data output current		225	–	–	mA
$I_{OAUX(max)}$	maximum auxiliary output current	note 9	335	–	–	mA
$\Delta I_O/I_O$	output current deviation between channels	note 7	–	–	0.5	dB
I_{AUX}	relative auxiliary write current increase	note 10	1	1.2	1.4	dB
I_e	additional output current	note 3	–	–	80	mA
V_{ref}	reference voltage (pin 9)	$I_O < 3$ mA	2.4	2.5	2.6	V
Current amplifier (pins 1 to 4)						
V_{sense}	sense voltage regulation between pins 3 and 4		140	150	160	mV
V_1, V_2	maximum DC voltage level (pins 1 and 2)		–	–	500	mV

Notes

1. 1 kΩ erase adjust resistor connected between pins 5 and 6, no load at pin 9.
2. Momentary maximum value during write data; see Table 1; I_O = 225 mA.
3. Momentary maximum value during erase AUX; see Table 1 and Fig.5; resistor R_e connected between pins 5 and 6 (see Fig.7).
4. Momentary maximum value during write AUX; see Table 1; I_O = 255 mA.
5. Standby mode; see Table 1; $I_{sb} = I_{DD} + I_{DDO} + I_{clamp}$.
6. Auxiliary and data write mode; I_d = 170 mA; R_L = 3 Ω (between current outputs); R_{clamp} = 12 Ω.
7. Data channels (pins 13 to 17 and 19 to 22); maximum output load resistance is 5 Ω; I_O = 225 mA. Deviation defined as $20\log\{(I_{O(max)} - I_{O(min)})/I_{o(av)}\}$ for channels 0 to 7.
8. Auxiliary channel (pins 22 and 23); auxiliary erase mode; I_O = 335 mA.
9. Auxiliary channel (pins 22 and 23); auxiliary erase mode; maximum output load resistance is 4 Ω.
10. Defined as $20\log\{(I_d + I_x)/I_d\}$ when $R_x = 6.7 \times R_d$.

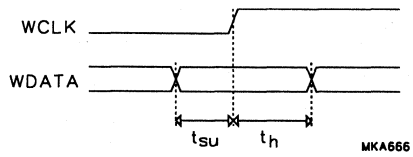


Fig.8 Timing relationship between the edges of WCLK and WDATA.

TEST AND APPLICATION INFORMATION

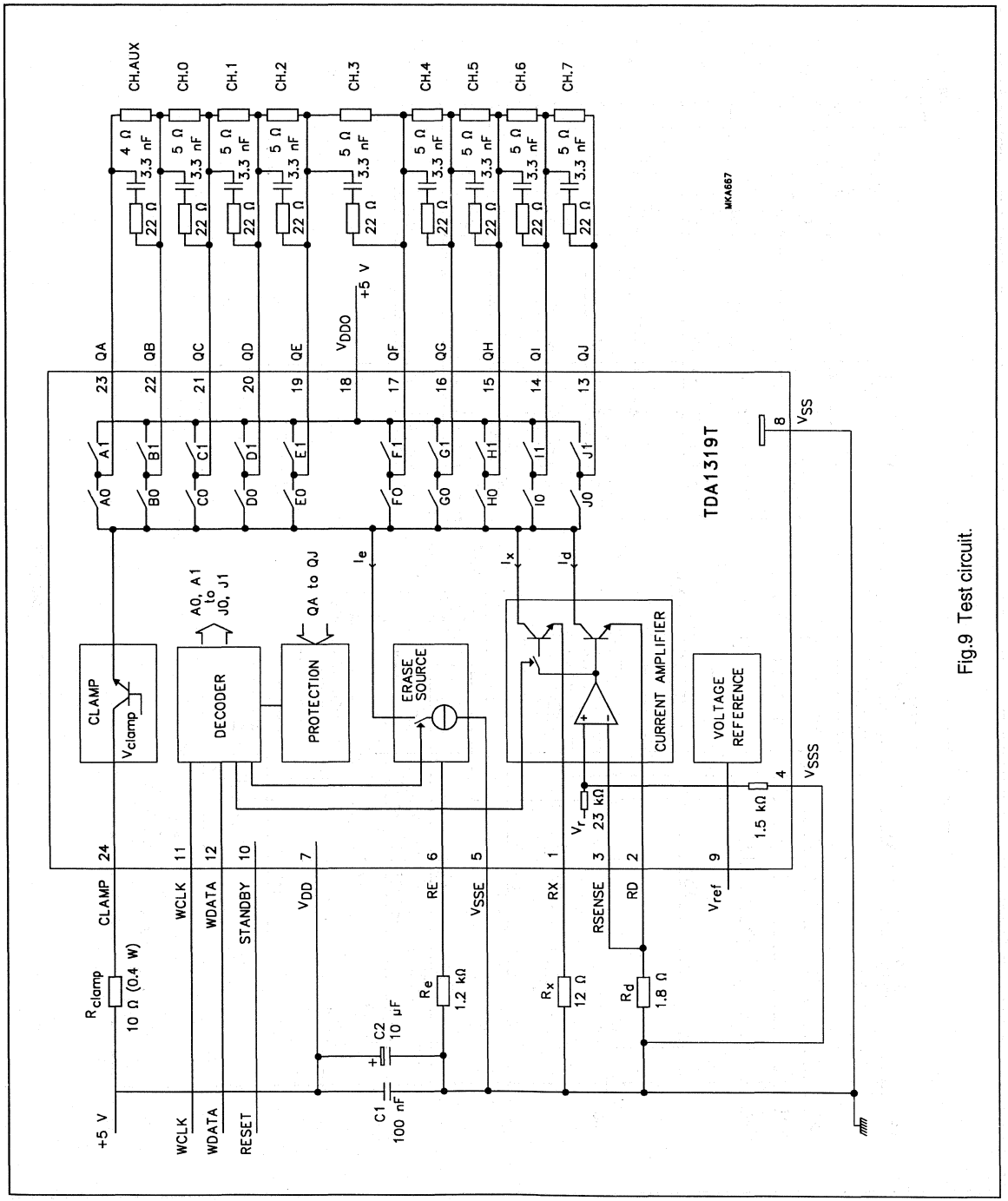


Fig.9 Test circuit.

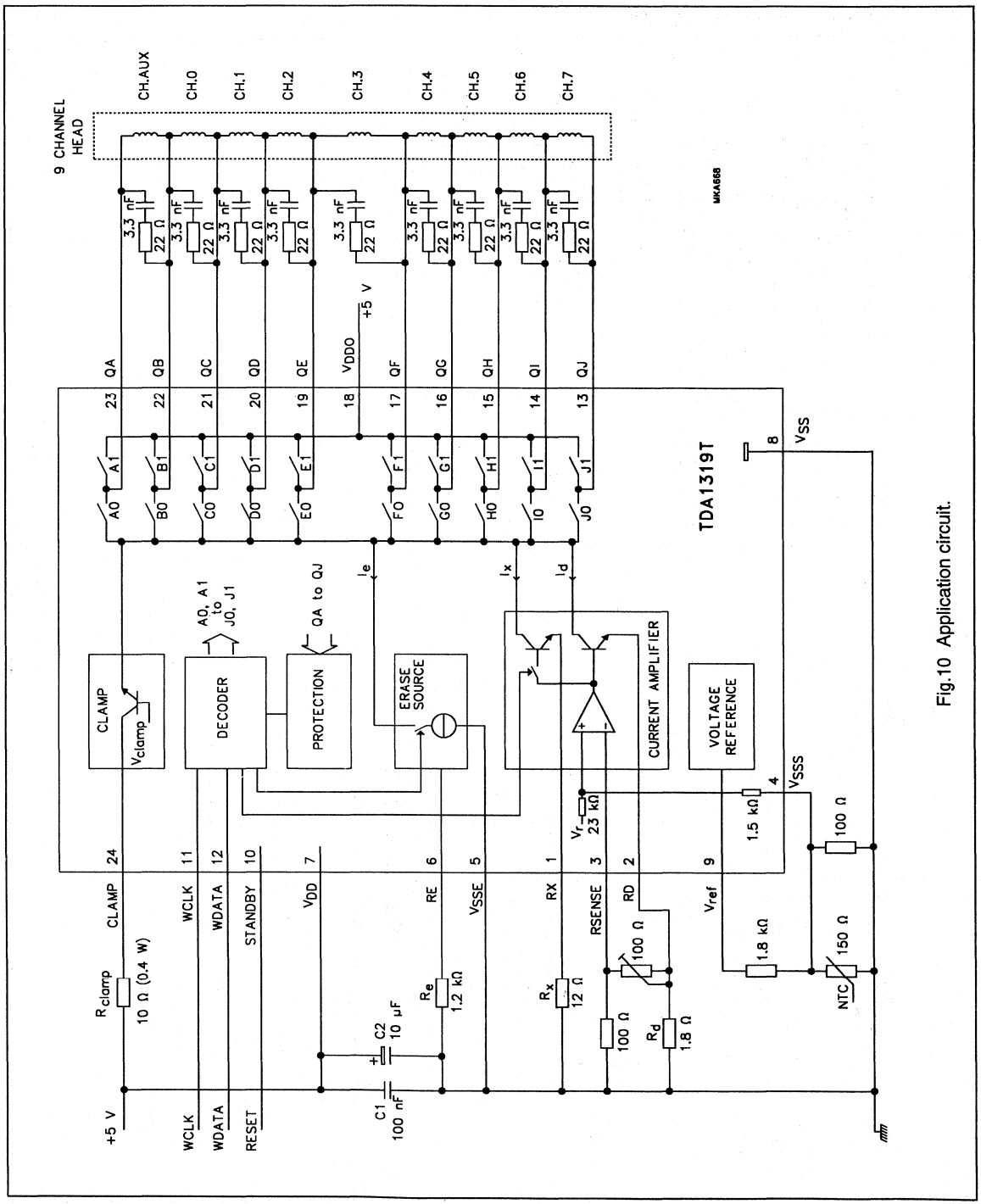


Fig.10 Application circuit.

DCC read amplifier (READ 3) TDA1380

FEATURES

- Single 3 V supply
- Low power consumption
- Differential inputs for low power head configuration
- Can be used with 1st, 2nd and 3rd generation digital signal processing ICs
- Automatic gain control for DCC preamplifiers
- Selectable input amplifiers for A or B side of cassette
- ACC playback via DCC preamplifiers
- Uncommitted amplifiers for equalization during ACC playback
- Low noise current sources for the sense currents of the DCC heads
- Generates reference sense current for temperature compensation of the write current, in recordable application with the TDA1381
- High feedback application possible (for adjustment minimization)
- Suitable for digital post-processor.

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

The TDA1380 amplifies, filters and multiplexes signals that are input from an 18-channel magnetoresistive thin film head (MRH) suitable for the DCC (Digital Compact Cassette) and ACC (Analog Compact Cassette) systems. The device also contains current sources to provide sense currents through the heads and amplifiers for magnetic feedback and biasing. Two uncommitted amplifiers are available for analog equalization.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1380	TQFP64[1]	plastic thin quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"*: (order number 9398 510 63011) are followed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS ON PINS[1]			MIN.	TYP.	MAX.	UNIT
		CS	SA	AB				
V_{DD}	supply voltage	–	–	–	2.7	3.0	5.5	V
V_{CCM}	supply voltage feedback amplifiers	–	–	–	2.7	3.0	5.5	V
$I_{DDDCC} + I_{CCM}$	supply current DCC mode	1	0	X	28	39	53	mA
$I_{DDACC} + I_{CCM}$	supply current ACC mode	1	1	X	26	35	47	mA
I_{DDRS}	supply current reference sense current mode	0	0	X	0.6	1.2	1.6	mA
I_{DDAB}	supply current sense AB mode	0	1	1	1.5	2.7	3.7	mA
$I_{DDstb} + I_{CCM}$	supply current standby mode	0	1	0	–	0.2	0.3	mA
$P_{(tot)DCC}$	total power dissipation DCC mode; note 2	1	0	X	–	120	–	mW
$P_{(tot)ACC}$	total power dissipation ACC mode; note 2	1	1	X	–	105	–	mW
T_{amb}	operating ambient temperature	–	–	–	−30	–	+85	°C

Notes

1. In the conditions column 0 = LOW; 1 = HIGH; X = don't care.
2. $V_{DD} = V_{CCM} = 3$ V; $I_{DSEN} = 0$; $I_{FB} = 0$.

BLOCK DIAGRAM

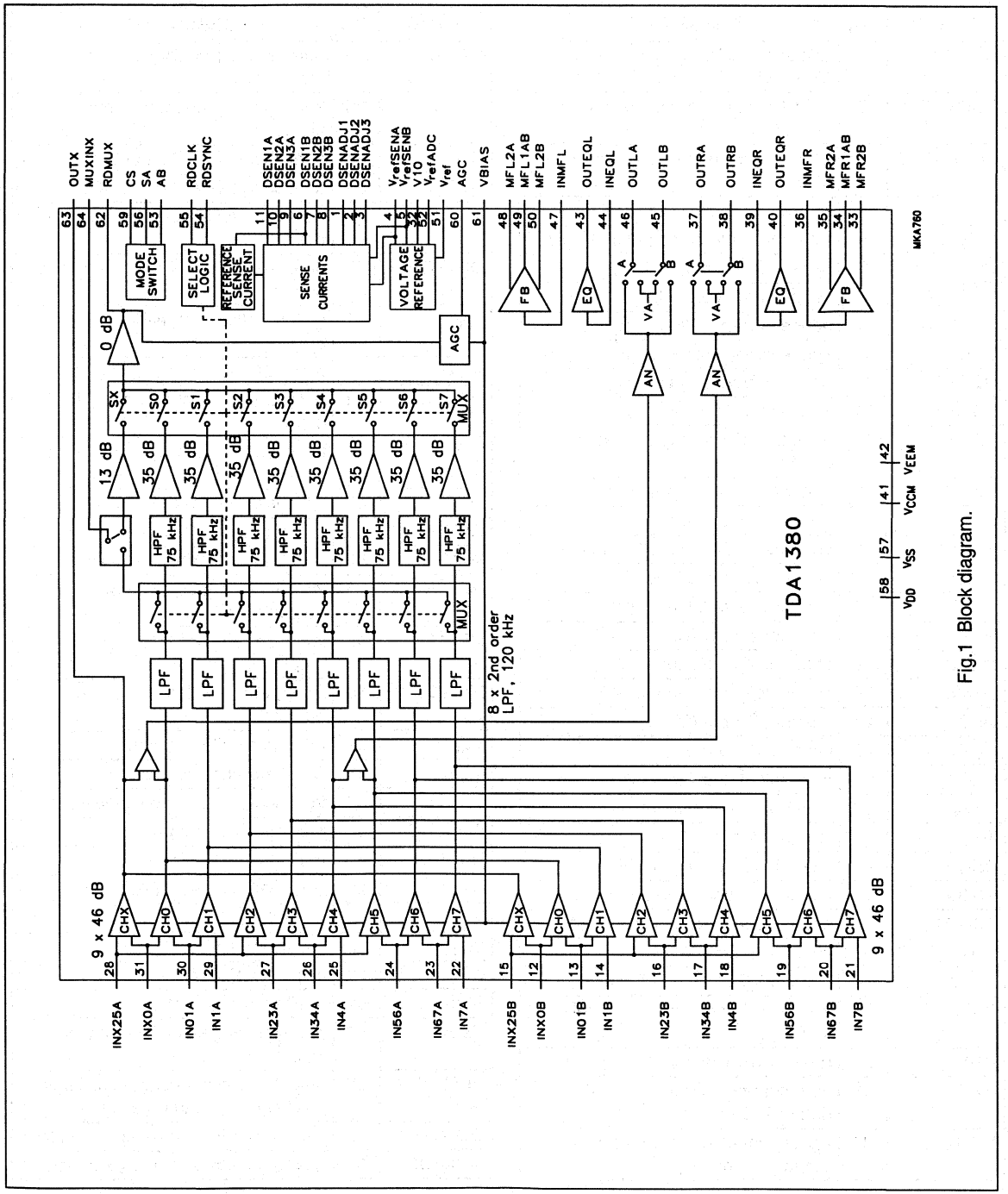


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DSENADJ1	1	adjustment pin for sense current 1 (A and B)
DSENADJ2	2	adjustment pin for sense current 2 (A and B)
DSENADJ3	3	adjustment pin for sense current 3 (A and B)
$V_{refSENA}$	4	reference voltage output sense (A)
$V_{refSENB}$	5	reference voltage output sense (B)
DSEN1B	6	sense current output 1 (B)
DSEN2B	7	sense current output 2 (B)
DSEN3B	8	sense current output 3 (B)
DSEN3A	9	sense current output 3 (A)
DSEN2A	10	sense current output 2 (A)
DSEN1A	11	sense current output 1 (A)
INX0B	12	auxiliary channel input/channel 0 input (B)
IN01B	13	channel 0 and 1 input (B)
IN1B	14	channel 1 input (B)
INX25B	15	channels AUX, 2 and 5 input (B)
IN23B	16	channels 2 and 3 input (B)
IN34B	17	channels 3 and 4 input (B)
IN4B	18	channel 4 input (B)
IN56B	19	channels 5 and 6 input (B)
IN67B	20	channels 6 and 7 input (B)
IN7B	21	channel 7 input (B)
IN7A	22	channel 7 input (A)
IN67A	23	channels 6 and 7 input (A)
IN56A	24	channels 5 and 6 input (A)
IN4A	25	channel 4 input (A)
IN34A	26	channels 3 and 4 input (A)
IN23A	27	channels 2 and 3 input (A)
INX25A	28	channels AUX, 2 and 5 input (A)
IN1A	29	channel 1 input (A)
IN01A	30	channels 0 and 1 input (A)
INX0A	31	auxiliary channel input/channel 0 input (A)
V10	32	reference voltage for DCC inputs
MFR2B	33	right channel feedback amplifier output 2 (B)
MFR1AB	34	right channel feedback amplifier output 1 (A and B)

SYMBOL	PIN	DESCRIPTION
MFR2A	35	right channel feedback amplifier output 2 (A)
INMFR	36	right channel feedback amplifier input
OUTRA	37	right channel ACC output (A)
OUTRB	38	right channel ACC output (B)
INEQR	39	right channel equalization amplifier input
OUTEQR	40	right channel equalization amplifier output
V_{CCM}	41	supply voltage for feedback amplifiers
V_{EEM}	42	ground for feedback amplifiers
OUTEQL	43	left channel equalization amplifier output
INEQL	44	left channel equalization amplifier input
OUTLB	45	left channel ACC output (B)
OUTLA	46	left channel ACC output (A)
INMFL	47	left channel feedback amplifier input
MFL2A	48	left channel feedback amplifier output 2 (A)
MFL1AB	49	left channel feedback amplifier output 1 (A and B)
MFL2B	50	left channel feedback amplifier output 2 (B)
V_{ref}	51	reference voltage output
V_{refADC}	52	ADC reference voltage output
AB	53	tape sector A or B selection input
RDSYNC	54	read sync pulse input
RDCLK	55	read clock pulse input
SA	56	select ACC mode input
V_{SS}	57	ground
V_{DD}	58	supply voltage
CS	59	chip select input
AGC	60	AGC time constant
VBIAS	61	preamplifier gain control voltage input
RDMUX	62	output of sampled and multiplexed auxiliary and main data signals
OUTX	63	auxiliary channel preamplifier output
MUXINX	64	auxiliary channel multiplexer input

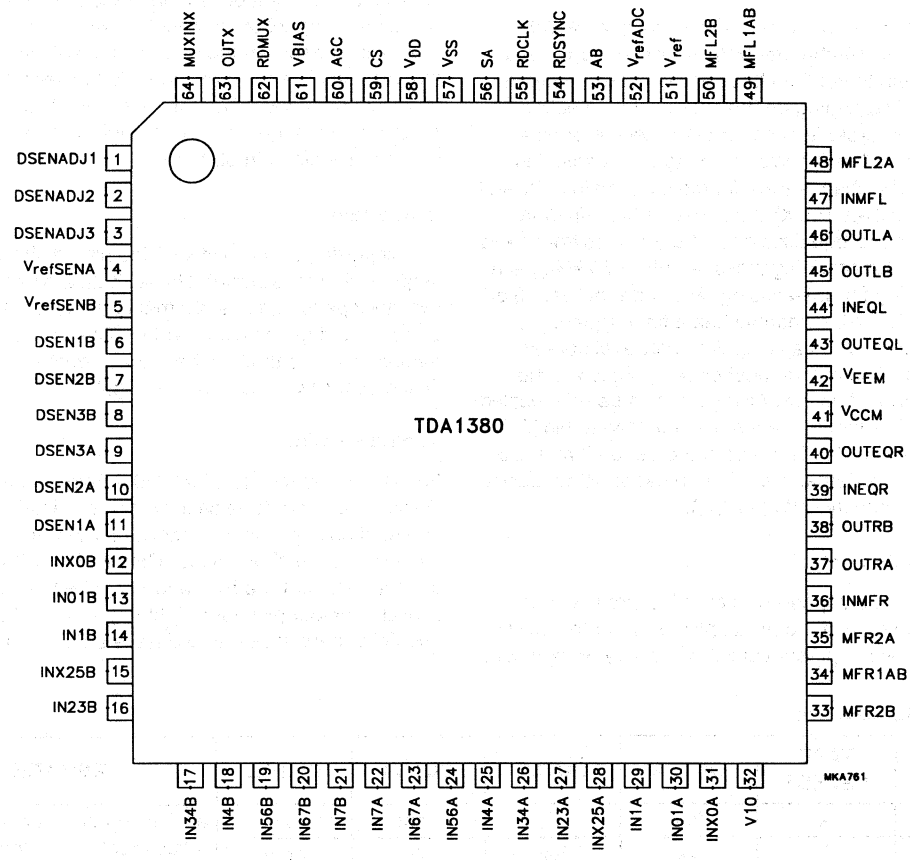


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

DCC data amplifiers and filters

The TDA1380 has 18 low-noise preamplifiers, which are connected to an 18-channel MRH. For each tape sector the MRH is partitioned into three strings of three heads (see Fig.11). Depending on the tape sector selection signal AB, nine preamplifiers for the A-sector, or nine preamplifiers for the B-sector of the tape are selected. Eight of the nine channels are for the DCC main data, and one for the auxiliary (AUX) data. The eight main data channels have pre-equalization for frequencies from 1 kHz up to 50 kHz (1st order highpass, –3 dB at 75 kHz), and lowpass filtering for anti-aliasing (2nd order active, –3 dB at 120 kHz). The AUX channel has a flat frequency response. The AUX data is continuously available at output OUTX. This output must be AC-coupled to the multiplexer input MUXINX. All inputs must be AC-coupled to the MRH. The inputs are internally biased at pin V10. The voltage at pin V10 is temperature dependent and is not intended for external use. Pin V10 has to be decoupled to the positive supply voltage (V_{DD}).

Automatic gain control

The DCC part is equipped with an AGC circuit which decreases the gain of the preamplifiers when the level at RDMUX exceeds a preset value. In this way an optimum voltage swing at the RDMUX output is obtained (for the ADC input of SAA2051, SAA2032, SAA2023 or SAA3323). The response time of the AGC can be set by an external capacitor connected to pin 60. There is a fixed relationship between the source and sink current at this pin, resulting in a fixed relationship between the decay time and the recover time of the preamplifier gain. The AGC is active only in the DCC mode and can be switched off by connecting pin 60 to V_{SS}.

Multiplexer

A multiplexing circuit switches the nine digital channels sequentially to the output. The AUX data is sampled during two clock periods, the eight main data channels are sampled during one clock period. The effective sample frequency is one tenth of the clock frequency at RDCLK. A timing overview is illustrated in Fig.4.

Analog amplifiers

For ACC playback the TDA1380 employs four DCC preamplifiers (per tape sector) for amplification of the left and right analog signals. Amplifiers CHX and CH0 are used for the left channel and CH4 and CH5 for the right channel. The buffered left and right channel outputs are available at four pins (see Table 1). Pins that carry no left and right channel signals will have a DC level V_A.

Table 1 ACC playback.

AB	TAPE SELECT	OUTLA	OUTLB	OUTRA	OUTRB	REMARKS
1	A	left	V_A	right	V_A	allows separate amplitude adjustment for sectors A and B
0	B	V_A	left	V_A	right	
1	A	left	note 1	right	note 1	allows one amplitude setting only for sectors A and B (DSP operation; high feedback operation)
0	B	left	note 1	right	note 1	

Note

1. At least one of OUTLB and OUTRB are externally connected to V_{DD}.

Feedback amplifiers

Two feedback amplifiers are available for driving a conductor in the MRH, thus providing magnetic feedback to improve the linearity of the analog audio response. In both the ACC and DCC mode, the feedback amplifiers are used for DC biasing of the MRH. The circuit principle of the feedback amplifiers is illustrated in Fig.9.

Equalization amplifiers

Two uncommitted operational amplifiers are available for pre-equalization of the left and right ACC outputs. These amplifiers are only operational during ACC playback. The non-inverting input is internally connected to a DC voltage which is approximately equal to V_{ref}. If the amplifiers are not used in the application, it is advised to connect the outputs to the inputs.

Current and voltage sources

Separate, adjustable low-noise current sources are available to provide the sense currents to the MRHs. The active current outputs are controlled by the mode switch (see Table 2). In the reference sense current mode, only one source is active (DSEN1B, pin 6). This current can be used for temperature measurement of the DCC head, thereby enabling control of the write current (TDA1381) when recording. The principle of the sense current sources is illustrated in Fig.8. The typical value of the output current is determined by resistors connected between the adjust pins and V_{SS}; where $I_{DSEN} = 0.33/R_{ADJUST}$.

The DC output voltages V_{ADC}, V_{ref}, V10, $V_{refSENA}$ and $V_{refSENB}$ are derived from an internal bandgap reference voltage source. The voltage V_{refADC} (referenced to V_{SS}) can be used as a reference voltage for analog-to-digital conversion of the RDMUX output.

Table 2 Sense current sources.

MODE	DIGITAL INPUTS(1)			AVAILABLE SENSE CURRENT	ACTIVE DC OUTPUTS
	CS	SA	AB		
Standby	0	1	0	–	–
Reference sense current	0	0	X	DSEN1B	–
Sense AB	0	1	1	DSEN1A; DSEN2A; DSEN3A DSEN1B; DSEN2B; DSEN3B	$V_{refSENA}$ $V_{refSENB}$
ACC playback A	1	1	1	DSEN1A; DSEN2A; DSEN3A	$V_{refSENA}$
ACC playback B	1	1	0	DSEN1B; DSEN2B; DSEN3B	$V_{refSENB}$
DCC playback A	1	0	1	DSEN1A; DSEN2A; DSEN3A	$V_{refSENA}$
DCC playback B	1	0	0	DSEN1B; DSEN2B; DSEN3B	$V_{refSENB}$

Note

1. Where X = don't care; 0 = LOW; 1 = HIGH.

Modes of operation

The amplifiers and sense current sources for the ACC and DCC parts can be switched ON/OFF separately by the mode switch signals CS, SA and AB. Also, a connection between OUTLB or OUTRB or both to V_{DD} is recognized as a single output ACC mode where the left and right outputs are present at OUTLA and OUTRA only.

Table 3 Modes of operation.

MODE	DIGITAL INPUT(1)			ACTIVE PARTS (see Fig.1)	ACTIVE DC REFERENCE OUTPUTS
	CS	SA	AB		
Standby	0	1	0		
Reference sense current	0	0	X	reference sense current source	V_{ref}
Sense AB	0	1	1	sense current sources	V_{ref}
ACC playback A/B	1	1	1 or 0	sense currents, data preamplifiers, AN, EQ and FB	V_{ref}; V10
ACC playback A/B via OUTLA and OUTRA only (note 2)	1	1	1 or 0	sense currents, data preamplifiers, AN, EQ and FB	V_{ref}; V10
DCC playback A/B	1	0	1 or 0	sense currents, data amplifiers and filters, multiplexer, AGC and FB	V_{ref}; V10; V_{refADC}
Test mode (note 3)	1	0	1 or 0	sense currents, data amplifiers and filters, multiplexer, AGC and FB	V_{ref}; V10; V_{refADC}

Notes

1. Where X = don't care; 0 = LOW; 1 = HIGH.
2. At least one of OUTLB or OUTRB are externally connected to V_{DD}.
3. INEQL or INEQR connected to V_{DD} (no user function).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages referenced to V_{SS} and V_{EEM}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	$V_{SS} = V_{EEM} = 0$ V	−0.3	5.5	V
V_{CCM}	supply voltage feedback amplifiers	$V_{SS} = V_{EEM} = 0$ V	−0.3	5.5	V
V_{SS}–V_{EEM}	difference in ground potential between pins 57 and 42		0	0	V
V_I	voltage input on any pin	$V_{DD} + 0.3 < 5.5$ V	−0.3	$V_{DD} + 0.3$	V
$I_{I(max)}$	maximum supply current (pins 41, 42, 57 and 58)		–	±120	mA
I_{FBmax}	maximum current for feedback amplifiers (pins 33 to 35 and 48 to 50)		–	±80	mA
$I_{sense(max)}$	maximum current on sense current source (pins 1 to 3 and 6 to 11)		–	±30	mA
$I_{n(max)}$	maximum current on any other pin		–	±10	mA
P_{tot}	total power dissipation		–	650	mW
T_{amb}	operating ambient temperature		−30	+85	°C
T_{stg}	storage temperature		−65	+50	°C
V_{es}	electrostatic handling		−3000	+3000	V

ELECTROSTATIC HANDLING

Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	60	K/W

CHARACTERISTICS

$V_{DD} = V_{CCM} = 3$ V; $V_{SS} = V_{EEM} = 0$ V; $T_{amb} = 25$ °C; $f_{clk} = 3.072$ MHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.7	3.0	5.5	V
V_{CCM}	supply voltage feedback amplifiers		2.7	3.0	5.5	V
I_{DDDCC}	supply current DCC mode	CS = 1; SA = 0	18	27	37	mA
I_{DDACC}	supply current ACC mode	CS = 1; SA = 1	16	23	30	mA
I_{DDRS}	supply current reference sense current mode	CS = 0; SA = 0	0.6	1.2	1.6	mA
I_{DDAB}	supply current sense AB mode	CS = 0; SA = 1; AB = 1	1.5	2.7	3.7	mA
I_{CCM}	supply current feedback amplifiers	CS = 1	7.5	12	17.5	mA
$I_{DDstb} + I_{CCM}$	supply current standby mode	CS = 0; AB = 0; SA = 1	–	0.2	0.3	mA
V_{refADC}	reference voltage for ADC	CS = 1; SA = 0; $R_L = 1$ kΩ	1.95	2.05	2.15	V
$V_{refSENA}$	sense A reference voltage	CS = 1; AB = 1; $I_O < 5$ µA; $I_{DSEN} = 10$ mA	1.0	1.1	1.2	V
$V_{refSENB}$	sense B reference voltage	CS = 1; AB = 0; $I_O < 5$ µA; $I_{DSEN} = 10$ mA	1.0	1.1	1.2	V
V_{ref}	reference voltage output	$I_O < 5$ µA; all modes except standby mode	1.18	1.25	1.32	V
V10	reference voltage for DCC inputs	CS = 1; $I_O < 5$ µA	0.9	1.0	1.1	V
DCC part						
DATA AMPLIFIERS, CHANNELS 0 TO 7; NOTE 1						
G_{50}	gain at 50 kHz		72	75	78	dB
ΔG_{10}	relative gain at 10 kHz	note 2	–14	–12	–10	dB
G_{100}	gain at 100 kHz		71	76	79	dB
ΔG_{300}	relative gain at 300 kHz	note 2	–22	–12	–3	dB
$V_{n(ref)}$	input referred noise voltage	$f_i = 50$ kHz; $R_{source} = 70$ Ω	–	2.0	–	nV/√Hz
$\Delta V_{n(ref)}$	3 × standard deviation of input referred noise voltage	$f_i = 50$ kHz; $R_{source} = 70$ Ω	–	0.5	–	nV/√Hz
THD	total harmonic distortion	$f_i = 10$ kHz; $V_{62} = 0.35$ V (RMS)	–	–40	–30	dB
$Z_{i(d)}$	input impedance differential mode		–	7	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$Z_{i(c)}$	input impedance to V_{SS} common mode		–	7.5	–	kΩ
α_{CS}	channel separation	f_i = 10 kHz	30	40	–	dB
SVRR	supply voltage ripple rejection	f_i = 50 kHz; note 3	–	–20	–	dB
Auxiliary amplifier, channel X; note 1						
G_{63}	gain at OUTX (pin 63)	100 Hz to 100 kHz	43	46	49	dB
G_{62}	gain at RDMUX (pin 62)	100 Hz to 100 kHz; note 4	56	59	62	dB
$V_{n(ref)}$	input referred noise voltage	f_i = 50 kHz; R_{source} = 70 Ω	–	2.0	–	nV/√Hz
$\Delta V_{n(ref)}$	3 x standard deviation input referred noise voltage	f_i = 50 kHz; R_{source} = 70 Ω	–	0.5	–	nV/√Hz
$V_{o(rms)}$	maximum output voltage (pin 63) (RMS value)	f_i = 10 kHz	0.35	–	–	V
THD	total harmonic distortion	f_i = 10 kHz; V_{63} = 0.35 V (RMS)	–	–40	–30	dB
SVRR	supply voltage ripple rejection	f_i = 1 kHz; note 3	–	–3	–	dB
$R_{L(DC)}$	DC load at pin 63	load connected to V_{SS}	10	–	–	kΩ
$C_{L(AC)}$	AC load at pin 63	load connected to V_{SS}	–	–	100	pF
Output buffer, RDMUX (pin 62)						
$V_{62(rms)}$	maximum output voltage (RMS value)	R_L = 2 kΩ	0.35	–	–	V
V_{DC}	DC voltage level at pin 62		0.95	1.15	1.35	V
$\Delta V_{DC(os)}$	DC offset voltage between sampled outputs	note 5	–	–	200	mV
$R_{L(DC)}$	DC load at pin 62	load connected to V_{SS}	1.5	–	–	kΩ
$C_{L(AC)}$	AC load at pin 62	load connected to V_{SS}	–	–	100	pF
t_{set}	settling time of sampled outputs	C_L = 50 pF; within 10 mV	–	100	150	ns
$V_{62(M)}$	AGC detector level (peak value)	note 5	320	465	570	mV
AGC_{CR}	AGC control range		9	11	13	dB
I_{source}	AGC source current (pin 60)		16	21	26	µA
I_{sink}	AGC sink current (pin 60)		0.3	0.5	0.8	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Select logic inputs (RDCLK and RDSYNC) and mode switch inputs (CS, SA and AB)						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
I_{IL}	input leakage current		–2	0	+2	µA
C_i	input capacitance	note 7	–	–	10	pF
t_{su}	set-up time for RDSYNC	see Fig.3	35	–	–	ns
t_h	hold time for RDSYNC	see Fig.3	35	–	–	ns
t_r	rise time for RDCLK	see Fig.3	–	–	50	ns
V_{det}	ACC single output mode detection level (pins 38 and 45)		$V_{DD} - 0.45$	$V_{DD} - 0.35$	–	V
Sense current sources						
$I_{DSENmin}$	minimum output current	note 8	–	–	1	mA
$I_{DSENmax}$	maximum output current	note 8	20	–	–	mA
I_{DSEN1B}	reference sense current (pin 6)	note 9	2.7	3.0	3.3	mA
I_{ON}	output current noise	note 10	–	20	–	pA/√Hz
Z_{DSEN}	output impedance	note 10	20	–	–	kΩ
V_{DSEN}	DC voltage level of current outputs (pins 6 to 11)		1.0	–	–	V
ACC part						
ACC AMPLIFIERS						
G_{ACC}	ACC gain	20 Hz to 20 kHz	44	46	48	dB
$V_{n(ref)}$	input referred noise voltage	f_i = 10 kHz; R_{source} = 70 Ω	–	2.0	–	nV/√Hz
$\Delta V_{n(ref)}$	3 x standard deviation of input referred noise voltage	f = 10 kHz; R_{source} = 70 Ω	–	0.5	–	nV/√Hz
$V_{o(rms)}$	maximum output voltage (RMS value)	f_i = 1 kHz	0.35	–	–	V
V_A	DC output voltage	see Table 1	0.6	0.9	1.2	V
THD	total harmonic distortion	f_i = 1 kHz; V_o = 0.35 V (RMS)	–	–40	–30	dB
SVRR	supply voltage ripple rejection	f_i = 1 kHz	–	tbf	–	dB
α_{CS}	channel separation	f_i = 1 kHz	40	–	–	dB
$R_{L(DC)}$	DC load (pins 37, 38 45 and 46)	load connected to V_{SS}	10	–	–	kΩ
$C_{L(AC)}$	AC load (pins 37, 38 45 and 46)	load connected to V_{SS}	–	–	300	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Equalization operational amplifiers (EQ); note 11						
$V_{EQ(rms)}$	maximum output voltage (RMS value)	f_i = 1 kHz	0.35	–	–	V
B_{EQ}	bandwidth	at –3 dB	50	–	–	kHz
THD	total harmonic distortion	f_i = 1 kHz; V_O = 0.35 V (RMS)	–	–70	–55	dB
α_{CS}	channel separation	f_i = 1 kHz	60	–	–	dB
$R_{L(DC)}$	DC load at OUTEQL	load connected to V_{SS}	10	–	–	kΩ
$C_{L(AC)}$	AC load at OUTEQL	load connected to V_{SS}	–	–	300	pF
Feedback amplifiers (FB); note 12						
I_{FBmax}	maximum output current (RMS value)	f_i = 1 kHz	25	–	–	mA
THD	total harmonic distortion	f_i = 1 kHz; I_{FB} = 25 mA (RMS)	–	–60	–50	dB
B_{FB}	bandwidth	at –3 dB	50	–	–	kHz
V_{IFB}	DC voltage level input (pins 36 and 47)		–	1.15	–	V

Notes

1. AGC off (maximum gain; pin 60 connected to V_{SS}).
2. Gain relative to gain at f_i = 50 kHz (see Fig.5).
3. Heads connected according to the circuit of Fig.11 (see also Fig.6 for typical supply rejection).
4. OUTX AC-coupled to MUXINX via 100 nF capacitor.
5. The difference between minimum and maximum DC voltage level at the outputs of the data channels. To be measured at RDMUX.
6. Measured with continuous sine wave of 10 kHz at RDMUX, multiplexer in a fixed position. A 1 V (p-p) sine wave corresponds to a multiplexed DCC signal of 1.25 V (p-p).
7. Periodically sampled, not tested.
8. Pins 6 to 11. The output current is inversely proportional to the value of the resistor connected between the adjust pin DSENADJ1, DSENADJ2, DSENADJ3 and V_{SS}. A resistor of 33 Ω will give 10 mA (typ.) sense current. Other currents can be calculated: 0.33 V/R_{ADJUST}.
9. CS = 0, SA = 0; Resistor of 33 Ω connected between DSENADJ1 and V_{SS}. Typical reference sense current is 100 mV/R_{ADJUST}.
10. From 10 to 100 kHz, IDSEN = 10 mA, a 10 µF capacitor connected between $V_{refSENA}$ and V_{SS}, a 10 µF capacitor connected between $V_{refSENB}$ and V_{SS}.
11. Closed loop configuration, unity gain, in accordance with Fig.10.
12. Closed loop, unity gain, R_L = 25 Ω, in accordance with Fig.9.

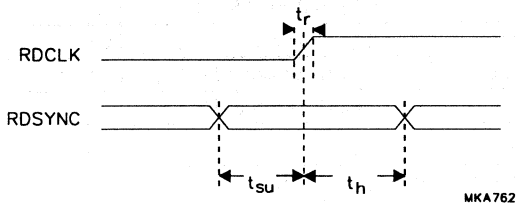


Fig.3 Timing relationship between edges of RDCLK and RDSYNC.

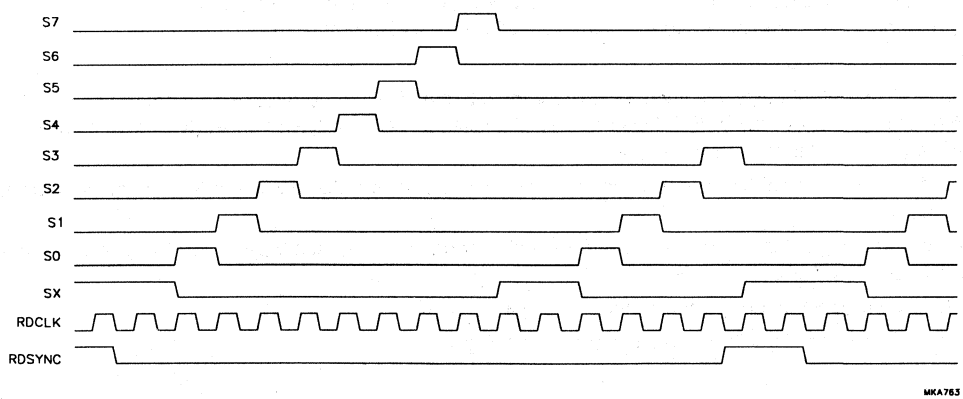


Fig.4 Multiplexer timing diagram.

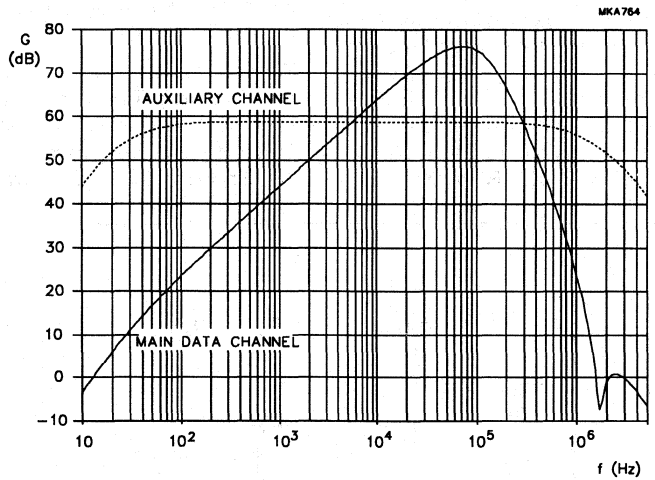


Fig.5 Typical gain of the auxiliary and main data channel (AGC off).

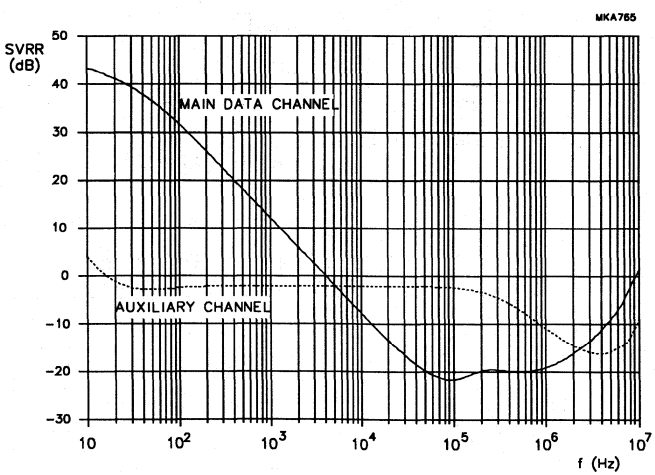


Fig.6 Typical supply rejection of the auxiliary and main data channel (AGC off).

TEST AND APPLICATION INFORMATION

The TDA1380 can be set to the TEST mode by connecting INEQL or INEQR (or both) to V_{DD}. In this mode the switch at pin MUXINX enables monitoring of the input stage and lowpass filter of each data amplifier and also allows input to the highpass filters and following stages. The test multiplexer operates in phase with the output multiplexer. Measurement of the gain of the data channels can be performed in two steps: step 1, gain from the inputs to MUXINX; step 2, gain from MUXINX to RDMUX.

Figure 7 illustrates how to use pin MUXINX in the TEST mode, $C_L < 20$ pF, $R_L > 100$ kΩ, $C_i > 47$ nF and $R_{bias} = 1$ kΩ. The DC voltage, when driving MUXINX, should be 0.7 V higher than the measured DC level of the preamplifier output in order to shut off the emitter follower.

The impedance of the sense current source outputs can be measured from the difference in sense current when applying different voltages to the sense current output. This voltage can vary from 1 V to V_{DD}. Figure 8 illustrates the principle of the sense current sources.

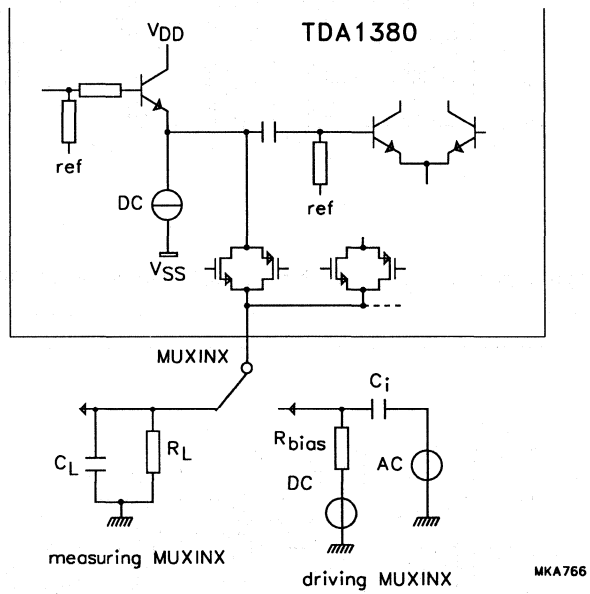


Fig.7 Use of the MUXINX pin in the TEST mode.

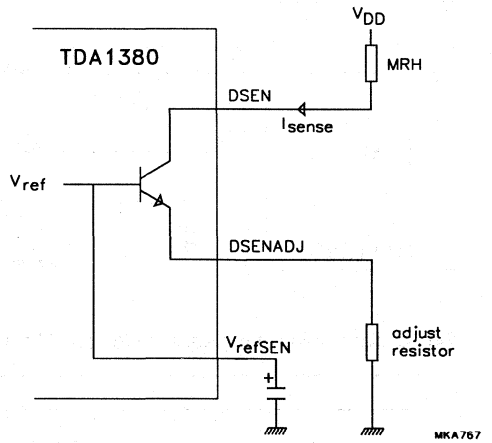


Fig.8 Principle of the sense current sources.

The feedback amplifiers consist of three operational amplifiers providing one input and a differential output with respect to an internal 1.15 V reference. The active output A or B is selected by the tape sector selection signal AB.

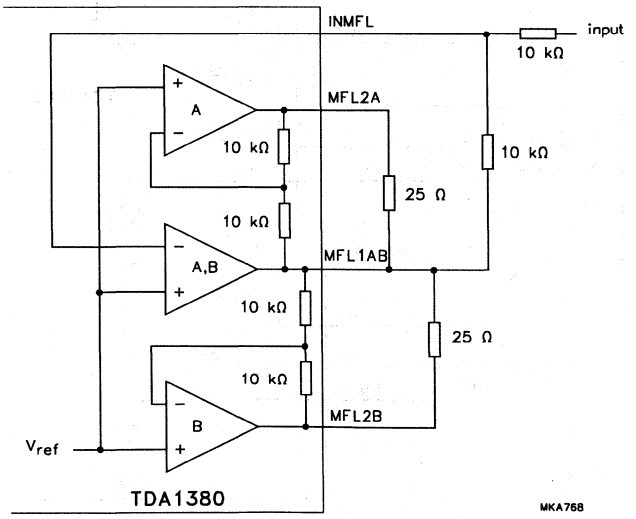


Fig.9 Principle of the feedback amplifiers and TEST circuit.

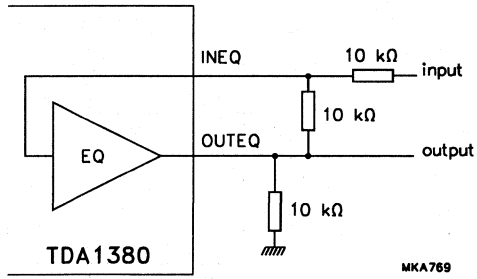


Fig.10 Test circuit of the equalization amplifiers.

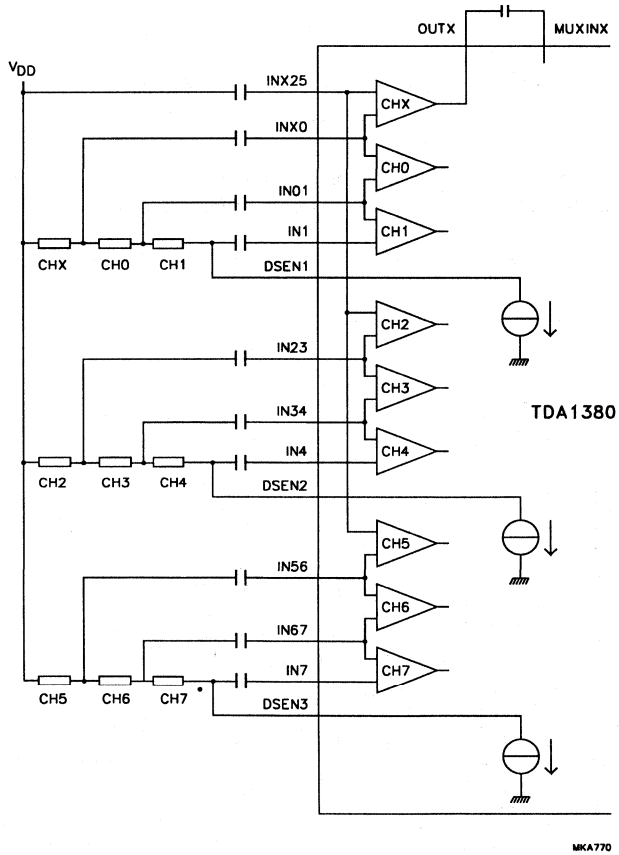
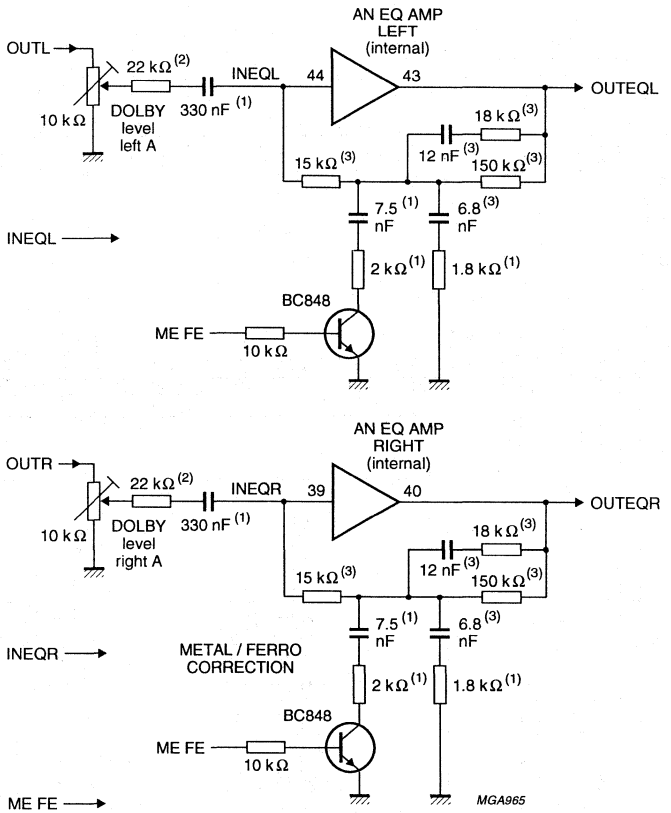


Fig.11 Connection of the TDA1380 to the MRH (partial).



Frequency compensation values are totally dependent on head frequency response characteristics.

(1) Less than 10%.

(2) Less than 5%.

(3) Less than 2%.

Fig.12 Analog equalizer.

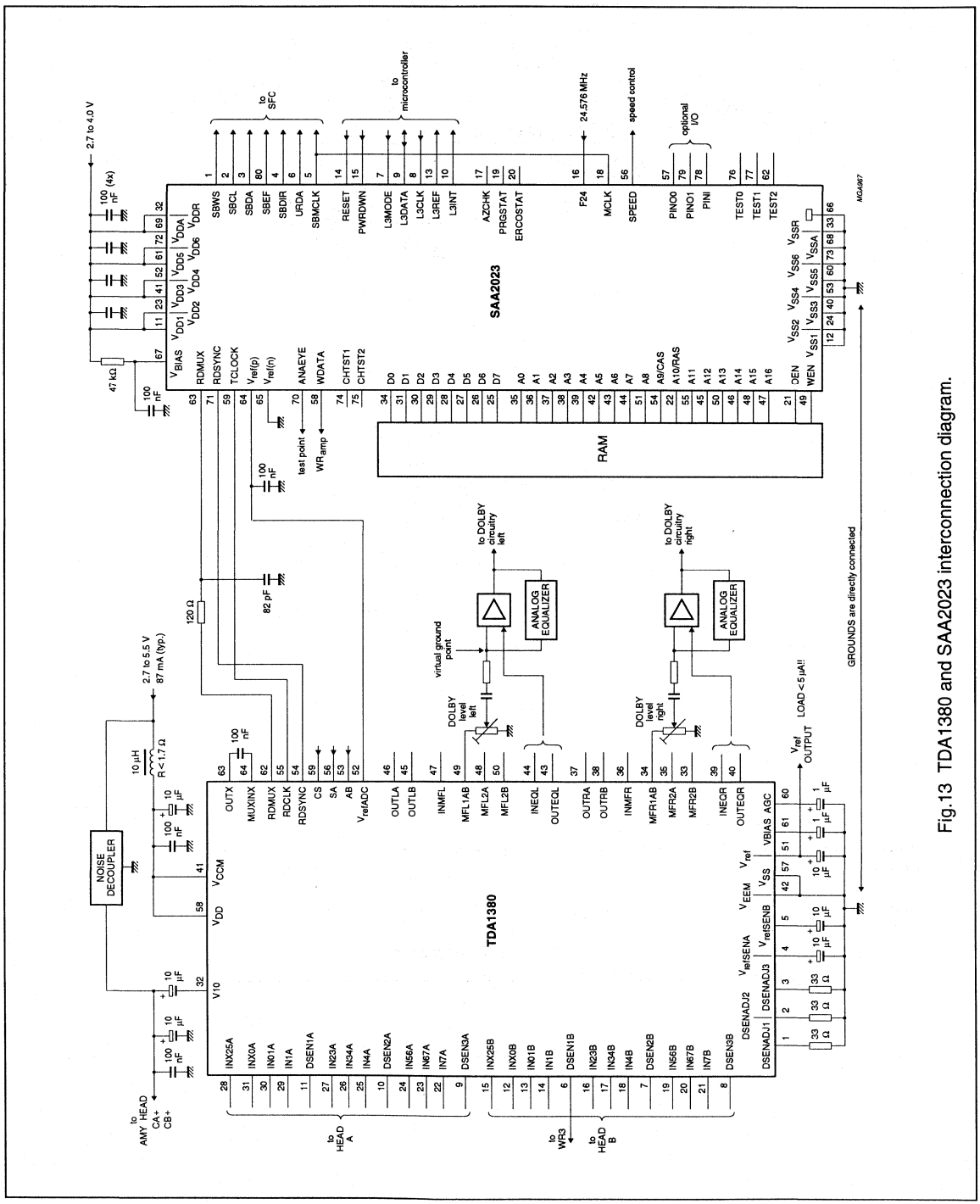
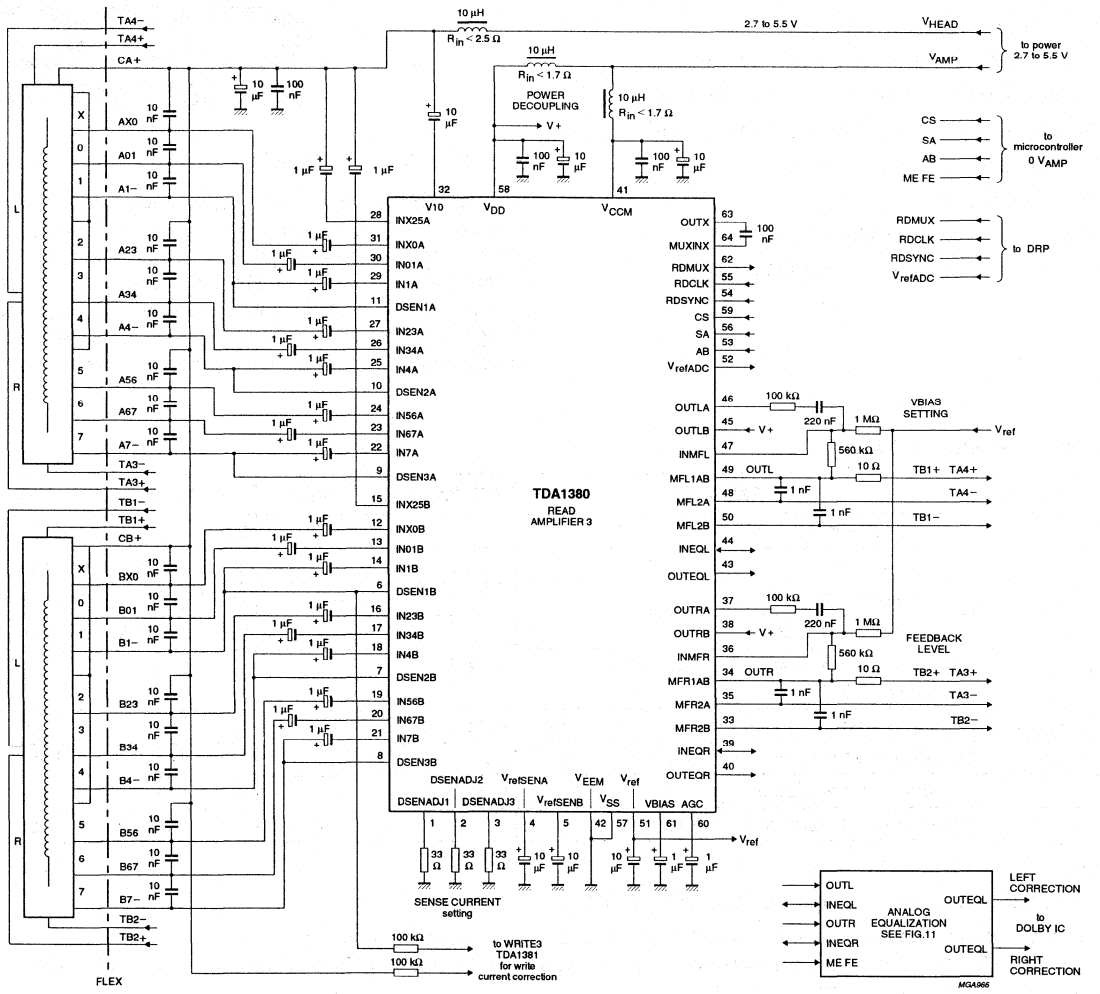


Fig.13 TDA1380 and SAA2023 interconnection diagram.



Power V_{HEAD} and power V_{AMP} have to be very clean in the frequency range 0 to 1 kHz.
With respect to power consumption:

(1) V_{HEAD}; $3 \times I_{sense} \times V_{HEAD}$.

(2) V_{AMP}; ≤ 42 mA at 3 V.

(3) START-UP I_{peak}; 150 mA at V_{HEAD}.

Fig.14 Application diagram.

DCC write amplifier (WRITE3) TDA1381

FEATURES

- Single 3 V power supply
- Low standby current consumption
- 20 bidirectional current outputs (2 × nine heads)
- Single point main data and auxiliary current setting
- Reduction of power consumption between write pulses
- Soft switching of output currents
- Serial data input
- Timing is compatible with TDA1319T
- Uncommitted operational amplifier available.

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

The TDA1381 has been designed to drive an 18-channel inductive recording head which is suitable for the DCC (Digital Compact Cassette) system. The bidirectional current outputs are controlled by a two-wire serial bus. The amplitude of the write current pulses can be set by either voltage or current control. The circuit can be switched to standby mode to minimize supply current consumption.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.7	3.0	4.0	V
I_{DD}	supply current	note 1	–	9	12	mA
$I_{DD(av)}$	average supply current	note 2	–	26.5	–	mA
I_{stb}	total standby current		–	0.1	0.3	mA
$I_{WDAT(max)}$	maximum write current for main data channels 0 to 7	note 3	100	–	–	mA
$I_{WAUX(max)}$	maximum write current for auxiliary channel	note 3	115	–	–	mA
$I_{EAUX(max)}$	maximum erase current for auxiliary channel	note 3	153	–	–	mA
$P_{d(av)}$	average power dissipation	note 2	–	80	–	mW
T_{amb}	operating ambient temperature		−30	–	+85	°C

Notes

1. No head connected; all outputs unloaded; V_{DD} = 3 V.
2. In the auxiliary and data write mode; writing DCC data; I_{WDAT} = 60 mA; V_{DD} = 3 V; f_{clk} = 3.072 MHz. Data channels resistively loaded with 6 Ω, auxiliary channel resistively loaded with 4 Ω between pins 23 and 24, and 37 and 38.
3. Resistors connected in accordance with test circuit of Fig.7.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1381H	TQFP48[1]	plastic thin quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-1

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

BLOCK DIAGRAM

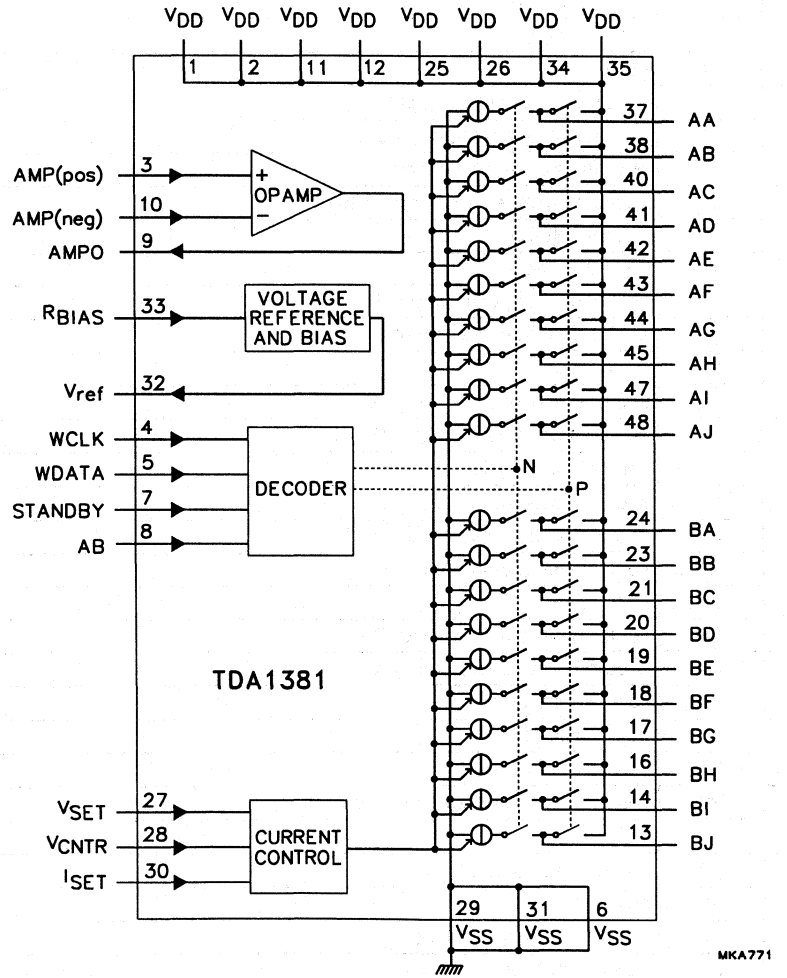


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DD}	1	supply voltage
V_{DD}	2	supply voltage
AMP(pos)	3	operational amplifier non-inverting input
WCLK	4	write clock input
WDATA	5	write data input
V_{SS}	6	ground
STANDBY	7	standby mode control input
AB	8	tape sector A or B select input
AMPO	9	operational amplifier output
AMP(neg)	10	operational amplifier inverting input
V_{DD}	11	supply voltage
V_{DD}	12	supply voltage
BJ	13	sector B write pulse output J
BI	14	sector B write pulse output I
n.c.	15	not connected
BH	16	sector B write pulse output H
BG	17	sector B write pulse output G
BF	18	sector B write pulse output F
BE	19	sector B write pulse output E
BD	20	sector B write pulse output D
BC	21	sector B write pulse output C
n.c.	22	not connected
BB	23	sector B write pulse output B
BA	24	sector B write pulse output A
V_{DD}	25	supply voltage
V_{DD}	26	supply voltage
V_{SET}	27	control voltage input
V_{CNTR}	28	voltage-to-current conversion setting input
V_{SS}	29	ground
I_{SET}	30	control current input
V_{SS}	31	ground
V_{ref}	32	reference voltage output
R_{BIAS}	33	bias current resistor
V_{DD}	34	supply voltage
V_{DD}	35	supply voltage
n.c.	36	not connected
AA	37	sector A write pulse output A
AB	38	sector A write pulse output B
n.c.	39	not connected
AC	40	sector A write pulse output C

SYMBOL	PIN	DESCRIPTION
AD	41	sector A write pulse output D
AE	42	sector A write pulse output E
AF	43	sector A write pulse output F
AG	44	sector A write pulse output G
AH	45	sector A write pulse output H
n.c.	46	not connected
AI	47	sector A write pulse output I
AJ	48	sector A write pulse output J

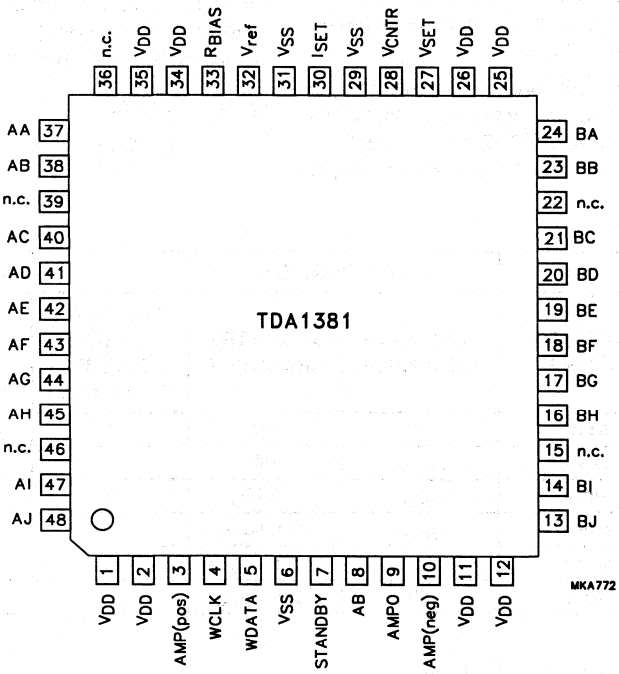


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1381 is designed to drive the elements of an 18-channel recording head, containing nine elements for tape sector A and nine elements for sector B. A brief functional description of each block (see Fig.1) is given below.

Decoder

The IC is controlled by the 32-bit wide serial data word which is clocked in at WDATA (pin 5). The clock frequency (WCLK, pin 4) is 3.072 MHz with a clock period of 325 ns. The write pulses are made available at the outputs AA to AJ when tape sector A is selected (pin 8 HIGH) or at the outputs BA to BJ when tape sector B is selected (pin 8 LOW). The principle of connection of the recording head to the IC is illustrated in Fig.4.

The timing sequence of the write pulses is shown in Fig.5. The operating mode of the IC can be set by the first 3 bits of WDATA. The signals TCH0 to TCH7 and TCHAUX determine the direction of the write current. When TCH_n is HIGH, the current flows as indicated in Fig.4. When TCH_n is LOW current flows in the opposite direction. The various modes of operation are given in Table 1. The standby mode can also be forced by setting the STANDBY input (pin 7) HIGH.

Current control

The write current at the outputs is regulated by the current control circuit. The principle of this circuit is shown in Fig.3.

The value of the current I_{WDAT} can be set using an external voltage V_{SET}, connected between pin 27 and V_{SS}. In this configuration, pin 28 has to be resistively loaded to another voltage source or V_{SS} (see Fig.7). The current control circuit regulates the voltage between pins 27 and 28 to zero. When a resistor R_{set} is connected between pin 28 and V_{SS}, a current gain factor (G_{if}) can be defined as:

$$G_{if} = \frac{I_{WDAT}}{\left(\frac{V_{SET}}{R_{SET}}\right)}$$

Table 1 Modes of operation.

MODE		WRITE CURRENT		CONTROL BIT[1]		
MAIN DATA CHANNELS	AUXILIARY CHANNEL	MAIN DATA CHANNELS	AUXILIARY CHANNEL[3]	TDAPLB[2] (DATA CHANNEL PLAYBACK)	TAUPLB[2] (AUXILIARY CHANNEL PLAYBACK)	TERAUX (AUXILIARY CHANNEL ERASE)
Read	read	off	off	1	1	X
Write	read	I_{WDAT}	off	0	1	X
Write	write	I_{WDAT}	AW × I_{WDAT}	0	0	0
Write	erase	I_{WDAT}	AE × I_{WDAT}	0	0	1
Read	write	off	AW × I_{WDAT}	1	0	0
Read	erase	off	AE × I_{WDAT}	1	0	1

Notes

1. Where 0 = LOW, 1 = HIGH and X = don't care.
2. When both TDAPLB and TAUPLB are HIGH, the IC is set to the standby mode.
3. A_W and A_E are multiplication factors (see Section "Current control").

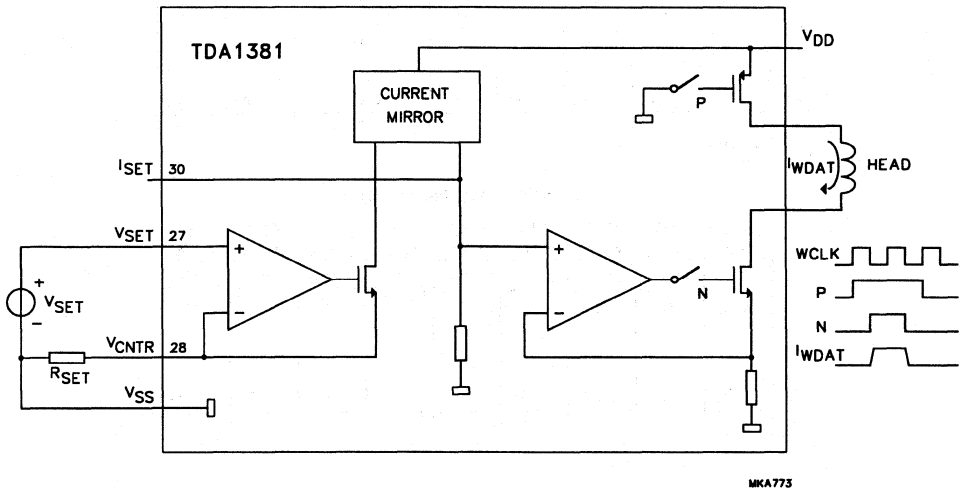


Fig.3 Principle of the write current control circuit.

It is also possible to set the write current by providing a current I_i into I_{SET} (pin 30). In this configuration pin 27 must be connected to V_{SS} and pin 28 must be connected to V_{DD}.

The current gain factor is now defined as: $G_{if} = \frac{I_{WDAT}}{I_i}$

During AUX write (outputs AA, AB or BA, BB active) the output current I_{WDAT} is increased by a factor A_W. During the erase mode of the auxiliary channel (TERAUX = HIGH, see Table 1), the output current I_{WDAT} is increased by a factor A_E.

Outputs

Each channel of the chosen sector is selected in sequence. Depending on the data word, the current is directed forward or reversed through the heads. The outputs that are not selected are kept floating to prevent any incorrect current flow. In HIGH state (one of the switches P is closed) the output is internally connected to V_{DD}. In the LOW state (one of the switches N is closed) the output is connected to a current source.

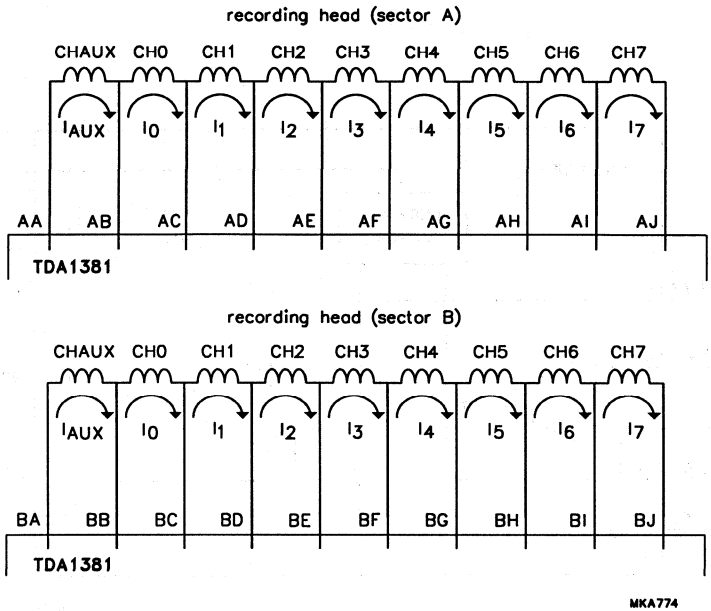


Fig.4 Definition of the output currents.

Voltage reference

A reference voltage is available at pin 32. This voltage is derived from a bandgap reference source, and can be used to derive a control voltage for the current control circuit.

Standby

The circuit is set to the standby mode when TDAPLB = 1 and TAUPLB = 1 (see Table 1), or when a HIGH level is applied to pin 7. After a HIGH-to-LOW transition at pin 7, the IC will remain in the standby mode until TDAPLB = 0 or TAUPLB = 0. When the IC is in the standby mode, the current amplifier is switched off to minimize the power consumption, all write current outputs are floating, and the voltage reference is switched off.

Operational amplifier

An uncommitted operational amplifier is available for use in a tape head temperature compensation circuit with the read IC TDA1380.

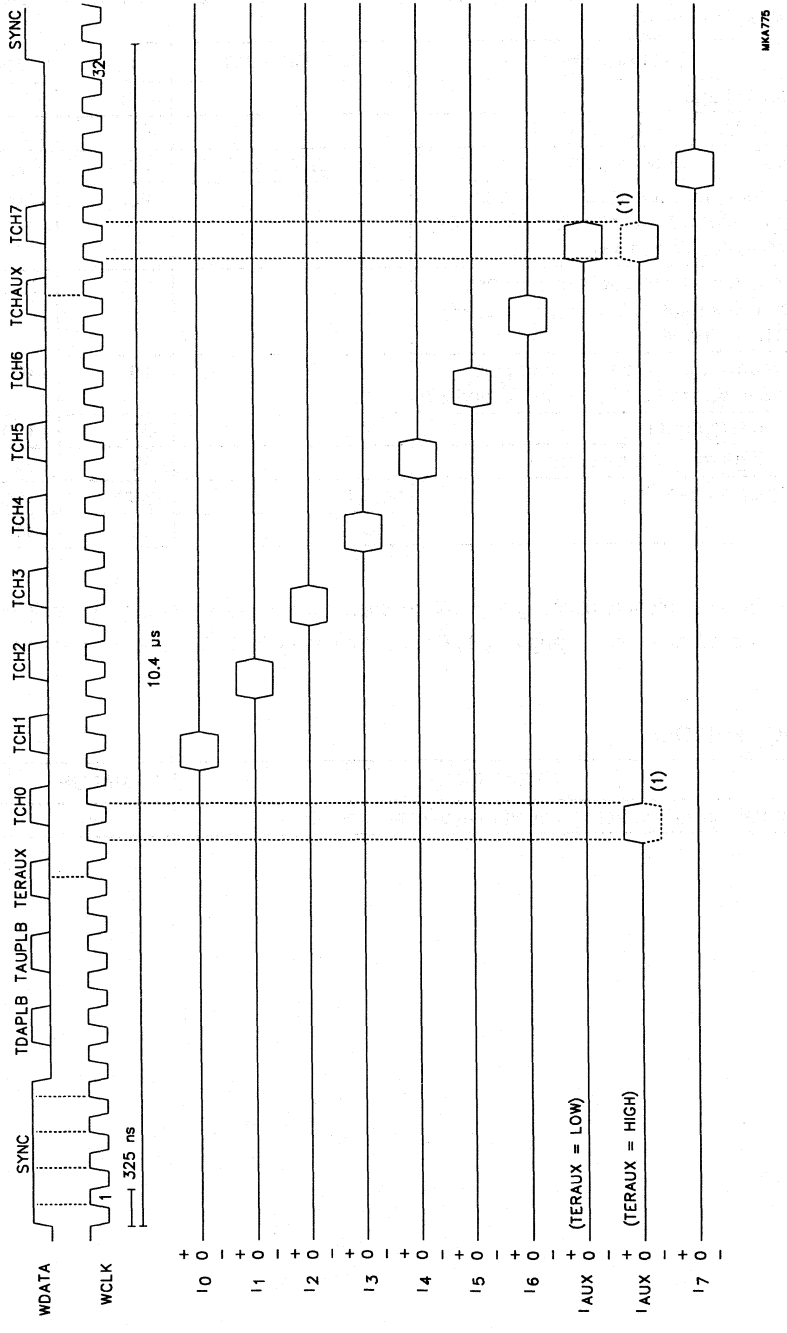


Fig.5 Data format and timing sequence of the write pulses.

(1) Erase pulses are inverted every other cycle of 32 clock pulses.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); all voltages referenced to V_{SS} (pins 6, 29 and 31); all currents are positive into the IC.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	5.5	V
V_I	input voltage pins 4, 5, 7 and 8		−0.3	5.5	V
V_n	input voltage on other pins	V_{DD} + 0.3 V < 5.5 V	−0.3	V_{DD} + 0.3	V
$I_{IW(max)}$	maximum input current on write pulse outputs (pins 13, 14, 16 to 21, 23, 24, 37, 38, 40 to 45, 47 and 48)		−200	+200	µA
$I_{I(max)}$	maximum input current on supply and ground pins (pins 1, 2, 6, 11, 12, 25, 26, 29, 31, 34 and 35)		−250	+250	µA
$I_{n(max)}$	maximum input current on other pins (pins 3 to 5, 7 to 10, 27, 28, 30, 32 and 33)		−10	+10	µA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−30	+85	°C
V_{es}	electrostatic handling	note 1	−3000	+3000	V
		note 2	−300	+300	V

Notes

1. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
2. Machine model: equivalent to discharging a 200 pF capacitor through a 25 Ω series resistor and a 2.5 µH series inductor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	65	K/W

CHARACTERISTICS

V_{DD} = 3 V (pins 1, 2, 11, 12, 25, 26, 34 and 35 tied together externally); T_{amb} = 25 °C; f_{clk} = 3.072 MHz; measured in test circuit of Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.7	3.0	4.0	V
I_{DD}	supply current	note 1	–	9	12	mA
I_{stb}	total standby current	standby mode	–	0.1	0.3	mA
$P_{d(av)}$	average power dissipation	note 2	–	120	–	mW
Digital inputs (pins 4, 5, 7 and 8)						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	V_{DD}	5.5	V
V_{IL}	LOW level input voltage		−0.3	0	$0.3V_{DD}$	V
I_{LI}	input leakage current		−10	0	+10	µA
t_{su}	WDATA set-up time	see Fig.6	30	–	–	ns
t_h	WDATA hold time	see Fig.6	30	–	–	ns
Analog inputs/output (pins 27, 28, 30, 32 and 33)						
V_{SET}	input voltage (pin 27)		0.4	–	V_{DD} − 1.3	V
V_{CNTR}	input voltage (pin 28)		0.4	–	V_{DD} − 1.3	V
V_{ref}	output reference voltage (pin 32)	I_o < 500 µA	1.95	2.05	2.15	V
G_{if}	current gain factor	with voltage input	550	700	850	
		with current input	590	720	850	
Write pulse outputs (pins 13, 14, 16 to 21, 23, 24, 37, 38, 40 to 45, 47 and 48)						
$I_{WDAT(min)}$	minimum output current channels 0 to 7	f_{clk} = 6.15 MHz	–	–	20	mA
$I_{WDAT(max)}$	maximum output current channels 0 to 7	note 3	100	–	–	mA
$I_{AUX(max)}$	maximum output current auxiliary channel	note 3	153	–	–	mA
A_W	relative auxiliary write current increase		1.0	1.2	1.4	dB
A_E	relative auxiliary erase current increase		3.0	3.7	4.4	dB
ΔI_{WDAT}	deviation between main data channels per sector	note 4	–	–	0.5	dB
$\frac{\Delta I_{WDAT}}{\Delta T}$	temperature coefficient of the output currents	note 5	–	200×10^{-6}	–	K^{-1}

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operational amplifier (pins 3, 9 and 10); note 6						
G_o	DC open loop gain		–	45	–	dB
B_G	gain bandwidth		–	1	–	MHz
V_o	output voltage (pin 9)		0.5	–	$V_{DD} - 1.3$	V
$V_{i(cm)}$	common mode input voltage (pins 3 and 10)		0.85	–	V_{DD}	V

Notes

1. No head connected, all outputs unloaded.
2. Auxiliary and data write mode; $I_{WDAT} = 100$ mA.
3. Maximum resistive load of auxiliary channel is 6.5 Ω; maximum resistive load of data channels is 10 Ω.
4. $20 \log \frac{I_{WDAT(max)}}{I_{WDAT(min)}}$ for channels 0 to 7, $I_{WDAT} = 100$ mA.
5. With constant V_{SET} or I_{SET} (see Fig.7).
6. $R_L > 100$ kΩ; $C_L < 100$ pF; load connected between pin 9 and V_{SS}.

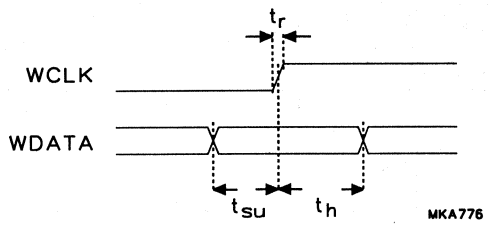


Fig.6 Timing relationship between the edges of WCLK and WDATA.

TEST AND APPLICATION INFORMATION

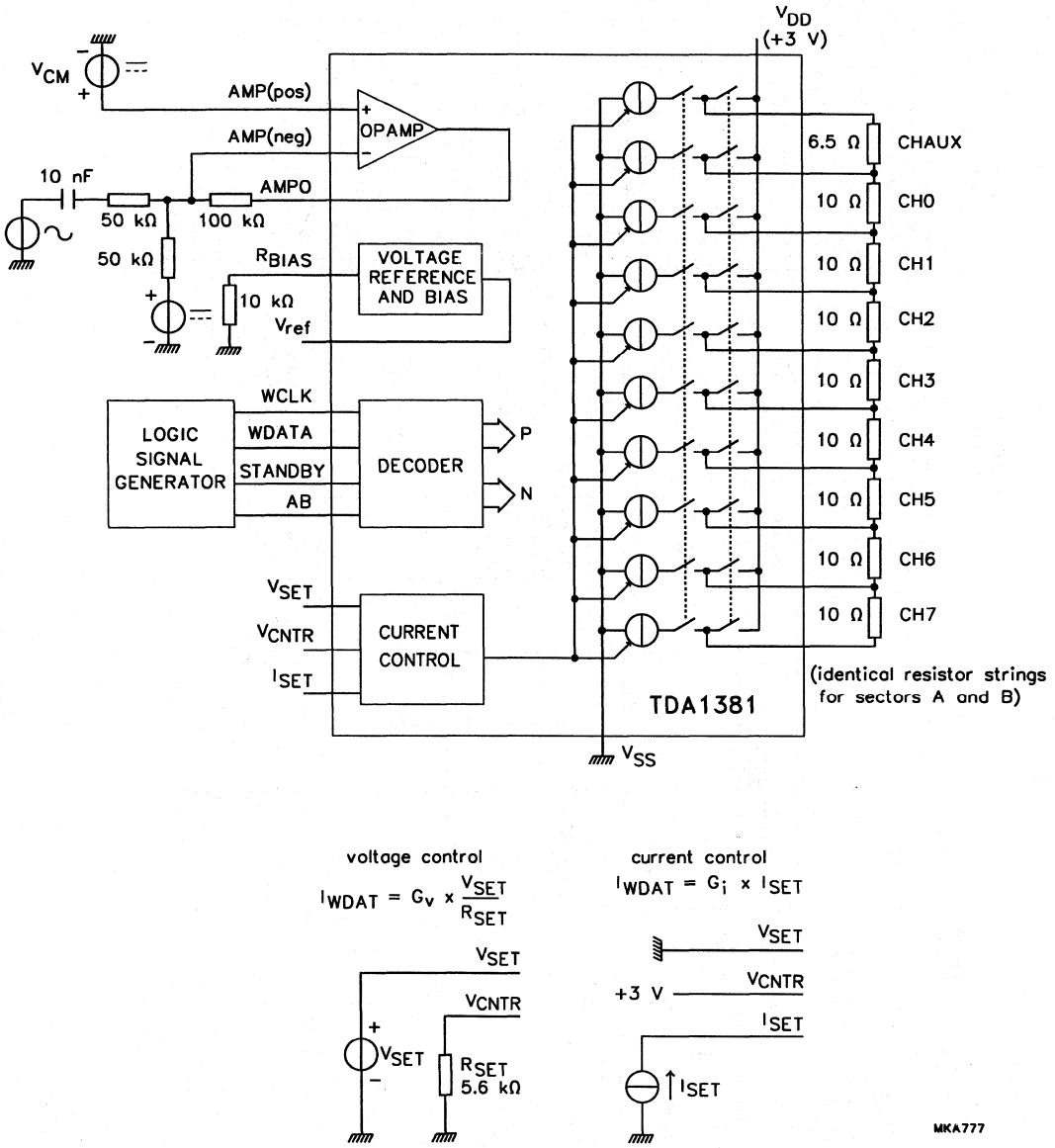


Fig.7 Test circuit.

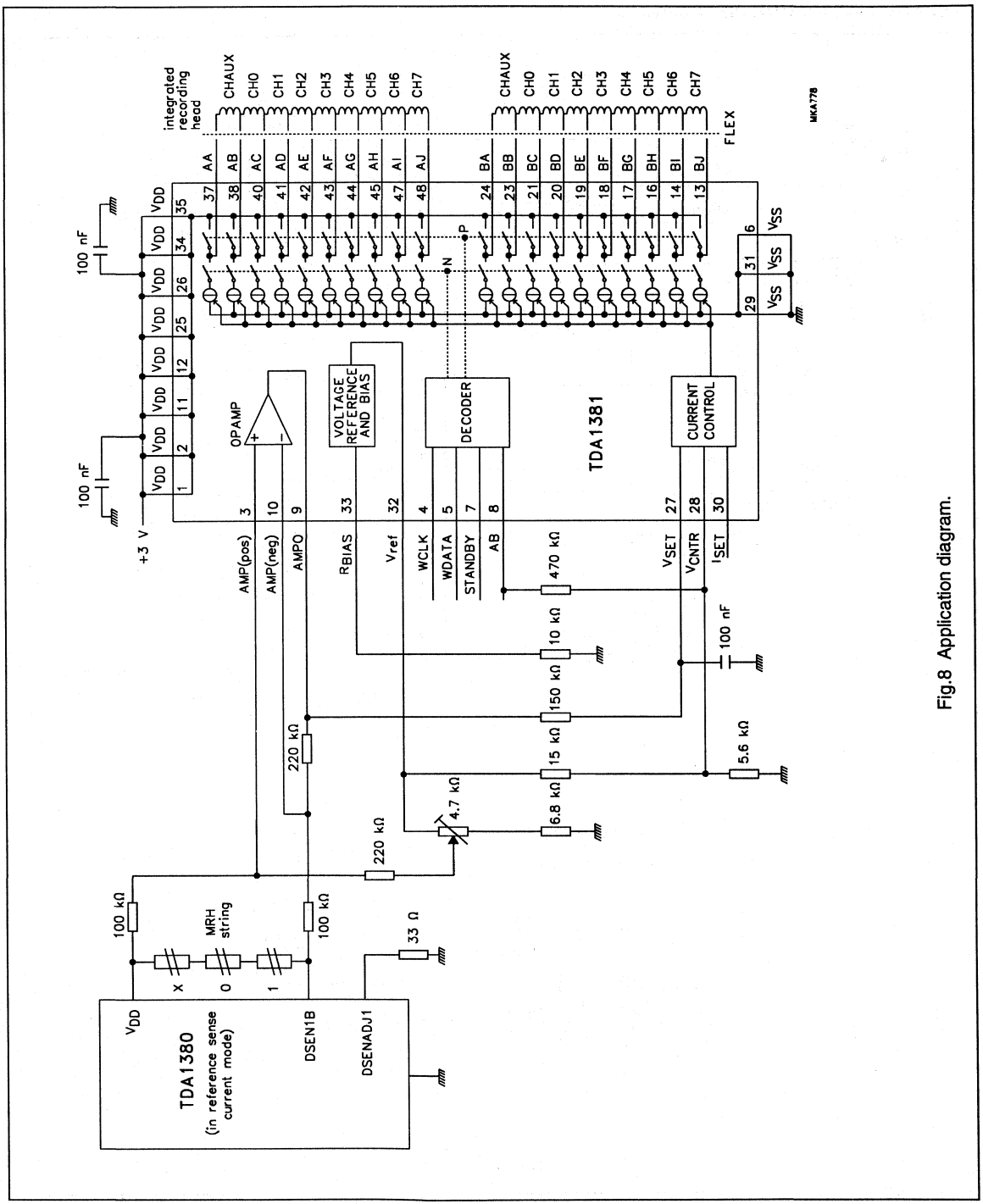


Fig.8 Application diagram.

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